Hopping Conduction and Metallic behavior in 2D Silicon Surface States induced by an Ionic Liquid

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JJ Nelson

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A. M. Goldman

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Dedication

To the wife: For patiently awaiting the completion of this PhD.

Abstract

Ionic liquids (ILs) are essentially molten salts with a melting point below room temperature. When used as the gate dielectric of a transistor, carrier densities on the order of 10^{15} cm^{-2} can be achieved. These record high carrier densities are significantly higher than the maximum carrier density achievable with oxide dielectrics. The physical mechanism for inducing carriers to such a high carrier density is not well understood. Some groups have reported that the induced carriers are a result of electrostatic and electrochemical processes. Other groups have suggested that carriers induced with an IL may be entirely due to electrochemical reactions.

Here we report on IL gated Si at carrier densities from 10^{11} cm^{-2} to 10^{13} cm^{-2}. The experiment was designed to preferentially induce electrostatic carriers over electrochemical reactions. At low carrier densities, sample surface conductivity follows nearest neighbor hopping conduction. This form of conduction has also been observed in experiments where surface conductivity was induced by implanting Na^+ near the oxide surface interface.

A surprising result of this work was that in some samples a 2D metallic state could be created on the surface of Si. The transition to metallic behavior occurred just below 10^{13} cm^{-2}. High quality Si transistors with oxide dielectric materials observe critical carrier densities around 10^{11} cm^{-2}. The critical carrier density observed in IL gated Si is the highest density reported to date.

At carrier densities higher than 10^{13} cm^{-2} it was observed that the sample conductivity decreased with increasing carrier density. The behavior was unexpected and not fully understood. Both metallic and non metallic samples show a similar reduction in

conductivity that is not thought to be due to sample degradation by the IL. The reduction in the sample conductivity at high carrier densities is thought to be due to surface roughness scattering. Similar behavior has been observed in other IL gated experiments on different materials.

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Chapter 1

Introduction

Superconductivity, which was discovered in 1911 by Kamerlingh Onnes, is a quantum state where electric properties of a material are quantized into units of two electrons.[1, 2] Superconducting materials have zero resistance and some are perfect diamagnets. In 1957 a theory by Bardeen, Cooper, and Schrieffer (BCS) was the first microscopic theory to describe existing superconducting properties.[3] In their theory, two electrons can overcome repulsive Coulomb interactions by a mutual attraction involving vibrations of positively charged nuclei in the atomic lattice, known as phonons. The energy scale for the electron phonon interaction made it unlikely that superconductors of this type could exist above 40 K. Thus the advantages one would gain from the superconducting properties of a material are hindered by the requirement of temperatures accessible only though the use of liquefied helium or helium based refrigerators.

The field was revolutionized in 1986 by the discovery of superconductors with transition temperatures above the boiling point of liquid nitrogen.[4] In these materials, superconducting planes composed of Cu and O intercalated with Group II, Group III, and f-block elements. In addition to doping with oxygen, the interstitial elements can

alter the bonds and carrier densities of the CuO planes leading to superconductivity. Unlike BCS superconductors, the microscopic mechanism leading to the pairing of electrons could not be explained by the phonon mediated model. Since then, several other families of superconductors have also been discovered that fall outside of BCS theory. A special issue on superconductivity in preparation had identified 32 classes of superconducting materials where at least a third are thought to be non-BCS.[5] In addition to new forms of superconductivity, electron-electron interactions have given rise to other unpredicted behavior like the possibility of 2D metallic behavior at $T = 0$ and heavy fermion materials where the electron effective mass can be orders of magnitude above the free electron rest mass.[6] Heavy fermion materials have also been shown to be superconducting.[7] These are examples of the many unsolved problems that exist regarding electron interactions in solids.

The motivation for this thesis stems from the discovery of superconductivity in Group IV materials. Coined covalent superconductors, the discovery of superconductivity in heavily boron doped diamond attracted significant interest to the subject. It was found that when single crystals of carbon with the diamond crystal structure were doped with boron at concentrations of 10^{21} cm^{-3}, the materials were superconductors with a transition temperature, T_c, near 4 K.[8] It was later reported that crystals could be produced with $T_c = 8$ K[9]. It is an open question as to whether or not superconductivity of Group IV materials can be described by the BCS theory. The two additional theories that have been proposed involve electron pairing by spin flip interactions and interactions associated with boron impurity bands.[10]

Shortly after the discovery of superconductivity in diamond, it was found that other Group IV elements were superconductors by doping with Group III acceptors at similar boron concentrations as that of diamond. A brief summary of the experiments shows that single crystal silicon could also be made into a superconductor with $T_c = 350$mK

at sufficient boron concentrations[11]. The solubility limit of B in Si is lower than 10^{21} cm^{-3} so the crystals were created through gas immersion laser doping. The dopant depth was estimated to be within 100nm of the surface and it is thought that boron acceptors are substitutional and not interstitial. SiC crystals could be made into a superconductor with B or Al acceptors at the 10^{21} cm^{-3} level[12]. For the SiC films, $T_c \sim 1$K falls in between T_c for crystals of C and Si. Measurements of the specific heat indicate the existence of an energy gap and calculations based on the density of states agree with the gap being isotropic. While Si forms the diamond crystal structure, the equivalent structure for SiC is referred to as zincblende. In effect, SiC can be viewed at two inter-penetrating FCC crystals of Si and C as opposed to an FCC crystal with two atoms per site in the unit cell. The jump in the specific heat was small compared to the jump expected from BCS theory.

In an effort to constrain the theories for superconductivity in Group IV materials, we developed an experiment to electrostatically induce holes at carrier densities similar to the level required for superconductivity in Si and SiC with B. The experiment would require carrier densities beyond the limit of conventional solid dielectrics.[13] Recently, record high carrier densities have been realized though the use of an ionic conductor as a dielectric material in a transistor configuration.[14] The dielectric is a binary compound of charged organic molecules, which is liquid at room temperature, referred to as an Ionic Liquid (IL). Ionic liquid transistors are referred to as electric double layer transistors, as the ions in the dielectric will form electric double layers with both the sample and the gate electrode. The high carrier density achievable has been sufficient to observe superconductor-insulator transitions.[15, 16, 17] Metal-insulator transitions have also been observed when gating with an IL.[18, 19] A microscopic mechanism for the high carrier accumulation is currently being investigated.[20, 21] At high carrier densities the sample surface will be subject to large electric fields, which have been shown to cause

reversible structural changes in some samples.[22]

Experimental details of the electric double layer transistor are covered in Chapter 2. A model for electrostatic carrier induction by an ionic liquid is discussed in Chapter 3. The purpose of the model is to understand the microscopic physics of carrier induction by an ionic liquid at low carrier densities. Once the low carrier density behavior is understood future experiments could extend the model to the record high carrier densities reported in IL gating experiments. Ionic liquids can induce carrier densities as high as 10^{15} cm^{-2} in surface layers only a few Å thick on the surface, suggesting that carrier densities of 10^{21} cm^{-3} required for superconductivity in diamond or silicon should be accessible.

A study of T_c as a function the volume carrier density, n_b, of boron dopants in Si observed that $n_b d$ determined T_c by the phenomenological equation

$$\frac{T_c(n_b)}{T_{c0}} = 1 - \frac{A}{n_b d} \tag{1.1}$$

[23]. Here A is a constant found to be of the order of 10^{15} cm^{-2}, and d is the doping depth of the B layer. One hypothesis derived from the results is that this is an example of interface superconductivity where $n_b d$ is an approximate 2D sheet carrier density. Superconductivity may be related to an interface between a layer of heavily boron doped Si and bulk Si or the crystal surface.

When monolayers of Pb or In deposited on top of cleaved Si $\langle 111 \rangle$ surfaces, the interfaces were also observed to be superconducting. The monolayers of metal had a density of 10^{15} atoms/cm^2. This atomic density is similar to the sheet carrier densities observed in the boron doping experiments. The superconducting gap was measured by scanning tunneling spectroscopy. Angle resolved photoemmision spectroscopy measurements indicated that superconductivity was associated with covalent Pb-Si bonds and not due to the thin Pb film which was a single monolayer in thickness.[24] Thicker Pb film overlayers showed superconducting properties that are consistent with Pb. Interface

superconductivity has also been observed at interfaces of $LaAlO_3$ with $SrTiO_3$.[25]

Our experiment involved inducing a conducting layer on $\langle 100 \rangle$ Si wafers using an ionic liquid. Details regarding the sample design and the measurement are covered in chapter 2 This chapter also contains the details of calculating the induced carrier density in Si. Si has been referred to as the hydrogen atom of solid state physics. Isolated donors with the background of full valence shell of Si atoms have an electron binding energy with a hydrogen-like spectrum. The bound electrons have a hydrogen like wave functions. Overall, the physics of Si is well understood, which makes this system an ideal platform for the microscopic study of gating with an ionic liquid.

Chapter 3 contains a description of a model of electrostatic carrier induction using an ionic liquid. The chapter will cover the onset of conduction at the low carrier density of 10^{11} cm^{-2}, and the conduction mechanism of the induced carriers. The IL was found to induce surface acceptor states where conduction happens by tunneling of holes between localized states. The behavior of holes on the Si surface due to the charged ions in the ionic liquid were found to conduct in a manner similar to that of electron clouds formed by Na^+ ions implanted within a SiO_2 overlayer of a Si wafer.[26]

At high carrier densities the double layer is often viewed as a uniform sheet of charge. The similarities to the Na^+ experiment suggests that at low carrier densities one should consider the ions in the liquid as a series of discrete charges. Our experiment was also designed to suppress electrochemical reactions observed in other experiments.

Chapter 4 will focus on behavior at carrier densities between 10^{12} cm^{-2} and 10^{13} cm^{-2}. The carrier density range is still well below the high 10^{15} cm^{-2} density achievable with an IL liquid. The carrier densities studied in this Chapter are within densities achievable with conventional transistors using high dielectric constant gate insulators. A very interesting and unexpected result of this study was the discovery of 2D metallic behavior at carrier densities much higher than those at which metallic behavior was

previously observed. Data on the high carrier density metal-insulator transition (MIT) is presented and discussed in the framework of existing MIT physics. Only a subset of samples showed metallic behavior and the reason for this is not yet understood.

At densities higher than 10^{13} cm^{-2} further increase of the carrier density lead to the samples becoming more insulating. In effect the sample mobility exhibits a peak as a function of carrier density. This was true for both metallic and nonmetallic Si samples. This peak behavior is not yet well understood but has been observed in experiments on other materials. The behavior has been explained by theories that can account for the behavior by calculating the effect of surface roughness scattering at high carrier densities. Covered in Chapter 5 is the observed mobility peak as a function of carrier density, the reproducability of the observed peak, and a theory that calculates the mobility as a function of carrier density.

We were unable to induce superconductivity into a surface layer which was the original goal of the experiment. The discovery a high carrier density metal-insulator transition is one of significant experimental interest. Si was also found to be a platform where an IL can be used to electrostatically induce carriers in a surface state. Further experiments may lead to a better understanding of the microscopics of carrier induction at high carrier densities. In addition, IL gating of Si could be used to study the transition from electrostatic to electrochemical processes and the interplay of the two mechanisms in EDLTs.

Chapter 2

Techniques and Materials

2.1 Introduction

This chapter will cover some of the basic experimental details of ionic liquid (IL) gated silicon. The chapter consists of three sections. Section 2.2 covers the basic details of the electric double layer transistor (EDLT) and the methods we used to determine sheet carrier densities. High carrier densities can be achieved with EDLTs using ionic liquids, but the microscopic physics is not yet understood. The current model is that of the formation of a Helmholtz layer as a uniform sheet of ions. Using ionic liquids in EDLTs involves both electrostatic and electrochemical processes and a review of electrochemical observations is discussed in section 2.2.2. Our experiments were designed to suppress electrochemical reactions and we have several observations that lead us to believe the carriers we discuss are electrostatically induced.

Section 2.3 covers the measurement system used and the considerations required to work at cryogenic temperatures when using ionic liquids. This section will also cover the procedure used to calculate sheet resistance using the van der Pauw method. Details involving sample fabrication can be found in section 2.4. Samples were prepared using

equipment available at the University of Minnesota Nanofabricaiton center.

2.2 Electric Double Layer Transistors

This year marks the 50th year of Moore's Law which was an observation that on-chip transistor density increased in a linear log relationship with time. The transistor is a three terminal device whose name is derived from transconconductance and resistance.[27] In its realization as a field effect device, it is a combination of a capacitor and resistor. Capacitors are devices that store charge with an applied voltage. Thus the charge density is altered on the capacitor electrodes. If one also adds an additional wire to one of the capacitor electrodes, the electrode conductivity can be measured. For a material where the conductivity varies exponentially with carrier density this configuration can be used as an electrical switch. The invention of the transistor and the use of silicon transistors in technology has lead some to refer to the past 50 years as the "Age of Silicon."

In the laboratory, transistor configurations can be a tool to measure material properties as a function of carrier density. Conventional solid dielectrics have several limitations that prevent their use at the high carrier densities involved in our experiments. High carrier densities can be achieved by using either large capacitance transistors or high gate voltages. In the later case one is limited by the breakdown voltage of the measurement lines or capacitor or gate dielectric. Increasing the capacitance of a transistor is another way to increase carrier densities at a fixed gate voltage; however one must either increase the dielectric constant of the insulator or decrease the thickness of the capacitor. Quantum mechanics allows for electrons to tunnel though sufficiently thin dielectric materials thus leading to a upper bound on carrier density achievable though the reduction of capacitor thickness. In EDLTs using ionic liquids as dielectrics will result in atomically thin capacitors without the added complication of electron tunneling,

and densities of 10^{15} cm^{-2}are routinely achieved. Conventional dielectrics are unable to reach the 10^{15} cm^{-2} carrier density possible using ionic liquids.[28]

Figure 2.1 is a cartoon depicting the interaction between the IL and the sample surface. Without an applied V_g the cations and anions are randomly distributed throughout the liquid. There are equal numbers of cations and anions at the sample surface and there are no screening charges due to the collection of ions being neutral. When a negative voltage is applied to the gate, anions are repelled and pushed to the sample surface while cations will be attracted to the gate. This model of carrier induction is discussed in greater detail in Chapter 3. The excess anions will induce screening holes in the Si. At low gate voltages the number of excess anions at the surface are much smaller than the number of total ions at the sample surface. At higher gate voltages and high carrier densities, anions are considered to be a uniform sheet of charge with a second, less dense, layer of cations attracted to the sheet of anions. Voltages must remain within the electrochemical window of the IL. The electrochemical window is defined as the range of voltages over which oxidation and reduction of the ionic liquid does not take place.[29]

2.2.1 High Carrier Density

Interest in ionic liquids dates back as far as the thermal battery. Thermal batteries contain an electrolyte that is solid and inert at room temperature. Energy can be released from the battery by warming it to a temperature where the electrolyte no longer remains solid. The batteries are single use but have a very high power output due to large ionic conductivities and high carrier densities. Significant focus has been on producing rechargeable batteries with high energy density and decreasing the operating temperature. The ionic liquids we use are molten salts with freezing temperatures below room temperature. The ions are composed of charged molecules and the increase in their

sizes compared to those of single atoms reduces the Coulomb energy between a pair of ions by increasing their separation. It is this reduction in the Coulomb attractive energy that allows ionic liquids to be liquids at room temperature.

Thermal batteries are able to store large amounts of energy due to the ability to reach extremely high carrier densities a property shared by capacitors. This can be seen in the following equation expressing the relationship between stored energy and charge

$$U = \frac{1}{2}CV^2 \tag{2.1}$$

Here V is the voltage on a plate and the capacitance C is the ratio of the amount of stored charge for a given voltage given by

$$Q = CV \tag{2.2}$$

At a fixed voltage the energy density of a capacitor is entirely determined by its capacitance. It should be noted that while a battery chemically stores energy, in a capacitor the energy is stored as an electric field. In the simple case of the parallel plate capacitor the capacitance is determined by

$$\frac{C}{A} = \frac{\epsilon}{d} \tag{2.3}$$

Here d is the separation of the plates, ϵ is the dielectric constant of the insulating material, and A is the area of the electrodes. The variable C/A is the capacitance per unit area used to determine the charge density at a fixed voltage. Higher carrier densities can be achieved by increasing the capacitance and that comes from using an insulator with a higher dielectric constant, or reducing the separation of the metal electrodes. The former case is limited by the physical materials that are available. Increasing the capacitance by reducing the thickness of the capacitor has recently approached a physical limit.

Quantum mechanics tells us that in the limit of very thin finite potential barrier there is a nonzero tunneling probability that increases with decreasing thickness. In the

limit of an atomically thin capacitor electrons can pass through the insulator thereby reducing the total charge that one can accumulate in the capacitor. One solution to this problem is to construct a circuit where the charge carriers are not electrons. By using a dielectric material composed of conducting ions, the ions are able to move to the surface of the electrodes but must remain in the dielectric material. The electrons on either plate remain separated by distances where quantum tunneling is not an issue yet are within nanometers of the ions.

The model of the Helmholtz double layer involves the formation of an atomically thin capacitor between the ions in the liquid and the screening electrons in the electrode. When a voltage is applied, the ions will form a layer of cations at the negative electrode and anions at the positive electrode. A second layer of cations will form on the anion layer as well as a second layer of anions on the cation layer. The configurations at each electrode are referred to as double layers. Double layers are formed at both electrodes leaving the bulk liquid in a net neutral state. The combined double layer along and electrode is an individual capacitor with an effective nanometer level separation where the charges are composed of the ions and electrons. The ions have a much lower tunneling probability and so high carrier densities can be achieved. There will be two double layers in series and while capacitors in series store less charge for a given voltage the increase in the capacitance at each electrode more than makes up for this effect. In our experiments a thin layer of SiO_2 roughly $10 - 15$Å, as measured by ellipsometry, was on the Si surface separating the ions from the electron channel. In the 2D limit where the the screening electrons are assumed to be confined to the Si/SiO_2interface, the expected capacitance per unit area of the thin SiO_2 layer is $4\mu F/cm^{-2}$. The ions in the ionic liquid are typically cylindrical shaped molecules and the simple calculation assumed the charged portion of the ion is resting on the SiO_2 surface.

2.2.2 Electrostatic or Electrochemical Changes

While ILs can achieve high carrier densities, the mechanism in some instances has been shown to be a combination of electrochemical and electrostatic processes. An electrochemical processes is a redox reaction between an electrode and an ionic conductor. Oxidation was also determined to be the source of carrier modulation in the experiment in which VO_2 was shown to undergo a MIT.[30]. Several observations were made that all support the oxygen vacancy scenario. XPS measurements were conducted and found that V^{4+}changed to V^{3+}as a function of gating. When O^{17} was introduced during the gating process, its concentration within the VO_2 film would be significantly above the atmospheric concentration. When the gate voltage was removed after VO_2 had been gated into the metallic state the material remained metallic, even hours after the removal of the ionic liquid. To restore insulating sample behavior a negative voltage as large as the largest positive voltage had to be applied. The applied voltages were lower than the energy required to form oxygen vacancies so the reduction process was thought to be related to migration of oxygen from the ionic liquid into VO_2 due to the high electric fields that were present.

There was evidence for oxidation even in the gating of Au. By using low angle X-rays, it was shown that IL gating of Au resulted in monolayers of Au_2O_3.[31] The removal of electrons due to the formation of the oxide greatly exceeded the number of electrostatic carriers and was determined to be the origin of the high carrier modulation. In the previous two experiments, the gate voltage was applied at room temperature.

It has been suggested that carrier modulation is entirely an electrochemical process but oxidation processes have been shown to be be suppressed with the use of a thin insulating barrier.[32] In our experiments the electrochemical effects were suppressed by modulating the carrier density below room temperature; however, carrier modulation must be performed when the ions are in a mobile state. In addition a thin oxide was

used as a passivation layer to reduce trapping sites on the Si surface. Without the oxide, traps can number in excess of 10^{16} cm^{-2}, but the increased separation between the ions and the channel will reduce the capacitance of the transistor. It is therefore desirable to have a very thin oxide barrier.

When electrochemical processes are present, both the magnitude of the gate voltage and the amount of time spent with the IL in a liquid state are parameters that determine the change in resistance of the sample. There were no observed changes to the low temperature resistance unless the gate voltage was changed. Changing the gate voltage and waiting either for minutes or for an hour had the same effect. Warming to a temperature where the ionic liquid melts and not changing the gate voltage had no affect on the surface state resistance. Electrochemical processes will also lead to large leakage currents measured by the gate ammeter. For our measurements, the leakage currents were on the order of a nA or lower. The electrochemical window sets an upper limit to the voltage that, when exceeded, results in breakdown of the electrolyte. In our experiment we gated with voltages, < 2V, below the electrochemical window of 3V for DEME-TFSI. The value for the electrochemical window was determined at room temperature and should be larger at 230 K where the gate voltage was changed. Further evidence supporting electrostatic processes with IL gating of Si are presented in the following section in addition to Chapters 3 and 5. While more work needs to be done to better understand the role of oxygen when using an ionic liquid, in Chapter 3 a model for the electrostatic behavior when using an ionic liquid is presented.

A recent publication concluded that structural changes are also possible due to high electric fields from the sheet of ions.[22] The change was found to be a reversible process just like the electrochemical reactions. The carrier densities used in Chapter 3 and 4 of the IL gated Si experiment are similar to carrier densities used with conventional dielectrics and thus high electric field structural changes are thought not to occur; however

Chapter 5 covers carrier densities that are high enough to consider the possibility.

2.2.3 Calculating the Carrier Density

With an ammeter in series between the gate voltage source and the sample, one can monitor the current flowing to the electrodes as a function of time during the charging process. By Kirchhoff's law, this is a measure of the number of ions moving to the sample surface. Integrating the current as a function of time, one can then calculate the number of charges that have moved though the ammeter as the sample was charged. This process can be a measure of the number of ions that are now at the sample surface as long as there are no additional chemical reactions that would lead to an additional leakage current though the transistor. In an ideal capacitor, no current should flow once the capacitor voltage is charged to the source voltage. In Fig 2.2 a plot of two charging curves are presented. They are representative of all the charging curves measured for each sample presented in this work. During charging, we see what appears to be an exponential decay in the current as a function of time within the first 10 s of charging after which the current level is below the noise level of ~ 0.8 nA at low voltages and around 2 nA near a gate voltage of 2V.

To determine the carrier density, the area under the curve of current vs time is measured relative to the background current. This subtraction of the leakage current leads to a shift in the amount of calculated charge by about 10. This method can be problematic in situations where the leakage current is much higher, as the subtracted area approached the order of the integrated area.

Situations where the leakage current is high involve higher temperatures and higher gate voltages. Below 200 K, the ammeter displays a value consistent with the ammeter reading a broken connection and we interpret the disappearance of any ionic conductivity with the solidification of the ionic liquid. Above 200 K, there is a finite leakage

current that increases with temperature, and at temperatures near room temperature the leakage current is constant on the order of $1 - 10$ nA. At higher gate voltages the leakage current is much higher and is no longer found to exponentially decay but decays with a $\sqrt{t}$ time dependence. In these situations, the integrated density will differ from measurements of the carrier density using the Hall effect by a couple orders of magnitude. In our samples the Hall carrier density is a factor of 2 below the integrated carrier density. One example of this is shown in Fig 2.3. The reason for this dependency is not known at this time but both methods have complications that are discussed in Chapters 3 and 4.

2.3 Cryogenic Resistance Measurements with an Ionic Liquid

2.3.1 Measurement Cryostat and Charging Procedure

Samples were measured in a Quantum Design Physical Properties Measurement System (PPMS) with a 2K base temperature. An optional ^{3}He refrigerator insert could be used to lower the base temperature to 450mK. The PPMS system was chosen because of the need to temperature cycle the sample above the melting point of the IL. This procedure allows the ions to be mobile and the carrier density to be altered. While the optional ^{3}He insert lowers the base temperature of the system, this comes at the cost of thermal cycling time as the additional mass must be heated and cooled with each cycle to 230K. Most samples were screened without the insert to minimize measurement time. If a lower temperature was determined to be needed the sample would be installed on the refrigerator insert, but this required removing the sample from the system and thus discharging the conducting surface state. Once the sample was mounted to the insert and installed the measurement procedure would begin again.

The samples were loaded at room temperature with all the sample contacts grounded. The samples were then cooled to 180 K before beginning the measurement procedure. When the ionic liquid was in a liquid state (above 200 K) all the sample leads were grounded. Measuring the sample resistances when the conductivity of the ionic liquid is comparable to the sample can lead to measurement artifacts. This happens when the sample conductivity is low or at high gate voltages when the ionic liquid conductivity is high. While the conductivity of the bulk Si wafer is significantly higher than the ionic liquid conductivity, all the sample leads were grounded when the ions were mobile so as to not skew the carrier density with stray electric fields.

At 180 K the sample leads with the exception of I^- were ungrounded and permuted with a Keithley 7001 electric switch. Even though the IL is solid, V^- of the gate source remained connected to I^- of the current source and the sample, throughout the measurements. Resistance measurements were made in a 4-terminal configuration and the sheet resistance was calculated by the van der Pauw method. Resistance was measured as a function of time as the sample was slowly cooled. Upon reaching base temperature, current-voltage sweeps were made to determine if the contacts were ohmic and the range of currents were within the linear regime. Then, a constant current within the linear regime was be used to measure the sample resistance as it was incrementally warmed. To nullify any DC offset the resistance was calculated from the following formula

$$R_i = \frac{V(+I) - V(-I)}{2I} \tag{2.4}$$

where R_i is the resistance for a given permutation of the contacts.

2.3.2 Sheet Resistance Calculation

The Van der Pauw method allows one to calculation of the sheet resistance of an object with an unknown geometry.[33] Four contacts are placed on the perimeter of the

sample, ideally at the center of mass. By rotating the contacts and making multiple resistance measurements, two orthogonal measurements can be combined to check the sheet resistance. If the sample is known to have a large amount disorder, the Van der Pauw method is not advised. Specifically, if a permutation of the contacts by 180 leads to resistance measurements than 10% apart then the sample is too disordered to use the van der Pauw method. A key advantage of the van der Pauw method is that two measurements made with a 90 permutation of the measurement leads can be combined to determine the sheet resistance independent of the sample geometry.

The sheet resistance is determined from the following formula

$$\exp(-\pi R_H/R_S) + \exp(-\pi R_V/R_S) = 1 \tag{2.5}$$

where R_S is the sheet resistance and $R_H$and R_V are two orthogonal resistance measurements of the sample. If the ratio $r = R_H/R_V$ is close to 1, then the sheet resistance can be determined from the following simplification

$$R_S = \frac{R_H + R_V}{2}\frac{\pi}{ln(2)} * f \tag{2.6}$$

When $r \neq 1$, f must be determined analytically. Using the dimensionless variable

$$u = \frac{r-1}{r+1} \tag{2.7}$$

f can be determined from the following equation

$$\exp(u/f_1) - \exp(-u/f_1) - \exp(1/f_1) = 0 \tag{2.8}$$

where $f = f_1 ln(2)$. For most of our sample patterns r fell within the range of $1.4 - 4$ but in some geometries the ratio was as high as 15. We also used a Hall bar geometry to measure the sheet resistance and found that the results agreed with the values produced by the van der Pauw method.

2.3.3 Determination of the Hall Resistance

The Hall coefficient is an off-diagonal term of the conductivity matrix and must be odd with respect to the sign of magnetic field. To remove components of the sample magnetoresistance when determining the Hall coefficient, the following calculation was made.

$$2R_{ODD} = R(B) - R(-B) \tag{2.9}$$

The variable R_{ODD} should be the contribution that is odd in field. We define the Hall coefficient as

$$R_{Hall} = \frac{dR_{ODD}}{dB}$$

. The density of holes is related to the Hall coefficient by

$$R_{Hall} = \frac{1}{en_h}\left(\frac{1 - ab^2}{(1 + ab)^2}\right) \tag{2.10}$$

where $a = n_e/n_h$ and $b = \mu_e/\mu_h$.[35] n_i and μ_i are the carrier density and mobility respectively, with the index i indicating either electrons or holes. In semiconductors, the product of n_h and n_e is referred to as the law of mass action is independent of the doping level following

$$n_e n_h = N_e N_h \exp\left(-\frac{E_g}{T}\right) \tag{2.11}$$

where N_i are the density of states for electron and holes. At temperatures where the Hall effect was measured, the intrinsic carrier density is suppressed enough that the densities of holes from the Hall coefficient were determined using $n_h = (eR_{Hall})^{-1}$.

2.4 Sample Design and Cleanroom process

2.4.1 Silicon fabrication

There is a large market established for silicon wafers. Silicon can be purchased undoped or doped at a variety of concentrations with both n and p-type dopants. A very common transistor is one based on the p-n junction of a Si MOSFET where n type contact are placed in p-type silicon.

The wafers used in this study were supplied by Silicon Quest International. They were single side polished, boron, doped $\langle 100 \rangle$ wafers, 100 mm in diameter. The quoted total thickness variation (TTV) was 15μm. The wafers were test grade with $\rho = 1 - 5$ Ωcm corresponding to boron dopants on the order of 10^{16} cm^{-3}. The density was confirmed by measuring the Hall effect at 180 K and is shown in Fig 2.5. A commercial wafer saw was used to dice the wafer into 6 mm square substrates that were then further processed for the study. Shipley's 1800 series photoresist was used to protect the wafer surface during the cutting procedure. The photoresist was kept on the samples during storage and only removed prior to metal deposition.

A silicon surface without a passivation layer has trap density on the order of 10^{16} cm^{-2}[36]. The trapping sites are due to dangling silicon bonds. Trapping sites can be reduced by bonding the surface silicon atoms to another element like hydrogen or oxygen. Dilute hydrofluoric acid can be used to remove a surface oxide of silicon and terminate the surface with hydrogen atoms.[37] The hydrogen terminated surface is metastable and the surface will oxidize in the presence of dry oxygen or water. The growth of SiO_2 on Si is a self-limiting process that occurs over a 10 minute time period.[38] The presence of an oxide can lower the trap density down to 10^{11}cm^{-2} after annealing in a forming gas solution. A forming gas is typically a mixture of an inert gas or N_2 with H_2. The presence of H_2 increases the number of hydrogenated bonds on the silicon atoms not

bonded to the oxide.

No surface state could be formed on devices that had the oxide removed prior to the application of the ionic liquid. Attempts were made to decrease the roughness of the silicon surface by annealing but this procedure also did not produce a functional device. Silicon surface states could be formed on devices where the oxide was regrown at room temperature with the use of ozone. These devices were not as conducting as devices that were made using the native oxide that was formed on the wafer at the factory. Most publications on transistor fabrication focus on very thick oxides that would reduce the capacitance of the IL transistor. Further study is needed to produce good quality thin oxides with low oxide charge, uniform coverage, and low surface roughness. Available cleanroom tools were considered to follow Volmer–Weber growth mode of cluster nucleation as opposed to layer by layer or Stranski–Krastanov growth.[39] Atomic layer deposition (ALD) tools have promise for the formation of thin uniform oxides.[40] In addition, SiN has been found to be an effective passivation layer.[41, 42]

All the devices presented in this dissertation used the native oxide as a passivation layer and ellipsometry measurements indicated the oxide was roughly $15 - 20$ Å thick. The sample contacts were made of a metal stack of Al, Ti and Au. Al makes ohmic contact to p-type silicon and also has the potential to create an enhanced hole doped region under the contact. Aluminum has the added benefit of making ohmic contact to the underlying silicon by dissolving the surface oxide.[43] The Al_2O_3 that forms will diffuse into the bulk Al. The layer of Au on top of the metal stack was to reduce any electrochemical effects the Al contacts may encounter from electrostatic gating. Titanium was used as a diffusion barrier during subsequent annealing as Au atoms in silicon devices are recombination centers. All 3 metals were deposited in the same sputtering chamber without breaking vacuum and were patterned with a shadow mask.

The metal stack was annealed at 350°C in a forming gas solution for 5 minutes. The annealing temperature was chosen to be well under the Au/Si eutectic temperature of 380°C.[44] There was some interdiffusion of the three metals which occurred in the annealing process. The first few samples were made in a modified process where Al was deposited and annealed before the deposition of Ti and Au. In the latter, case one must remove the samples from the sputtering chamber for the annealing step and the devices were the same as those produced using the aforementioned procedure. Figure 2.6 is a typical resistance vs temperature measurement of the bulk wafer.

2.4.2 Sample design

In some samples, a SiN layer was deposited to define the channel exposed to the IL. In those cases the SiN layer was grown by Plasma Enhanced Chemical Vapor deposition and pattered with UV lithography using a single layer of Shipley's 1813. Both Hall bar geometries and square patterns were made with SiN. Hall bar patterns were made using positive UV lithography and an image reversal process.[45] The photo masks were designed for material deposition into Hall bar patterns. Positive lithography was chosen as the resist sidewalls will have a negative slope after the image reversal process.[45] With positive lithography exposure to UV light increased the solubility of the resist to a developing solution. The image reversal process involves an additional chemical reaction within the photoresist before development. Exposure to NH_3 will cause the portions of the resist that are more soluble due to UV exposure to harden and become nonreactive to the developing solution. After the image reversal process, the wafers were flood exposed to UV light to chemically activate the previously unexposed regions after which were developed away. Square pattern geometries were also formed using positive photoresist lithography but in this case the pattern on the photo mask did not require the use of the image reversal process. The relatively large 0.5mm square contact pads

were covered in Kapton tape so as to not coat them with SiN during the deposition.

A glass cylinder was used to contain the IL on the Si surface. Some cylinders had an inner diameter that was slightly larger than the area of the square SiN pattern. In some samples the smaller diameter cylinder was used to define the sample area and the insulating SiN layer was not deposited. In this case the the cylinder was positioned with the assistance of an optical microscope to ensure that the 4 metal electrodes would be exposed to the liquid. Any unexposed Si would be an insulator, isolating an electrode from the surface state at low temperatures. The cylinders were attached with Epoxy 220 and allowed to cure for the manufacturer's allotted time. In some cases the IL was found to have escaped confinement after several thermal cycles. While possible that the IL acts as solvent for the epoxy, several samples were observed to be very robust. A few samples were each used in up to four different gating experiments, being removed and cleaned in propanol between each experiment, with no signs of liquid loss after each measurement.

Second generation devices made use of a planer side gate, a configuration that does not require the attachment of a glass cylinder to the sample surface. Figure 2.8 is an example of a second generation pattern but with a planer gate. The gate must be sufficiently insulated from the wafer as as to not short the EDLT. The conductivity between the gate and the wafer at 230 K for the sample in the figure was too high for a proper gating experiment. Although work is being done to improve second generation devices, all data presented in the following Chapters were taken using the first generation devices.

2.5 Summary

To induce an IL liquid surface state in Si, ohmic contact was made to p-type Si wafers. A glass cylinder was epoxied to the Si surface with a with Pt. metal coil inserted as a gate

electrode. The cylinder was filled with the IL, DEME-TFSI before each measurement. If the sample was removed from the cryostat, the liquid would be removed and new IL used before another experiment. A PPMS was used for the measurements as modulation of the carrier density must be done with the IL in a liquid state. DEME-TFSI freezes at 200 K. The gate voltage was adjusted at 230 K with all the sample contacts grounded. At 180 K the contacts were ungrounded and resistance measurements were made using the van der Pauw method.

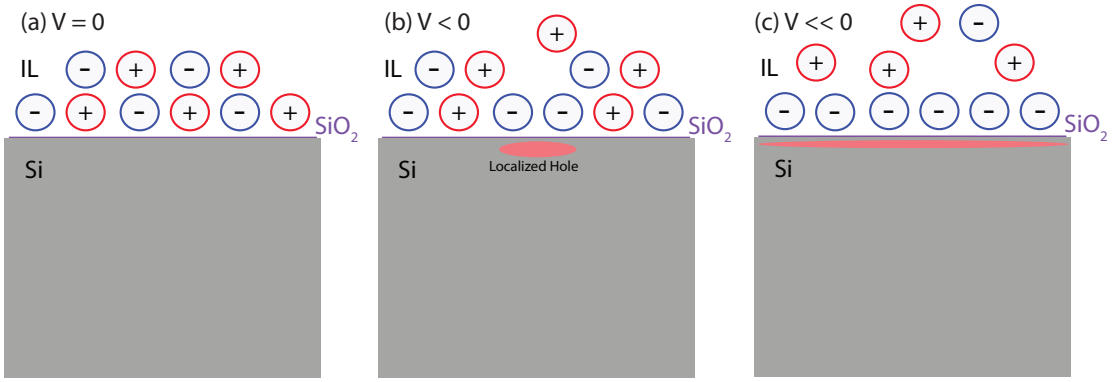

Figure 2.1: Cartoons of an EDLT transistor at different values of V_g. The gate electrode is not shown. In each case the cations on the gate are assumed to exhibit the same behavior as the ions at the IL to sample interface. (a) IL to sample interface at $V_g = 0$. (b) At low carrier densities and with $V_g < 0$ excess anions will repel electrons from the sample surface. Here the anions are treated as dilute descrete quantities on the sample surface. This model is discussed in greateer detail in Chapter 3 (c) EDLT cartoon when $V_g \ll 0$. The anions are viewed as a uniform sheet of charge in the high density limit.

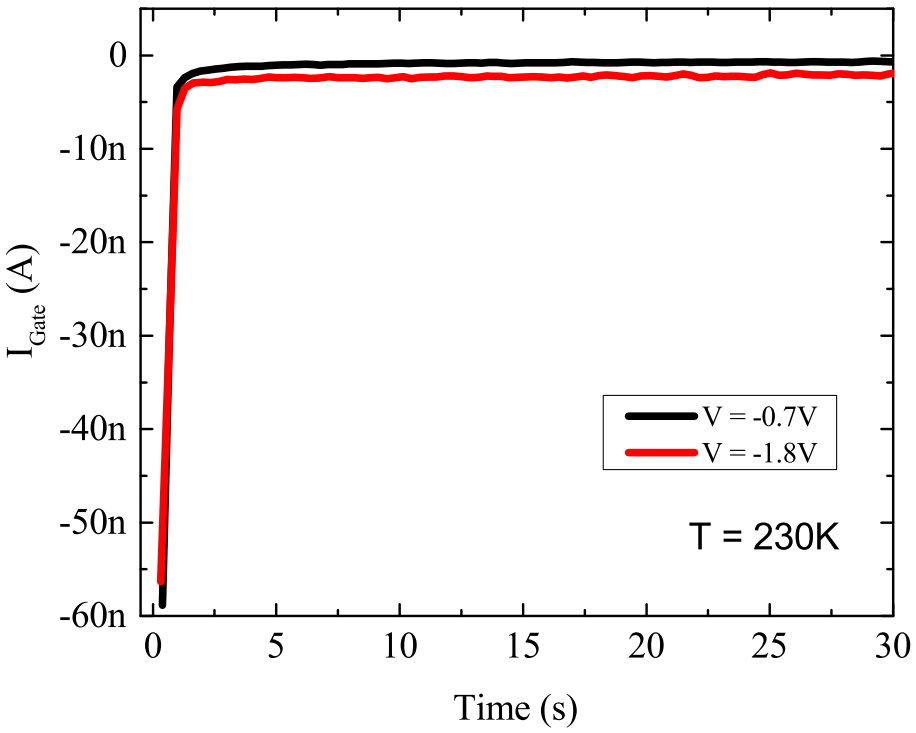

Figure 2.2: Current measured by an ammeter in series with the sample and the gate during charging. The charging curves were recorded for each increment of the gate voltage. Plotted are an example of two of the curves. From the graph one can see that the current decays to the background level within the first few seconds and the background level increases with gate voltage. To determine charge transferred to the sample surface the gate, current was integrated as a function of time up to 10s subtracting off the average current level taken from the 20s to 30s time interval.

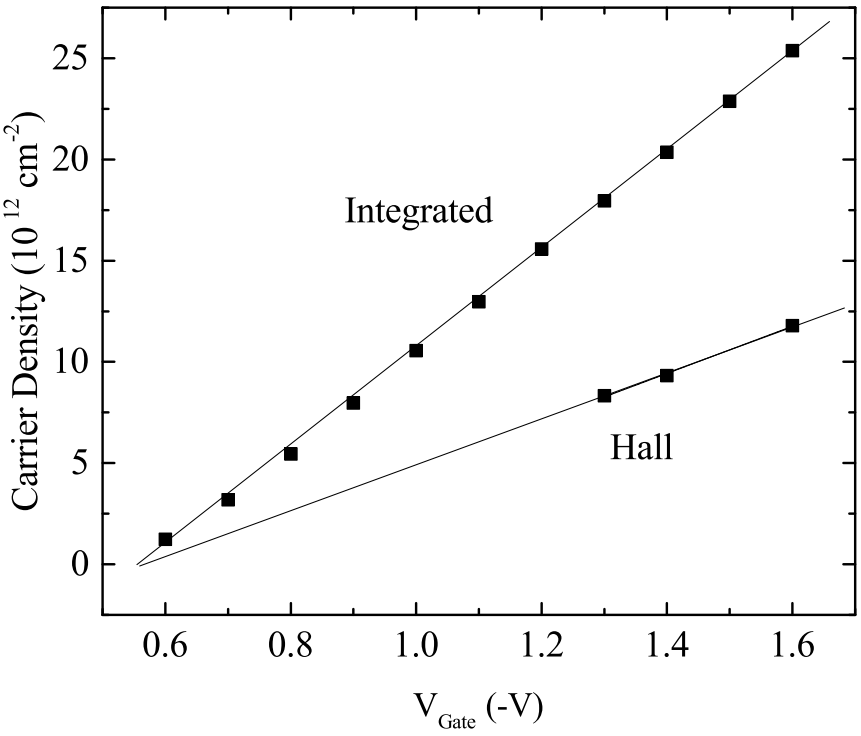

Figure 2.3: Carrier densities as a function of gate voltage calculated using the integration method and determined from the Hall coefficient at 2 K. Both methods produce a linear carrier density as a function of gate voltage. For multiple samples the Hall slope is typically half of the slope found by the integration method. Extrapolation of the Hall carrier density to the origin predicts that the onset of conduction should occur near $V = -0.6$ V which was the case for this sample. The integrated carrier density was determined by counting only charges transferred to the surface after V_T, determined by the onset of conduction, was reached.

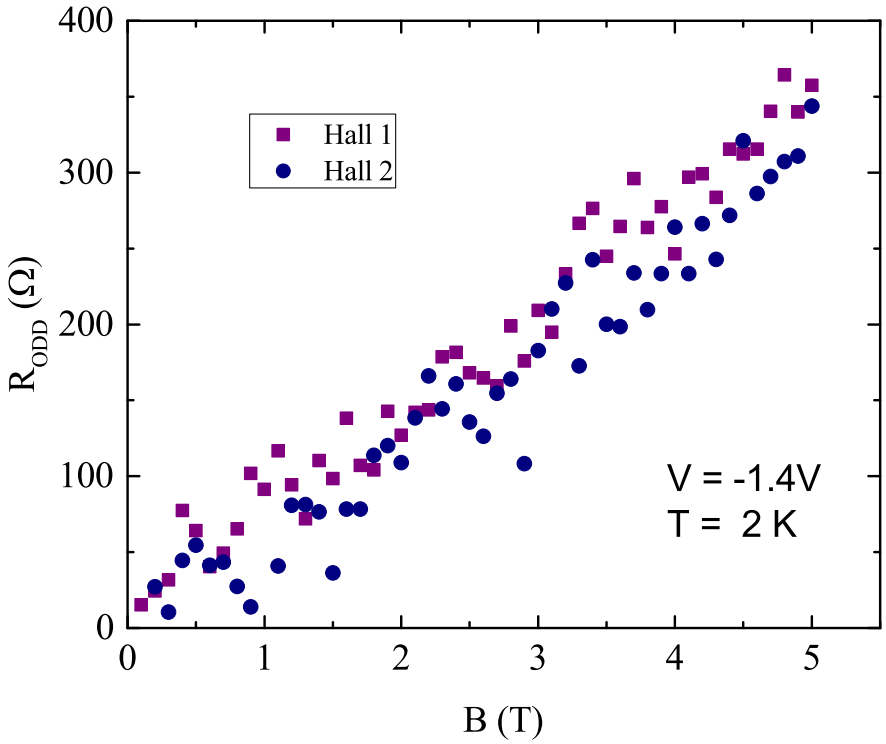

Figure 2.4: Example of Hall effect data taken at $V = -1.4$ V for both Hall orientations. The data was taken from -5 T to 5 T and R_{ODD} was calculated using Eq. 2.9. The two curves represent orthogonal measurement in of the van der Pauw geometry for Hall effect measurement.[34] Both slopes agree with each other and the scattering of the points leads to Δn of 2%. The voltmeter was connected in an orientation where holes would produce a positive slope with field.

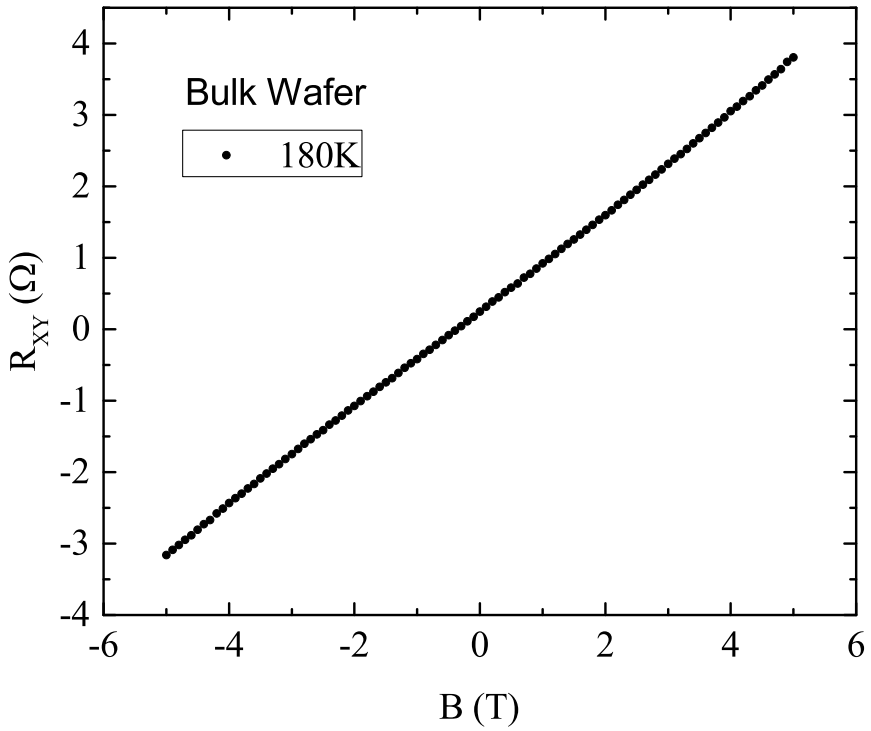

Figure 2.5: Transverse resistance, R_{XY}, vs magnetic field at 180 K. The Si wafers were 500 μm thick. The volume carrier density determined from the wafer thickness and the slope of the graph was calculated to be 1.6×10^{16} cm^{-3}. The voltmeter was connected in a manner where holes produced a positive Hall resistance. 180 K is well above the freezeout range for such a high doping. The measured carrier density was determined to be an accurate measurement of the extrinsic carrier density.

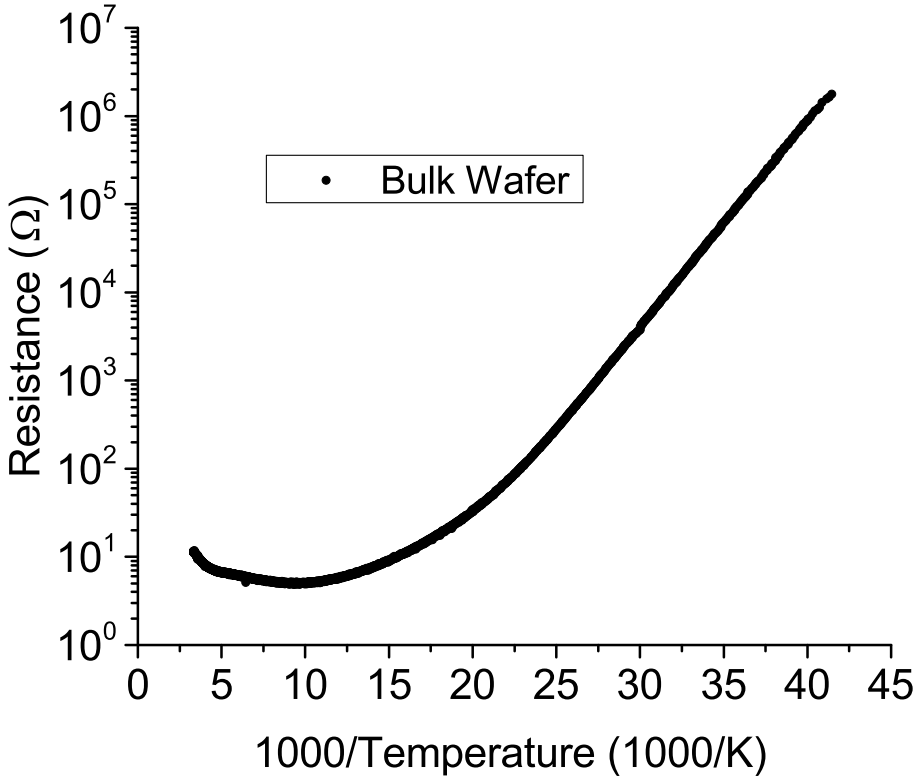

Figure 2.6: Resistance vs temperature for boron doped Si after annealing. The x-axis was scaled to match standard industry plots of semiconductor resistance vs temperature. After annealing to make ohmic contact to the bulk Si wafer several samples were screened though the PPMS to make sure the contacts to the wafer remained ohmic. The figure is a standard curve for a sample determined to be good.

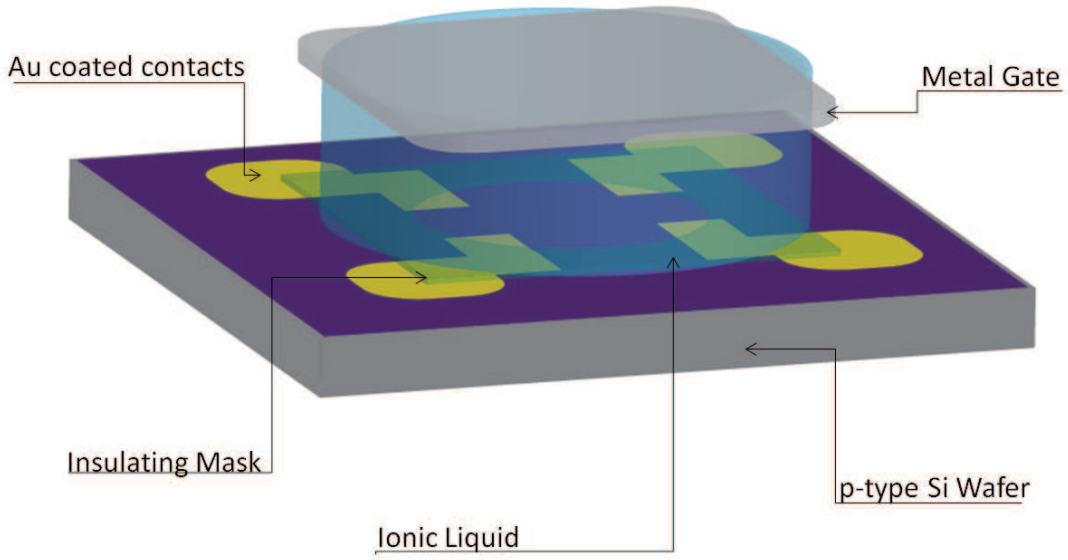

Figure 2.7: Cartoon of the device used to measure silicon surface states induced by an ionic liquid. The contacts were an annealed stack of Al, Ti, and Au. A layer of SiN used in some samples as an insulating mask to define the gated channel. Not shown is a glass cylinder epoxied to the surface that was used as a containment vessel for the IL. The metal gate was a Pt. coil submerged in the IL and is depicted as a planer gate for clarity in the figure.

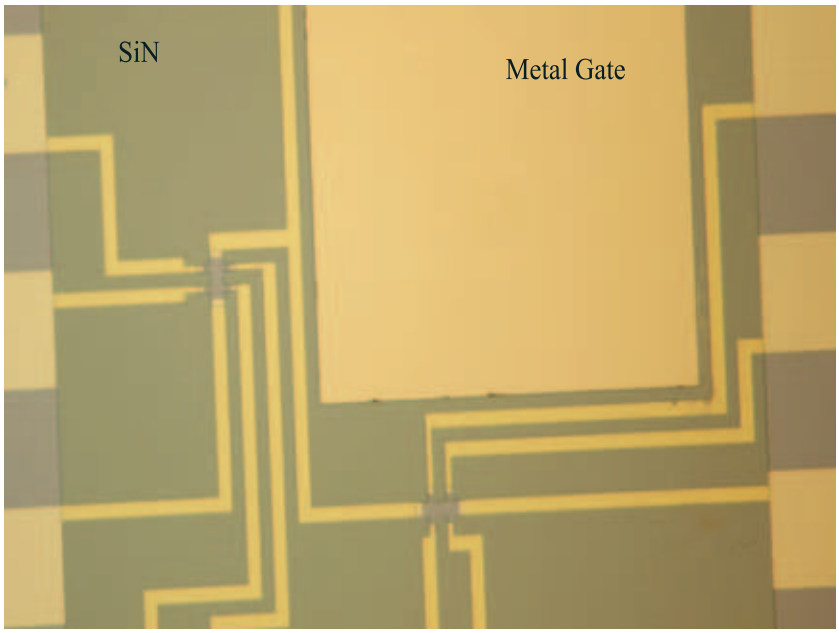

Figure 2.8: Photograph taken with a microscope camera of a completed second generation device. Second generation devices employed a planar side gate that does not require the use of a metal coil submerged within the liquid and as well as a glass containment vessel. The use of epoxied cylinders was sometimes a point of failure for the experiment. Instead a drop of IL would be applied directly to the wafer covering both the sample area and the wafer. A cover glass in addition to the liquid surface tension was sufficient to hold the liquid in place. Because of the high conductivity of the bulk wafer, side gates must be sufficiently insulated from the wafer at gating temperatures to prevent shorting the transistor. In the pictured device, the conductivity between the gate and the wafer was too large at 230 K for a proper gating experiment.

Chapter 3

2D Silicon Surface State and Hopping Conduction

3.1 Introduction

This chapter will focus on gating with an ionic liquid (IL) at carrier densities below 10^{12} cm^{-2} along with a model for the process. When the IL is in contact with the Si wafer, there are both cations and anions on the SiO_2 surface. The ions have cylindrical geometries that when approximated as a sphere, the radius of the anion TFSI is roughly 4.4 Å.[46] whereas the cation DEME is slightly larger. Based on the size of the ions there are roughly 10^{15} ions cm^{-2} at the sample surface. Being equal in number and opposite in charge has the result that there will be no net charge over the whole sample surface. When the gate is negatively biased excess, anions will be driven towards the Si surface leaving it with a net negative charge. The result is that electrons in semiconducting Si are repelled by the charged surface leaving behind a screening cloud of holes. The screening holes will form a 2D conducting layer just below the Si surface at non zero temperatures.

The configuration is similar to that of Fowler were 2D electron surface states where created by implanting Na^+ into the SiO_2 layer and diffusing them to the interface. In these experiments, the Na^+ ion produced a screening electron cloud at the Si/SiO_2 interface. The conductivity of the surface layer as a function of temperature was shown to follow a two parameter function of the form

$$\sigma_{2D} = \sigma_1 \exp(-\epsilon_1/T) + \sigma_3 \exp(-\epsilon_3/T) \tag{3.1}$$

where ϵ_i is an activation energy and σ_i a conductivity prefactor.[26] The first term represents activation to the mobility edge with energy $\epsilon_1$which is observed at high temperatures. The second term represents nearest neighbor hopping of electrons between the surface states. Section 3.2 covers the theory of nearest neighbor hopping in greater detail. We would like to understand the physics of ionic liquid gating at low carrier densities similar to those employed in the Na^+experiments, which were 10^{11} cm^{-2}.

At densities of 10^{11} cm^{-2}, the number of anions leading to the formation of the screening layer is much less than the total number of anions on the oxide surface. This is thought to be due to the large number of cations that will also be on the sample surface. In our model, equal numbers of cations and anions can be treated as a neutral background. Treated this way, the excess anions are the equivalent of isolated charges. If this model is accurate, the physics of the screening hole layer should follow the same physics as screening electrons induced by isolated Na^+ ions. An example of this mapping is shown in Fig. 3.1. To test the validity of treating the ions as a series of discrete isolated charges, ϵ_3 and σ_3 were measured at densities similar to those measured in the Na^+ experiments. A comparison between the two experiments is made in Section 3.5. Other sections of this thesis will cover the physics of surface state conduction in Si for carrier densities between 10^{11} cm^{-2} and 10^{12} cm^{-2}. Data for $n \geq 10^{12}$ cm^{-2} is discussed in Chapters 4 and 5. The following section summarizes some of the relevant theory for the case of bound charges due to Na^+ atoms embedded in the oxide[26, 36]

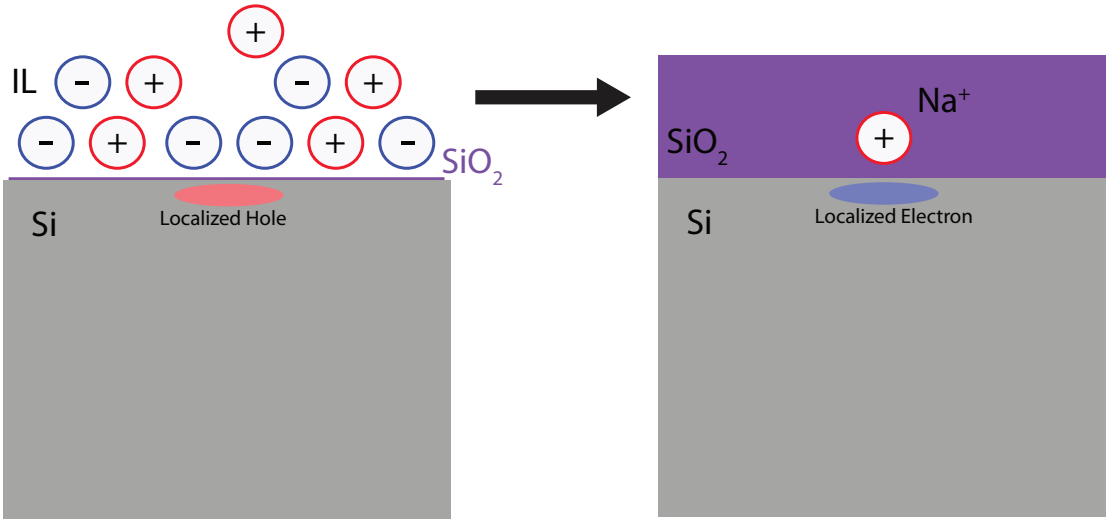

Figure 3.1: Illustration of ionic liquid carrier induction in the low density limit. Here we will compare the IL induced Si surface state to the one formed by Na^+ implanted in the oxide at the SiO_2 interface. The remarkable agreement between the two suggests excess quantities of one type of ion can be treated as isolated charges with a neutral background.

3.2 Nearest Neighbor Hopping Theory

When Group V elements are substituted for Si in the lattice, the extra electron is found to be bound to the donor with a hydrogen-like energy spectrum. Electrons bound to positive charges in the oxide are also found to have a hydrogen-like binding energy. Initially at low carrier densities the Na^+will act like donors and form electron bound states in the silicon layer. The electron and Na^+ are attracted by the Coulomb potential

$$V = \frac{e^2}{\kappa r} \tag{3.2}$$

where κ is the average of the dielectric constants of Si and SiO_2. The screening electrons have hydrogen-like wave functions that decay as $\exp(-r/a)$.[26]

3.2.1 2D Surface State

In the 2D limit of the screening layer, the electrons are considered to be confined to the interface. In actual devices, there is a thickness to the screening electron layer. An approximation of the thickness of the layer can be made by

$$g(z) = \frac{b^3}{2} z^2 \exp(-bz) \tag{3.3}$$

where z is the distance in Si from the interface and b is a parameter calculated to minimize the total energy per electron in the screening layer.[26] The potential barrier at the interface is large enough that the electron wave function must go to zero at $z = 0$ and be entirely confined to the Si layer. The parameter b is a measure of the average depth, z_0, of the charge layer in Si given by

$$z_0 b = 3 \tag{3.4}$$

At $n \sim 10^{12}$ cm^{-2} , the charge density as a function of thickness was calculated for accumulation and inversion devices and the calculation produced a peak in the density

roughly 30 Å from the interface.[47]

3.2.2 Mechanism of Conduction

As the number of Na^+ ions increases, distance between two neighboring bound states will decrease and the wave functions will begin to overlap. Once the wave functions overlap, electrons will be able to tunnel between neighboring bound states. The process is referred to as nearest neighbor hopping and expressed as the second term of Eq. 3.1 with the hopping activation energy ϵ_3 that is lower than ϵ_1.[26] At higher densities the states form an impurity band.[48] At even lower temperatures and very high resistance, it is proposed that variable range hopping can occur thus requiring a third term to be added to Eq. 3.1. The temperatures and resistance required to observe variable range hopping are not within the accessible parameters of the low carrier density IL experiment.

3.3 Ionic Liquid Surface State in Silicon

In our experiment, ohmic contact was made to a boron doped Si wafer. In addition to the surface conductivity induced by the ionic liquid, the wafer has conductivity due to bulk conduction. Figure 3.2 shows the natural logarithm of the sheet resistance as a function of temperature for an ionic liquid gated Si sample. At temperatures below 50 K, the resistance was initially independent of the applied gate voltage and followed

$$R_S = \frac{1}{\sigma_{Bulk}} \exp(T_A/T) \tag{3.5}$$

where $T_A = 43$ meV. Boron acceptors in silicon have an activation energy $T_A = 45$ meV so we attribute the measured resistance to the conduction of the bulk wafer.[36] Influence on the conduction due to the ionic liquid induced surface state is seen only at temperatures below 20 K, but at low gate voltages a surface state is not observed.

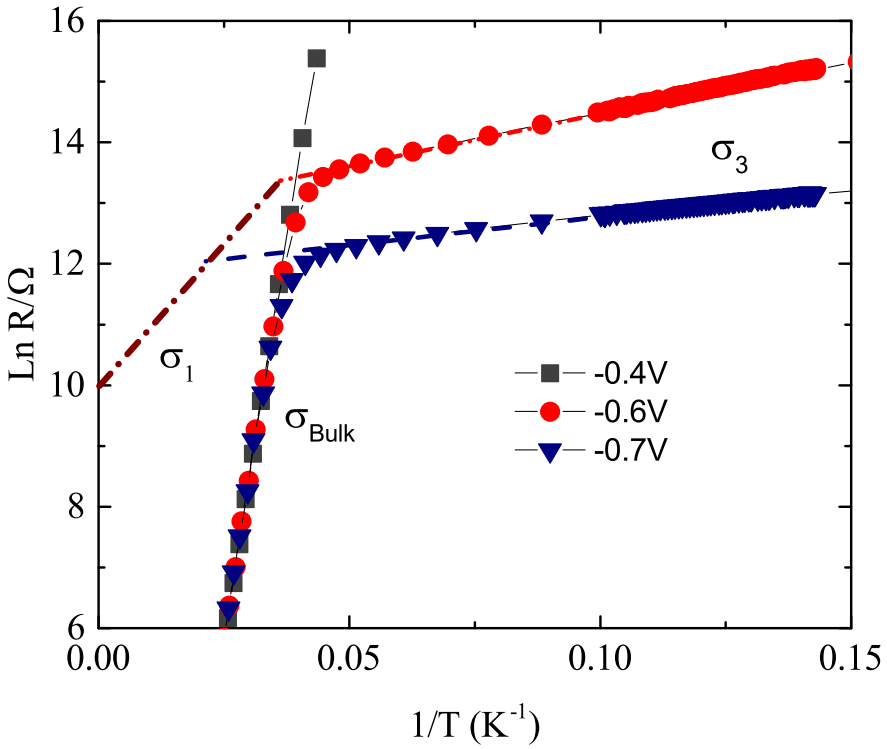

Figure 3.2: Natural logarithm of sheet resistance plotted as a function of inverse temperatures. At high temperatures, the resistance is independent of gate voltage where at lower temperature a conduction surface state is observed. The dotted lines are guides to the eye showing that conducting due to σ_1 is completely shorted by bulk conduction.

Semiconductor surfaces can exhibit either p or n type surfaces with silicon typically forming an n-type surface.[36] It is believed that the observed effect is do to trapped positive charge within the oxide. If the trapped charge is in p-type Si, and is large enough, a natural inversion layer is formed on the surface. Although rare, the behavior was observed in some samples.

In all samples we observed a threshold voltage,V_T, for surface conduction. Interface charge and trapped positive oxide charges are thought to exist at the Si/SiO_2 interface. This results in a downward bending of the energy bands.[36] A different V_T was observed in almost every sample and we interpret this as a different amount of band bending for each sample. This is also supported by the observation of electron surface states in some ungated samples. In the latter case, application of a negative V_g will first dissipate the electron surface state before a hole conducting state is formed.

The resistance in hopping conduction has an exponential temperature dependence. Other forms of conduction such as 2D Mott or Efros-Shklovskii variable range hopping have a stretched exponential temperature dependence with $x = 1/3$ and $x = 1/2$ respectively, where x is the temperature exponent of

$$R = R_0 \exp(T_0/T)^x \tag{3.6}$$

One method of determining x is by measuring the slope of w vs T on a log-log scale where

$$w = \frac{d(lnR)}{d(lnT)} \tag{3.7}$$

[49]. This is shown in Fig 3.3 where a red dashed line with a slope $m = -1$ corresponds to the value $-x$ in Eq. 3.6. This shows that the IL surface state in Si has a temperature dependence consistent with the nearest neighbor hopping model. To test the hypothesis that the surface state was due to nearest neighbor hopping we measured ϵ_3 and σ_3 as a function of carrier density n in the low density limit was performed. The results of the

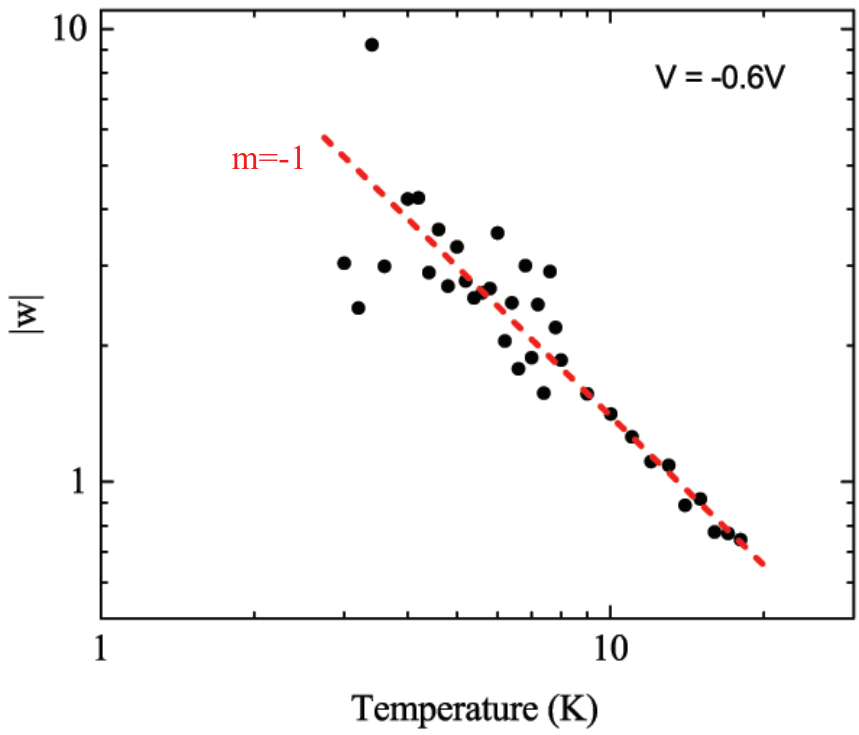

Figure 3.3: Log-log plot of w vs T . The data is plotted for one of the curves in Fig 3.2 below 20 K. The dashed line is a guide to the eye, but is the expected slope for Arrhenius behavior. At 2 Kthe resistance was nearly 10% of the input impedance of the measurement system. Data from 2 K to 5 K were not in the calculation used to produce the Zabrodskii plot.

experiment are discussed in the following sections.

The surface states in Fowler's work had two Arrhenius conduction regimes as seen in Eq. 3.1. Accounting for the fact that the IL ions will be at the SiO_2 surface, the binding energy of a hole to the anion results in $\epsilon_1 = 8$ meV. At high temperatures, the first term will be shorted by bulk conduction as $\sigma_{Bulk} \gg \sigma_1$. The experiments performed by Fowler were on inversion mode devices where the bulk was isolated by the depletion layer. Estimates for the two conduction terms are drawn as dashed lines in Fig 3.2 and the transition from conduction associated with ϵ_1 to that given by ϵ_3 is also thought to be shorted by the bulk; therefore only surface conduction due to nearest neighbor hopping is measurable in this experiment.

3.4 Low Carrier Density and High Resistance Measurements

The low carrier density limit was studied by first increasing V_g until a surface state was formed. Carriers were then removed from the surface by decreasing V_g in small steps. The low temperature activation energy and prefactor were measured at each step. This was done to minimize the measurement time as V_T will depend on several unknown microscopic parameters.

Below V_T, no surface state can be seen this is thought to be due to the trapped positive charge in the oxide, as mentioned above. The negative ions that move to the surface are first attracted to the fixed positive charge. The effect is to dissipate a screening electron attached to the oxide charge. Once all the oxide charge is saturated, the additional negative ions will then form a screening hole gas in the sample. Based on the capacitance of the ionic liquid transistor and V_T the trapped charge could be as numerous as 10^{12} cm^{-2}. While this number is larger than the number of anions

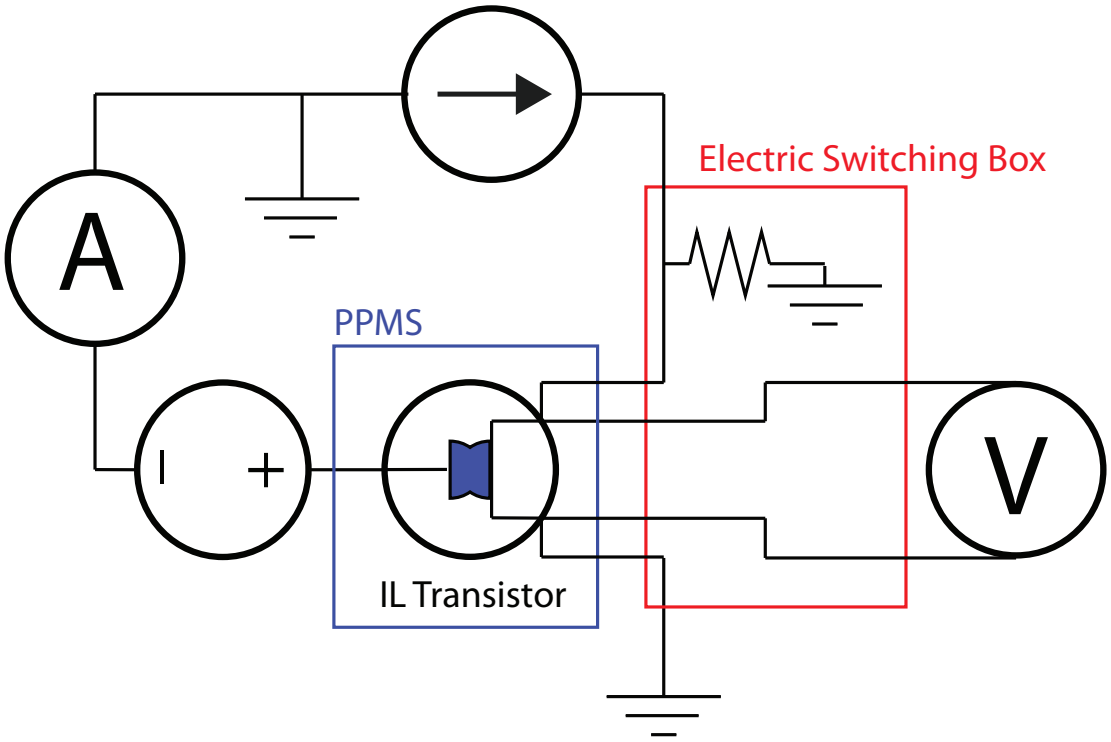

Figure 3.4: Electrical schematic of IL gated Si. The high resistance short is thought to be in the Keithley electrical switching card used to permute the contacts. The data sheet for a Keithley 7012 suggests the isolation to ground > 1 GΩ. The input impedance of the voltmeter is > 10 GΩ. Removing the electrical switch only lead to a marginal increase in measurable resistance suggesting that there is an additional impedance to ground preventing higher resistance measurements. The additional limiting impedance is thought to be in the PPMS and could be overcome with the use of external user run wires. In addition resistance measurements > 10 GΩ will require the use of an electrometer to measure the voltage drop across the sample. Electrometers can have an input impedance of > 200 TΩ.

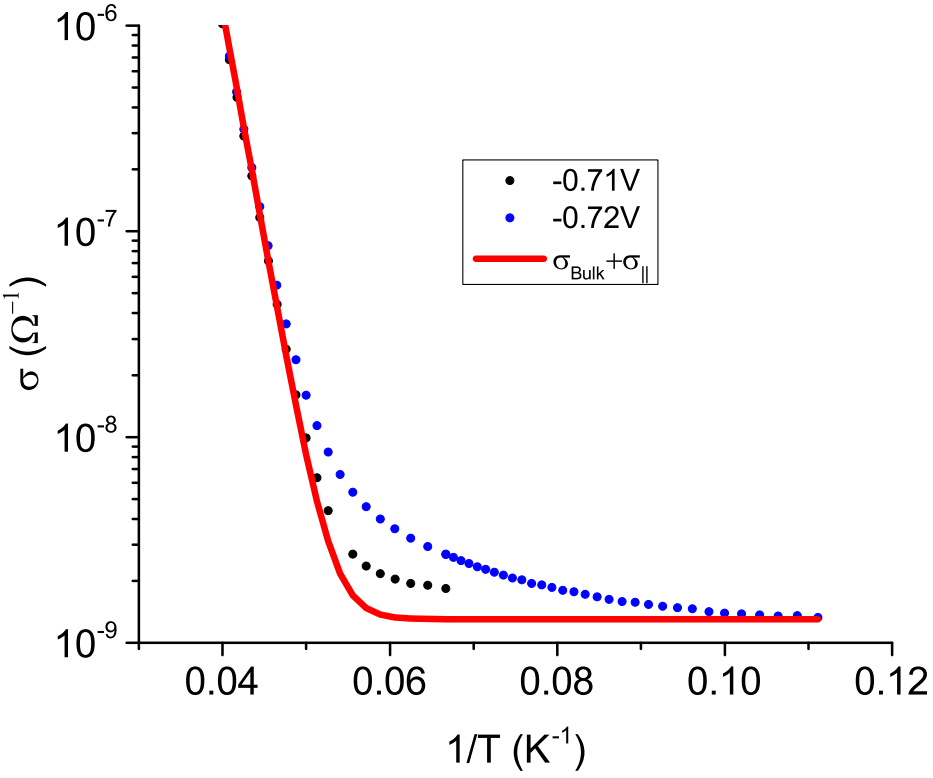

Figure 3.5: Conductance vs inverse temperature for the two lowest gate voltages. The red line is a calculation of the net conductance thought to be due to the bulk wafer and a parallel conduction channel of the level of GΩ within the measurement electronics. V_T was determined to be between -0.71 V and -0.72 V with an error of $\pm$5mV. The surface state at -0.72 V was not analyzed as carrier density and error would be of similar size.

contributing to the surface conducting state, the inferred number of trapped charge is much smaller than the number the positive ions, $\sim 10^{15}$ cm^{-2}, that are within the ionic liquid.

The highest resistance measurable in the experiment was limited by the input impedance of an electrical switch used to permute the sample leads for van der Pauw measurements. Each line in the switching card had an impedance on the order of 1 GΩ to ground. We modeled the sheet conductance, depicted in Fig 3.4, as

$$\sigma = \sigma_{Bulk} + \sigma_3(n) + \sigma_{||} \tag{3.8}$$

where $\sigma_{||}$ was the conductivity due to parallel current paths to ground. The data for σ_{Bulk} was determined from the change in resistance between 50 K and 20 K for measurements where $V_g < V_T$ during the initial charging process. In Fig. 3.5 we plot the conductance as a function of temperature for the two lowest measured gate voltages after forming the surface state. The red line is a calculation of the conductance expected from the bulk wafer, σ_{Bulk}, in parallel with a 1.3 GΩ resistor. The input impedance of our electrical switch box has an input impedance of > 1 GΩ. The value of the resistor was chosen so that the calculated value matched the lowest temperature conductance measured at $V = -0.72$ V. From results presented in Fig. 3.5, it was determined that $-0.71\text{V} \leq V_T < -0.72\text{V}$. Based on the voltage step size, the error in the accuracy of zero charge is $\Delta n \pm 6 \times 10^{10}$ cm^{-2}. The conductance vs temperature for $V = -0.72$ V indicates there is excess conductance not accounted for by the bulk. We attribute the excess conduction to the presence of a surface state. While parameters for the surface state could by extracted by subtracting off the calculated curve, this was not done as the calculated carrier density would be of similar magnitude to the carrier density error.

Carrier densities were calculated by the integration method starting from V_T . Figure 3.6 shows the conductance as a function of temperature and carrier density for the

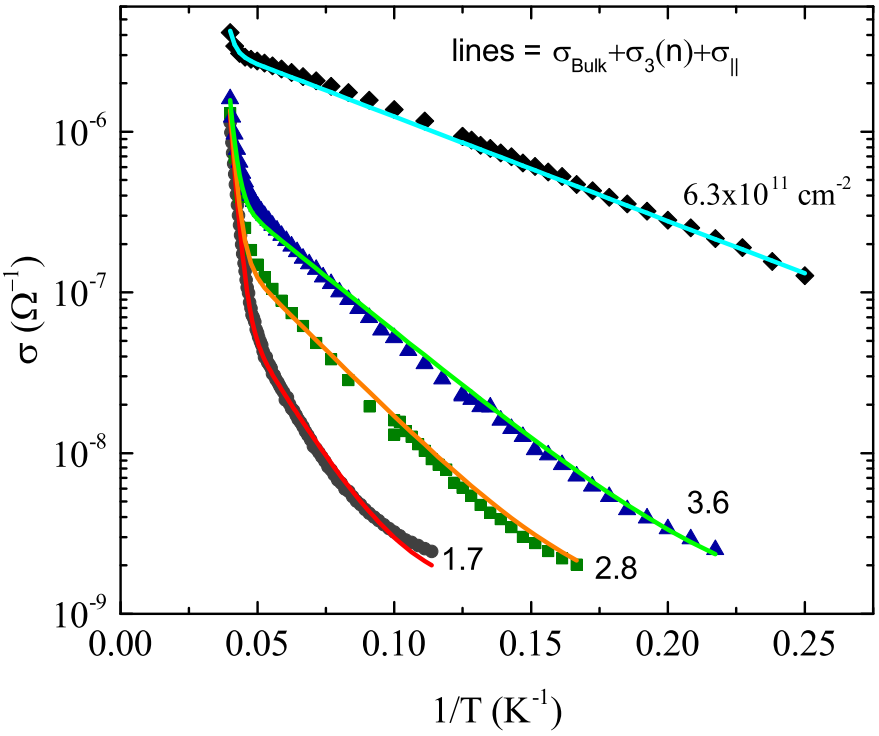

Figure 3.6: Conductance of silicon surface states plotted vs inverse temperature. Data for four surface states is plotted over the full measurement range. The lines are fits to the conductance assuming three contributions. The bulk conduction parameters were extracted from the linear regime at high temperatures with no surface state. The parallel conduction channel was determined by the low temperature limit of the -0.72 Vcurve in Fig. 3.5. The parameters for the σ_3 term were determined from the visible straight line portions of the data. The fits show good agreement with the data and that above 100 MΩ the source current is not confined to the sample; therefore data for $R_S \geq$ 200 MΩ was masked for the nearest neighbor hopping analysis.

next four measured gate voltages. For the low carrier density measurements, the conductivity due to the input impedance of the electrical switch was noticeable when the sample resistance is larger than 100 MΩ. The lines on the figure are calculations of the conductivity from Eq. 3.8. The linear region in resistance was used to determine the parameters of nearest neighbor hopping conduction. The data is in good agreement with Eq. 3.8. Because of artifacts in the sample resistance measurement (caused by$\sigma_{||}$) data above 200 MΩ was masked and not considered in the determination of ϵ_3 and σ_3.

3.5 Hopping Conduction Analysis

Figure 3.7 shows the natural log of the sheet resistance as a function of inverse temperature. From this we can extract ϵ_3 and σ_3 from linear fits below 15 K. A mask to high resistance data was only applied to the three lowest carrier densities. The two highest carrier density measurements were measured down to 2 K but the data was not plotted to greater emphasize the low carrier density curves. In addition, two curves were omitted for clarity, as the data would overlap with that plotted in the figure.

Figure 3.8a is a plot of the activation energy as a function of carrier density for the curves shown in the inset. In addition the results for Si, the activation energy taken from Table III in the review by Ando *et al.* for Na^+ surface states were added for comparison.[26] In the experiments by Fowler, the carrier density was determined as the number of Na^+at the Si/SiO_2 interface. In the IL experiment, the carrier density was determined by integrating the leakage current which is a measure of the number of ions that moved to the SiO_2 surface. The activation energies as a function of carrier density overlap between the two experiments.

Plotted in Fig 3.9 is prefactor σ_3 as a function of the inverse root of the carrier density. The prefactor was determined form the intercept of the linear fits to the data

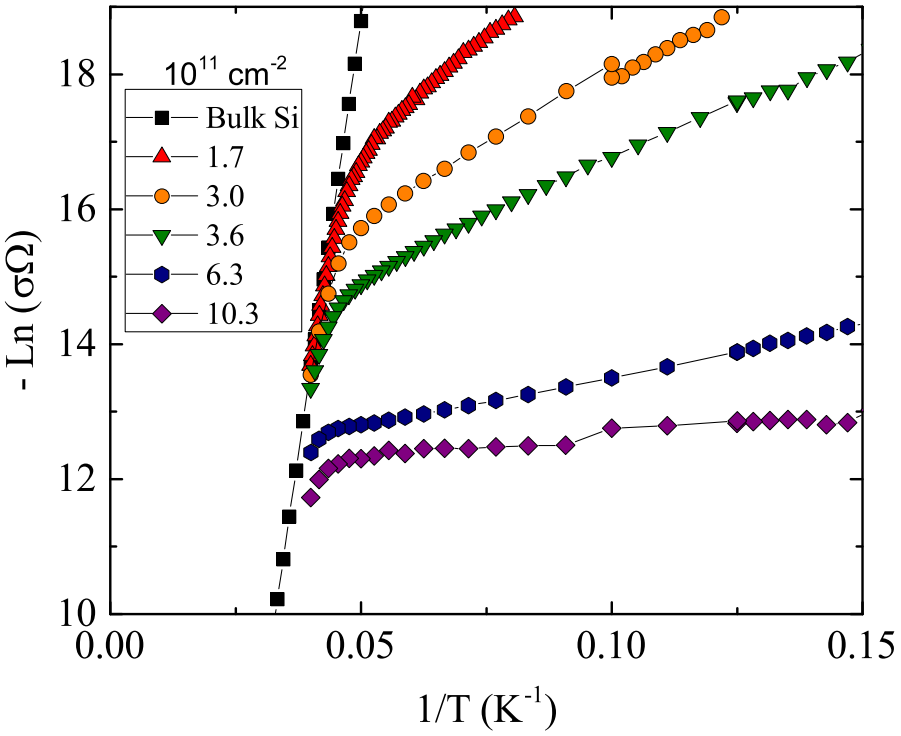

Figure 3.7: Natural logarithm of the sheet resistance as a function of carrier density. The data was taken by starting at the highest carrier density and depleting holes until the surface state was no longer seen. The carrier density was determined by the integration method with zero carrier density determined to be the onset of surface conduction. From this plot, ϵ_3 and σ_3 can be obtained as a function of carrier density.

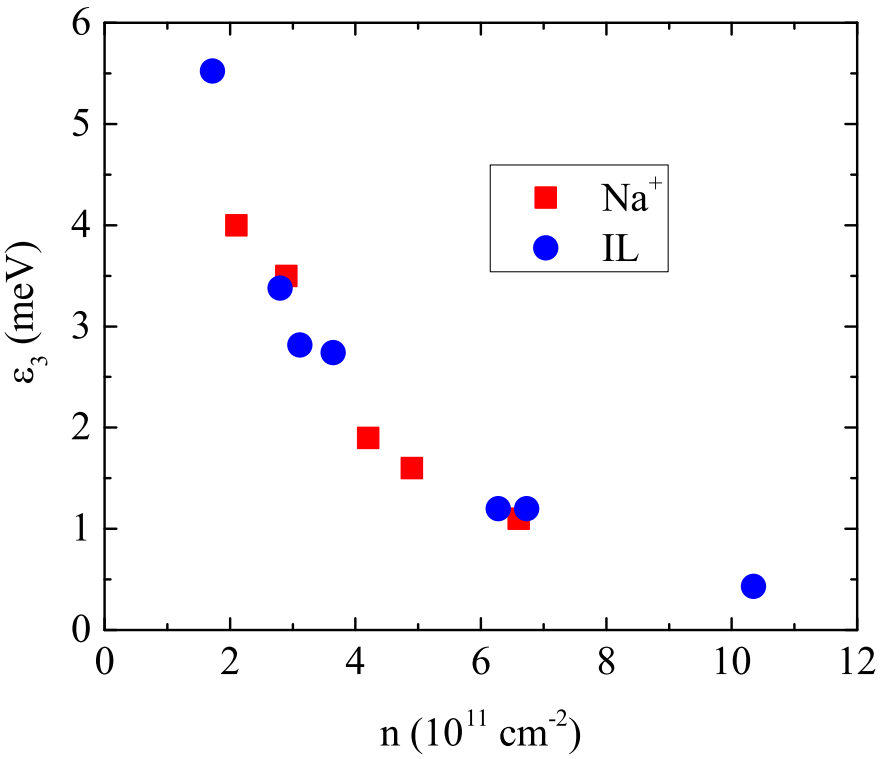

Figure 3.8: Activation energy as a function of carrier density. Data is plotted for the low temperature slope of the resistance plotted in Fig 3.7. In addition, data for activation energies reported for Na^+implanted Si are plotted. The error in the accuracy is $\Delta n \pm 6x10^{10}$ cm^{-2} while the error in the precision of the points is $< 10\%$. ϵ_3 for IL gated Si as a function of carrier density is in good agreement with nearest neighbor hopping conduction.

in Fig. 3.7. The wave function localization length, a, can be determined from σ_3 using

$$Ln(\sigma_3) \propto -2.4/\sqrt{na^2} \tag{3.9}$$

.[26, 50]

The x-axis was chosen to linearize the data following Eq. 3.9. The data for Na^+ was also taken from Table III.[26] For the decay length of IL gated Si $a_{\mathrm{IL}} = 83 \pm 20$Å.

The error for the IL localization length is dominated by the accuracy of V_T. In addition the value for the conductivity prefactor at the highest carrier density (1×10^{12} cm^{-2}) was not used to calculate the localization length. At such a high carrier density, the separation of holes will be comparable to the measured localization length and the data is expected to deviated from nearest neighbor hopping conduction. In other samples at higher carrier densities the surface state no longer follows Arrhenius behavior. This is discussed in Chapter 4.

3.6 Summary

By using an IL, a 2D hole gas was created at the surface of a p-type Si wafer. At carrier densities from 10^{11} cm^{-2} to 10^{12} cm^{-2}, the conduction mechanism for the surface state was determined to be nearest neighbor hopping. Excess negative ions on the SiO_2 surface attract and bind holes at the interface. As the carrier density increases, the wave functions overlap and electrons can hop between sites. Hopping conduction follows an activated form and was studied some years ago by diffusing Na^+ though SiO_2 onto the surface of Si. In a similar manner excess negative ions in an IL produce a surface conducting state in Si just like the Na^+ ions but with the opposite charge. This demonstrates that in the low carrier density limit, the IL can be treated as a series of discrete ions on top of a neutral background. It has also been shown that, in addition

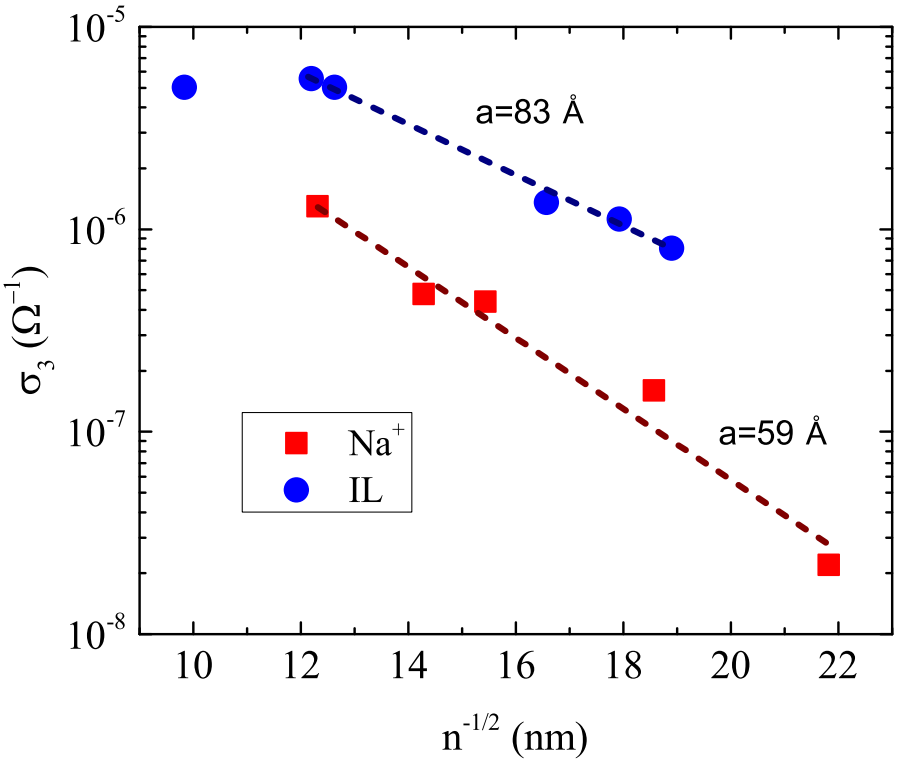

Figure 3.9: σ_3 on a log scale plotted against the inverse root of the carrier density. Plotted in this way the localization length a can be determined from the slope using Eq. 3.9. The error, $\Delta a \pm 20$ Å, for the IL gated data was determined from the carrier density accuracy.

to electrochemical processes, ILs can be used to electrostatically induce carriers on the surface of a sample. Further study is require to fully understand the difference between carriers induced electrostatically and those that are induced electrochemically. The physics of silicon is understood well enough that IL gating of Si can serve as a platform to produce a complete model of carrier induction by an IL.

Chapter 4

Silicon Metallic State

4.1 Introduction

In chapter 3, the details of IL gating of Si at carrier densities of 10^{11} cm^{-2} were discussed. Excess anions on the SiO_2 surface create bound states for holes near the Si/SiO_2 interface. When the wave functions of the holes overlap, conduction happens by tunneling between adjacent localized states. This chapter will focus on surface state conduction at densities of order 10^{12} cm^{-2} where the bound states give rise to an impurity band.[26] Figure 4.1 shows the sheet resistance as a function of temperature at different gate voltages as the surface state transitions out of the nearest neighbor hopping conduction regime. The high temperature conduction remains independent of gate voltage. This suggests that we are witnessing the evolution of the surface state, as evidenced by the changes in the low temperature data. Figure 4.2 is a Zabrodskii plot using data at a carrier density beyond that at which nearest neighbor hopping holds, with w defined in Eq. 3.7 . The resistance as a function of temperature for the sample plotted in Fig 4.2 is similar to that of the curve for $V = -0.7$ V of Fig. 4.1. The data in Fig. 4.1 was taken as a function of time as the sample was slowly cooled. The noise in the data was too

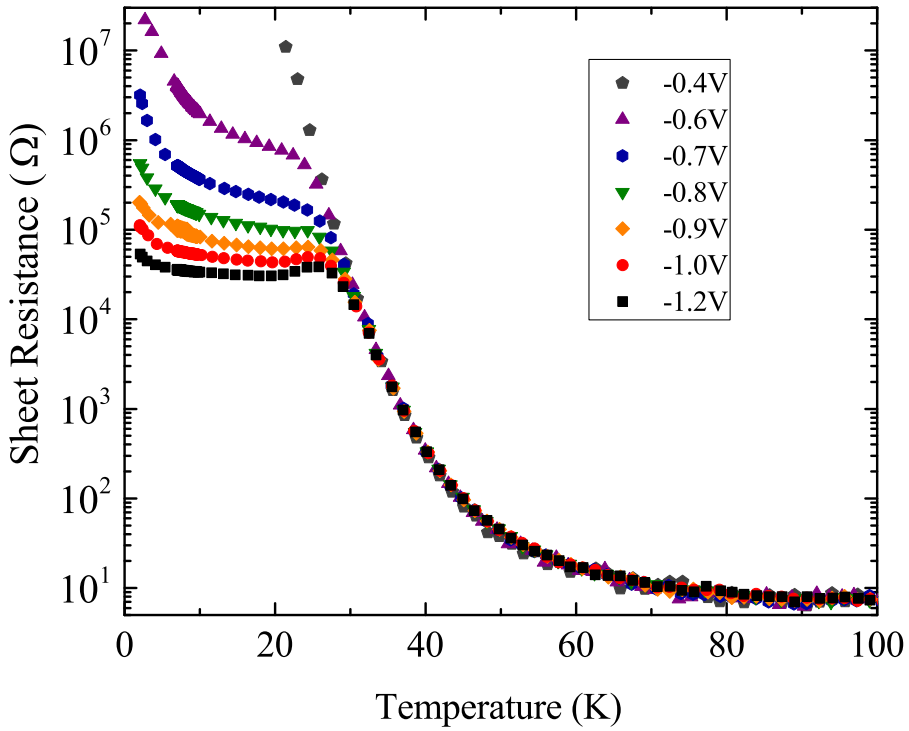

Figure 4.1: Resistance as a function of temperature plotted for several different gate voltages. The goal of the experiment was to study the high carrier density behavior. As high carrier densities the localized states will form an impurity band and conduction will no longer be due to Nearest Neighbor hopping conduction. Only the low temperature behavior is altered by measurements with increasing gate voltages indicating that we are still working with a 2D Si surface state.

large to extract an exponent from a Zabrodskii plot. The exponent of Eq 3.6 for nearest neighbor hopping is $x = 1$, where the activation energy decreases with increasing carrier density. At higher carrier densities, the exponent decreased to $x = 0.7$ and continued to decrease as the carrier density was increased further. The lowest exponent determined using a Zabrodskii plot was $x = 0.44$. As the sample continued to become less resistive, the change in resistance over the measured temperature range became insufficient to accurately determine the form of the conduction.

A surprising result was that at densities just below 10^{13} cm^{-2} an apparent metal insulator transmission (MIT) was observed, which is the subject of this chapter. Densities above 10^{13} cm^{-2} will be discussed in chapter 5, along with samples that did not display metallic behavior. The high carrier density MIT was a surprising results as it is believed not to exist in two dimensional systems. Data for the IL induced metallic state is presented in Section 4.3. A review of current MIT physics is discussed in section 4.2 with a possible theory for the high carrier density transition in section 4.4.

4.2 Metal Insulator Transition

It was previously believed that a metallic regime could not exist in a 2D system. As a function of carrier density, there would only be a crossover from weak to strong localization[51]. This scenario was confirmed experimentally in highly disordered silicon transistors almost 30 years ago with no metallic state being found. However, over time, as sample mobilities increased, metallic regimes were observed. The physics of the transition to 2D metallic behavior is still debated. The first observation of metallic behavior was by Zataritskaya and Zavaritskaya where n-type and p-type inversion layers were found to have a positive temperature coefficient of resistance at carrier densities above a critical carrier density n_c.[52] By extrapolating their data, one would expect that at zero temperature, there would be two possible ground states with either finite

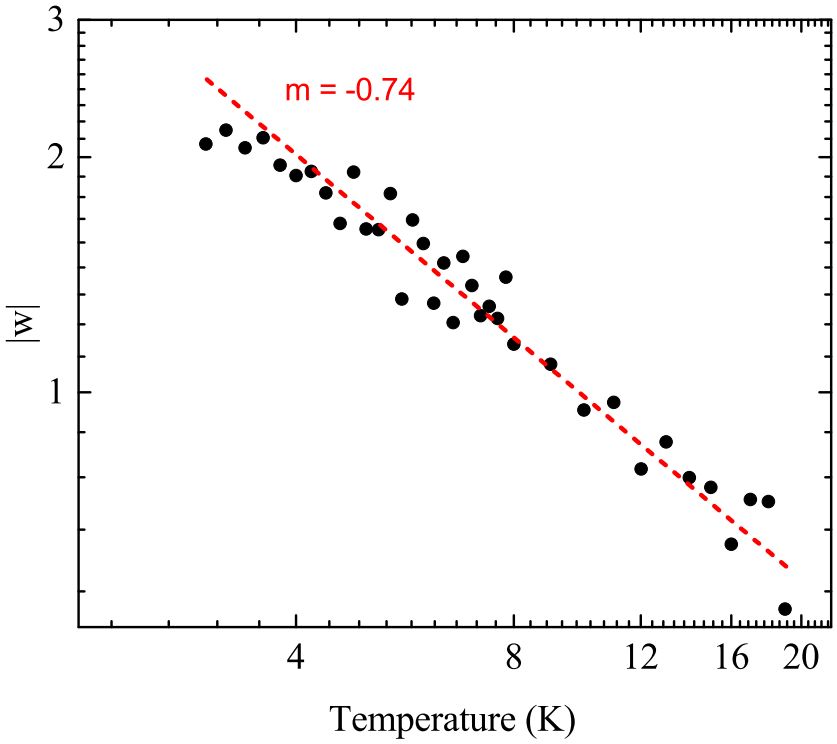

Figure 4.2: Zabrodskii plot beyond nearest neighbor hopping. The slope is no longer $m = -1$ indicating a deviation from activated behavior. At higher carrier densities the value of m will continue to decrease in magnitude. The change in resistance at higher carrier densities was of insufficient range to determine if 2D Mott or Efros-Shklovskii hopping was operative.

or zero conductivity determined by $n > n_c$ or $n < n_c$ respectively.

In this picture, the transition to the metallic state is an example of a Quantum Phase Transition (QPT).[53] At $T = 0$, by adjusting an additional parameter in the Hamiltonian it is thought that one can alter the ground state of the system. While defined for $T = 0$ any experimental measurements must be made at a finite temperature and with a finite size limiting the divergence of a correlation length. It is debated as to whether these observations at nonzero temperature are signatures of a QPT. In the case of the MIT, the alternative suggestions are that the observed metallic behavior is a crossover or percolation phenomenon, or that the metallic behavior would be suppressed by going to lower temperatures.

The physics of MITs is thought to be determined by interactions between electrons. Adjusting the carrier density alters the potential due to electron-electron interactions in the Hamiltonian by

$$E_{e-e} \sim \frac{e^2}{\epsilon}\sqrt{\pi n} \tag{4.1}$$

where n is the 2D carrier density. The strength of E_{e-e} is measured by comparing the interaction energy to the Fermi energy

$$E_F = \frac{\hbar^2}{2m^*}\pi n \tag{4.2}$$

where $m*$ is the effective mass. The ratio, E_{e-e}/E_F when simplified is equal to the dimensionless Wigner Seitz radius

$$r_s^{-1} = a_B\sqrt{\pi n} \tag{4.3}$$

where a_B is the Bohr radius defined as

$$a_B = \frac{\epsilon\hbar^2}{m^*e^2} \tag{4.4}$$

[54] In this simplified form r_s^{-1} can seen of as the number of electrons per a_B with predictions for the MIT to occur at $r_s \sim 38$ suggesting very dilute electron systems.

Metallic behavior was confirmed by other works on n-type Si MOSFETs with mobility $\mu \sim 10^4 \frac{cm^2}{Vs}$, metallic behavior was found when $n_c \sim 10^{11} cm^{-2}$[6]. In addition to Si, n- and p- type GaAs/AlGaAs heterostructures and quantum wells with $\mu \sim 10^6 \frac{cm^2}{Vs}$, a transition was found at $n_c \sim 10^{10} cm^{-2}$[55, 56]. The resistance at the critical carrier density in several of these experiments was found to be a multiple of h/e^2, often 1.5 to 3 for Si MOSFETs. Typical experimental values for r_s are $5 - 20$ for MOSFETs and $10 - 40$ for p-GaAs MITs. A thorough review of the experiments can be found in the paper of Spivak *et al.*[57].

Another surprising result was that in a parallel magnetic field the metallic behavior of Si MOSFETs could be suppressed.[58] A field strength of $\sim$ 2T led to an increase in the low temperature resistance by several orders of magnitude. The response to a parallel field suggests that the electron spin is an important physical parameter in MIT physics. The resistance saturates at higher magnetic fields.

There has yet to be a complete theory that describes all of the features of the transition to a metallic state. Recent experimental work was focused on creating samples with higher mobilities. These samples would show metallic behavior at more dilute electron concentrations. In addition, thermopower measurements of the MIT can provide additional physics of the electrons in the metallic state. The thermopower of a material is related to the entropy per charge carrier. The Nernst effect has recently been observed to be sensitive to quantum fluctuations but there have yet to be any measurements of the Nernst coefficient near the MIT.[59, 57]

4.3 High Critical Carrier Density

The data in Fig 4.3 were taken starting from 2 K and measuring the resistance each time the temperature was increased incrementally and carrier densities were calculated using the integration method. Starting at the lowest carrier density, we observe behavior that

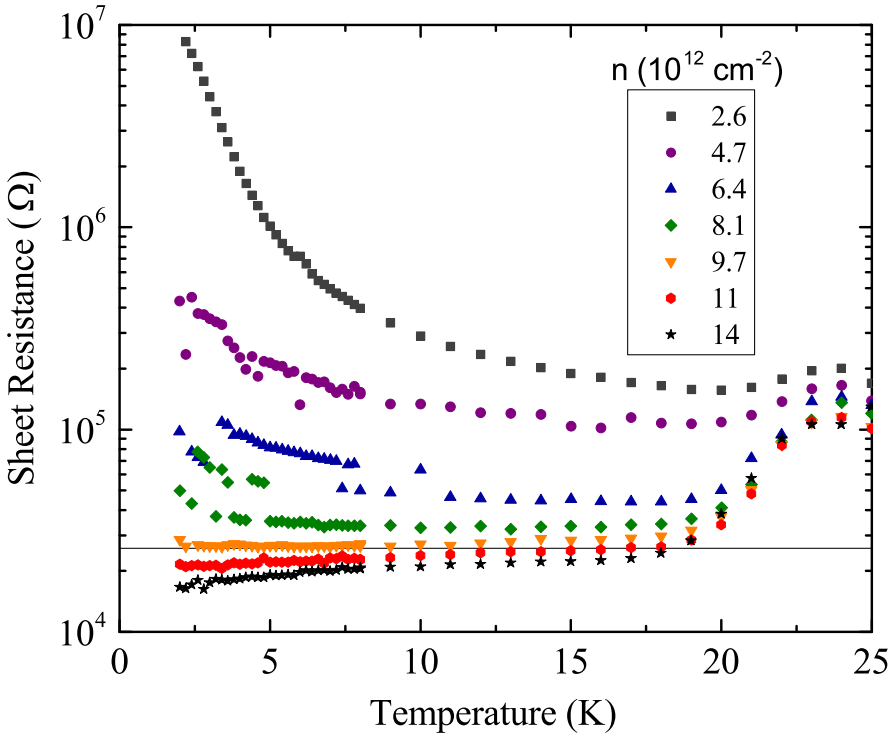

Figure 4.3: Sheet Resistance as a function of temperature for a sample showing metallic behavior. The horizontal line is drawn at h/e^2. The curve at $2.6x10^{12}$ cm^{-2} follows Arrhenius behavior. At higher carrier densities the resistance is better fit to a stretched exponential as a function of temperature. Just below $n = 10^{13}$ cm^{-2} the high temperature resistance falls close to h/e^2 and metallic behavior emerges. The sample became more metallic as the carrier density increased. The carrier density was calculated by the integration method. Hall effect measurements were not made on this sample. The apparent critical carrier density, n_c, for metallic behavior is $10x$ higher than previously reported $n_c \sim 10^{11}$ cm^{-2} in high mobility Si MOSFETs. The mobility calculated from the carrier density at the transition is 20 cm^2/Vs. The base temperature for this graph is 2 K. The downturn in resistance between 20 K and 25 K where the transition between bulk and surface conduction occurs has been observed in many samples only at higher carrier densities and is not yet understood.

is consistent with nearest neighbor hopping. The uncertainly in the carrier density is much higher than that of the sample studied in chapter 3 and estimated to be around $5x10^{11}$ cm^{-2}. The jumps in the resistances observed in the insulating samples are the result of increased noise as the voltmeter jumped between different range settings. The jumps are only seen in one of the Van der Pauw orientations as there is a slight difference between the two directions. At higher carrier densities the resistance appears to flatten and no longer changes as a function of temperature. Carrier densities above 9.7×10^{12} cm^{-2} have a positive temperature coefficient of resistance. The critical carrier density for metallic behavior in this sample is at least 10 times higher than those seen in Si MOSFETs and 30 times larger than the value for p-type inversion layers measured by Zataritskaya and Zavaritskaya.[52] In other samples, carrier densities calculated from the Hall effect were a factor of 2 below the value produced by the integration method but a factor of 2 is insufficient to explain the discrepancy in n_c when comparing with Si MOSFETs.

The line in Fig 4.3 is drawn at h/e^2 which is close to the resistance at the critical carrier density. The mobility

$$\mu = \frac{\sigma}{ne} \tag{4.5}$$

when calculated from the crossing resistance and the critical carrier density produces $\mu = 20$ cm^2/Vs which is at least 3 orders of magnitude below the lowest mobility found in other MIT experiments.

Previous experiments on a MIT with IL gating showed that the metallic state is a result of electrochemical reactions between the sample and the IL liquid. When VO_2 was gated, the metallic behavior was found to remain even after the IL was washed off the sample. If the IL was not removed and the gate voltage cycled to the opposite sign, hysteresis was seen in the conductivity. Figure 4.4 shows data that was taken by discharging the sample from the metallic state. We observed that IL gating of Si

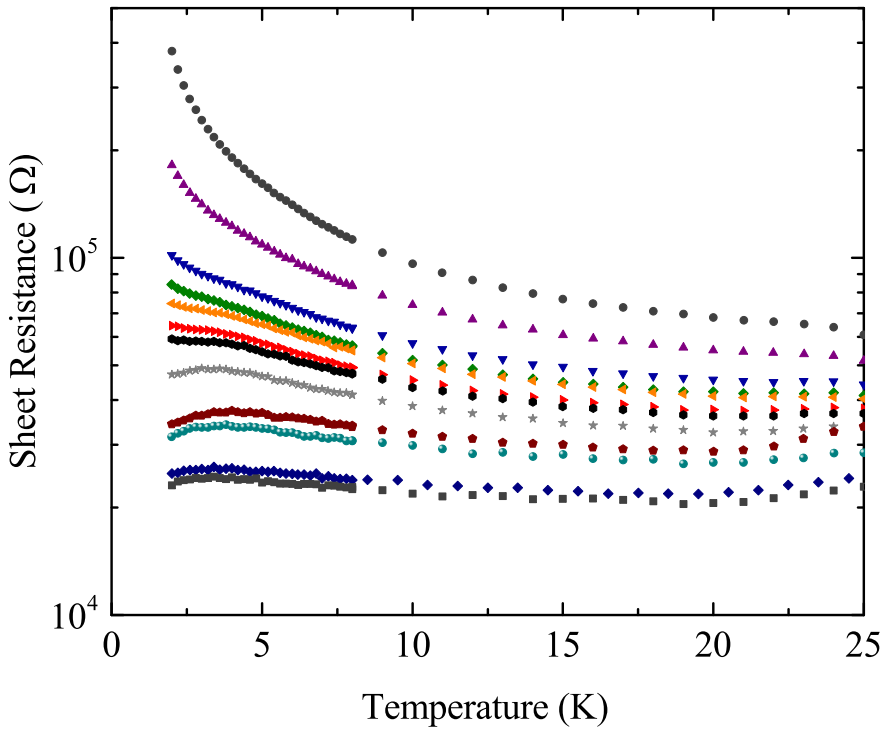

Figure 4.4: Sheet resistance vs temperature for a sample starting from the metallic state and driven insulating by reducing the number of holes. The sample was incrementally charged to -1.4V with the data for -1.0V and -1.2V taken during this process while the rest were measured as the density of holes decreased. Starting from the top the gate voltages are -0.7, -0.75, -0.8, -0.825, -0.85, -0.875, -0.9, -0.95, -1.0, -1.1, -1.2, and -1.4V. The graphs show that the sample returns to an insulating state when the gate voltage is removed and that there is no indication of hysteresis when gating Si surface states to a metallic state.

was reversible without hysteresis. This is further evidence suggesting that the induced carriers are due to an electrostatic process.

Figure 4.5 shows data taken using the optional ^{3}He refrigerator insert. Samples that are metallic remain so from 2 K to 500 mK. The sample plotted in Fig 4.4 was also measured at lower temperatures but IV measurements made below 1 K were nonlinear unlike the sample in Fig 4.5 where linear IV measurements were made at 500 mK. This sample also did not show a resistance increase. Several samples did not show metallic behavior and chapter 5 will discuss these nonmetallic samples. Attaching the samples to the optional refrigerator insert required discharging the metallic state and removing the sample from the measurement system. When this was done, the IL was removed with isopropol alcohol and fresh IL was applied before the next measurement. Samples that underwent a MIT only did so a finite number of times suggesting there is some possible degradation with the sample is cleaned or stored between measurements. Chapter 5 discusses the repeatability of the experiments in greater detail.

Using the heavy hole mass and dielectric constant for Si, $r_s \sim 5$. Long range Coulomb interactions are important to the physics of the low carrier density MIT where here the higher electron densities will be subject to increased screening. In addition $E_F =$ meV which is at least 10 time larger than the dilute systems.

4.4 Critical Carrier Density and Sample Peak Mobility

The transition to a metallic state at high carrier density was an unexpected result that was predicted to not exist even though a critical carrier density in low mobility samples had been calculated. In section 4.2, it was noted that in MIT physics the desire to achieve high mobility samples leads to lower n_c. A natural extension of this would be to explain the high critical carrier density observed in IL gated Si as the result of low mobility in the system. Das Sarma and Hwang proposed a theory to quantify the

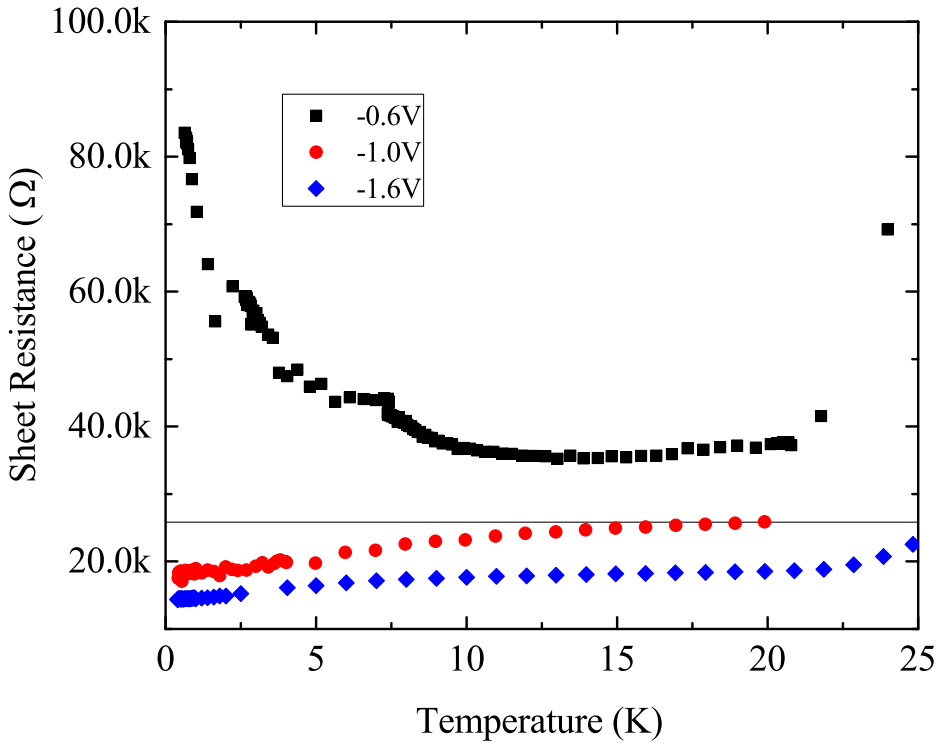

Figure 4.5: Resistance vs temperature at different gate voltages measured to a base temperature of 480 mK. The horizontal line is drawn at h/e^2. Samples that show metallic behavior at higher temperatures down to 2 K continue to show metallic behavior down to below 500 mK.

relation and suggested that

$$n_c \sim \mu_{peak}^{-\gamma} \tag{4.6}$$

The details of the theoretical prediction are discussed in this section.[60] Furthermore, Das Sarma and Hwang predicted that in older low mobility systems, a value of $n_c \sim 10^{12}$ cm^{-2} would be expected but is unlikely to exist. At such a high carrier density, $E_F = 73$ K which was considered to be too high and that a metallic state at these densities could not be the result of an electronic mechanism.

Determination of n_c was done with the by applying the Ioffe-Regel criterion which states that $n_c \to k_f l = 1$. In 2D the conductivity can be simplified and expressed as

$$\sigma_{2D} = \frac{e^2}{h} k_f l \tag{4.7}$$

where k_f is the Fermi wavevector and l is the mean free path with $l = v_f \tau$. Written in this way e^2/h is a constant referred to as the quantum of conductance and the dimensionless parameter $k_f l$ determines the behavior of the sample. The expression is a simplification of the Drude conductivity

$$\sigma = \frac{ne^2\tau}{m} \tag{4.8}$$

The Fermi wavevector k_f is derived from E_F by

$$k_f^2 = 2mE_F/\hbar^2 \tag{4.9}$$

Equation 4.7 is the result of combining Eq 4.9 and Eq. 4.2 while replacing τ with l. To determine the dependence of n_c on μ Das Sarma and Hwang considered the Drude conductivity at $T = 0$ (defined in Eq 4.7) and the Ioffe-Regel criterion; therefore one needs to determine $k_f(n)$ and $l(n)$. From Eq. 4.5 and Eq. 4.8 one can see that μ depends on only τ and m as

$$\mu = e\frac{\tau}{m} \tag{4.10}$$

While $k_f(n)$ was calculated from

$$k_f^2 = \frac{4\pi}{g_s g_v} n$$

where g_i is the spin and valley degeneracy, respectively. The disorder induced mean free path, $l(n)$, on the other hand is a more complicated function that can be determined from the transport relaxation scattering time τ. The Boltzmann transport equation was used to determine $\tau(n)$ and therefore both μ and l. Si $\langle 100 \rangle$ is known to have $g_v = 2$ and using $g_s = 2$ leads to the prediction that the critical resistivity for the transition to occur at $0.5h/e^2$ and not h/e^2 as Eq. 4.7 would predict. The discrepancy is the result of different assumptions that went into the derivation of E_F in Eq. 4.2. Das Sarma and Hwang stated that the work is purely phenomenological in nature and that the goal is to determine the parameters that determine n_c. The discrepancy with the crossing resistance does not have a significant impact on the scaling of n_c on μ. In addition, application of the Ioffe-Regel criterion is arbitrary as there are other predictions like the Ioffe-Regel-Mott criterion which states n_c results from $k_f l = \pi$.[60] It was concluded that the metallic state is only an effective metallic state and what is observed is a crossover phenomenon. Evidence for localization in samples with metallic resistance has also been discussed.[61] It is not clear as to what category best describes a MIT; QPT, crossover, or percolation phenomenon.

The example of a MIT in IL gated Si has $\mu \sim 20$ cm^2/Vs well below the mobilities of the previous MIT and Na^+ experiments. Using Eq. 4.6 for $\mu > 10^4$ cm^2/Vs, a value for n_c can be determined by an extrapolation to the lower mobilities. The theory predicts that for samples with $\mu < 10^4$ cm^2/Vs one would find $n_c \sim 10^{12}$ cm^{-2}. While the prediction of a larger n_c was made, it was concluded that the metallic state could not exist due to electronic interactions with such a large E_F at those carrier densities. This also suggests that the metallic behavior of IL gated Si may not be similar to the metallic behavior observed due to electron-electron interactions at lower carrier density

and higher mobility.

4.5 Summary

A transition to metallic behavior in Si surface states induced by an IL has been observed. The transition to the metallic state happens at a carrier density of just under 10^{13} cm^{-2}, which is much higher than previously observed in any other 2D MIT systems. Metallic states at such a high carrier density were believed to not exist. Using parameters for the heavy hole mass $r_s \sim 5$ was calculated for the critical carrier density. Predicted values for the onset of metallic behavior are much higher with $r_s \sim 40$. If the light hole mass Si $\langle 100 \rangle$ was included in the calculation of r_s , the onset of metallic behavior would occur at an even smaller value. It is not clear as to whether or not the transition to metallic behavior with IL gated Si involves the same physics as the one observed in Si MOSFETs. It is an open question as to whether not the metallic behavior is either a QPT or crossover phenomenon.

The interesting experiment presented in this chapter has led to a wealth of new questions regarding MIT physics. It is predicted that the state is unlikely to be due to electronic properties; therefore it would be worthwhile to apply the scaling analysis performed on Si MOSFETs to our Si EDLT , which would indicate if the transition observed here fall into the same universality class. Measurements to suppress the metallic state in a parallel magnetic field could show the similarities between IL gated Si and the high mobility MOSFETs. The role of charged impurities could be examined by performing a series of experiments on Si wafers with different levels of B dopants, as a large range of wafers with different boron concentrations are available to purchase commercially. Experiments could be designed to use an IL to create inversion layers in Si to see if metallic electron clouds could also be created at high carrier densities.

A more complete understanding of the nature of the metallic behavior is required to

engineer better Si devices. Metallic behavior was only observed in a subset of IL gated Si samples. The reason for this is also not yet understood, and chapter 5 focuses on the non-metallic samples in addition to samples with carrier densities $> 10^{13}$ cm^{-2} .

Chapter 5

Mobility Peak

5.1 Introduction

Chapter 3 discussed the physics of IL induced surface states in Si at carrier densities below 10^{12} cm^{-2}. As the carrier density increased in the $10^{11}-10^{12}$ cm^{-2} range, metallic surface states were seen in some samples. The focus of this chapter will be on the non-metallic samples and the behavior of all Si samples at carrier densities above 10^{13} cm^{-2}. The conductivity of the surface state was found to be a nonmonotic function of the applied gate voltage V_g and above 10^{13} cm^{-2} carriers the sample became less conductive as the carrier density was increased further. This behavior has also been observed in experiments in which rubrene was gated with an IL.[62] It has also been shown that in Si inversion layers measured at low temperatures, the field effect mobility exhibits a peak as a function of V_g.[63]

This chapter is organized as follows: conductivity data for non-metallic IL gated Si samples is presented and discussed in section 5.2. Using Eq. 4.5 , μ can be calculated from the conductivity using n determined from the integrated current density. Section 5.3 focuses on the mobility peak and discusses other experiments in which similar

mobility peaks were seen. The observed mobility peak was observed in many samples and could be reproduced several times using a single sample. Section 5.4 covers an experiment where a sample was charged and discharged three times and in all three sequences of charging a mobility peak was observed. There are predictions as to the origin of the mobility peak but the theories tend to be phenomenological. In section 5.5, a model for the peak in the mobility is presented. In this model the reduction in the mobility is a result of a reduction in the electron scattering time due to surface roughness scattering. This is a short-range interaction that is predicted to be the dominant scattering mechanism at high carrier densities. Some open questions are discussed before the conclusion.

5.2 Non-Metallic Samples

Metallic behavior was never seen in early studies of low mobility Si MOSFETs.[26] In addition to Na^+ implantation in some experiments, metal electrodes were placed on top of thick oxides so the carrier density could be electrostatically modulated. At low carrier densities, the induced carriers were strongly localized. At higher carrier densities, it was concluded that the conductivity followed the theory of weak localization. Weak localization features a quantum mechanical treatment of electrons, where the reflected portion of a wave scattered off of an impurity can add coherently with the incident wave.[64] Corrections to the sample conductivity are expected to follow the form

$$\delta\sigma = \frac{e^2}{\pi h}\Big(\alpha p + 1 - \frac{3}{4}F\Big) ln\left(\frac{k_B T\tau}{\hbar}\right) \tag{5.1}$$

One can see that as $T \rightarrow 0$ the $ln(T)$ correction will to vanishing of σ . In Eq. 5.1 τ is the elastic scattering time, F is a value related to the electron screening function, p is the temperature exponent associated with the electron dephasing time, and α is a constant. Corrections due to weak localization were also observed in MIT MOSFETs

below the critical carrier density.[65]

Figure 5.1 shows data for a sample at voltages where the high temperature conductivity is near e^2/h. In the figure, σ is plotted as a function of T such that weak localization effects would appear linear. The data was taken using the optional ^{3}He refrigerator with a base temperature of 500 mK. While the data looks relatively linear the range of σ is too small to conclusively claim that the conductivity is due to weak localization. Each curve can also be fit by a stretched exponential following the theories of hopping conduction. The temperature exponent when the data is fit to Eq. 3.6 was found to decrease with increasing carrier density. The more likely scenario of these two is that at such a high conductivity, the data follows corrections due to weak localization where increasing carrier density leads to better screening and an increase of F, thus decreasing the slope of the curves in Fig. 5.1. A better confirmation of the conduction mechanism would require measurements at much lower temperatures where the conductivity would be significantly smaller. The sample in the figure is referred to as non-metallic as increasing the carrier density further leads the sample to become more insulating.

Figure 5.2 is a typical result for samples that are referred to as nonmetallic. At low values of V_g, a surface state is formed just like the samples discussed in Chapters 3 and 4. As V_g increases, so does the carrier density and the conductivity of the surface state. This is shown in Fig 5.2a. A surprising result of the sample was that at carrier densities higher than 10^{13} cm^{-2} the samples became more insulating as the gate voltage was increased. This can be clearly seen in Fig. 5.2b. The carrier density of this sample (calculated from the Hall coefficient measured at a gate voltage of -1.4 V) was $\sim 1 \times 10^{13}$ cm^{-2} . This particular set of data was shown in Fig 2.4 as a typical Hall measurement. Section 5.3 discusses the integrated carrier density with respect to the observed turn around in behavior of the conductivity. The cause of this turnaround,

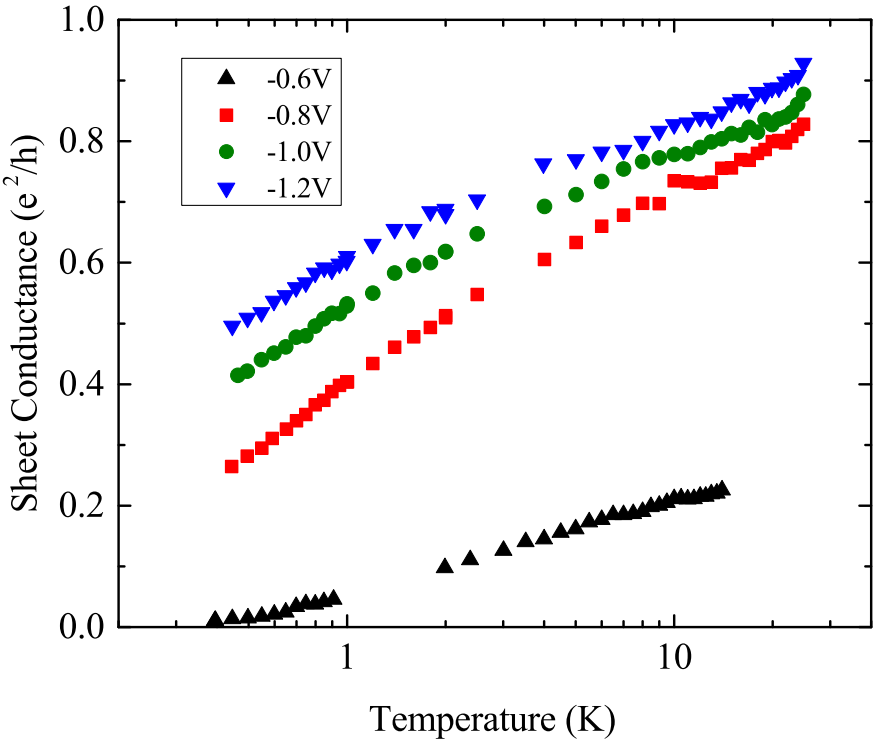

Figure 5.1: Sheet conductance for a nonmetallic Si sample measured down to 500 mK. The graph is a semilog plot where σ is plotted against T on a common logarithm scale. According to the theory of weak localization the conductivity should appear linear when plotted this way. While there is some agreement, the relatively high limit of the lowest temperature leads to an insufficient range of conductance to confirm weak localization.

appears to be from a decrease in the sample mobility and not the carrier density in the gate voltage ranges of those listed in Fig 5.2b.

At the voltage for the highest conductivity curve,V_g is well below the electrochemical window of DEME-TFSI; therefore, it is unlikely that the behavior is due to a breakdown of the molecules within the liquid.[29] In addition, when using the same drop of IL the conductance peak was found to be reproducible. Section 5.4 covers the reproducability of the peak behavior. An alternative possibility is that at electrochemical processes are more active at higher gate voltages. If this were the case, the reduction in sample conductivity would be from increasing the oxide thickness and decreasing the transistor capacitance. Measurements of charge transfer as a function of gate voltage indicate the capacitance of the transistor remains linear through the conductance peak.

The reproducability of the results suggests that it is also unlikely that it is due to sample degradation. There are high electric fields present at high carrier densities, and conducting paths can be created in insulating materials with a high enough electric field. The field at which this happens is known as the dielectric breakdown field. The electric field a distance d where $d \ll l$ and l is the shorter dimension for a sheet of charge is

$$\vec{E} = \frac{\sigma}{2\epsilon}\hat{z} \tag{5.2}$$

where $\epsilon = \epsilon_r\epsilon_0$. The direction $\hat{z}$ is normal to the surface of the charged sheet. For SiO_2 with $\sigma = 10^{13}$charges/cm^2 at the surface and $\epsilon_r = 4$, $E = 2.3$ MV/cm. It is worth noting that reported dielectric breakdown fields for SiO_2 are $E < 10$ MV/cm.[66] This explanation would only allow electronic wave functions to extend into the oxide layer as the anion in the liquid is too large to be embedded within the oxide. The charging curves still show an exponential decay indicating that electrons are not moving into the IL. One would expect holes within the oxide to be localized and would not contribute to the conduction of the surface state.[67] Other experiments see similar peak behavior in which the carrier density determined from the Hall coefficient continues to increase

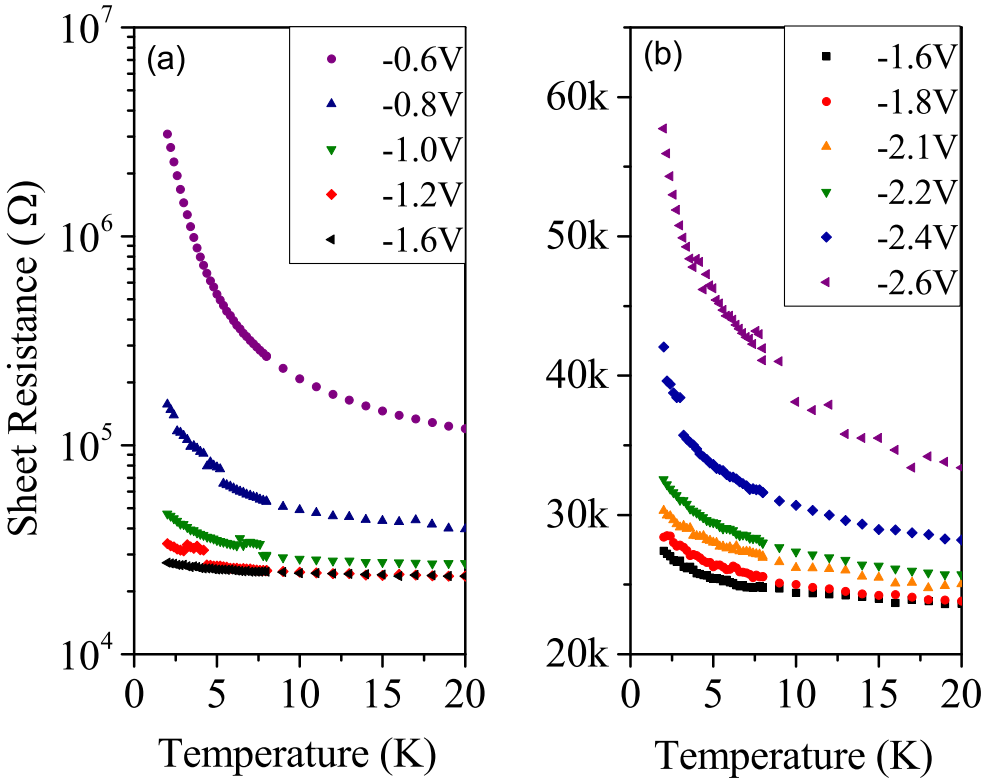

Figure 5.2: Resistance as a function of temperature plotted at different values of V_g. The data shown here is typical data observed in multiple IL gated Si samples. This sample did not show metallic behavior. (a) Resistance vs temperature where the sample conductivity increased with increasing V_g. (b) Resistance vs temperature where the sample conductivity decreased with increasing V_g. One can see that at a fixed temperature the mobility determined from the sample conductivity will show a peak as a function of V_g.

with decreasing sample conductivity.[62] In particular the experiment involving IL gated rubrene did not have a layer of SiO_2. The carrier density at the peak mobility in the rubrene experiment is similar to the one observed with IL gated Si and does not support the model of dielectric breakdown.

5.3 Mobility Peak

The mobilities calculated in Fig. 5.3 were determined from σ(2K) and the integrated carrier density. Plotted in the figure is the integrated carrier density as as function of gate voltage which shows that the carrier density remains linear while passing though the mobility peak. The transistor capacitance, determined from the slope, was found to be 4 μF/cm^2. The figure also shows that $\mu_{peak} = 11$ cm^2/Vs occurred at $n \sim 4{\times}10^{13}$ cm^{-2}. For this sample, at carrier densities near the peak mobility, the conductivity started to exhibit what looked like metallic behavior with $\sigma \sim 1.2e^2/h$. However the sample was not as strongly metallic as the ones discussed in Chapter 4.

As mentioned in section 5.2, experiments where rubrene was gated in an EDLT configuration showed a peak in the mobility with carrier density.[62, 68] The peak in the mobility occurred at $n \sim 3 \times 10^{13}$ cm^{-2}where the carrier density was determined from the Hall effect and $\mu_{peak} = 4$ cm^2/Vs. As discussed above, roughly the same carrier densities, experiments of IL gated rubrene and Si show a peak in the mobility. The value of μ_{peak} observed in our Si experiment was roughly four times larger than the one in the rubrene study. Metallic behavior was not observed in the rubrene experiment with $r_s \sim 10$ calculated at a carrier density near the mobility peak. A mechanism of surface scattering due to the random potential created by the IL ions was suggested as the origin of the observed mobility peak.

Mobility peaks were also observed in experiments with Si states induced by Na^+ ions as a function of the electrostatically induced carrier density, N_s, where the density

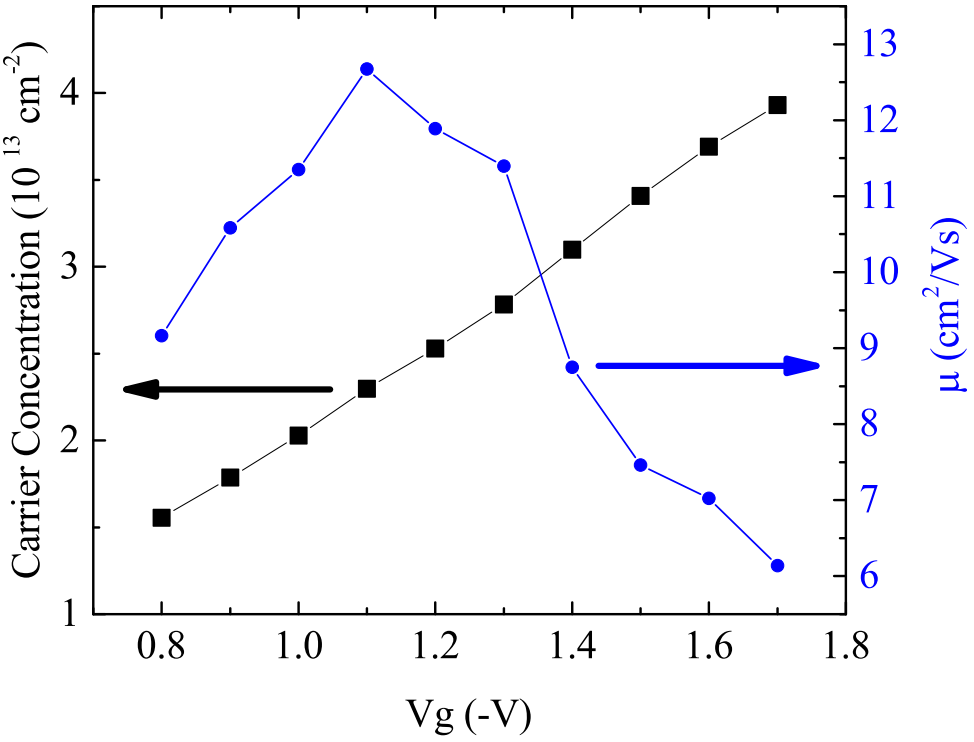

Figure 5.3: Integrated carrier density and the mobility measured at 2 K as a function of V_g. The mobility was determined from the sheet conductance of the sample at 2 K. The mobility is a nonmonotonic function of V_g. At the peak mobility, $\sigma \sim 1.2e^2/h$. The integrated carrier density as a function of V_g is linear and the capacitance calculated from the slope is similar to what one would expect from a planar SiO_2 capacitor 10Å thick. The linear behavior extends though the mobility peak, suggesting electrostatic behavior. Electrochemical processes are known to produce a nonlinear dependence of the integrated charge as a function of V_g.

of Na^+ ions was measured as N_{ox}. Depending on the concentration N_{ox}, peak mobilities $4 \times 10^3 < \mu_{peak} < 1.8 \times 10^4$ cm^2/Vs were measured with the carrier densities, N_s, of the peak falling in the range. $10^{12} - 10^{13}$ cm^{-2}. Higher values of μ_{peak} occurred at lower vales of N_{ox}.[26] Another observation was that at higher values of $N_s \sim 10^{13}$cm^{-2}, the mobilities at different values of N_{ox} appeared to approach the same value. It was thought that the limiting mobility was due to surface roughness scattering, resulting in the expectation that μ would decrease with increasing N_s. The mobilities were much larger than the mobilities observed with IL gated Si. In addition, the carrier density at peak mobility is roughly 10 times smaller than the carrier density observed with IL gated Si or rubrene. One possibility for the different carrier densities at μ_{peak} could be the result of the low mobilities observed in the IL gated experiment. If indeed at higher carrier densities the value of the mobility saturates then one would expect lower mobility samples to peak at a higher carrier density.

5.4 Repeatability

The mobility peaks were reproducible using two different methods. In the first method the surface states were discharged and the sample was removed from the system and stored in ambient conditions. Before storage, the IL was removed by first using a pipette followed by isopropyl alcohol to dissolve any residual IL. Even after a month of storage, when tested again, samples would have a similar V_T and show a mobility peak. In these scenarios a fresh application of IL was used.

The second reproducability test was to discharge the sample, and without removing the sample from the system, perform an additional gating experiment. A typical gating experiment would involve incrementing the gate voltage until surface conduction is seen. A gate voltage step size would be chosen, with a value determined by the desired data density. The gate voltage would then monotonically be incremented until carrier

densities beyond the mobility peak were reached. After which the sample would be discharged by incrementally reducing the gate voltage every $30 - 60$ s until $V_g = 0$ at the temperature used to charge the sample. A uniform increment in time was used in each experiment but the time step was sometimes altered between experiments.

Figure 5.4a shows data taken from a sample measured beyond the mobility peak. After $V_g = -1.8$ V the sample was discharged as outlined in the previous paragraph. When $V_g = 0$ the sample was slowly warmed to 280 K to increase the ionic conductivity of the IL. Even at $V_g = 0$ it was thought that some excess anions many remain on the oxide surface. The higher ionic conductivity was thought to reduce that possibility. After reaching 280 K, the sample was cooled to 180 K before performing an additional gating experiment. The results of the second experiment are plotted in Fig 5.4b where the line in the figure denotes h/e^2. After a peak in the conductivity as a function of V_g was realized the sample was discharged, again following the above procedure including the cycle to high temperatures at $V_g = 0$. A third gating experiment was performed with the results plotted in Fig 5.4c with the line drawn at h/e^2. The mobility peak was again observed.

It is evident in Fig 5.4 that V_T and V_g at μ_{peak} are increasing with each experiment. The behavior was not seen in the experiments where the IL was washed away, and a new liquid applied in between gating experiments. This suggests that there could be hysteresis between the induced charge and applied gate voltage. If the increase of V_T was due to anions remaining on the surface when $V_g = 0$, one would expect to see a decrease in V_T with successive gating cycles. If the oxide charge was altered over the course of the experiment one would expect to see similar behavior in the experiment where the liquid was removed and reapplied. Additional experiments need to be performed to understand why V_T increased with each gating experiment.

In each experiment, there is a gate voltage with the lowest resistivity as a function

of temperature. Across the three experiments we observe that the lowest resistive state increased in resistivity upon subsequent gating cycles. This was also observed in the experiments where the IL was replaced between gating experiments. It cannot be ruled out that there is some damage done to the sample over the course of the experiment, but the behavior is not consistent with the models we have used in this work. The change in resistance due to the decreasing mobility is much larger than the change in the resistance of the most conducting state between gating experiments. This gives a small insight to the behavior, as the repeatability of the mobility peak suggests that the increase in resistivity at higher carrier densities is not associated damage to the sample surface.

It has also been suggested that mobility peaks observed in rubrene can be explained by an increasing contact resistance at higher gate voltages. This conclusion was drawn by comparing 2 wire and 4 wire resistance measurements at high gate voltages where only the 2 wire resistance increased with gate voltage.[69] The IL Si experiment was performed entirely in 4 wire configurations and in addition the results of Wei *et al.* or *et al.* do not agree with the conclusion of Shimotani *et al.*[62, 68]

5.5 Reentrant Insulator Theory

In Chapter 4 a theory to understand the dependence of n_c on sample disorder was discussed. The Ioffe-Regel criteria, $k_f l = 1$, was used to determine n_c and with $k_f l$ calculated from the scattering time due to charged impurities. In an additional paper, Das Sarma and Hwang sought to understand the mobility peak observed in the early Si MOSFET experiments.[63][26]. One possibility for the decrease in the mobility at high carrier densities and low temperatures was thought to be due to surface roughness scattering.

Similar to their calculation of the scattering time due to charged impurities, the

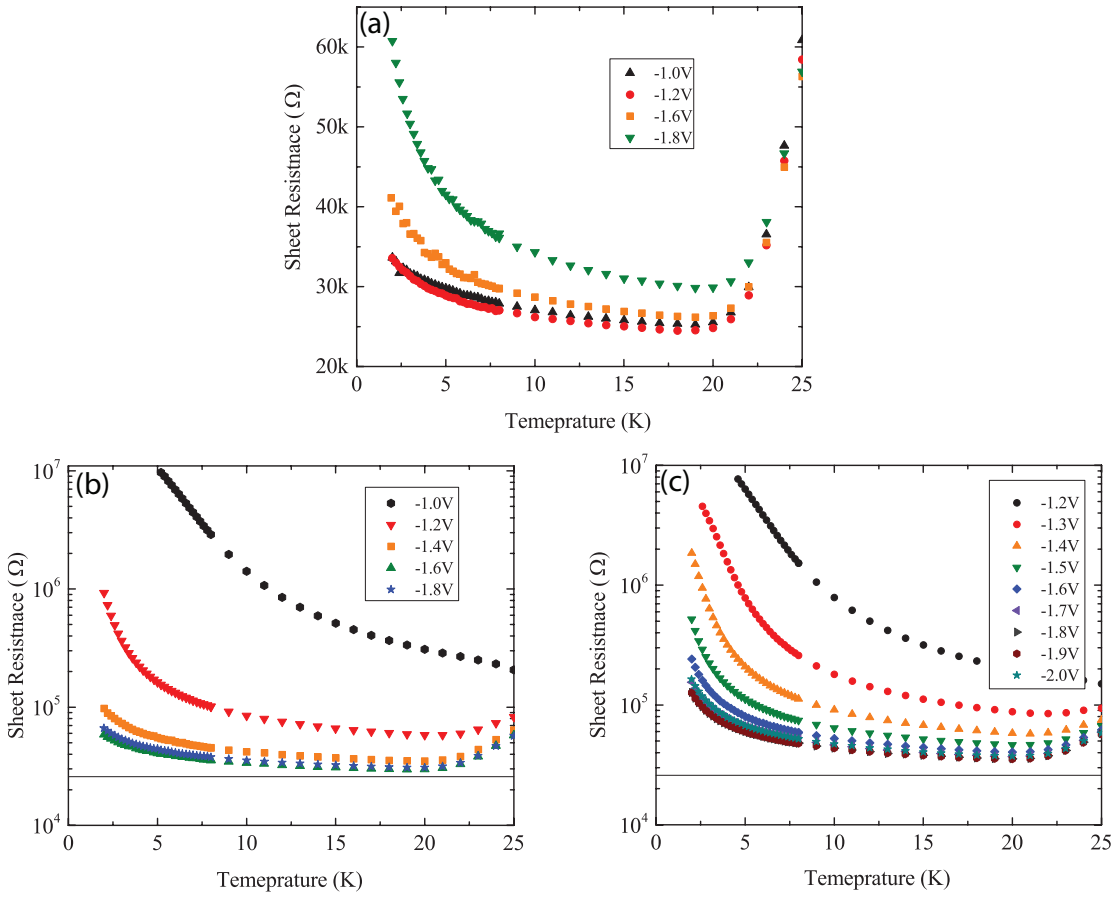

Figure 5.4: Sheet resistance as a function of temperature at different V_g. The data for this sample suggests that the mobility peak is not associated with damage done to the sample. The sample was initially charged until the mobility peak was observed. After which the gate voltage was removed at 240 K which was also the temperature used to charge the sample during the run. When $V_g = 0$, the sample was warmed to 280 K before cooling to 180 K after which the charging process was repeated. (a) The graph shows data recorded during the initial charging process. The graph shows that above $V_g = -1$ V the sample resistance increases with increasing V_g. (b) The data in this graph was recorded during the second charging process reproducing the mobility peak. The sample was discharged a second time after it was observed that the resistance was increasing with increasing V_g (c) Data from the third charging procedure performed on the sample. Once again the mobility peak was observed. It was also observed that V_T increased with each set of charging curves.

Boltzmann transport equation was used to calculated the scattering time due to surface roughness scattering. It was found that at low carrier densities, the scattering time was be limited by long-range Coulomb interactions. At high carrier densities (and thus high E_F) they suggested that short range interactions would have a greater effect on the transport scattering time, with surface roughness scattering being the limiting case.[70]

Overall, Das Sarma and Hwang found the scaling relation $\mu \sim n^{-2}$ due to surface roughness scattering. In the case of charged impurity scattering $\mu \sim n^{0.4}$. The scaling relations were calculated in the $T = 0$ limit. The total mobility and conductivity were calculated using

$$\mu^{-1} = \mu_{CI}^{-1} + \mu_{SR}^{-1} \tag{5.3}$$

where the two mobilities are due to charged impurity scattering and surface roughness scattering. The two opposite scaling relations reproduce the observed peak. The peak mobility was predicted to occur at $n_m \propto N_{CI} V_{SR}^{-2}$ where N and V are the charged disorder strength and surface roughness scattering strength, respectively. The relations $\mu \sim n^{-2}$ and $\sigma \sim n\mu$ suggests that the conductivity should decrease with increasing carrier density when surface roughness scattering is the limiting factor in determining the electronic transport properties.

Since $n_{c1} < n_m$ their work suggests that if the Ioffe-Regel criteria is satisfied at low carrier densities, n_{c1}, then there may exist a second high carrier density n_{c2} where the system would then reenter the insulating state. It was suggested that a likely value for n_{c2} is within $10^{13} - 10^{14}$ cm^{-2}. Metallic behavior should only be observed for $n_{c1} < n < n_{c2}$. An estimate for n_{c2} in Si MOSFETs was $3 - 5 \times 10^{13}$ cm^{-2}. It is also possible that surface roughness scattering would not be strong enough to cause $k_f l < 1$ thus there would be no n_{c2}.

Peak mobilities were observed for the samples discussed in Chapter 4. Although the sample conductivity started decreasing with increasing carrier density the samples

were not driven back into the insulating state. The sample in Fig 5.3 for the three highest mobilities showed a slight downturn in resistance but the metallic behavior in the sample was not conclusive. The theory of Das Sarma and Hwang is the first to explain the peak mobility behavior we observed in the metallic samples.

The theory also suggests why we do not see metallic behavior in every sample. If the charged impurity disorder was large enough such that $n_{c1} > n_{c2}$ then metallic behavior would not be observable. Further experiments on different Si doping levels could be done to verify this speculation. Oxygen inclusions and B acceptors are sources of charged impurities. Si wafers can be purchased with vastly different B concentrations and the number of oxygen inclusions in undoped Si are reduced with Si wafers grown by the float zone method.

The theory also suggests that for sufficiently weak surface roughness scattering the condition $k_f l = 1$ may never be satisfied at high carrier densities. The original motivation for the experiment presented here was to create surface states with $n = 10^{15}$ cm^{-2}. It is an experimental difficulty to make atomically thin and low disorder oxide layers. Thicker oxides will reduce the maximum induced carrier densities and atomically thin oxides may not provide uniform coverage. Atomic layer deposition techniques were being researched for second generation devices. The use of Al_2O_3 or HfO_2 could also be helpful in understand the physics of the metallic state in IL gated Si.

While Das Sarma and Hwang's theory predicted the reentrant behavior, and can explain many of our other experimental observations, the behavior of low mobility, high n_c samples is still not well understood. In addition the low value of r_s suggests that the metallic state may not be due to electrostatic interactions. A theory for the metallic behavior in Si would go a long way in engineering better more consistent devices. Ionic liquid gated Si may also serve as a platform for producing a theory of carrier induction by an ionic liquid. The study of the crossover from electrostatic to electrochemical

behavior in EDLTs would be very useful when designing IL gated experiments.

5.6 Summary

At carrier densities higher than 10^{13} cm^{-2}, both metallic and nonmetallic IL gated Si become more insulating with increasing carrier density. Theory shows that at this level of carrier density, short range interactions make a larger contribution to electron scattering than long range interactions. The most dominant short range interaction is considered to be surface roughness scattering and leads to $\mu \sim n^{-2}$. This leads to a peak in the mobility at carrier densities in the regime where short range interaction become important. Unlike the samples discussed in Chapter 4, several Si samples did not show metallic behavior before the mobility peak was observed. Similar mobility peaks were observed in the experiments where carriers in Si surfaces states were adjusted with Na^+ implantation in the oxide and in a MOSFET configuration. We can compare our observations on IL gated Si to previous experiments with IL gated rubrene, and both experiments show a mobility peak at the same carrier density. The mobility peak in rubrene was roughly four times smaller in magnitude than the one observed in Si.

Chapter 6

Conclusion

We designed an experiment to measure IL induced surface states in commercial Si wafers. The work was motivated by the possibility of observing superconductivity at 10^{15} holes cm^{-2}. This carrier density is near the record high carrier densities reported with EDLTs. Several other experiments have observed electrochemical reactions when using ILs, and naturally it was suggested that electrochemical reactions are the mechanism by which an IL can achieve such high carrier densities. While we designed our experiment to suppress electrochemical reactions, the physics of IL gating is still an open topic.

A model for electrostatic carrier induction using ILs was proposed in chapter 3. We argued that the ions in the liquid form a neutral background as there will be equal numbers of cations and anions. This is also true at the sample surface, and as long as the ion species are in equal quantities there will not be an electronic response from the sample. With negative applied gate voltages, additional anions will be driven to the sample surface and cations to the gate. The excess anions act as if they are isolated charges in a neutral background. This induces screening holes within the sample.

The model was tested by comparing the results of IL gated Si with experiments in

which surface conduction was observed when Na^+ions were implanted near the Si/SiO_2 interface. In both cases, the conductivity was found to follow nearest neighbor hopping conduction, which is a form of activated conduction. The activation energy as a function of carrier density of the two experiments overlapped. This suggests that the holes in Si were induced by anions on the oxide surface. Further experiments with IL gated Si may lead to a better understanding of how carriers are induced by an ionic liquid. The experiments with Na^+ were performed by Fowler with ion concentrations $\sim 10^{11}$ cm^{-2}. Measuring IL gated Si at lower carrier densities, 10^{10} cm^{-2}, would be a dilute enough system to calculate the binding energy of a holes to an anion on the surface.

At carrier densities higher than 10^{12} cm^{-2}, two unexpected observations were made with IL gated Si. While superconductivity was not observed, a transition to a metallic state was found, with a critical carrier density just below 10^{13} cm^{-2}(Section 4.3). This was shocking, as 2D insulator to metal transitions are only expected to be observed in high mobility, $> 10^4$cm^2/Vs, systems with critical carrier densities below 10^{11} cm^{-2}. The mobility of the IL gated samples was $\mu \sim 20$ cm^2/Vs. The current focus in 2D metal physics is on the achieving higher mobility samples where lower critical carrier densities are expected. While electrons are more dilute in low density system, the ratio of the Coulomb energy to the Fermi energy is larger than it would be at higher carrier densities. Electron interactions are thought to be the origin of the apparent 2D metallic behavior. It is still debated whether the observed behavior is a phase transition or a crossover phenomenon. By extrapolating the expected critical carrier density, low mobility samples have an expected critical density of 10^{12} cm^{-2}. The Fermi energy at such a high density was considered to be too large for metallic behavior. It is also an open question as to whether the metallic state with IL gated Si is due to electron-electron interactions.

At carrier densities higher than 10^{13} cm^{-2}, the mobility was found to decrease with

increasing carrier density (Section 5.3). The reduction in the mobility was large enough that this results in a decrease in the surface state conductivity. This phenomenon was observed with early Si MOSFETs and also IL gated rubrene. A theory was proposed where short range interactions should be more dominate at higher carrier densities. The scattering time due to surface roughness scattering was calculated and resulted in a mobility and conductivity that would decrease with increasing carrier density.

A mobility peak as a function of gate voltage was observed in both metallic and nonmetallic samples. Metallic samples were ones that showed a positive temperature coefficient of resistance before the mobility peak. Only a subset of the tested samples displayed metallic behavior, the reason why is not understood. Theories as to the origin of metallic behavior may help in the engineering of better samples.

6.1 Future Work

Further studies of the metallic state could involve measuring the thermopower and parallel magnetoresitance of the samples. In addition, no measurement of the Nernst effect has been made with MOSFETs that show 2D metallic behavior. Measuring the metallic state in parallel magnetic field may be possible with a side gate design, using a cover glass to assist in containing the ionic liquid. Another solution to the parallel magnetic field problem would be to rotate the sample once the liquid is frozen. The measurements are possible with the second generation design (depicted in Fig 2.8) once fabrication issues are resolved.

To measure the thermomagnetic response, thin film thermometers could be integrated into a third generation sample design.[71] Figure 6.1 depicts a thin film thermometer deposited on a Si wafer used to measure the Nernst effect in thin film Nb. The thermometers were capped in SiN for electrical isolation but the SiN layer could also be used to define the sample space. With a greater data density across the metallic

transition, a scaling analysis could be performed to determine the universality class of the transition.

Improved reliability and yields of metallic samples would greatly improve the results of future experiments. Some work had been performed on improving Si passivation by oxide depositions as opposed to the native growth in air. In addition to SiO_2 passivation layers, SiN and HfO_2 have been used to create high quality Si transistors. Typical growth recipes for those materials involve making thick oxides to minimize electron tunneling. A thicker oxide would reduce the capacitance of IL transistors and recipes for thinner passivation layers are desired. If surface roughness scattering is the cause of the high carrier density mobility peak, smoother oxides are desired. It was predicted that a reenetrant insulating state may not happen when there is low disorder in the oxide. One idea would be to lattice match the passivation layer to the diamond cubic structure of Si. Insulators are typically binary compounds of an element with O or N. Boron nitride is one insulating material with zincblende crystal structure and has also been shown to suppress the electrochemical effects of the IL. Monolayers of BN on Si may be the solution to observing the possible superconductivity electrostatically at 10^{15} carriers cm^{-2}.

Further experiments of IL gated Si could be performed in the low carrier density, high resistance regime. High resistance measurements are limited by the measurement lines and the input impedance of the measurement electronics. Electrometers typically have an input impedance of $> 200T\Omega$ and could be used to measure the sample voltage drop. There is the possibility for users to run external wires in QD PPMS systems. Experiments could be performed at carrier densities near 10^{10} cm^{-2} where current theories can calculate the binding energy of the screening holes and ions. One possible limitation to high resistance measurement on IL gated Si would be the conductivity of the frozen liquid. While low, its exact value is not known and could be a problem for resistance

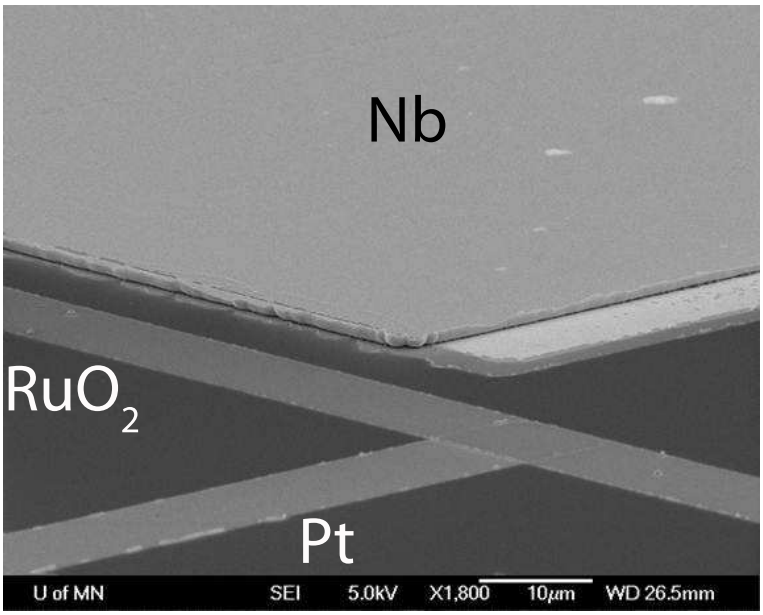

Figure 6.1: Thin film thermometers for use at low temperatures have been fabricated on Si wafers. The figure depicts a Si chip that was used to measure the Nernst effect in a thin Nb film. There are two RuO_2 thin film thermometers deposited on the surface of the wafer patterned with UV lithography. The thermometers are protected by a layer of SiN and were placed within 10 μm of the sample space. The protective SiN layer would protect the thermometers against exposure to the IL. An integrated heater was deposited onto one side of the Si chip. When combined with the second generation design and incorporating a side gate, measurement of both the thermopower and Nernst effect should be possible with IL gated Si. Further work needs to be done on creating a process that produces more robust metallic samples before work into thermomagnetic measurements can be made.

measurements $> 1G\Omega$. Higher resistance measurements could be performed with the first generation. Second generation designs would assure a better measure of the sample area and would greatly improve the accuracy of the integrated carrier density.

Measuring Si wafers with different amounts of B dopants could be one way to adjust the hole mobility in the surface layers. High quality Si wafers can be purchased with a wide range or both n and p type dopants. In addition, oxygen scattering is reduced with float zone growth wafers. Reducing the number of impurity scattering centers should reduce the critical carrier density to observe metallic behavior. It would also be interesting to see if inversion mode devices created with an IL could support 2D metallic behavior at high carrier densities.

The discovery of 2D metallic behavior in low mobility Si with high critical carrier densities was scientifically invigorating. The work presented here is a jumping off point for studies of 2D metallic behavior and also for the physics of IL gating.

References

[1] H Kamerlingh Onnes. Leiden comm. 120b, 122b. Technical report, 124c, 1911.

[2] Michael Tinkham. *Introduction to superconductivity*. Courier Corporation, 2012.

[3] J. Bardeen, L. N. Cooper, and J. R. Schrieffer. Theory of superconductivity. *Phys. Rev.*, 108:1175–1204, Dec 1957.

[4] J George Bednorz and K Alex Müller. Possible hight c superconductivity in the ba- la- cu- o system. *Zeitschrift für Physik B Condensed Matter*, 64(2):189–193, 1986.

[5] J.E. Hirsch, M.B. Maple, and F. Marsiglio. Superconducting materials classes: introduction and overview. arXiv:1504.03318[cond-mat.supr-con].

[6] S. V. Kravchenko, G. V. Kravchenko, J. E. Furneaux, V. M. Pudalov, and M. D'Iorio. Possible metal-insulator transition at b=0 in two dimensions. *Phys. Rev. B*, 50:8039–8042, Sep 1994.

[7] F. Steglich, J. Aarts, C. D. Bredl, W. Lieke, D. Meschede, W. Franz, and H. Schäfer. Superconductivity in the presence of strong pauli paramagnetism: $Cecu_2si_2$. *Phys. Rev. Lett.*, 43:1892–1896, Dec 1979.

[8] E. A. Ekimov, V. A. Sidorov, E. D. Bauer, N. N. Mel'nik, N. J. Curro, J. D. Thompson, and S. M. Stishov. Superconductivity in diamond. *Nature*, 428(6982):542–545, April 2004.

[9] Yoshihiko Takano, Masanori Nagao, Isao Sakaguchi, Minoru Tachiki, Takeshi Hatano, Kensaku Kobayashi, Hitoshi Umezawa, and Hiroshi Kawarada. Superconductivity in diamond thin films well above liquid helium temperature. *Applied Physics Letters*, 85(14):2851–2853, 2004.

[10] Konstantin Iakoubovskii. Superconductivity in covalent semiconductors. *Central European Journal of Physics*, 7(4):654–662, 2009.

[11] E. Bustarret, C. Marcenat, P. Achatz, J. Kacmarcik, F. Levy, A. Huxley, L. Ortega, E. Bourgeois, X. Blase, D. Debarre, and J. Boulmer. Superconductivity in doped cubic silicon. *Nature*, 444(7118):465–468, November 2006.

[12] M. Kriener, Y. Maeno, T. Oguchi, Z.-A. Ren, J. Kato, T. Muranaka, and J. Akimitsu. Specific heat and electronic states of superconducting boron-doped silicon carbide. *Phys. Rev. B*, 78:024517, Jul 2008.

[13] C. H. Ahn, A. Bhattacharya, M. Di Ventra, J. N. Eckstein, C. Daniel Frisbie, M. E. Gershenson, A. M. Goldman, I. H. Inoue, J. Mannhart, Andrew J. Millis, Alberto F. Morpurgo, Douglas Natelson, and Jean-Marc Triscone. Electrostatic modification of novel materials. *Rev. Mod. Phys.*, 78:1185–1212, Nov 2006.

[14] Hongtao Yuan, Hidekazu Shimotani, Atsushi Tsukazaki, Akira Ohtomo, Masashi Kawasaki, and Yoshihiro Iwasa. High-density carrier accumulation in zno field-effect transistors gated by electric double layers of ionic liquids. *Advanced Functional Materials*, 19(7):1046–1053, 2009.

[15] Xiang Leng, Javier Garcia-Barriocanal, Boyi Yang, Yeonbae Lee, J. Kinney, and A. M. Goldman. Indications of an electronic phase transition in two-dimensional superconducting $yba_2cu_3o_{7-x}$ thin films induced by electrostatic doping. *Phys. Rev. Lett.*, 108:067004, Feb 2012.

[16] Rajiv Misra, Mitchell McCarthy, and Arthur F. Hebard. Electric field gating with ionic liquids. *Applied Physics Letters*, 90(5):–, 2007.

[17] J. Garcia-Barriocanal, A. Kobrinskii, X. Leng, J. Kinney, B. Yang, S. Snyder, and A. M. Goldman. Electronically driven superconductor-insulator transition in electrostatically doped $la_2cuo_{4+\delta}$ thin films. *Phys. Rev. B*, 87:024509, Jan 2013.

[18] Hidekazu Shimotani, Haruhiko Asanuma, Atsushi Tsukazaki, Akira Ohtomo, Masashi Kawasaki, and Yoshihiro Iwasa. Insulator-to-metal transition in zno by electric double layer gating. *Applied Physics Letters*, 91(8):–, 2007.

[19] Takuya Fujimoto and Kunio Awaga. Electric-double-layer field-effect transistors with ionic liquids. *Phys. Chem. Chem. Phys.*, 15:8983–9006, 2013.

[20] Shun Wang, Mingjing Ha, Michael Manno, C Daniel Frisbie, and C Leighton. Hopping transport and the hall effect near the insulator–metal transition in electrochemically gated poly(3-hexylthiophene) transistors. *Nat Comms*, 3:1210, nov 2012.

[21] Wei Xie, Shun Wang, Xin Zhang, C. Leighton, and C. Daniel Frisbie. High conductance 2d transport around the hall mobility peak in electrolyte-gated rubrene crystals. *Phys. Rev. Lett.*, 113:246602, Dec 2014.

[22] Jaewoo Jeong, Nagaphani B Aetukuri, Donata Passarello, Steven D Conradson, Mahesh G Samant, and Stuart SP Parkin. Giant reversible, facet-dependent, structural changes in a correlated-electron insulator induced by ionic liquid gating. *Proceedings of the National Academy of Sciences*, page 201419051, 2015.

[23] A. Grockowiak, T. Klein, H. Cercellier, F. Lévy-Bertrand, X. Blase, J. Kačmarčik, T. Kociniewski, F. Chiodi, D. Débarre, G. Prudon, C. Dubois, and C. Marcenat. Thickness dependence of the superconducting critical temperature in heavily doped si:b epilayers. *Phys. Rev. B*, 88:064508, Aug 2013.

[24] Tong Zhang, Peng Cheng, Wen-Juan Li, Yu-Jie Sun, Guang Wang, Xie-Gang Zhu, Ke He, Lili Wang, Xucun Ma, Xi Chen, Yayu Wang, Ying Liu, Hai-Qing Lin, Jin-Feng Jia, and Qi-Kun Xue. Superconductivity in one-atomic-layer metal films grown on si(111). *Nat Phys*, 6(2):104–108, February 2010.

[25] S Gariglio, N Reyren, AD Caviglia, and JM Triscone. Superconductivity at the laalo3/srtio3 interface. *Journal of Physics: Condensed Matter*, 21(16):164213, 2009.

[26] Tsuneya Ando, Alan B. Fowler, and Frank Stern. Electronic properties of two-dimensional systems. *Rev. Mod. Phys.*, 54:437–672, Apr 1982.

[27] J. Bardeen and W. H. Brattain. The transistor, a semi-conductor triode. *Phys. Rev.*, 74:230–231, Jul 1948.

[28] CH Ahn, J-M Triscone, and J Mannhart. Electric field effect in correlated oxide systems. *Nature*, 424(6952):1015–1018, 2003.

[29] Shyue Ping Ong, Oliviero Andreussi, Yabi Wu, Nicola Marzari, and Gerbrand Ceder. Electrochemical windows of room-temperature ionic liquids from molecular dynamics and density functional theory calculations. *Chemistry of Materials*, 23(11):2979–2986, 2011, http://dx.doi.org/10.1021/cm200679y.

[30] Jaewoo Jeong, Nagaphani Aetukuri, Tanja Graf, Thomas D. Schladt, Mahesh G. Samant, and Stuart S. P. Parkin. Suppression of metal-insulator transition in vo2 by electric fieldinduced oxygen vacancy formation. *Science*, 339(6126):1402–1405, 2013.

[31] Trevor A. Petach, Menyoung Lee, Ryan C. Davis, Apurva Mehta, and David Goldhaber-Gordon. Mechanism for the large conductance modulation in electrolyte-gated thin gold films. *Phys. Rev. B*, 90:081108, Aug 2014.

[32] Patrick Gallagher, Menyoung Lee, Trevor A. Petach, Sam W. Stanwyck, James R. Williams, Kenji Watanabe, Takashi Taniguchi, and David Goldhaber-Gordon. A high-mobility electronic system at an electrolyte-gated oxide surface. *Nat Commun*, 6:–, March 2015.

[33] LJ van der Pauw. A method of measuring specific resistivity and hall effect of discs of arbitrary shape. *Philips Res. Rep.*, 13:1–9, 1958.

[34] LJ Van der Pauw. A method of measuring the resistivity and hall coefficient on lamellae of arbitrary shape. *Philips technical review*, 20(8):220–224, 1958.

[35] Simon M Sze and Kwok K Ng. *Physics of semiconductor devices*. John Wiley & Sons, 2006.

[36] R.S.C. Cobbold. *Theory and applications of field-effect transistors*. Wiley-Interscience, 1970.

[37] Hanne Neergaard Waltenburg and John Yates. Surface chemistry of silicon. *Chemical reviews*, 95(5):1589–1673, 1995.

[38] M Morita, T Ohmi, E Hasegawa, M Kawakami, and M Ohwada. Growth of native oxide on a silicon surface. *Journal of Applied Physics*, 68(3):1272–1281, 1990.

[39] JA Venables, GDT Spiller, and M Hanbucken. Nucleation and growth of thin films. *Reports on Progress in Physics*, 47(4):399, 1984.

[40] B. Hoex, J. Schmidt, R. Bock, P. P. Altermatt, M. C. M. van de Sanden, and W. M. M. Kessels. Excellent passivation of highly doped p-type si surfaces by the negative-charge-dielectric al2o3. *Applied Physics Letters*, 91(11):–, 2007.

[41] Armin G Aberle. Overview on sin surface passivation of crystalline silicon solar cells. *Solar Energy materials and solar cells*, 65(1):239–248, 2001.

[42] Thomas Lauinger, Jan Schmidt, Armin G. Aberle, and Rudolf Hezel. Record low surface recombination velocities on 1 Ω cm p-silicon using remote plasma silicon nitride passivation. *Applied Physics Letters*, 68(9):1232–1234, 1996.

[43] Howard C Card. Aluminumsilicon schottky barriers and ohmic contacts in integrated circuits. *Electron Devices, IEEE Transactions on*, 23(6):538–544, 1976.

[44] RF Wolffenbuttel and KD Wise. Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature. *Sensors and Actuators A: Physical*, 43(1):223–229, 1994.

[45] Eric Ailing and Craig Stauffer. Image reversal of positive photoresist a new tool for advancing integrated circuit fabrication. In *1985 Microlithography Conferences*, pages 194–218. International Society for Optics and Photonics, 1985.

[46] Suojiang Zhang, Ning Sun, Xuezhong He, Xingmei Lu, and Xiangping Zhang. Physical properties of ionic liquids: database and evaluation. *Journal of physical and chemical reference data*, 35(4):1475–1517, 2006.

[47] T. Ando. Density-functional calculation of sub-band structure in accumulation and inversion layers. *Phys. Rev. B*, 13:3468–3477, Apr 1976.

[48] A. Hartstein and A.B. Fowler. Impurity bands in inversion layers. *Surface Science*, 73(0):19 – 30, 1978.

[49] A Zabrodskii and K Zinoveva. Low-temperature conductivity and metal–insulator transition in compensate n-ge. *Zh. Eksp. Teor. Fiz*, 86:742, 1984.

[50] Boris Isaakovich Shklovskii and Alex L Efros. *Electronic properties of doped semiconductors*. Springer, 2012.

[51] E. Abrahams, P. W. Anderson, D. C. Licciardello, and T. V. Ramakrishnan. Scaling theory of localization: Absence of quantum diffusion in two dimensions. *Phys. Rev. Lett.*, 42:673–676, Mar 1979.

[52] T. N. Zavaritskaya and É. I. Zavaritskaya. Metal-insulator transition in inversion channels of silicon mos structures. *JETP Letters*, 45:609, 1987.

[53] Subir Sachdev. *Quantum phase transitions*. Wiley Online Library, 2007.

[54] Eugene Wigner. On the interaction of electrons in metals. *Physical Review*, 46(11):1002, 1934.

[55] Y. Hanein, U. Meirav, D. Shahar, C. C. Li, D. C. Tsui, and Hadas Shtrikman. The metalliclike conductivity of a two-dimensional hole system. *Phys. Rev. Lett.*, 80:1288–1291, Feb 1998.

[56] S. C. Dultz, H. W. Jiang, and W. J. Schaff. Absence of floating delocalized states in a two-dimensional hole gas. *Phys. Rev. B*, 58:R7532–R7535, Sep 1998.

[57] B. Spivak, S. V. Kravchenko, S. A. Kivelson, and X. P. A. Gao. Colloquium. *Rev. Mod. Phys.*, 82:1743–1766, May 2010.

[58] D. Simonian, S. V. Kravchenko, M. P. Sarachik, and V. M. Pudalov. Magnetic field suppression of the conducting phase in two dimensions. *Phys. Rev. Lett.*, 79:2304–2307, Sep 1997.

[59] Zengwei Zhu, Huan Yang, Benoit Fauque, Yakov Kopelevich, and Kamran Behnia. Nernst effect and dimensionality in the quantum limit. *Nat Phys*, 6(1):26–29, January 2010.

[60] S. Das Sarma and E. H. Hwang. Two-dimensional metal-insulator transition as a strong localization induced crossover phenomenon. *Phys. Rev. B*, 89:235423, Jun 2014.

[61] S. Das Sarma, E. H. Hwang, K. Kechedzhi, and L. A. Tracy. Signatures of localization in the effective metallic regime of high-mobility si mosfets. *Phys. Rev. B*, 90:125410, Sep 2014.

[62] Wei Xie, Shun Wang, Xin Zhang, C. Leighton, and C. Daniel Frisbie. High conductance 2d transport around the hall mobility peak in electrolyte-gated rubrene crystals. *Phys. Rev. Lett.*, 113:246602, Dec 2014.

[63] F. F. Fang and A. B. Fowler. Transport properties of electrons in inverted silicon surfaces. *Phys. Rev.*, 169:619–631, May 1968.

[64] BL Altshuler, D Khmel'Nitzkii, AI Larkin, and PA Lee. Magnetoresistance and hall effect in a disordered two-dimensional electron gas. *Physical Review B*, 22(11):5142, 1980.

[65] Elihu Abrahams, Sergey V. Kravchenko, and Myriam P. Sarachik. Metallic behavior and related phenomena in two dimensions. *Rev. Mod. Phys.*, 73:251–266, Mar 2001.

[66] N Klein and H Gafni. The maximum dielectric strength of thin silicon oxide films. *Electron Devices, IEEE Transactions on*, (2):281–289, 1966.

[67] M. V. Fischetti, Z. A. Weinberg, and J. A. Calise. The effect of gate metal and sio2 thickness on the generation of donor states at the si-sio2 interface. *Journal of Applied Physics*, 57(2):418–425, 1985.

[68] Yu Xia, Wei Xie, P. Paul Ruden, and C. Daniel Frisbie. Carrier localization on surfaces of organic semiconductors gated with electrolytes. *Phys. Rev. Lett.*, 105:036802, Jul 2010.

[69] Hidekazu Shimotani, Haruhiko Asanuma, and Yoshihiro Iwasa. Electric double layer transistor of organic semiconductor crystals in a four-probe configuration. *Japanese journal of applied physics*, 46(6R):3613, 2007.

[70] S. Das Sarma and E. H. Hwang. Short-range disorder effects on electronic transport in two-dimensional semiconductor structures. *Phys. Rev. B*, 89:121413, Mar 2014.

[71] J. Nelson and A. M. Goldman. Thin film cryogenic thermometers defined with optical lithography for thermomagnetic measurements on films. *Review of Scientific Instruments*, 86(5):–, 2015.