QUADRATURE FREQUENCY SYNTHESIS FOR WIDEBAND WIRELESS TRANSCEIVERS

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To my dear parents...
To Dalia

Abstract

In this thesis, three different techniques pertinent to quadrature LO generation in high data rate and wideband RF transceivers are presented. Prototype designs are made to verify the performance of the proposed techniques, in three different technologies: IBM 130nm CMOS process, TSMC 65nm CMOS process and IBM 32nm SOI process. The three prototype designs also cover three different frequency bands, ranging from 5GHz to 74GHz.

First, an LO generation scheme for a 21 GHz center-frequency, 4-GHz instantaneous bandwidth channelized receiver is presented. A single 1.33 GHz reference source is used to simultaneously generate 20 GHz and 22 GHz LOs with quadrature outputs. Injection locking is used instead of conventional PLL techniques allowing low-power quadrature generation. A harmonic-rich signal, containing both *even and odd harmonics* of the input reference signal, is generated using a digital pulse slimmer. Two ILO chains are used to lock on to the 10^{th} and 11^{th} harmonics of the reference signal generating the 20 GHz and the 22 GHz quadrature LOs respectively. The prototype design is implemented in IBM's 130 nm CMOS process, draws 110 mA from a 1.2 V supply and occupies an active area of 1.8 mm^2.

Next, a wide-tuning range QVCO with a novel complimentary-coupling technique is presented. By using PMOS transistors for coupling two VCOs with NMOS g_m-cells, it is shown that significant phase-noise improvement (7-9 dB) can be achieved over the traditional NMOS coupling. This breaks the trade-off between quadrature accuracy and phase-noise, allowing reasonable accuracy without a significant phase-noise hit. The proposed technique is frequency-insensitive, allowing robust coupling over a wide tuning range. A prototype design is done in TSMC 65nm process, with 4-bits of discrete tuning

spanning the frequency range 4.6-7.8 GHz (52% FTR) while achieving a minimum FOM of 181.4dBc/Hz and a minimum FOMT of 196dBc/Hz.

Finally, a wide tuning-range millimeter wave QVCO is presented that employs a modified transformer-based super-harmonic coupling technique. Using the proposed technique, together with custom-designed inductors and metal capacitors, a prototype is designed in IBM 32nm SOI technology with 6-bits of discrete tuning using switched capacitors. Full EM-extracted simulations show a tuning range of 53.84GHz to 73.59GHz, with an FOM of 173 dBc/Hz and an FOMT of 183 dBc/Hz. With 19.75GHz of tuning range around a 63.7GHz center frequency, the simulated FTR is 31%, surpassing all similar designs in the same band. A slight modification in the tank inductors would enable the QVCO to be employed in multiple mm-Wave bands (57-66 GHz communication band, 71-76 GHz E-band, and 76-77 GHz radar band).

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Chapter 1

Introduction

With the proliferation of wireless technology in the last two decades, a plethora of new devices and applications have revolutionized our everyday life. Portable devices with wireless connectivity have become ubiquitous, while continuously getting thinner and lighter (Fig. 1.1). Moreover, wireless data rates have increased rapidly from the slow rates of the earliest cellular networks of the late nineties to the dazzling speeds of the next generation 4G-LTE (Fig. 2). In addition to the increased speeds, the wireless capabilities have also increased. Modern smartphones and tablets have GPS (for navigation), Bluetooth (for wireless headsets and file transfer), WiFi (for wireless internet), GSM and CDMA (for phone calls and texting), and FM radio. And some even have wireless NFC (Near Field Communication) capabilities allowing us to pay for drinks and food on the go with cell phones.

These advances, however, do not come for free. Higher data rates come with the cost of higher power consumption, adversely affecting battery life of portable devices. This is further aggravated by the small form factors which don't allow large batteries. Additionally, the multiple radios needed require the use of a large number of integrated circuit chips. This, in turn, makes it more difficult to reduce form factors and power

Figure 1.1: Evolution of the cell-phone [1]

consumption. With the widespread use of high-definition multi-media, data rates are projected to increase and higher speed wireless standards (such as WirelessHD [3]) are expected to emerge.

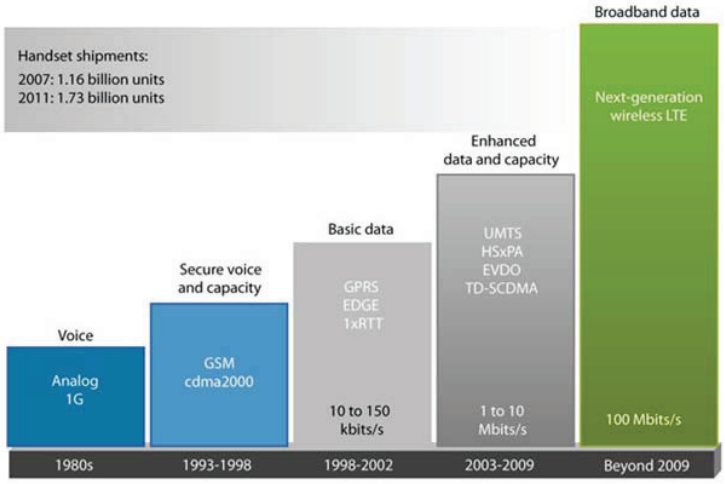

Figure 1.2: Evolution of the cellular data rates [2]

In high data rate wireless receivers, a major power hog is the analog-to-digital converter (ADC) (which is responsible for converting radio signals at the antenna into digital ones-and-zeros that can be shown on the screen or heard via the speaker). One

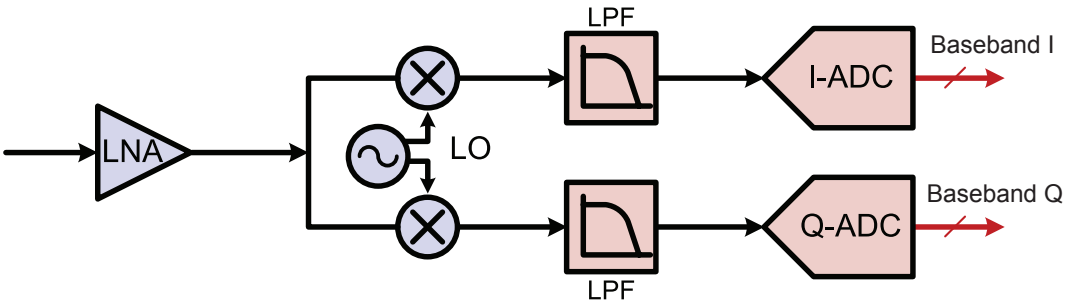

Figure 1.3: A typical direct-conversion receiver

way to reduce the power consumption in such receivers is to split the incoming signal into a number of parallel streams (channelization), each with a smaller data rate. The aggregate data rate remains the same, but the overall energy is reduced [4]. On the other hand, the number of chips can be reduced by incorporating programmability into the radio design, allowing a single radio to be used with multiple wireless standards, i.e., by designing software defined radios (SDR). An important component of an SDR is wide tuning range quadrature oscillator, that enables quadrature LO generation for direct downconversion in different bands.

This work presents a quadrature LO generation scheme for a high data rate (4GHz instantaneous bandwidth) wireless receiver, as well as wide tuning range quadrature VCO design for SDR-type applications in both the lower GHz range (5-10GHz) and millimeter-wave range (50-70GHz).

1.1 Frequency Channelization

Fig. 1.3 shows a typical direct-conversion receiver. A low-noise amplifier amplifies the input signal, which is passed on to quadrature mixers for downconversion. Quadrature mixing is typically done by using quadrature LO, although quadrature signal generation can be done as well. A low-pass filter follows the mixer, to filter out the higher frequency

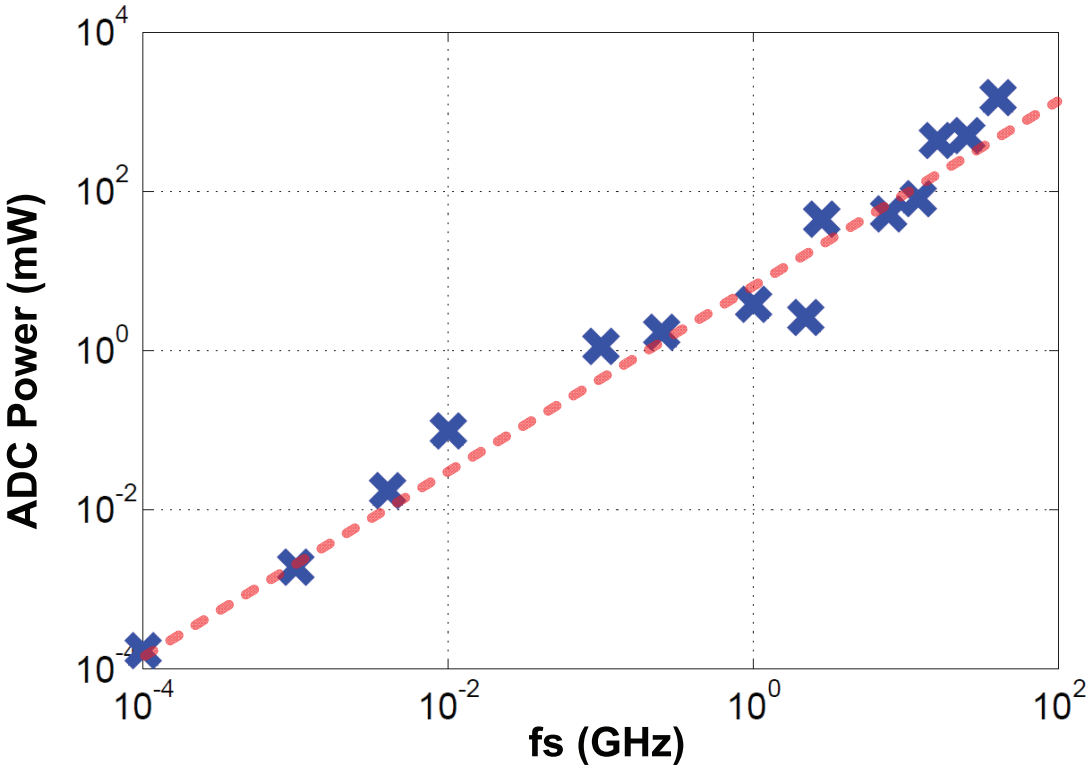

Figure 1.4: ADC power consumption versus sampling rate (f_s)

component. Finally, an ADC converts the downconverted and filtered data into digital for demodulation and post-processing. A major burden of the receiver linearity lies on the ADC, since it is the last block in the receiver and subject to large signal amplitudes specially in the presence of in-band blocker signals (the filter attenuates out-of-band blockers) [5]. Due to this linearity constraint, the ADC block usually has significant power consumption.

Unlike the RF front-end, the ADC power consumption rises exponentially with increased bandwidth. To illustrate this point, consider [6] which presents a GSM receiver with bandwidth of 200kHz, and [7] which presents a 60GHz WirelessHD receiver with

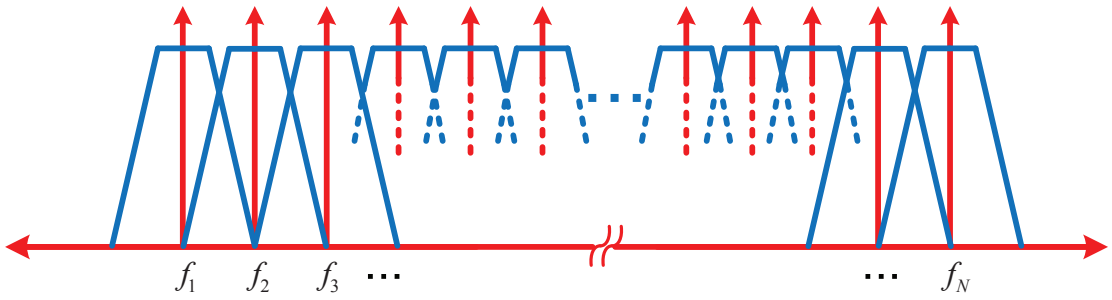

Figure 1.5: Frequency channelization

1GHz of bandwidth. Although the bandwidth of the WirelessHD receiver in [7] is 50-times higher than the bandwidth of the GSM receiver in [6], the power consumption of the RF front-end in [7] is only 1.6 times higher than that in [6] (454mW for WirelessHD versus 235mW for GSM).

Fig. 1.4, on the other hand, shows the power consumption of ADCs versus their sampling rate based on the data in [8]. At each sampling rate, the ADC with the lowest power consumption at that sampling rate is chosen for the plot. Power versus sampling frequency (f_s) is, then, plotted on a Log-Log scale. As evident from Fig. 1.4, the power consumption increases exponentially with sampling rate (f_s), i.e. $Power \propto (f_s)^n$. Fitting shows that $n \approx 2$; a large power saving can be achieved by reducing the ADC sampling rate.

To maintain the overall bandwidth, while reducing the ADC sampling rate, frequency channelization can be employed as shown in Fig. 1.5. The signal bandwidth (BW) is divided into N different chunks, each of bandwidth $\frac{BW}{N}$. Hence, N different streams need to be digitized, requiring N ADCs each with a sampling rate $\frac{f_s}{N}$ (f_s being the sampling frequency of the unchannelized signal). Hence, the ratio of the power consumption of the channelized ADCs P_c to the power consumption of a single ADC P_s can be given by:

$$\frac{P_c}{P_s} \approx \frac{N \times \left(\frac{f_s}{N}\right)^2}{f_s^2} = \frac{1}{N} \tag{1.1}$$

This means that the ADC power consumption can be reduced roughly N times by using channelization. Actual power savings will depend on the extra power consumed for performing channelization, as well as additional amplification that might be needed post-channelization. Nevertheless, significant power savings can be achieved through channelization. Moreover, channelization improves the RF receiver performance by making the system more interference tolerant [9]. For instance, if an interferer falls onto one of the channels, that channel and the associated ADC can be shut-off, reducing the data rate but without compromising the overall performance. If a single ADC is used, on the other hand, a single large interferer can overwhelm leading to a total signal blockage. *A major challenge for channelization is the generation of multiple, uniformly spaced, quadrature LOs for downconversion of the different channels.*

1.2 Software Defined Radio

Software-defined radio receivers allow a single front-end to be used for multiple standards, through software programmability and reconfigurability. While the original "Mitola" [10] SDR has an ADC directly following the antenna, allowing all downconversion and post-processing to be performed in digital domain, this approach is not practical with current technology. A more practical approach is to use a generic direct-conversion receiver, similar to that shown in Fig. 1.3, with programmable filters as well as programmable LO to cover multiple bands [11].

For very wideband programmability in the LO path (close to a decade), banks of VCOs are needed [11]. Quadrature VCOs allow the direct generation of quadrature LOs without requiring the VCO to operate at twice the desired operating frequency.

Moreover, a wide tuning range in the QVCO allows less number of QVCOs in the bank, thus reducing area requirements, complexity, and design time.

1.3 Organization

This thesis is focused on quadrature LO generation techniques for wideband applications. "Wideband" includes instantaneous wide bandwidth system, as well as systems with smaller instantaneous bandwidth but have a wide range of center (or carrier frequencies).

Chapter 2 explores the use of injection locking techniques to generate simultaneous LOs for a channelized receiver. Two injection-locking based chains are designed to generate two simultaneous carriers at 20 and 22-GHz with quadrature outputs. This enables the operation of 4-GHz bandwidth receiver while relaxing the constraints on the required ADCs (as discussed in section 1.5).

Chapter 3 presents a wide tuning range QVCO which can be tuned from 5.5–10.1 GHz. A new simple and robust quadrature coupling technique is introduced that allows the wide tuning range to be achieved without sacrificing the VCO's Figure-Of-Merit (FOM). The proposed technique is compatible with low supply voltages of current technologies, and is frequency insensitive, relaxing the classical design constraints/trade-offs found in other QVCOs.

Chapter 4 presents a wide tuning range mm-Wave QVCO. Through merging two different coupling techniques, and by the use of custom-designed passives, a 19.75GHz tuning-range is achieved around a ≈64GHz center frequency for a 31% tuning range. With a slight modification, the presented design can cover three different mm-Wave bands, possiblt allowing a mm-Wave SDR.

Finally, chapter 5 some of the research contributions of the presented work, as well as possible future work.

Chapter 2

Channelized ILO

2.1 Introduction

Wireless technology continually demands higher data rates. Increasing the bandwidth is the most effective way to achieve higher data rates [12]. Higher bandwidths, however, imply a high ADC clocking speed as well as a high dynamic range making the ADC power-hungry and difficult to design, if at all feasible. Frequency channelization is an effective way to alleviate this problem. It reduces the clocking speed of the ADC and also increases the immunity to narrow-band interferers, hence reducing the ADC dynamic range requirements [4]. Channelization also reduces the number of independent in-band signals, hence, reducing the peak to average power ratio (PAPR) [13], leading to an overall reduction in power consumption.

A channelized receiver, capable of achieving 4-GHz of instantaneous bandwidth, around a 21 GHz center frequency, is shown in Fig. 2.1. An external wideband LNA amplifies the entire band. The wideband signal is then down-converted into two 2-GHz channels using two sets of quadrature mixers, operating at 20 GHz and 22 GHz. Two sets of lowpass filters complete the channelization. The desired wideband signal

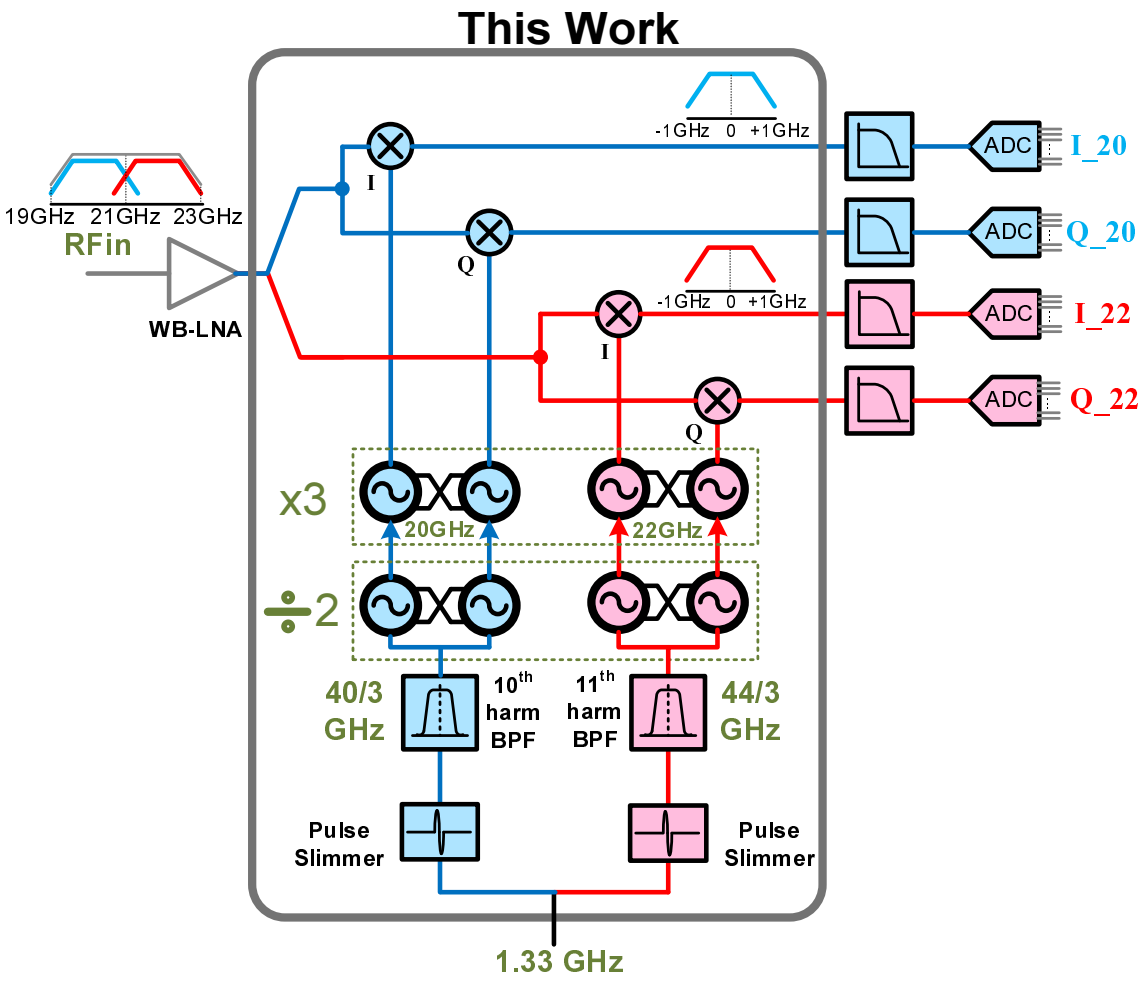

Figure 2.1: Simultaneous dual channel 19GHz - 23GHz receiver

can then be reconstructed digitally by upsampling each digitized stream by two and the use of digital reconstruction filters to account for the filters' phase and amplitude responses [4]. For a faithful reconstruction of the original signal, the two channels need to be phase synchronous.

A major challenge for the receiver in Fig. 2.1 is the generation of two phase synchronous quadrature LOs at 20 GHz and 22 GHz. PLL-based solutions such as [9] are ineffcient at mm-wave frequencies due to the need of power-hungry high frequency dividers and SSB mixers. Besides, parasitics become prominent at these frequencies, limiting mixer linearity and resulting in a large number of spurious components.

Injection locking is an alternative approach for LO generation in mm-wave designs [14–17]. Most designs, however, are aimed at a single LO. The design in [14] implements simultaneous LOs but it has two drawbacks: it is not capable of quadrature signal generation and it can only generate integer multiples of the reference signal. Hence, a different approach needs to be used for a more generalized solution.

This work addresses the use of injection locking to simultaneously generate 20 GHz and 22 GHz phase synchronous quadrature LOs using a single 1.33 GHz reference [18]. Compared to [19] this paper provides additional details on the circuit design, supporting simulation results, an overview on the electromagnetic (EM) design methodology and new measurement results. Section 2.2 provides an overall system overview. Section 2.3 presents circuit design details and simulation results. Section 2.4 discusses the EM design methodology used to ensure proper operation of high frequency oscillators. Section 2.5 discusses PVT considerations. Section 2.6 provides measurement results. Finally, Section 2.7 outlines overall conclusions.

2.2 System Overview

The LO system block diagram is shown in Fig. 2.1. For this specific design, only two channels are implemented. The system, however, can be extended to an arbitrary number of channels. The major limiting factor would be the diminishing amplitude of higher harmonics of the pulse-slimmer for a given process technology. Both even and odd harmonics of the input signal are used, unlike the designs in [20–22], making the system more flexible and allowing smaller channel spacing.

The n^{th} and $(n+1)^{th}$ harmonics of the reference are generated using pulse-slimmers. The pulse-slimmers' outputs contains a large number of undesired harmonics as well. Hence, the pulse-slimmer in each chain is followed by a bandpass filter (BPF) to emphasize the harmonics of interest and suppress the undesired harmonics. Up to this point, only a single phase is present. To generate quadrature outputs, the BPF's output is then fed to an injection locked frequency divider (ILFD) which performs a divide-by-2 operation. The quadrature outputs are further multiplied using quadrature injection locked frequency multpliers (ILFM), generating $\frac{3}{2}nf_{ref}$ and $\frac{3}{2}(n+1)f_{ref}$ LOs. To generate 20 GHz and 22 GHz, $n = 10$ and $f_{ref} = 1.33$ GHz are chosen. System aspects and architectural choices of each block are discussed further in the following subsections.

2.2.1 Pulse Slimmer

Each chain in Fig. 2.1 starts with a pulse-slimmer which generates all the harmonics of the input signal. The duty cycle of the pulse-slimmed signal is optimized in order to maximize the harmonics of interest. For a square wave with a duty cycle D and a unity peak-to-peak amplitude, the amplitude y of the n^{th} harmonic can be given by [23]:

$$y = D\frac{sin(n\pi D)}{n\pi D} \tag{2.1}$$

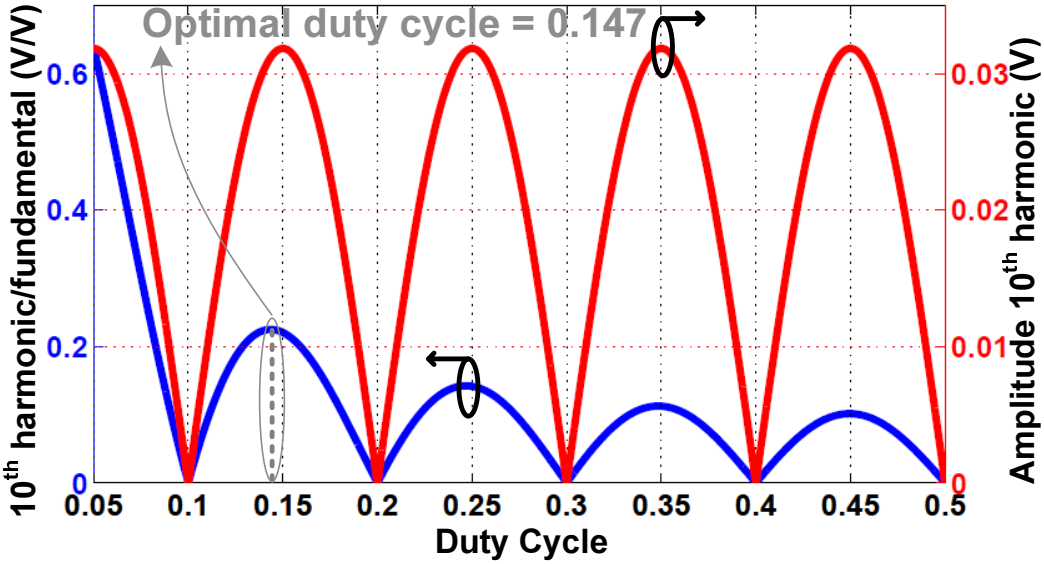

Figure 2.2: Amplitude of 10^{th} harmonic and ratio of 10^{th} harmonic to fundamental

For the n^{th} harmonic, there exists several values of D for which the amplitude is maximized. In fact, according to Eqn.(2.1) the absolute value of the amplitude of the n^{th} harmonic is periodic in D with a period $D = \frac{1}{n}$. Hence, an additional criterion is needed to select the optimum duty cycle. In this case, it is desirable to reduce the amplitude of the lower harmonics (which is naturally larger) as well. This reduces the amount of desensitization, caused by the undesired low-frequency (and high amplitude) harmonics, to the following stage (the BPF).

Based on these two criteria, a plot is made for the amplitude of the 10^{th} harmonic and the ratio of the 10^{th} harmonic to the fundamental versus D. As shown in Fig. 2.2, the maximum value of the 10^{th} harmonic is periodic in D with a period of $\frac{1}{10}$. Nevertheless, the ratio of the 10^{th} harmonic to the fundamental is higher for lower values of D. The absolute maximum of the ratio, which simultaneously corresponds to a maximum of the absolute value of the harmonic, occurs for $D \approx \frac{1}{20}$. This value of D is too small to be realized practically, hence the next higher value (highlighted in Fig. 2.2) is chosen. In

a practical scenario, a value of D ranging from $\frac{1}{8}$ to $\frac{1}{6}$ can be used. This range of D is also usable for the other chain $n = 11$. This means that a single pulse slimmer can be used for both chains. However, in our design, chip floorplan considerations lead to the use of two pulse-slimmers (one for each chain) as discussed in Section 2.3.5.

In addition to duty cycle optimization, a differentiator is added after the pulse slimmer to further enhance higher harmonics and suppress lower ones. The circuit implementation details of the slimmer and the differentiator are discussed in Section 2.3.1.

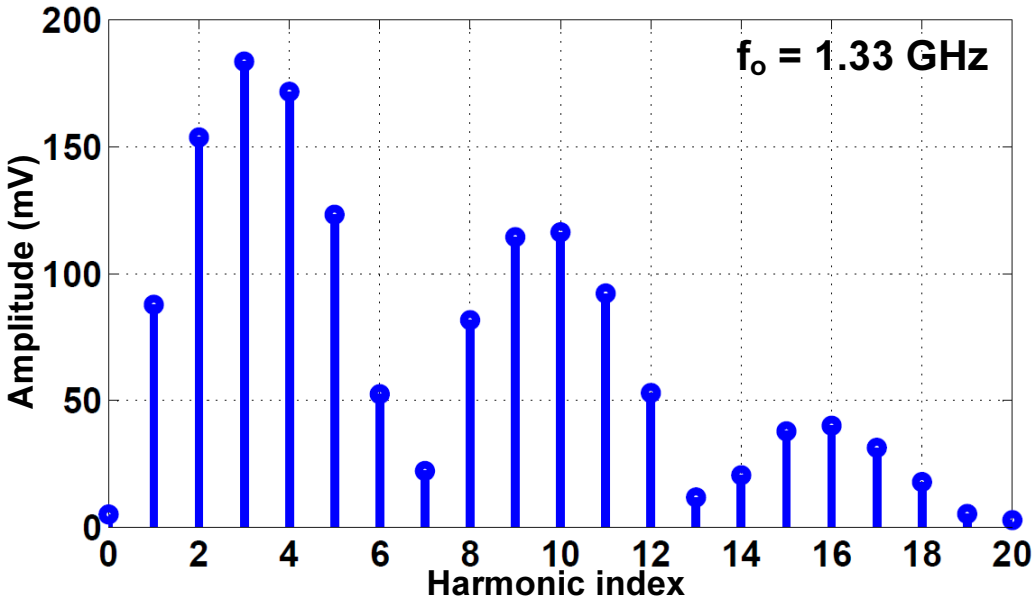

Figure 2.3: Pulse slimmer output spectrum (SpectreRF® simulation)

2.2.2 Bandpass Filter

The techniques discussed in Section 2.2.1 help reduce the amplitude of the undesired harmonics. Nevertheless, the amplitude of lower harmonics remains higher than the desired harmonics. Fig. 2.3 shows the output harmonics of the pulse slimmer used in the 20 GHz chain as predicted by SpectreRF® simulations. It can be clearly seen

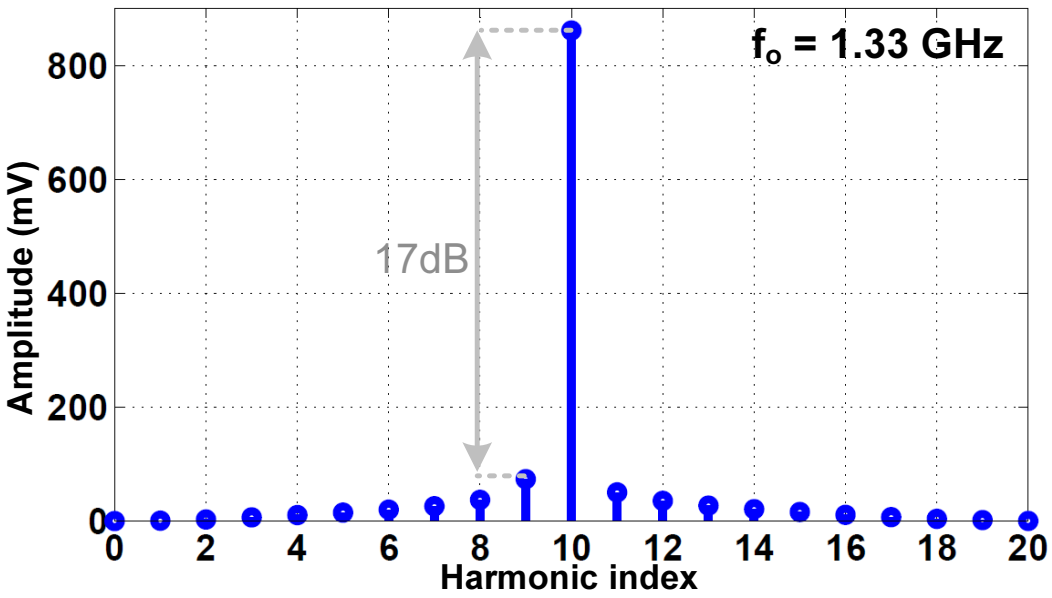

Figure 2.4: BPF output spectrum (SpectreRF® simulation)

that the harmonics close to the fundamental are 2-3 times higher than the desired 10^{th} harmonic. In the absence of a BPF, this would have an adverse effect on the ILFD. The high-amplitude low-frequency harmonics would saturate the input g_m stage of the ILFD, desensitizing it with respect to the desired harmonic. This, in turn, results in a limited lock range and hence higher phase noise [24] and lower process tolerance. In the presence of the BPF, on the other hand, the low frequency harmonics are highly suppressed as shown in Fig. 2.4 (SpectreRF® simulations). Unlike the BPF in [20], an active injection-locking based BPF is used in this design. This has the advantage of higher gain at the frequency of interest, as well as higher Q for the filtering action with a lower power consumption (the 10^{th} harmonic is amplified by a factor of 7 and the highest harmonic is 17dB below desired signal). The drawback, however, is the possibility for higher phase noise due to the intrinsic phase noise of the injection-locked oscillator (ILO). The output phase noise of a conventional BPF is approximately the same as the

input's phase noise. With an injection-locked BPF, however, additional phase noise is added by the oscillating core. Nevertheless, with proper design the additional phase noise can be made negligible while retaining the high gain and high Q advantages [24]. A more detailed comparison between conventional and injection-locked based BPF is provided in Section 2.3.2.

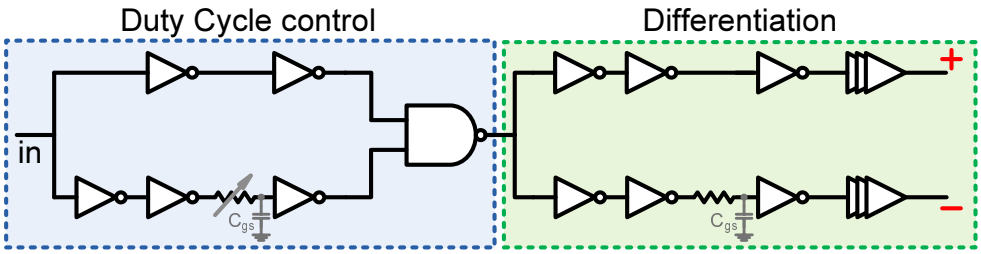

Figure 2.5: Digital pulse slimmer (PSLIM) circuit diagram

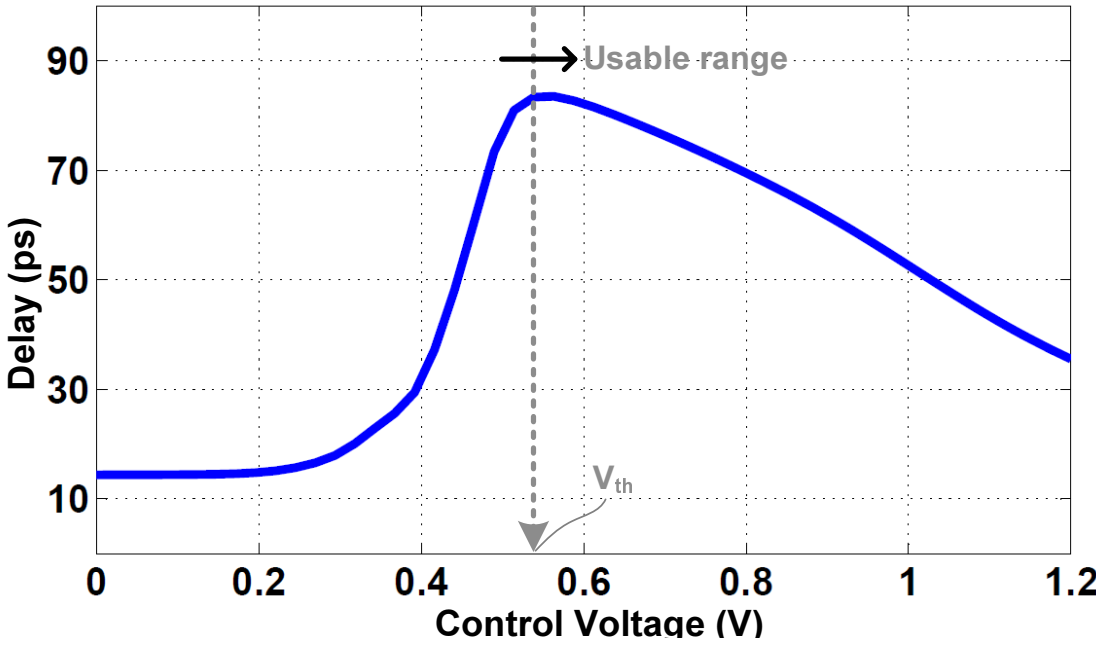

Figure 2.6: Variable delay versus control voltage

2.2.3 Injection Locked Frequency Divider

Following the BPF, an injection-locked frequency divider similar to the one in [20] is used. The injection method, however, is different than the one in [20]. This is discussed in detail in Section 2.3.3.

An ILFD is used for quadrature generation to get good phase accuracy [20, 25, 26] without the use of multi-stage polyphase filters (which would result in signal attenuation [27]). It is to be noted that the ILFD in each chain operates at one third the final LO frequency. A similar divide-by-2 scheme for quadrature generation in a PLL would have required operation at *twice the final LO frequency*. The suggested scheme, hence, provides a more feasible solution with a lower power consumption.

2.2.4 Injection Locked Frequency Tripler

The final stage in each chain is an injection-locked frequency tripler. The tripler takes I and Q injection inputs and generates I and Q outputs at three times the input frequency [28]. Circuit design details of the multiplier are presented in Section 2.3.4.

2.3 Circuits

In this section, the circuit details of each of the synthesizer chain blocks are discussed and relevant simulation results are presented.

2.3.1 Pulse Slimmer

One of the key features of the proposed synthesizer architecture is that it makes use of both the even and odd harmonics of the reference clock signal. As discussed in Section 2.2.1, the 10^{th} and 11^{th} harmonics have to be maximized while suppressing the other unwanted harmonics as much as possible. This is achieved by a two-stage,

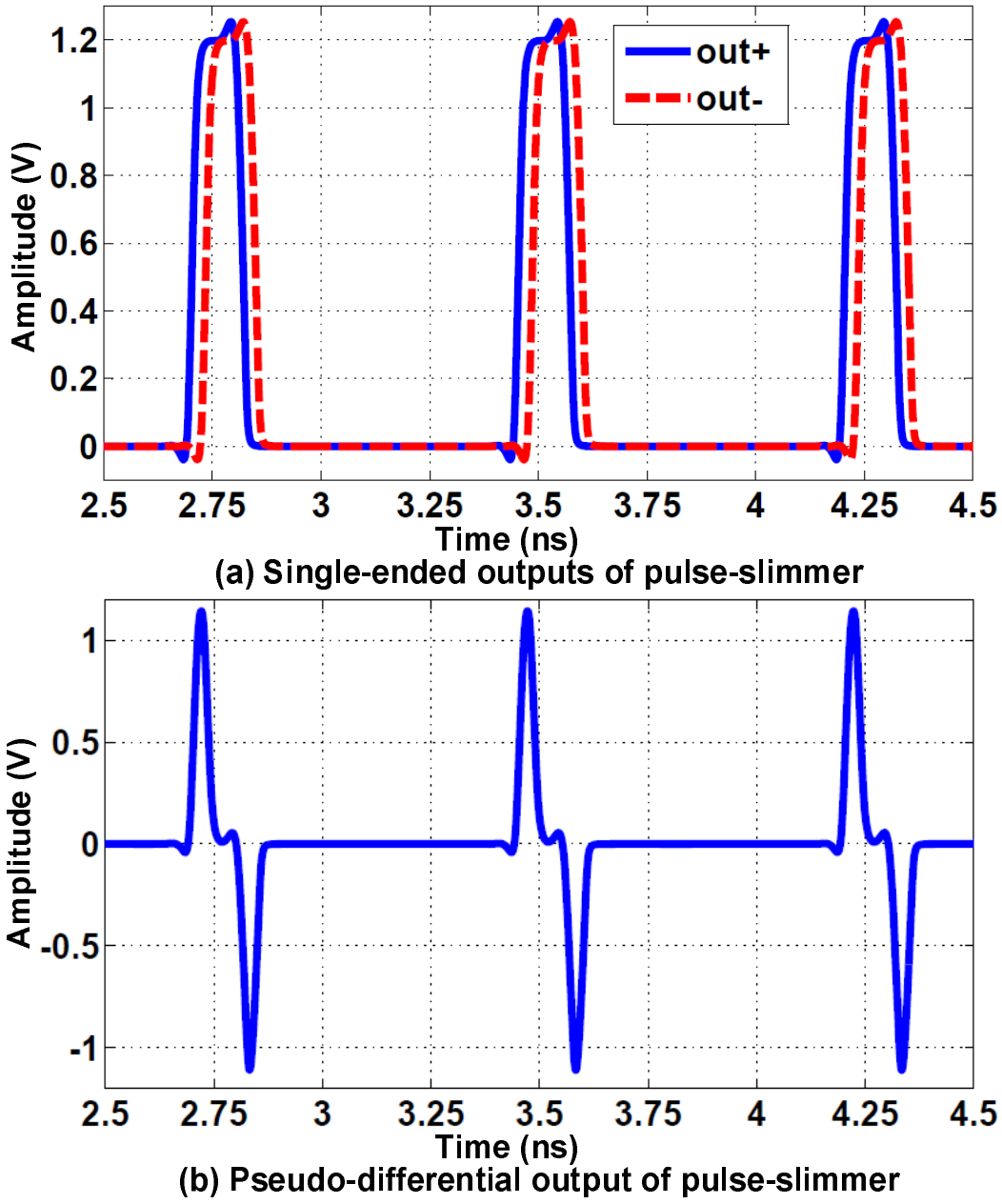

Figure 2.7: Pulse-slimmer output

semi-digital design as shown in Fig. 2.5.

The first stage is a duty cycle control stage; it converts the input 50% duty cycle clock to the optimal value discussed in Section 2.2.1 ($\frac{1}{6}$ to $\frac{1}{8}$). This is done by NAND'ing two paths with a one inverter delay difference. Since the required delay is slightly higher, additional fine delay is added by means of a MOS resistor. This delay can be controlled off-chip. In this process, one inverter delay amounts to around 26 ps; the variable delay can be changed from 35 ps to 83 ps as shown in Fig. 2.6.

The second stage performs two functions: it acts as a discrete-time differentiator, and it converts the single-ended signal to a pseudo-differential signal. This is done by splitting the signal into two paths with equal number of inverters. One of the two paths, however, has an additional small delay implemented by a fixed MOS resistor (the two output signals are shown in Fig. 2.7 (a)). Hence, the pseudo-differential output takes the form $\left(1 - z^{-1}\right) s(t)$, which is a differentiated version of the input signal $s(t)$. Here the z^{-1} is the delay difference between the two paths. Combining this with the inherent low-pass nature of the chain results in an overall bandpass response as evident from Fig. 2.7(b).

2.3.2 Bandpass Filter

As discussed in Section 2.2.2, an active injection-locking based bandpass filter is used in this design. Fig. 2.8 shows the schematics of a conventional bandpass filter and the injection-locking based bandpass filter used in this work. Under free-running conditions, the ILO's amplitude (V_{osc}) has a finite value. Once locked, the output amplitude remains the same creating an effective gain of V_{osc}/V_{inj}, V_{inj} being the injected signal's amplitude. With a constant output amplitude, the filter's gain depends on V_{inj} with smaller V_{inj} resulting in larger gain as shown in Fig. 2.9. This nonlinear behavior, though undesirable for general filtering applications, doesn't pose a problem here as the

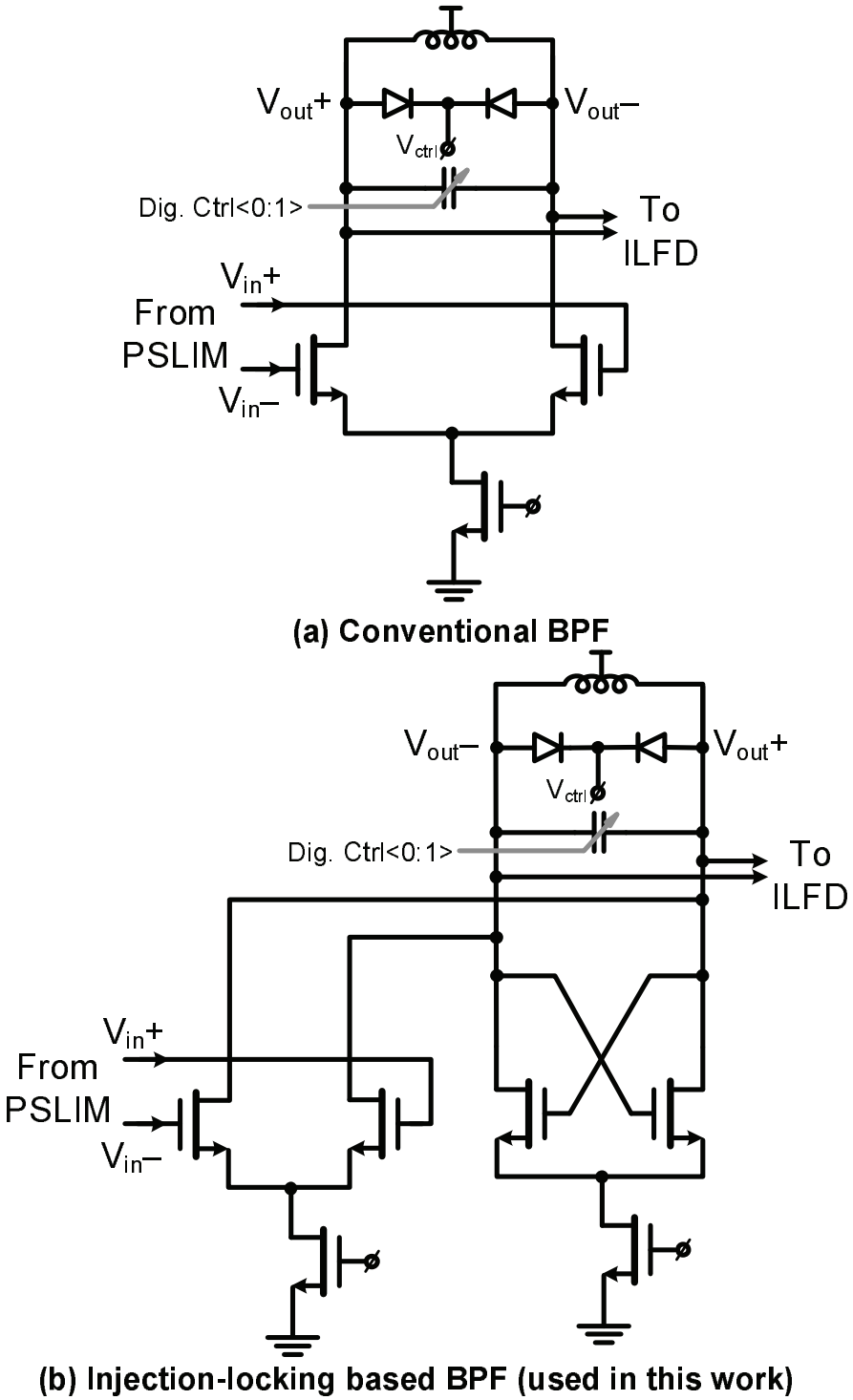

Figure 2.8: Bandpass Filter (BPF) - bias details omitted

desired signal is a single-tone sinusoid. As evident from Fig. 2.9, the conventional BPF has a flat gain versus input amplitude, whereas the ILO-based BPF's gain has a -6 dB/octave slope suggesting a $\frac{1}{V_{inj}}$ gain dependance. At a 100mV input amplitude (the amplitude of the 10^{th} harmonic from pulse-slimmer), the ILO-based BPF has a 3 dB higher gain than the conventional BPF. An additional benefit of the ILO based BPF is that the output amplitude saturates even for small inputs and remains relatively independent of the input signal amplitude, i.e., it behaves as an AGC providing constant amplitude to the next stage. The only tradeoff is that at lower amplitudes the phase noise increases [24] suggesting a moderate input level as a good compromise.

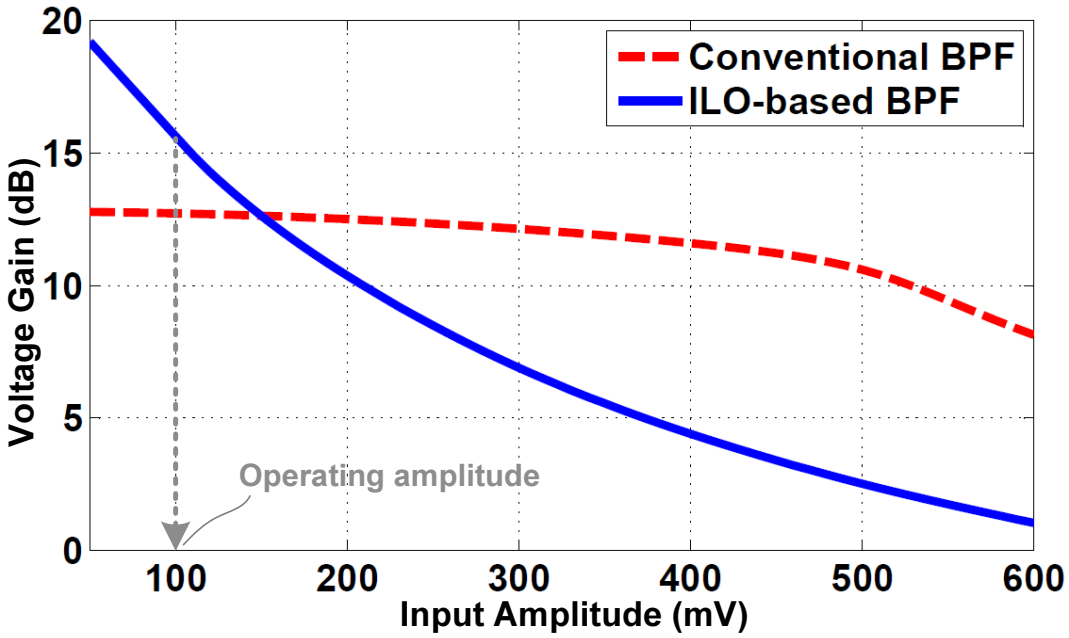

Figure 2.9: Simulated gain of BPF (under equal power consumption)

In addition to the higher gain, the injection-locking based bandpass filter also provides higher suppression of undesired harmonics. A spur at an offset f_m from the input signal is suppressed by f_m/f_L [21], where f_L is the single-sided lock range. As shown in fig. 2.10, the effective Q of the ILO-based BPF is almost twice that of the passive LC

tank (Q ≈30 for ILO-based filter versus Q ≈13 for conventional filter). Two ILO-based BPFs are designed for the 20 GHz and 22 GHz chains, with center frequencies of 13.33 GHz and 14.66 GHz respectively. Each ILO draws 4-mA from a 1.2 V supply.

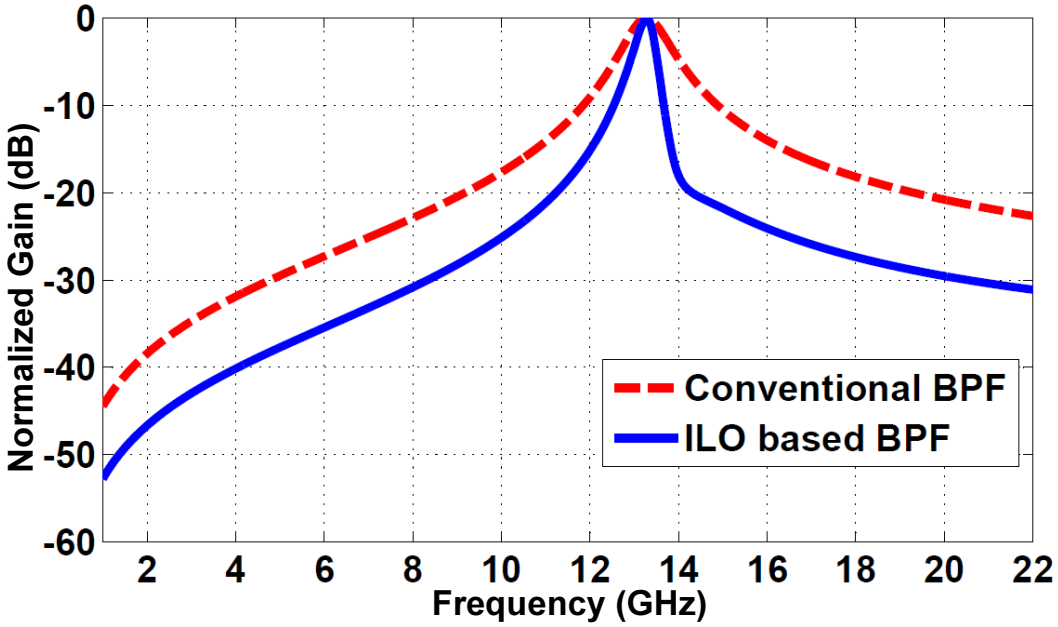

Figure 2.10: Simulated quality factor of conventional and ILO-based BPF

Varactor

Bias details of the varactor are shown in Fig. 2.12. The same structure is also used in the ILFD and the ILFM. Hyper-abrupt PN junctions are used as varactors since their quality factor is higher than that of the conventional MOS varactors at the frequencies of interest. As shown in Fig. 2.13, a large parasitic capacitor is formed between the varactor's negative terminal and the substrate degrading the Q-factor. The positive terminal, on the other hand, is not prone to this parasitic capacitance. Hence, the positive terminal has a Q-factor which is 3-5 times higher than that of the negative terminal as shown in Fig. 2.11.

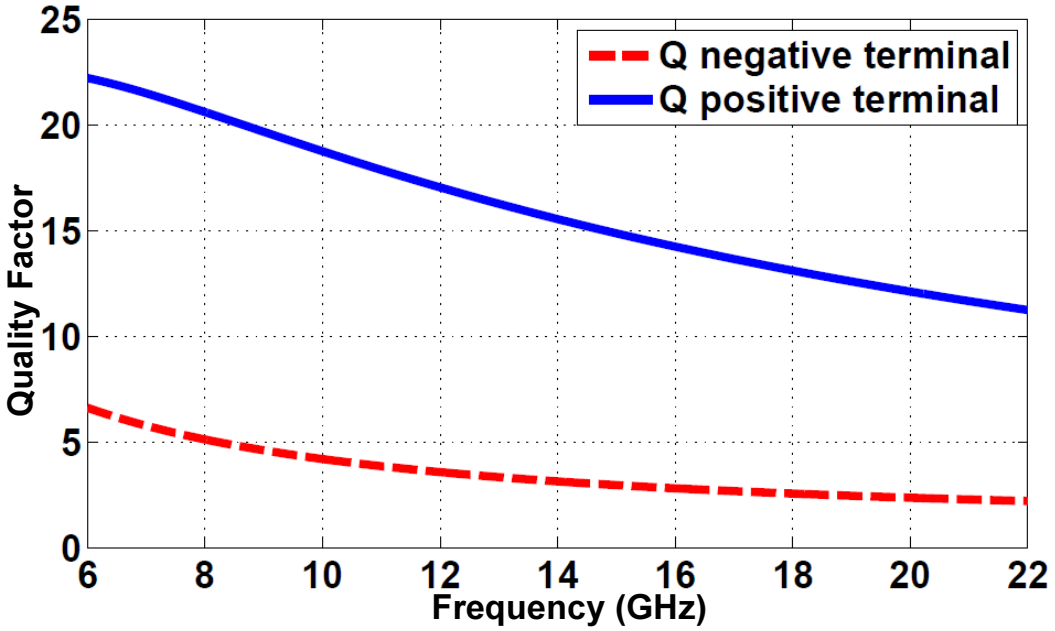

Figure 2.11: Varactor quality factor at negative and positive terminals

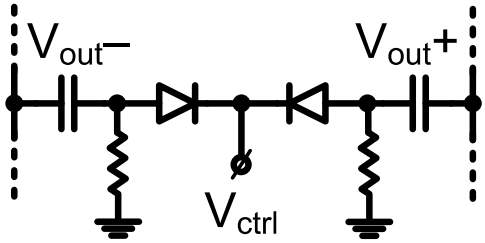

Figure 2.12: Varactor bias details

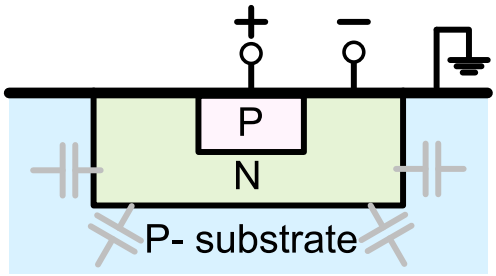

Figure 2.13: Structure of hyper-abrupt PN-junction varactor (parasitics highlighted)

Capacitor bank

The details of the two-bit capacitor bank are shown in Fig. 2.14 [29]. A similar capacitor bank structure is used in the ILFD and the ILFM. When the switch control is at V_{dd}, the resistor bias is at ground and vice-versa. Without this bias scheme, an off-switch might turn on if the output swing is high. This can happen when the output voltage is close to its trough. Parasitic switch capacitance would cause the switch source voltage to spike down, in effect producing a net positive V_{gs} and causing the switch to turn on for a fraction of the cycle. By forcing V_{dd} bias through a resistor, this undesired effect is avoided.

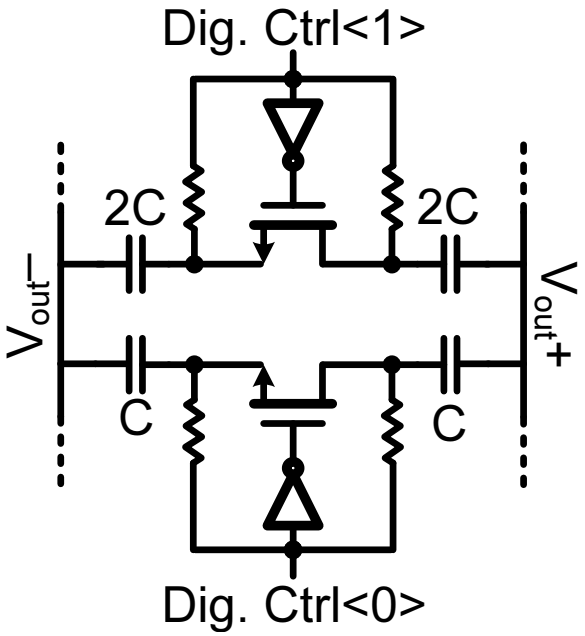

Figure 2.14: Two-bit capacitor bank details

2.3.3 Injection Locked Frequency Divider

As discussed in Section 2.2.3, an injection locked frequency divider is used in this work to generate a quadrature signal from the single phase reference. The design is based

on the work in [20]. This, in turn, is similar to the architecture proposed in [30] but with inter-oscillator injection added to form a quadrature oscillator as the core (the core quadrature oscillator is based on [31]). Unlike [20] and [30], however, injection is not performed at the tail current source as shown in Fig. 2.15. Since no buffer is used between the BPF and the ILFD, injection at the tail source presents a large load capacitance to the BPF increasing its power consumption considerably. To avoid this, direct injection is used as suggested in [32]. The injected signal is applied to an NMOS switch in parallel with the oscillator's LC tank. In this work, the input has a 50% duty cycle and hence the switch is on only once during a whole cycle of the injection signal. This, in effect, makes the output frequency half that of the input. The switch's input capacitance is roughly 25 times smaller than what would have been for the tail current transistor, simplifying the design of the preceding BPF. Two ILFDs are designed, a 6.66 GHz ILFD for the 20 GHz chain and a 7.33 GHz ILFD for the 22 GHz chain; each consumes 27 mA from a 1.2 V supply.

It is to be noted that the DC bias at the NMOS switch terminals in Fig. 2.15 is V_{dd}. Hence it is not possible to turn the switch on unless the bias point is adjusted, which necessitates the use of AC coupling. Towards this end, both the gate connection and the source and drain connections of the switch are AC coupled. This provides more flexibility in choosing the bias point. The bias details of the switch are shown in Fig. 2.16.

With the NMOS switch on, the quality factor of the tank is reduced. The time-averaged quality factor of the tank will thus depend on the switch on-resistance as well as the switch on time. The time-averaged quality factor, in turn, determines two important aspects of the ILFD: lock range and output amplitude. A wider lock range is desirable to suppress the ILFD's intrinsic phase noise and to cope with process variations. A higher output amplitude is also desirable to widen the lock range of the following stage,

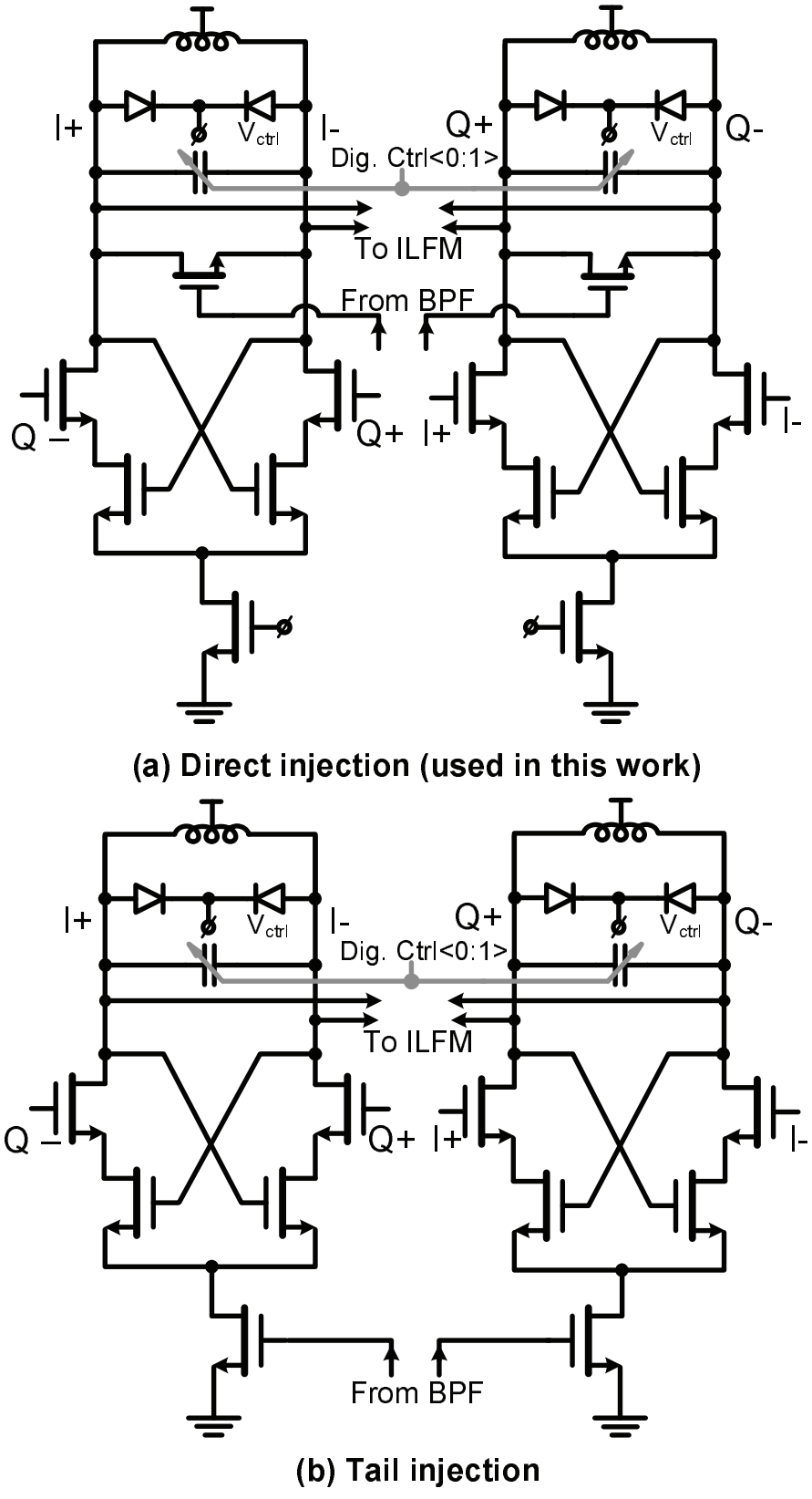

Figure 2.15: Injection Locked Frequency Divider (ILFD) - bias details omitted

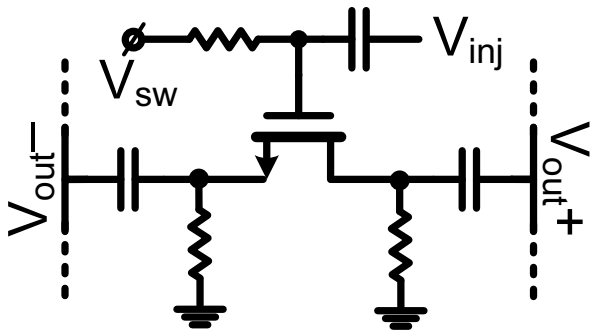

Figure 2.16: Injection switch bias details

the ILFM. There is a clear trade-off between the two requirements which is controlled by the switch's bias point. A higher bias point leads to a lower time-averaged quality factor and hence a wider lock range and a lower output amplitude and vice-versa. Fig. 2.17 shows the lock range and the output amplitude of the ILFD versus the switch bias point V_{sw}. A reasonable trade-off is achieved for $V_{sw} \approx 0.5$ V, resulting in a 190 MHz double-sided lock range and a 1.03 V output amplitude.

Monte-Carlo simulations are performed to determine the expected phase-error and amplitude mismatch in the ILFD's output. As shown in Fig. 2.18, the simulated 3σ phase error amounts to $\pm 1.27^{\circ}$ whereas the 3σ amplitude mismatch amounts to 0.12 dB.

2.3.4 Injection Locked Frequency Tripler

The injection locked frequency multiplier (ILFM), acting as a tripler, is shown in Fig. 2.19 [28]. At the core of the ILFM is a bottom-series-coupled quadrature VCO similar to [33]. The injection differential pair is biased in subthreshold, and is operated in class-B mode resulting in a strong third harmonic current component. As shown in Fig. 2.20, the third harmonic of the injection current has its peak below the threshold voltage V_{th}. An added advantage of subthreshold operation is the reduced power consumption in the injection pair. Two ILFMs are designed, with 20 GHz and 22 GHz

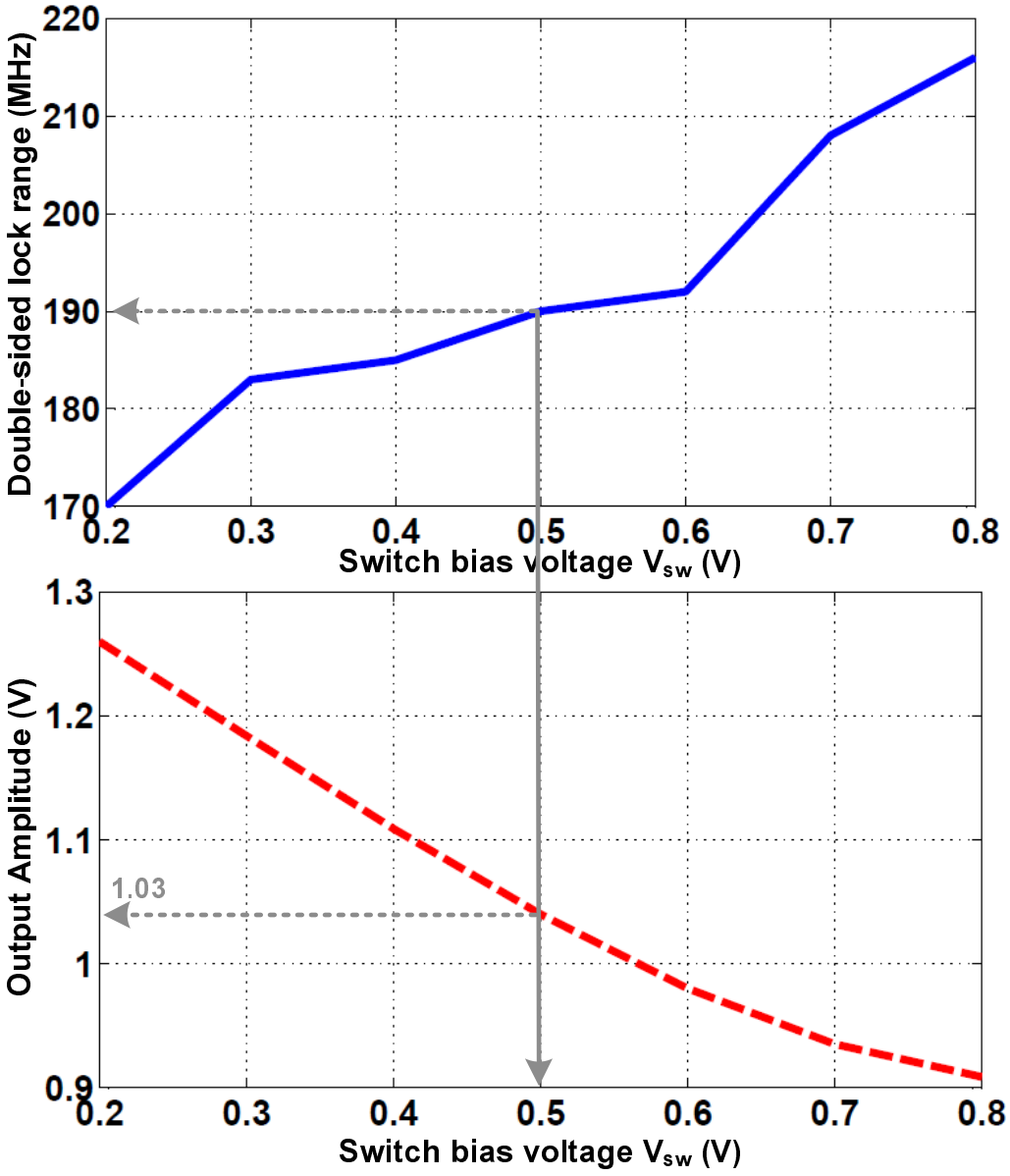

Figure 2.17: ILFD's lock range and output amplitude versus switch bias

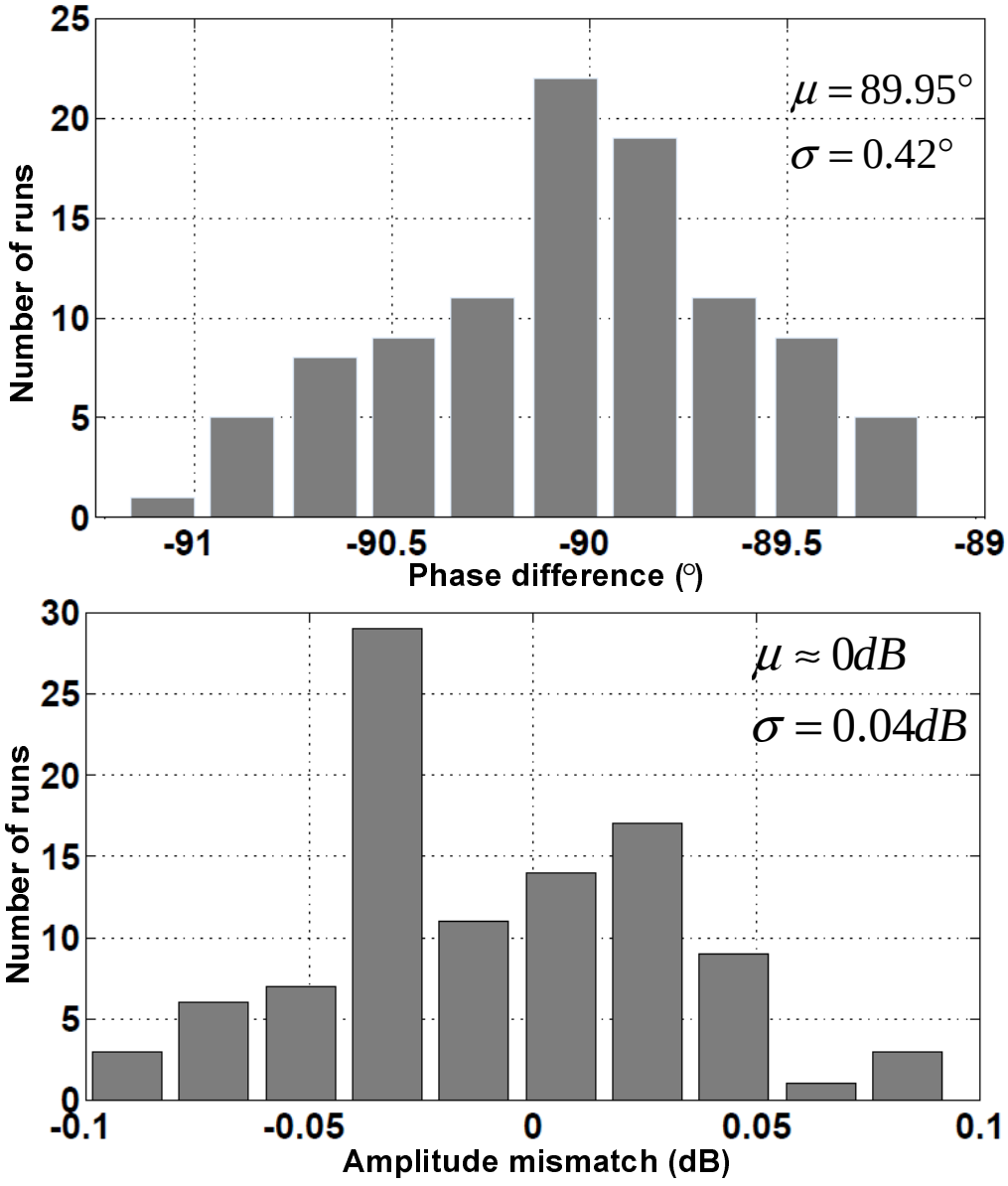

Figure 2.18: ILFD phase and amplitude mismatch - Monte Carlo simulations

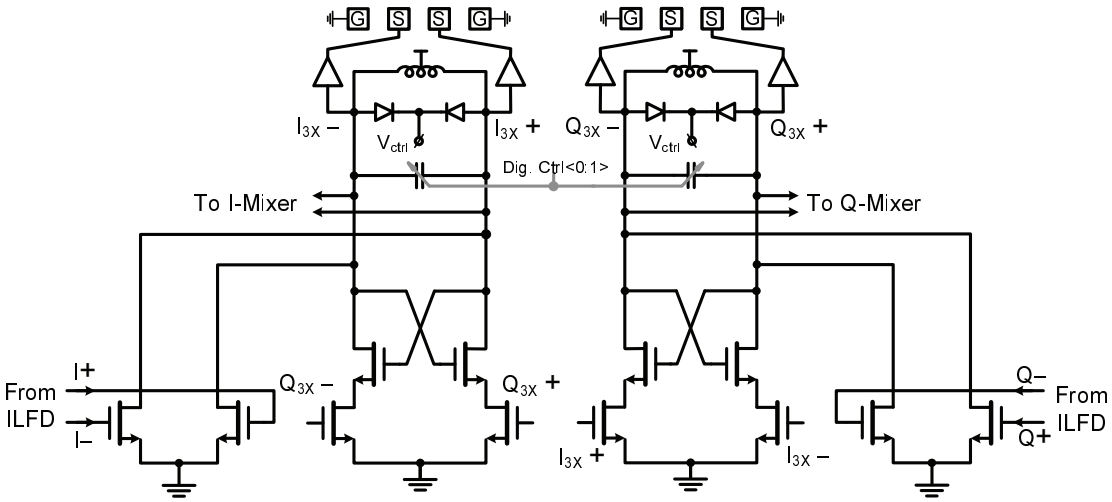

Figure 2.19: Injection Locked Frequency Multiplier (ILFM) - bias details omitted

center frequencies. Each consumes 21 mA from a 1.2 V supply.

Monte Carlo simulations are performed to estimate the phase and amplitude mismatch of the ILFM. The results, shown in Fig. 2.21, represent *the intrinsic* phase and amplitude mismatches of the ILFM. The intrinsic 3σ phase error amounts to $\pm 2.28^{\circ}$ whereas the 3σ amplitude mismatch amounts to 0.18dB.

Since the final LO amplitude is large enough for full mixer switching, amplitude mismatch at the LO output is irrelevant. Phase mismatch, however, is crucial. The total phase mismatch at the LO output is affected by the intrinsic phase mismatch of the ILFM, as well as the phase mismatch of the ILFD (which drives the ILFM). For a given fixed phase error of the ILFD $\Delta\phi_{in}$ and a fixed phase error of the ILFM $\Delta\phi_{int}$, a pessimistic estimate of the output LO phase error would be:

$$\Delta\phi_{LO} = \Delta\phi_{int} + 3 \times \Delta\phi_{in} \tag{2.2}$$

Hence, the standard deviation of the phase error at the output will be the r.m.s sum of the standard deviations of the two terms in Eqn.(2.2):

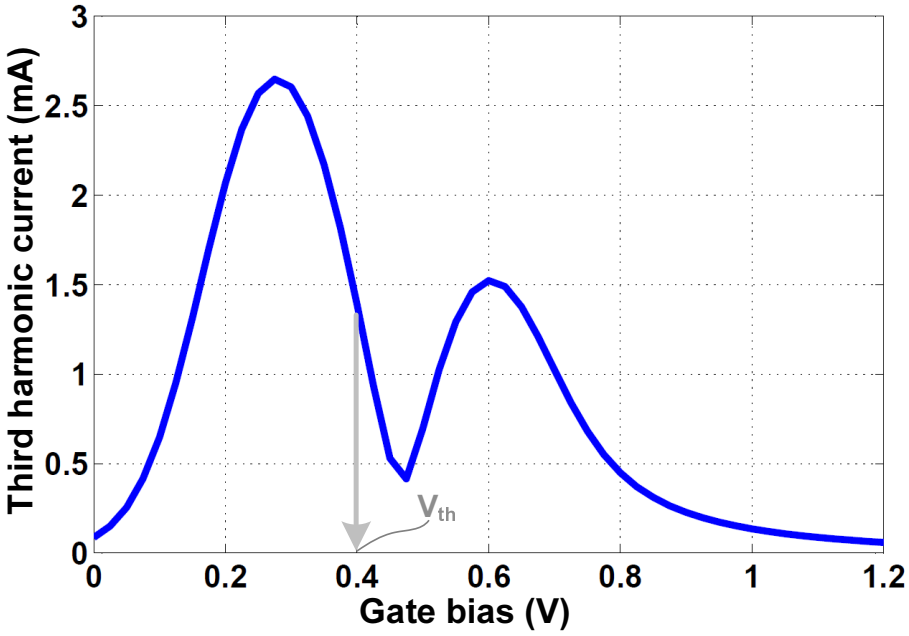

Figure 2.20: SpectreRF® simulation of the third harmonic current in injection pair

$$\sigma_{LO} = \sqrt{\sigma_{int}^2 + (3 \times \sigma_{in})^2} \tag{2.3}$$

Accordingly, the estimated 3σ phase error at the output of the LO is $\pm 4.4°$. This is a pessimistic estimate that represents an upper bound on the output phase error.

2.3.5 Chip Floorplan

The chip floorplanning is an integral part of the design process that is critical for successful operation. The floorplan of the chip in this work is presented in Fig. 2.22. The input reference clock signal is terminated on-chip via a 50Ω resistor for matching. The clock is buffered and then two separate paths are routed to the pulse-slimmer of each chain. Since the reference clock has a relatively low frequency, it is easier to route it for a longer distance. Another set of inverter buffers is also introduced along each path for

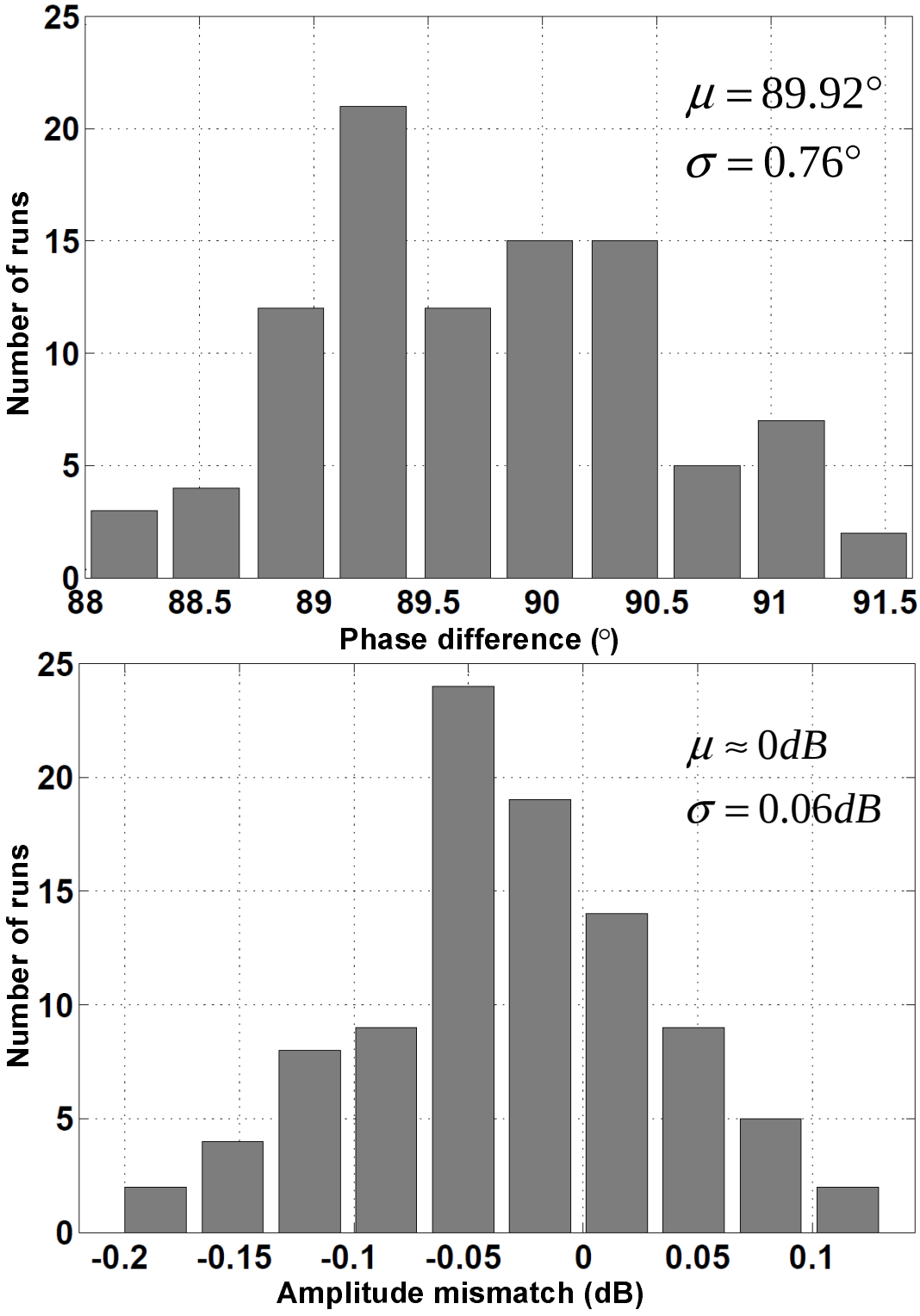

Figure 2.21: ILFM phase and amplitude mismatch - Monte Carlo simulations

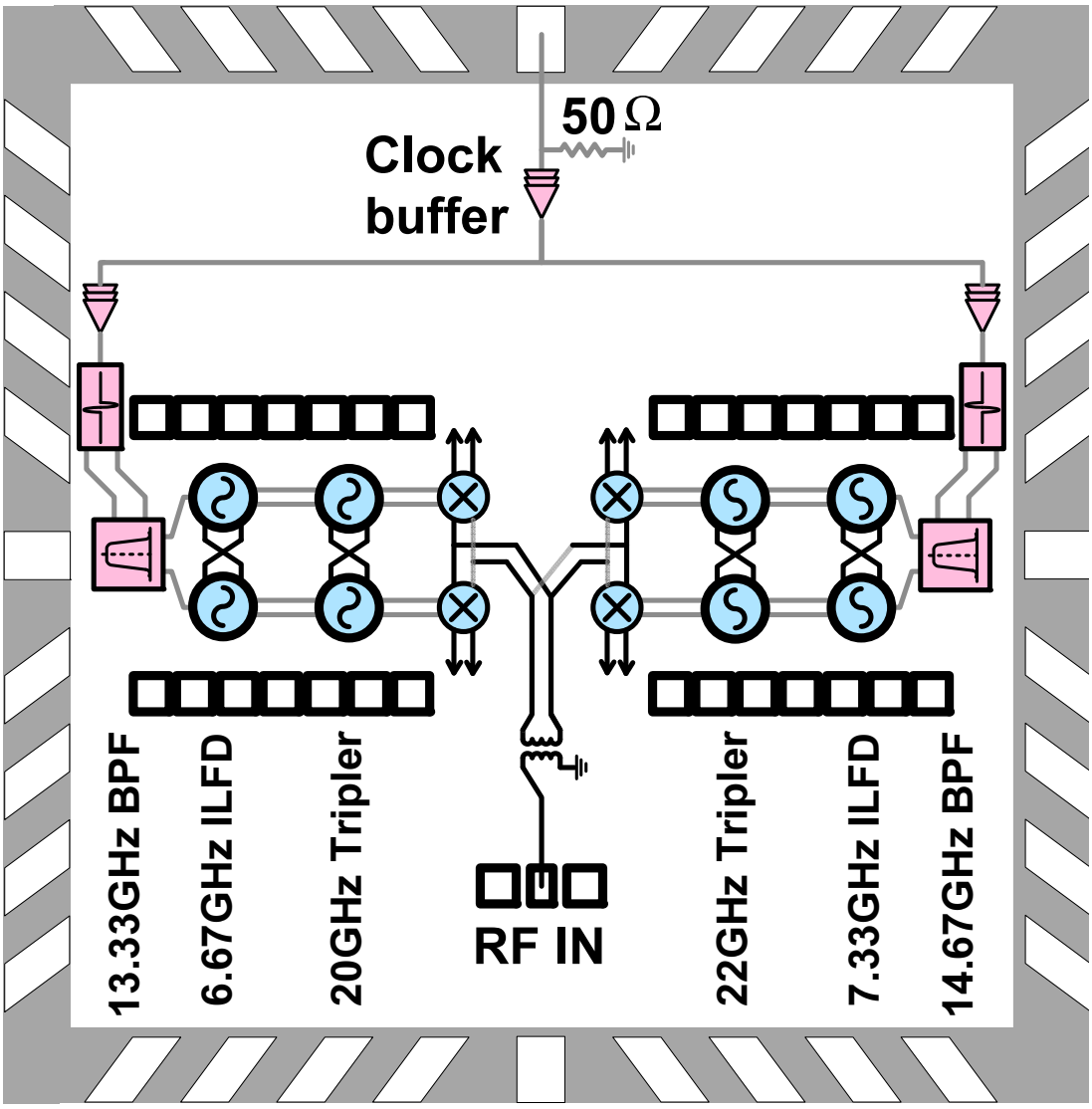

Figure 2.22: Chip floorplan

further signal enhancement. As noted in Section 2.2.1, a single pulse-slimmer could be used. However, this would require the output of the slimmer to be routed for a very long distance. This would, in turn, impose two problems: attenuation of the desired high frequency harmonic content of the output and undesired parasitic coupling to different points in the chain. Hence, two pulse-slimmers are used; one for each chain. The slimmer is placed as close as possible to the bandpass filter to minimize the routing distance and hence minimize signal loss and parasitic couplings. The associated area and power overhead are negligible. The output of the slimmer is not available for measurement and neither is the output of the bandpass filter. The injection locked divider and the injection locked multiplier follow in cascade. Care is taken to achieve maximum layout symmetry. The outputs of both the divider and the multiplier are buffered and fed to on-chip GSSG pads for probing. The final LO outputs are fed to active Gilbert-cell based double-balanced quadrature mixers for measurement purposes. The other input of the mixer is provided externally through probing via an on-chip GSG pad followed by an on-chip balun.

2.4 EM design methodology

In high frequency oscillators, interconnects play a critical role in the performance. Interconnects can no longer be treated as wires with a constant resistance (i.e. against frequency). Higher order effects kick-in, considerably altering the performance. The three major effects are: skin effect, substrate loss and current-crowding (or proximity effect) [34,35]. If not accounted for, the extra AC resistance added by these effects can cause a significant degradation in the oscillation amplitude or, in the extreme case, a total startup failure. Moreover, with low tank inductances (150 pH $\sim$ 750 pH) the interconnect inductance cannot be neglected and can cause considerable frequency shifts. Due to the complex nature of these effects, as well as the complex interconnect pattern

typical of integrated circuits, EM simulations become crucial for successful design validation. EM simulation tools, however, are not suited for extraction of the transistor parasitics. Moreover, as the number of simulated metal layers increases simulation times increase significantly.

To both accommodate transistor parasitics and speed-up EM simulations, a divide-and-conquer approach is used for extraction. Each oscillator layout is dissected vertically into two sections: a lower section (i.e. closer to substrate) which includes the transistors and the interconnects on the lower five metals and an upper section (i.e. farther away from substrate) including the inductors, capacitors and upper three metal interconnects. This choice is made because the high-frequency signals are routed on the top three metal layers (which are the thickest) to reduce DC resistance. Moreover since the thickness of the top three metals is larger than the skin depth, their resistance varies significantly at high-frequencies, as opposed to the thin lower metals whose resistance is dominated by the DC value. Conventional circuit extraction tools (in our case Calibre PEX®) are used on the lower section resulting in an extracted schematic with lumped resistor and capacitor parasitics. For the upper section, EM simulations are used to capture parasitic AC resistances and parasitic inductances and capacitances. Due to the large interconnect structures typical of quadrature VCOs, a fast and efficient EM simulation tool was needed. Towards this end, Integrand's EMX® EM-simulation tool [36] was used. The tool outputs an S-parameter data file, which is then combined with the extracted schematic from the lower section to perform a simulation of the whole structure. The circuit is then modified, if needed, and another simulation iteration is performed until the desired performance (frequency/output amplitude) is obtained. Fig. 2.23 summarizes the design methodology.

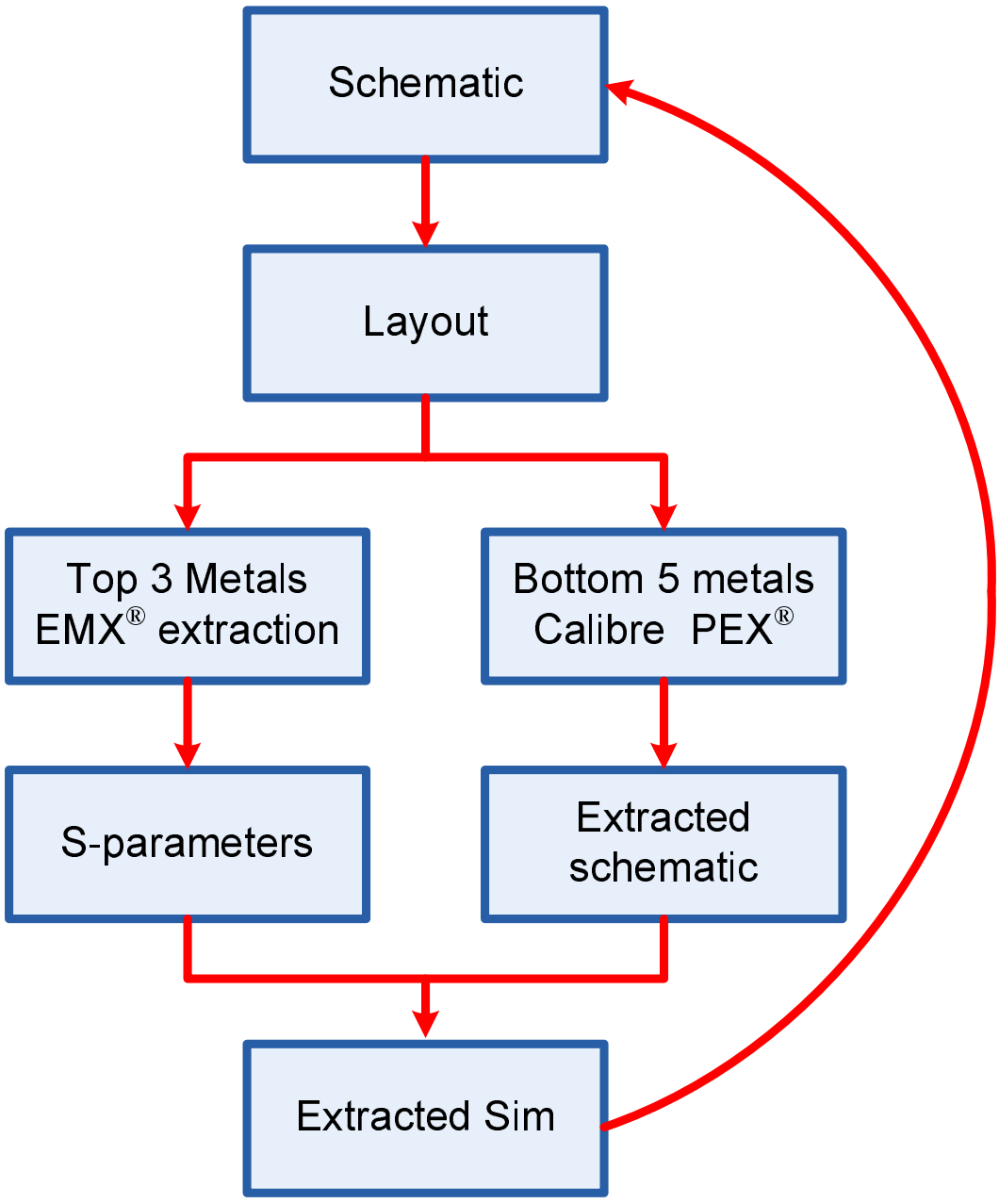

Figure 2.23: EM design methodology flow graph

2.5 PVT considerations

As discussed in Section 2.2.1, a duty cycle of $\frac{1}{8}$ to $\frac{1}{6}$ is required for maximum amplitude of the desired harmonics at the output of the pulse slimmer. To accomodate PVT variations, the gate voltage of the MOS resistor in the duty-cycle control section of Fig. 2.5 can be changed to control the variable delay, and change the duty-cycle accordingly. The variable delay is designed such that, at the worst PVT corner, the delay can be tuned to bring the duty cycle back to the acceptable range.

With three LC ILOs in each LO chain, it is instructive to investigate the effect of PVT variations. Typically LC oscillator frequency shifts due to PVT variations are in the order of $15\% - 20\%$. Hence, tuning for each ILO has to be designed to accomomdate the expected frequency shift.

Nevertheless, some amount of shift is usually allowed in the IF center frequency. This, in turn, translates to some amount of shift in the LO frequency. This can relax the tuning range requirements of the oscillators. For instance, let's assume that a 10% LO shift is acceptable. Hence, with a maximum PVT shift of 20%, the ILFM tuning range can be reduced to just 10%. A 10% shift in the ILFM frequency requires a similar 10% shift in the ILFD frequency. With a maximum PVT shift of 20%, the ILFD tuning range can be reduced to 10% as well. Similarly, the BPF tuning range can be reduced to 10%. In general, for an $x\%$ PVT shift and a $y\%$ acceptable LO shift the tuning range of each ILO can be reduced to $(x - y)\%$. The percentage tuning range is a design guideline; actual design has to ensure that in the worst PVT corner, tuning can bring back the oscillator to an acceptable frequency.

Automatic center-frequency tuning can be done by exploiting injection-locking. An ILO's amplitude is highest when the injected signal is close to the free-running frequency and decreases as the injected signal frequency deviates [37]. A possible procedure for automatic tuning based on this observation can be done as follows:

- With the ILFD and ILFM turned off, the pulse slimmer and the BPF are turned on. The delay setting in the pulse-slimmer is set to its nominal value. The BPF frequency control is swept and its output amplitude is monitored using a peak-detector. When the peak-detector's reading reaches its maximum value, the sweep is stopped and the BPF frequency setting is stored.

- With the ILFD and ILFM still off and the BPF frequency set to the value stored in the previous step, the delay control of the pulse slimmer is swept until the BPF output is maximized. The delay setting is stored.

- The ILFM is kept off, and the ILFD is turned on (together with the pulse slimmer and the BPF). The ILFD's frequency control is swept and its output is monitored using a peak-detector till the output hits a maximum. The ILFD's frequency setting is then stored.

- Finally, the whole LO chain is turned on and the ILFM frequency control is swept while its output is monitored using a peak detector. When the output is maximized, the sweep is stopped and the frequency setting is stored.

The stored values then represent the best frequency settings that ensure that each ILO is tuned as close as possible to its injection input.

2.6 Measurements and Discussion

The chip was fabricated in IBM's 130 nm CMOS technology. The chip micrograph is shown in Fig. 2.24. The active area is 1.8 mm^2. The test setup is shown in Fig. 2.25. A reference 1.33 GHz signal is supplied using an Agilent E8257D signal generator. An on-chip 50Ω resistor provides termination for the generator. The quadrature oscillator outputs are measured using GSSG probes and the output is displayed on an HP E4407B

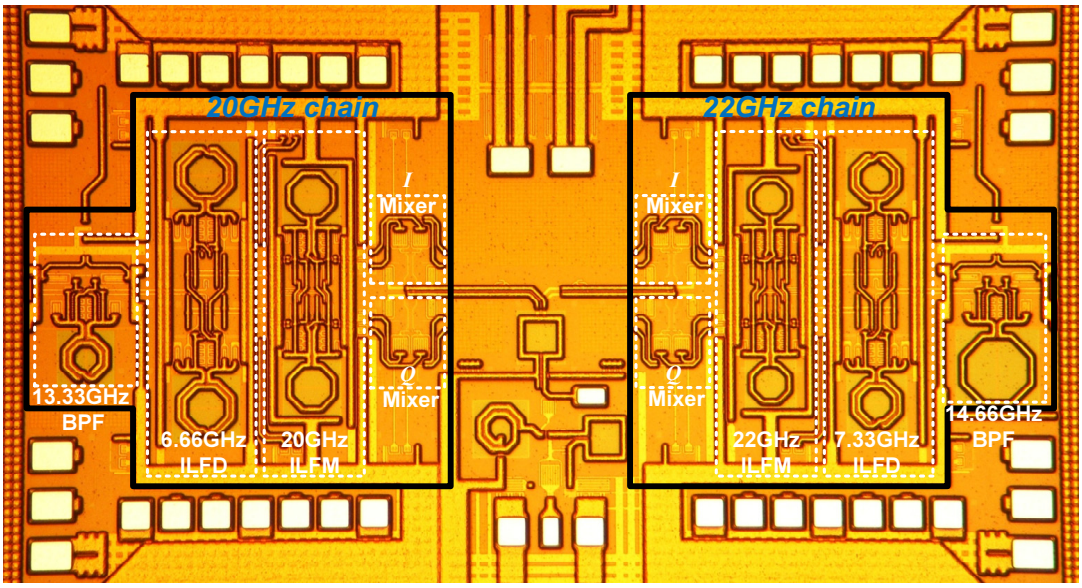

Figure 2.24: Chip Micrograph

Table 2.1: Current consumed per block

Block	Current (mA)
Digital (buffering + pulse slimmer)	3
Bandpass Filter (BPF)	4
Injection Locked Frequency Divider (ILFD)	27
Injection Locked Frequency Multiplier (ILFM)	21

spectrum analyzer where the spur levels are measured. A R&S FSP40 spectrum analyzer is used to measure the phase noise. The GSSG probes are driven by on-chip 50Ω buffers. The RF signal is supplied from an HP 8340A signal generator through GSG probes. The differential outputs of the quadrature downconversion mixers are connected to off-chip baluns. The single-ended outputs are then amplified and displayed on an Agilent DSO7104B oscilloscope.

Each chain consumes around 55 mA from a 1.2 V supply, for a total current consumption of 110 mA. The current consumed by each block is detailed in Table 2.1.

Fig. 2.26 shows the phase noise of the reference oscillator along with the phase noises of the 6.67 GHz ILFD and the corresponding 20 GHz ILFM, when the chain is locked

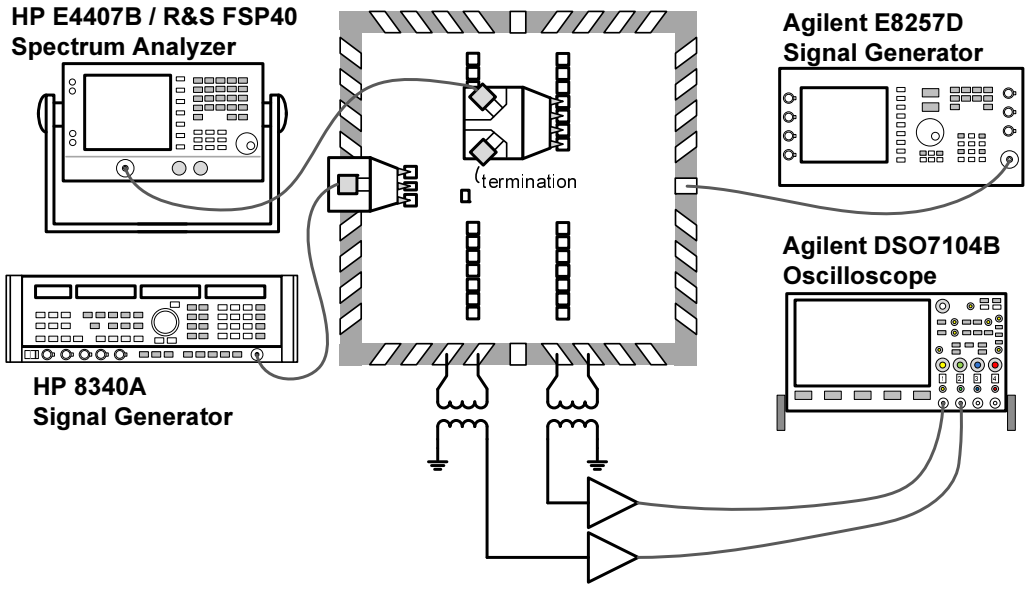

Figure 2.25: Test Setup

to the reference. The ILFD phase noise is measured at the output of the ILFD's 50Ω buffers using GSSG probes. Similarly, the ILFM phase noise is measured at the output of the ILFM's 50Ω buffers using GSSG probes as well. It is clear from Fig. 2.26 that the 20 GHz ILFM has negligible contribution to the output phase noise; the phase noise at the ILFM output is a faithful replica of the ILFD shifted by around +10dB (since the ILFM multiplies its input frequency by three, it adds $20log(3)\approx$9.5 dB to the input phase noise). This can be attributed to the relatively large lock range of the ILFM (single-sided lock range$>$ 350 MHz). In contrast, the loop bandwidth of a PLL is typically in the range of a few MHz leading to a large contribution from the PLL's VCO to the output phase noise. The 22 GHz chain performs in a similar manner to the 20 GHz chain as shown in Fig. 2.27. The spot phase noise values at 1-MHz and 10 MHz offsets along the two chains are summarized in Table 2.2.

It is instructive to find the contribution of the reference, BPF and ILFD to the output phase noise. Towards this end, the model in [24] is used. Each ILO acts as a first-order low-pass filter to its input phase noise, with the corner frequency determined

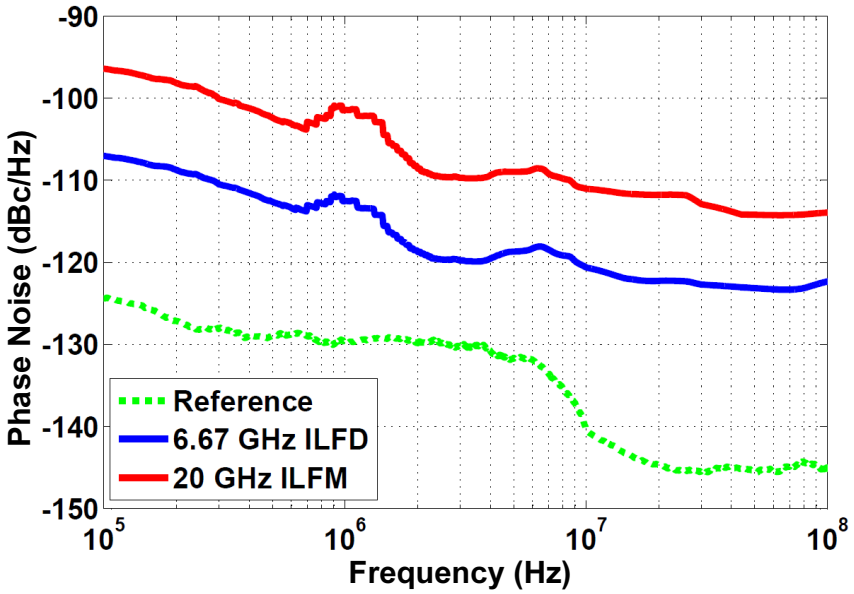

Figure 2.26: Measured phase noise along the 20 GHz chain

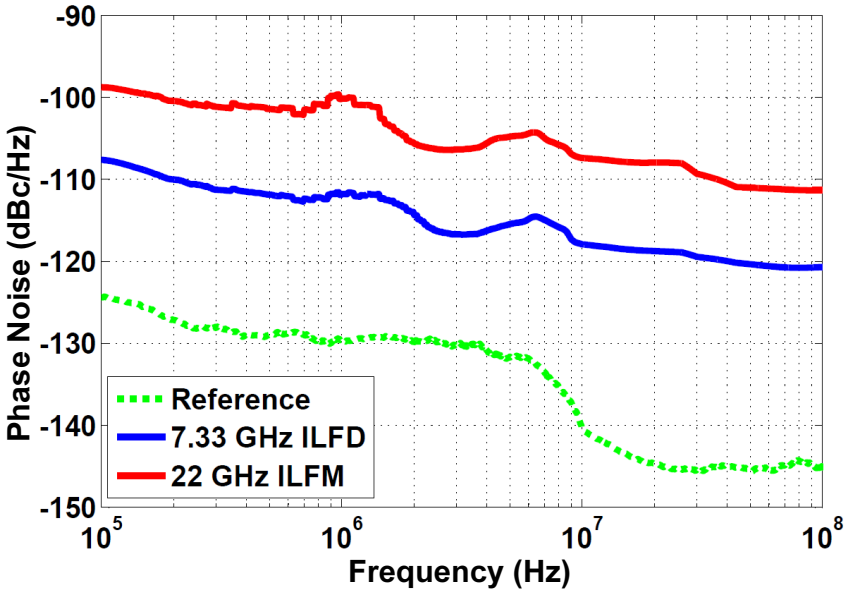

Figure 2.27: Measured phase noise along the 22 GHz chain

Table 2.2: Phase noise performance

Offset frequency (MHz)	1	10
Measured @6.67 GHz (dBc/Hz)	-112.5	-121
Measured @20 GHz (dBc/Hz)	-101.5	-111
Measured @7.33 GHz (dBc/Hz)	-112	-118
Measured @22 GHz (dBc/Hz)	-100	-107.5

by the single-sided lock range f_L. The intrinsic ILO phase noise is filtered by a first order high-pass filter of corner frequency f_L as well. Frequency division and multiplication scale the phase noise accordingly. The resultant model for the cascade of pulse-slimmer, BPF and ILFD is shown in Fig. 2.28.

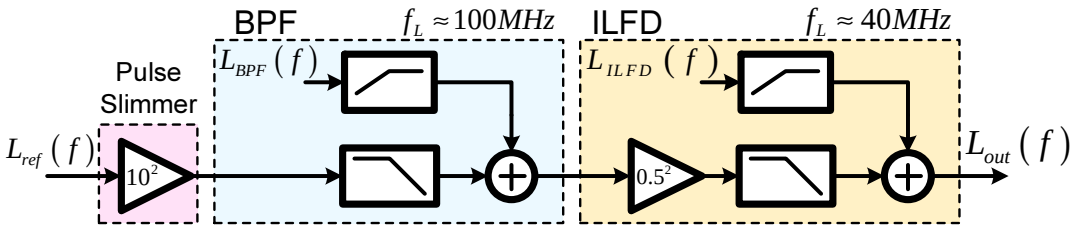

Figure 2.28: Phase noise model

Using this model, the output-referred phase noise contributions at the 6.67 GHz ILFD are plotted in Fig. 2.29 based on the simulated phase noise of the BPF and ILFD, and the measured reference phase noise. As evident from the figure, the BPF phase noise contribution is negligible. Even with the slight increase in actual BPF phase noise (due to modeling inaccuracies and supply-noise), BPF phase noise contribution remains negligible[1] . The simulated ILFD phase noise contribution is small but increases at larger offsets. The discrepancy between the simulated phase noise at the output of the ILFD (shown in Fig. 2.29) and the actual measured phase noise at the ILFD output (shown in Fig. 2.26) can be attributed to two reasons: 1) the actual ILFD phase noise is higher than simulated (again due to modeling inaccuracies and supply-noise) and

[1] The actual phase noise of BPF could not be measured because its output is not available for probing

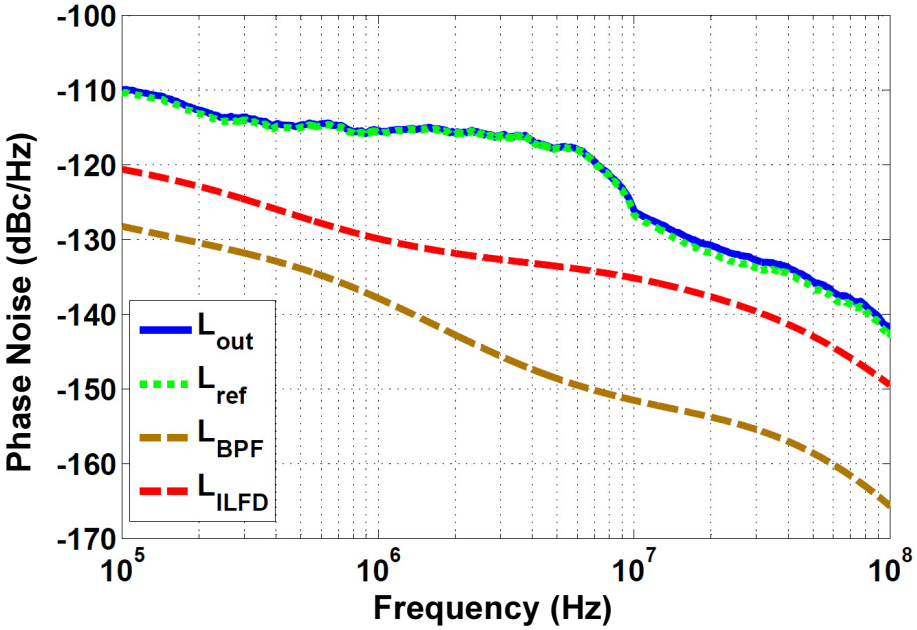

Figure 2.29: Simulated output-referred phase noise contributions at 6.67 GHz ILFD

2) the measurement instrument intrinsic phase noise is considerable compared to the up-converted reference phase noise [38]. This results in a final phase noise profile that is different from the simulated curve.

The spurious performance of the 20 GHz LO chain is shown Fig. 2.30. The spurs are at 1.33 GHz offset; the significant harmonics at the BPF's output are the 9^{th}, 10^{th} and 11^{th} harmonics. At the 6.67 GHz ILFD, the 10^{th} harmonic is divided down generating the 6.67 GHz signal. The 9^{th} and 11^{th} harmonics, on the other hand, mix with the 6.67 GHz LO generating spurs at $\pm$1.33 GHz offset. These spurs are suppressed by virtue of the ILFD's filtering effect (in a manner similar to the effect of the BPF). At the 20 GHz ILFM, the spur levels are further attenuated. The maximum spur at the output of the 20 GHz ILFM falls at -43 dBc as compared to -30 dBc at the output of the 6.67 GHz ILFD. While the BPF measurements are not available, the simulations shown in Fig. 2.4 suggest that the spurs at the BPF's output fall at around -17 dBc. Hence the

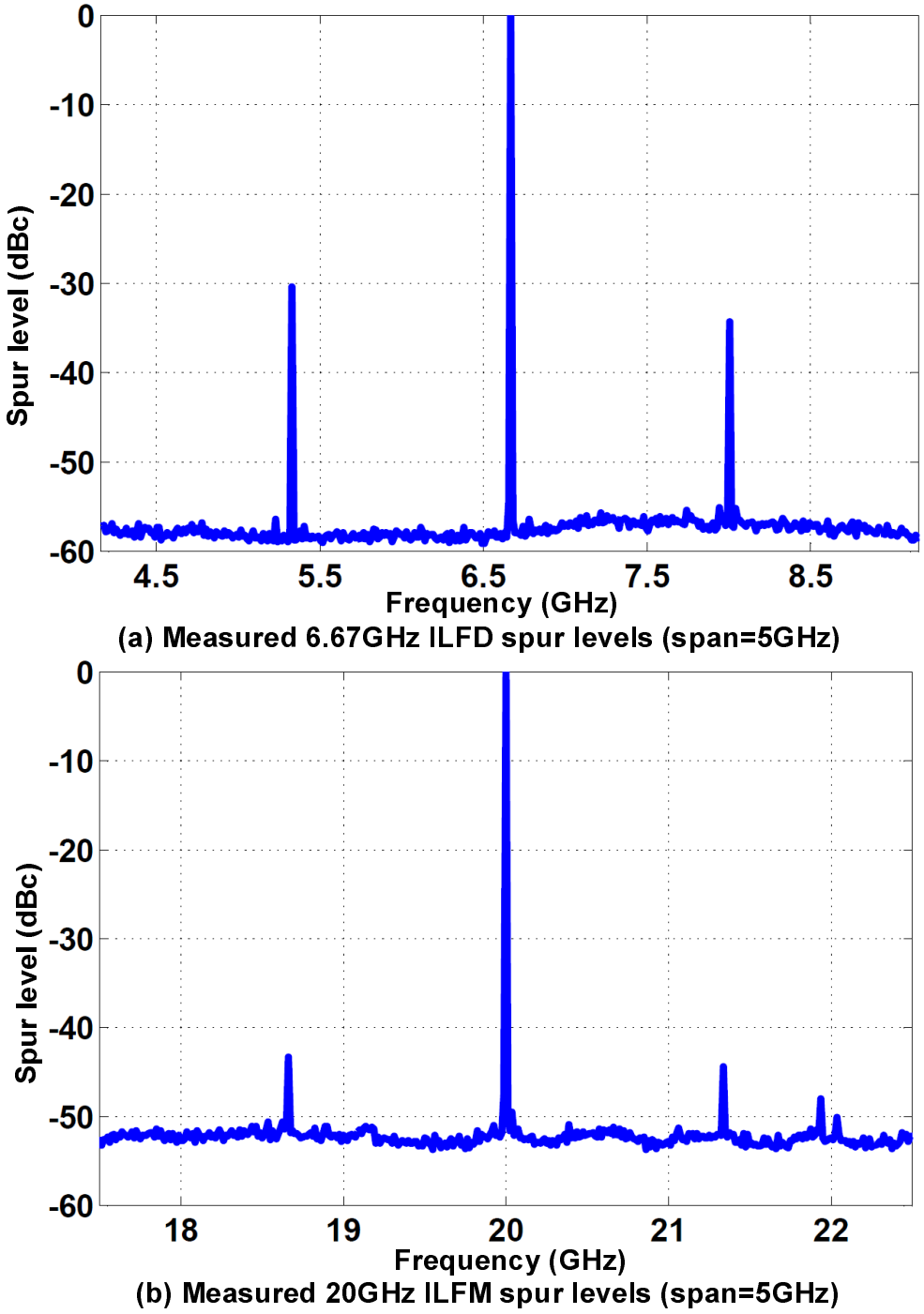

Figure 2.30: Spurious performance of the 20 GHz LO chain

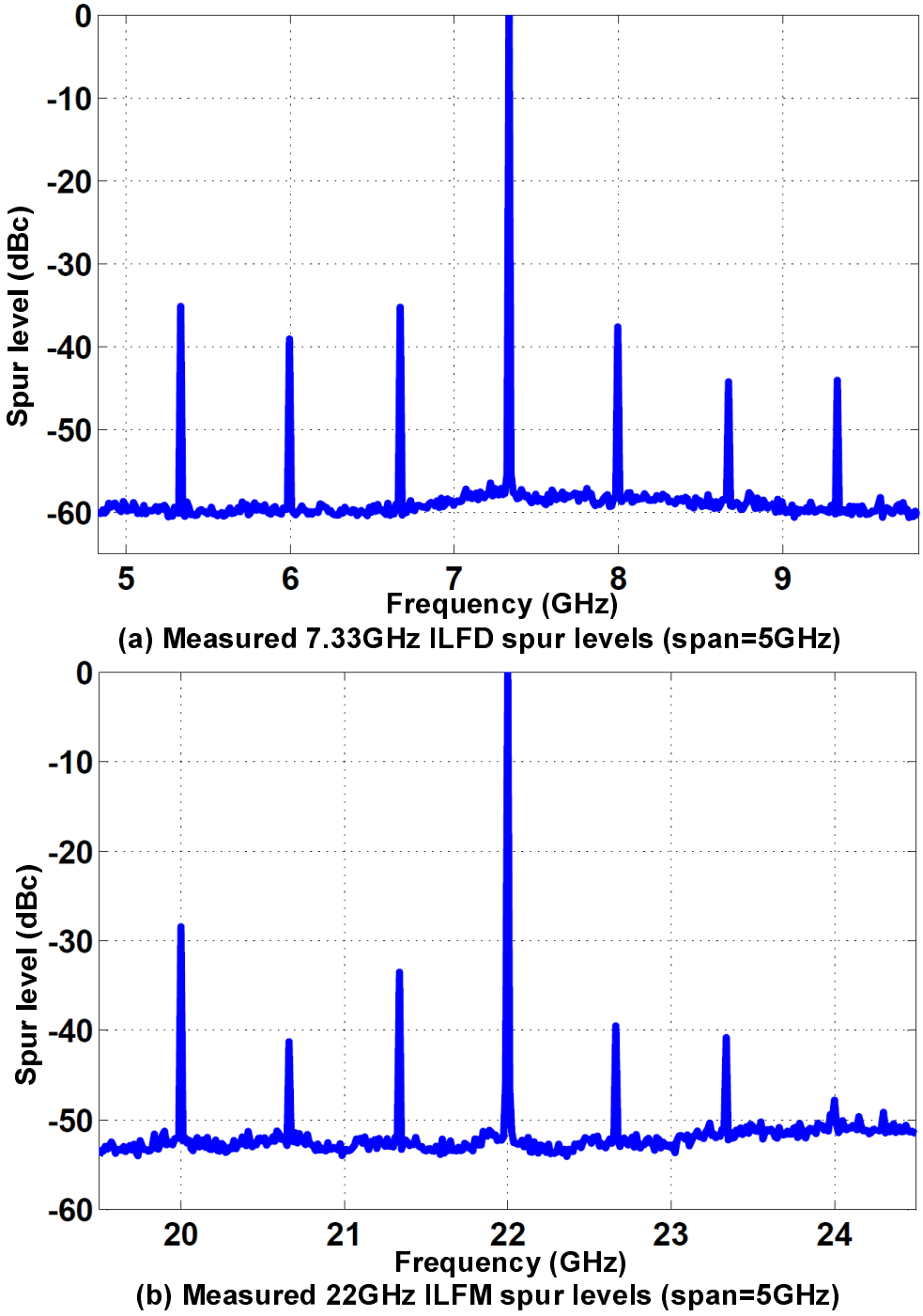

Figure 2.31: Spurious performance of the 22 GHz LO chain

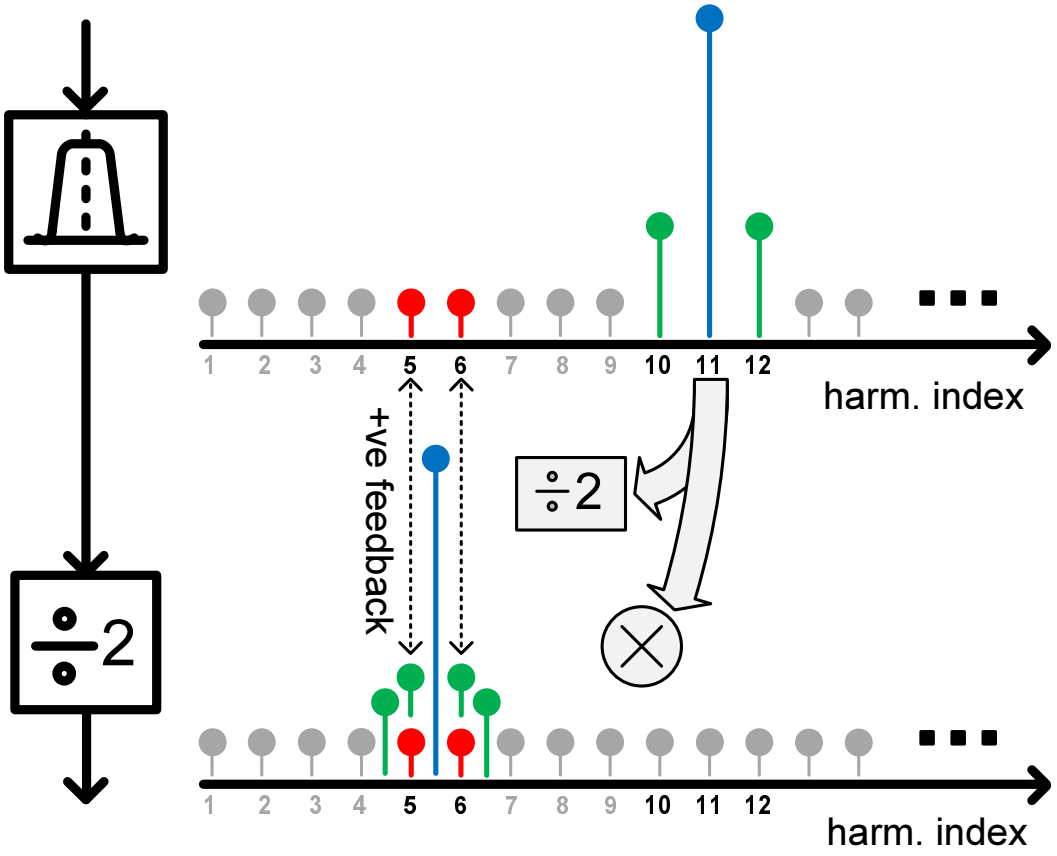

Figure 2.32: Generation of ±666 MHz spurs in 22 GHz LO chain

cascade of ILOs provide excellent spur suppression.

Fig. 2.31 shows the spurious performance of the 22 GHz LO chain. Similar trends can be observed for the ±1.33 GHz spurs which are generated in a manner similar to the spurs in the 20 GHz chain. However, additional spurs appear at ±666 MHz offset as well as at ±3×666 MHz offset. To explain the generation of the additional spurs, consider Fig. 2.32. The output of the BPF and ILFD is shown in terms of harmonics of the reference signal. When applied to the ILFD, the 11^{th} harmonic is divided by two, generating a frequency corresponding to the 5.5^{th} harmonic of the reference. The 10^{th} and 12^{th}

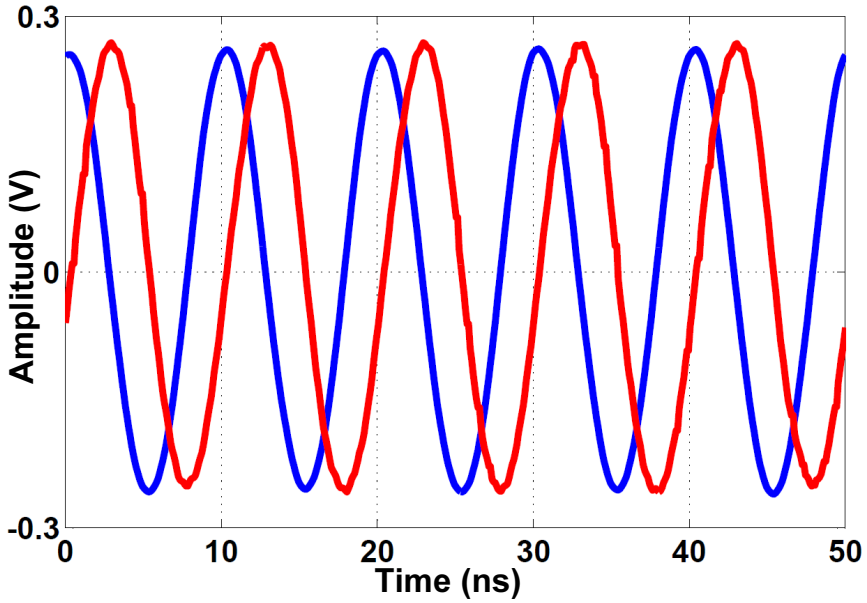

Figure 2.33: Measured downconverted quadrature outputs of the 20 GHz LO

harmonics are divided as well, generating very small components which fall onto the 5^{th} and 6^{th} harmonics of the reference. Due to the inevitable on-chip parasitic coupling (through electromagnetic radiation, substrate coupling, and capacitive coupling), the 5^{th} and 6^{th} harmonics at the output of the ILFD add to the similar components at the ILFD's input. A parasitic positive feedback loop is formed, enhancing these components which correspond to spurs at $\pm$666 MHz from the desired 5.5^{th} harmonic. The spurs at $\pm 3\times 666$ MHz are formed through third-order intermodulation of the $\pm$1.33 GHz spurs and the $\pm$666 MHz spurs. At the ILFM's output, the spur at $+3\times 666$ MHz is filtered out. The component at -3×666 MHz, however, remains and its amplitude increases due to parasitic reinforcement from the 20 GHz LO chain. One possible way to get rid of the $\pm$666 MHz spur and the subsequent $\pm 3\times 666$ MHz spurs is to use a pulse slimmer that only generates odd harmonics in the 22 GHz LO chain. This further justifies the use of a separate pulse-slimmer for each chain as suggested in Section 2.3.5.

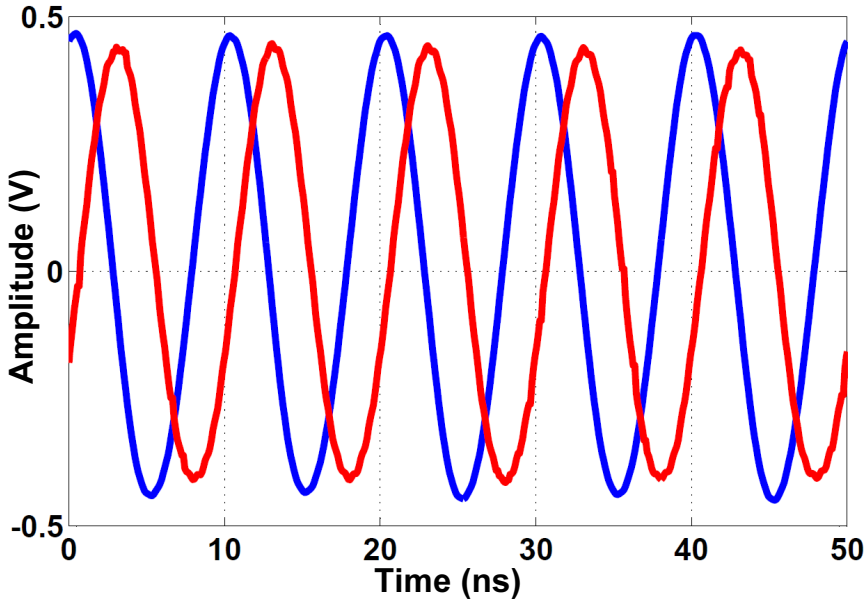

Figure 2.34: Measured downconverted quadrature outputs of the 22 GHz LO

The downconverted time domain I and Q outputs of the 20 GHz and 22 GHz LOs are shown in Fig. 2.33 and Fig. 2.34 respectively. Due to a limitation of the off-chip balun, the output frequency cannot be below 100 MHz. This, in turn, means that the mismatches between I and Q paths on board are not negligible and add considerably to the measured phase difference. Nevertheless, the measured average phase error under these conditions is 10° and 2° for the 20 GHz and the 22 GHz LOs respectively.

2.7 Conclusions

In this work an LO scheme for generating simultaneous phase synchronous quadrature LOs was presented for a $19 - 23$ GHz channelized receiver. The architecture developed here can easily be extended to more than two channels, and can be implemented at different frequencies. This provides a viable mechanism to realize mm-wave channelized

receivers. A number of novel techniques are used in the design, including a differentiating pulse-slimmer that exploits even and odd harmonics, an injection-locking based bandpass filter and an injection-locked quadrature frequency divider with direct injection. Building upon [19], more thorough discussion of the system-level and circuit-level design issues is presented. Additional measurements are presented, allowing the assessment of the contribution of each of the building blocks to the output phase noise. Moreover, an anomaly in the spurious response of the 22 GHz channel is explained and a less spurious alternative is suggested.

Chapter 3

Wideband QVCO

3.1 Introduction

With the advent of CMOS technology, direct downconversion receivers are becoming more popular due to low cost and simplicity. Quadrature LO generation is crucial to the operation of downconversion receivers [5]. Two common techniques for quadrature generation are using divide-by-two frequency dividers, and using polyphase filters [31]. Divide-by-two dividers require the system's oscillator to work at double the desired frequency, resulting in an overall increase in power consumption. Polyphase filters allow quadrature generation without the need for doubling the frequency. The lossy nature of polyphase filters, however, results in increased power consumption (for buffering and amplifying signals). Moreover, polyphase quadrature accuracy is sensitive to absolute component values. Hence, multistage polyphase filters are often employed to combat process variations, resulting in increased losses [27]. Quadrature accuracy is also reduced if the polyphase filter input is not a pure sinusoid. Generating a pure sinusoid can be elusive in today's submicron technologies, resulting in yet another source of quadrature error.

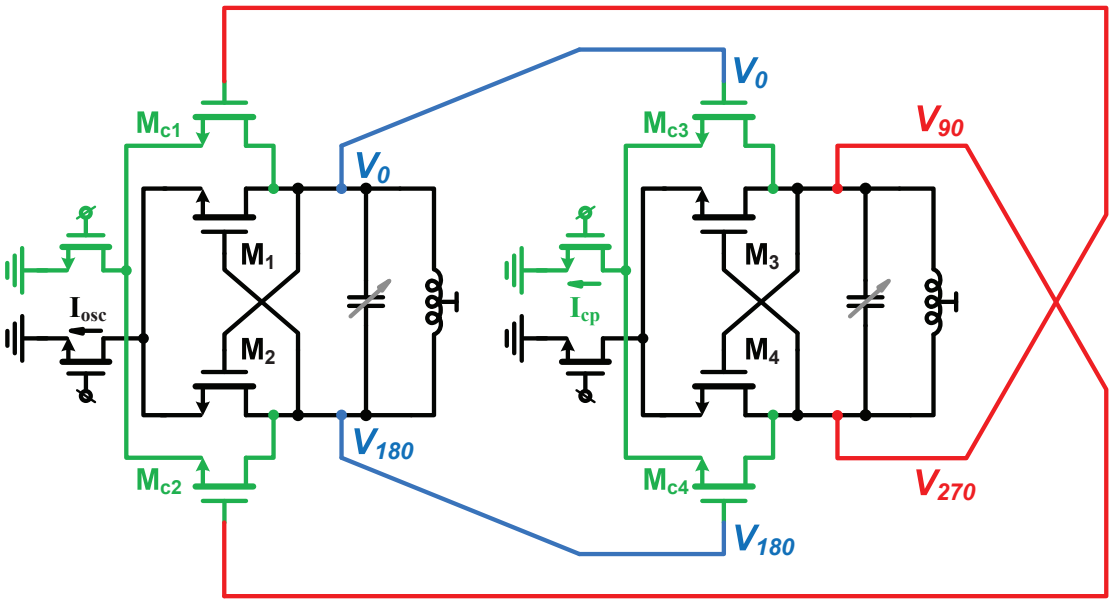

Figure 3.1: Basic LC QVCO

LC-based Quadrature Voltage Controlled Oscillators (QVCOs) allow the generation of quadrature LO signals without the need for doubling the frequency, and without the need for polyphase filtering. The basic structure of the LC-based QVCO is shown in Fig. 3.1 [39]. Two LC VCOs are coupled through both direct coupling (blue wires in Fig. 3.1), and cross coupling (red wires in Fig. 3.1). If both LC VCOs are matched, then owing to symmetry their differential outputs have to be in quadrature [40]. The QVCO can also be regarded as two inter-injection-locked VCOs [20].

The LC QVCO of Fig. 3.1 provides a simple and robust way for quadrature generation. However, it has an inherent trade-off between phase-noise and quadrature accuracy. If we denote the coupling strength as α, then it can be defined as:

$$\alpha = \frac{I_{cp}}{I_{osc}} \tag{3.1}$$

where I_{cp} is the tail current of the coupling transistor pairs (M_{c1}-M_{c2} and M_{c3}-M_{c4}), and I_{osc} is the tail current of the oscillator core transistor pairs (M_1-M_2 and M_3-M_4).

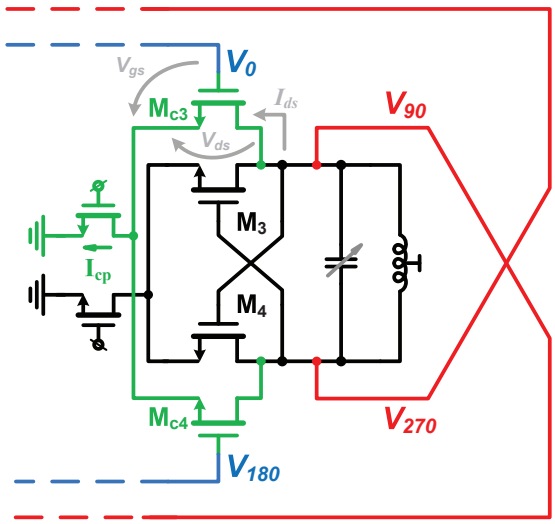

Figure 3.2: One LC VCO from the QVCO structure with voltages and currents of injection transistors highlighted

Increasing the coupling strength (α), improves the quadrature accuracy. It also leads to a degradation of phase noise, with increased phase noise contribution from the coupling transistors [31]. This trade-off between quadrature accuracy and phase-noise means that, for reasonable quadrature accuracy, the LC QVCO of Fig. 3.1 has relatively poor phase-noise performance. In fact, for a given power dissipation the phase noise of the basic LC QVCO is 3-5 dB worse than a stand-alone oscillator [41].

Fig. 3.2 shows one LC VCO from within the basic LC QVCO. The drain-source voltage (V_{ds}), gate-source voltage (V_{gs}) ,and drain current (I_{ds}) of the injection transistors are highlighted. The relatively poor phase-noise performance of the basic LC QVCO can be explained by referring to Fig. 3.3 which depicts the time-domain waveforms of V_{ds}, V_{gs} and I_{ds}.

Both V_{gs} and V_{ds} have a DC value of V_{dc}, which is lower than the supply voltage but considerably larger than the threshold voltage V_{th}. Both voltages swing with equal amplitudes around their DC value with a 90° phase shift in between them. The peak

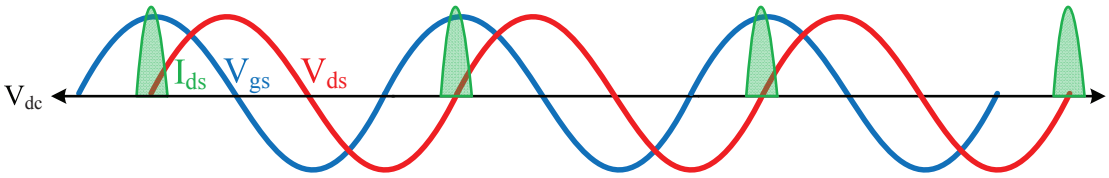

Figure 3.3: Gate voltage, drain voltage and drain current of transistors M_{c3} and M_{c4}

value of the I_{ds} current, thus, occurs when V_{gs} is at its peak. Note that at this instant, V_{ds} is at its DC value (V_{dc}) which is relatively large. Hence, *the injection current (I_{ds}) has its peak value when the oscillator's output voltage (V_{90}) is at its zero-crossing.* Since an oscillator is most vulnerable to phase-noise when its output is zero crossing [42], this leads to a large degradation in the phase-noise of the QVCO.

Regarding the LC VCO of Fig. 3.2 as an injection-locked oscillator (ILO), we note from Fig. 3.3 that the injection current in this ILO is 90° out of phase with the output voltage. From injection-locking theory [43], this implies that the ILO is operating at the edge of the lock range. Hence, the operating frequency of the QVCO does not coincide with the center frequency of the tank circuit [20]. Thus the effective tank Q at the QVCO's running frequency is lower than its peak value, leading to a further degradation of phase-noise performance. Moreover, by changing the tail-current of the injection-pair, the lock range of each ILO changes resulting in a change in the QVCO frequency. This "varactor-like" effect leads to flicker-noise upconversion, adding $\frac{1}{f^3}$ phase-noise [44].

Several techniques were presented in literature to overcome the shortcomings of the basic LC QVCO. Section 3.2 presents an overview, and categorization of these techniques. This is followed by section 3.3 in which a novel solution is proposed, which shares the simplicity and robustness of the basic LC QVCO [45]. Finally, measurement

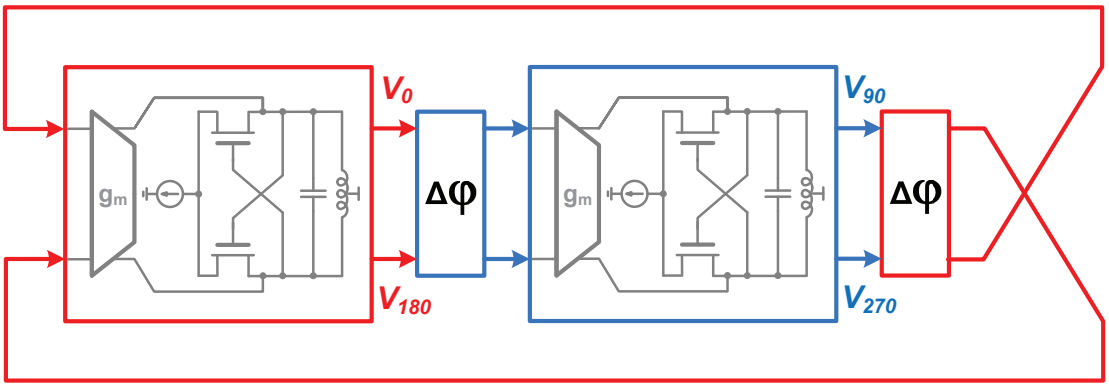

Figure 3.4: Block diagram of phase-shift based LC QVCO

results of a prototype design are presented in section 3.4.1 followed by conclusions in section 3.5.

3.2 Prior art

This section discusses the techniques used in literature to improve the performance of the basic LC QVCO [31, 44, 46–55]. These techniques can be classified into three broad categories: phase-shift based techniques, super-harmonic coupling based techniques, and alternative direct-coupling techniques. The following subsections give an overview of these techniques. Due to the large number of publications, the overview is not meant to be comprehensive.

3.2.1 Phase-shift based

The basic block diagram of this class of LC QVCOs is shown in Fig. 3.4. Similar to the basic LC QVCO, the phase-shift based LC QVCO consists of two injection-locked oscillators with both direct and cross-coupling. The difference, however, is that the output of each ILO is phase-shifted by $\Delta\varphi$ before injecting it into the next ILO. This, in turn, means that the injection current in each tank *(is not)* in quadrature with

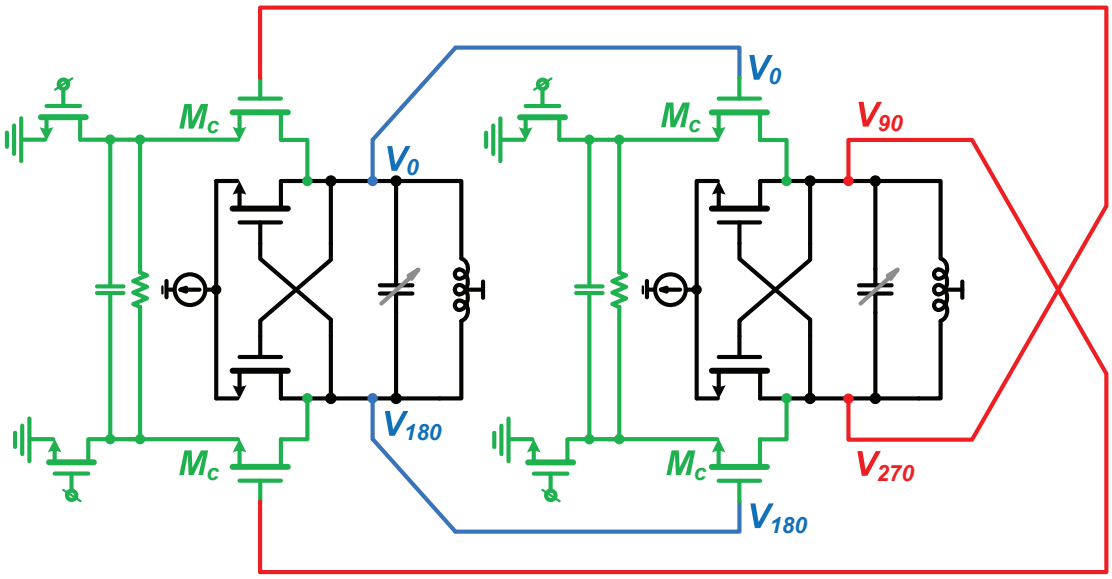

Figure 3.5: Phase-shift based QVCO using R-C degeneration

the tank's output voltage. Rather, injection current is shifted from quadrature by an additional angle equal to the phase shift ($\Delta\varphi$)(this is synonymous to shifting I_{ds} in Fig. 3.3 by an additional $\Delta\varphi$). Ideally, a phase shift of 90° would make the injection current coincide with the peak of the output voltage, resulting in minimal phase-noise penalty [42]. Moreover, the 90° phase shift would cause the QVCO frequency to coincide with the tank frequency, thus maximizing the Q-factor and eliminating the "varactor-like" effect and its consequent $1/f^3$ phase-noise. In practice, however, a 90° is hard to achieve. Nevertheless, a reasonable phase shift (in the order of 40°–50°) will help decrease the phase noise injected from one oscillator into the other [44].

One possible way to implement the phase-shift is through the use of R–C degeneration in the coupling transistors as shown in Fig. 3.5 [44]. The injection tail-current source is split in two to allow the use of R–C degeneration without hurting the headroom. Assuming the values of the resistor and the capacitor in Fig. 3.5 are $2R_s$ and $C_s/2$ respectively, then the resultant transconductance can be given by [44]:

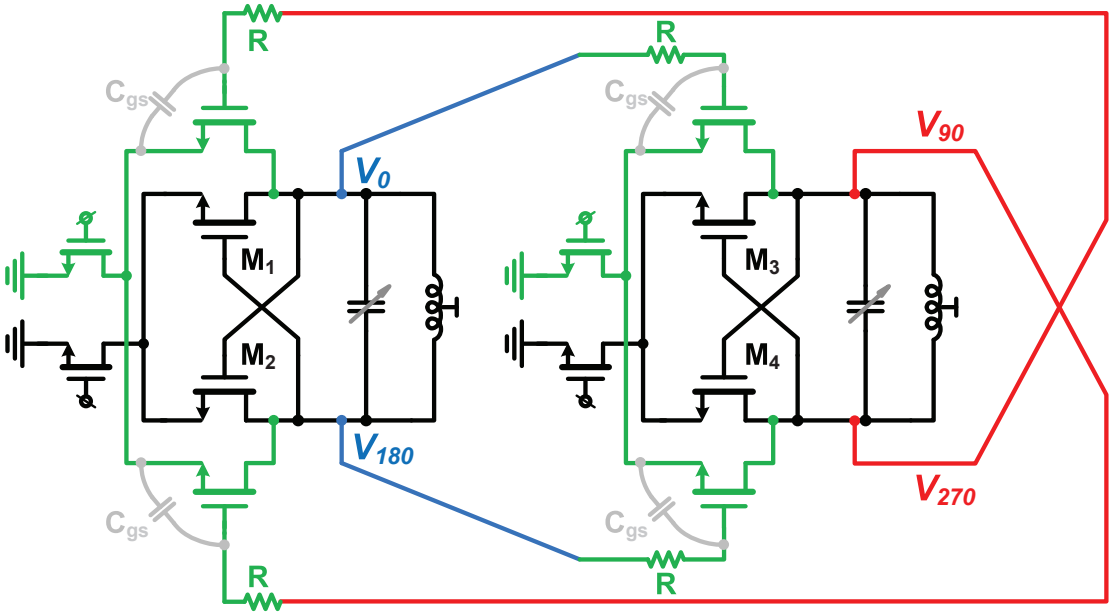

Figure 3.6: Phase-shift based QVCO using resistors in coupling path

$$G_m = \frac{g_m}{1 + g_m R_s} . \frac{1 + sR_sC_s}{1 + \left(\frac{sR_sC_s}{1+g_mR_s}\right)} \tag{3.2}$$

where G_m is the equivalent small-signal transconductance of the coupling structure, and g_m is the small-signal transconductance of the coupling transistors. It is clear from equation 3.2 that G_m has a zero and a pole, making a 90° phase-shift impossible. Nevertheless, with proper choice of R_s and C_s a phase shift of 40°–50° is achievable [44]. A clear disadvantage of this architecture is evident from equation 3.2; the achieved phase-shift is frequency dependent, requiring careful design of the phase-shift network.

Another implementation of a phase-shift based LC QVCO is shown in Fig. 3.6 [46]. Resistors are added in series with the gates of the coupling transistors, forming an R–C network with the parasitic C_{gs}. By adjusting the resistance value, the desired phase-shift can be achieved. The drawback, however, is that the parasitic C_{gs} capacitor is de-Q'ed by the value of the resistance. Since this parasitic capacitor is part of the tank,

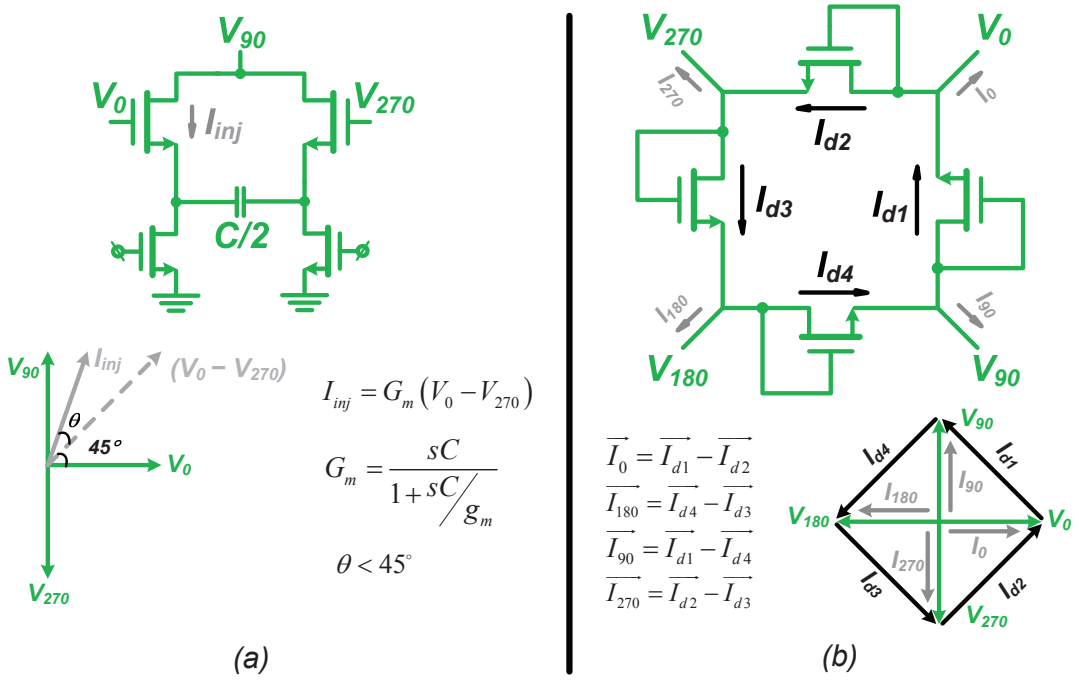

Figure 3.7: Phase-shift QVCO techniques using (a) current addition and capacitive degeneration and (b) frequency-independent injection

this means that the whole tank Q is reduced. Hence, to minimize the de-Q'ing effect, the C_{gs} capacitance has to be much smaller than the tank capacitance [46]. As in [44], the phase-shift is frequency dependent as well.

Several other phase-shift implementations are worth mentioning. In [47], phase-shift is implemented in two-steps. First, two quadrature currents are added generating a 45° phase-shift. Capacitive degeneration then *"ideally"* adds another 45° to get a total of 90° shift as shown in Fig. 3.7(a). Note that the phase-shift in this architecture is still frequency dependent (g_m/C is designed to be equal to the QVCO center frequency). Another drawback of this architecture is that eight transistors are used for coupling (instead of four), thus adding more noise.

A frequency-independent phase-shifting architecture is presented in [48]. A symmetric coupling network is formed using only transistors in class-C operation as shown

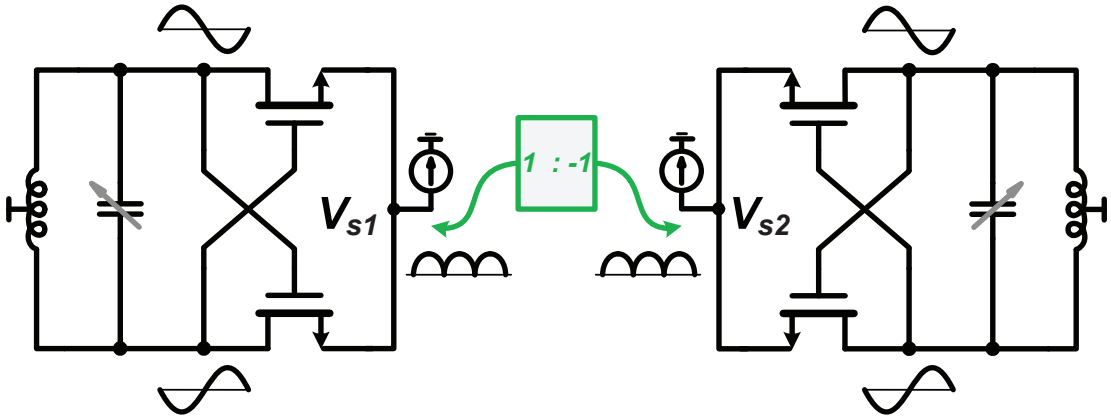

Figure 3.8: Generalized super-harmonic-coupling based LC QVCO

in Fig. 3.7(b). The network is formed such that the injection current at each node is the sum of two currents: one leading the node's voltage by 45°, and the other lagging the node's voltage by 45°. Consequently, the resultant injection current at each node is in phase with the node voltage [48], as evident from the phasor diagram in Fig. 3.7(b). Possible drawbacks are: the need of relatively large signal swing (to support class-C operation), as well tank de-Q'ing due to loading by diode-connected devices.

3.2.2 Super-harmonic-coupling based

A general representation of this class of LC QVCOs is shown in Fig. 3.8. Due to the hard-switching of the cross-coupled pair in the LC VCO, the common-source node is no longer a virtual ground (as in a small-signal differential pair). During each half-cycle, one of the cross-coupling transistors is on and the other is off. The on transistor, together with the tail current source, forms a source follower, replicating the input voltage to the common-source node. This happens twice during each switching cycle, leading to an effective doubling of frequency at the common-source node. The major premise of the super-harmonic coupling based LC QVCO is to couple the common-source nodes

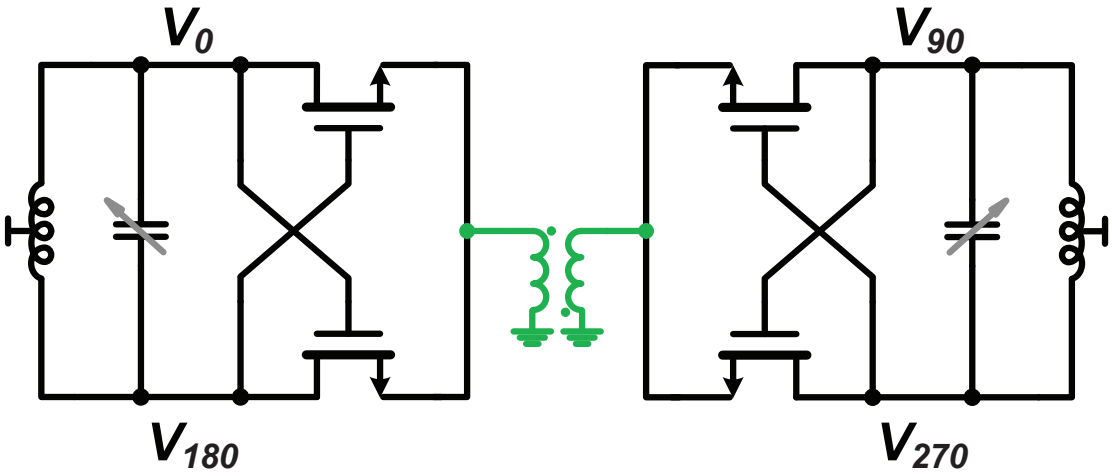

Figure 3.9: Transformer based super-harmonic coupled QVCO

of two LC VCOs in anti-phase. By forcing a 180° phase-shift between the common-source nodes (at double the output frequency), a 90° phase-shift is ensured between the outputs of the two LC VCOs.

One of the earliest implementations of the super-harmonic coupling concept is shown in Fig. 3.9 [49]. The tail current sources are removed and replaced by tail inductors. The tail inductors resonate with the parasitic capacitance at the common-source nodes, with a resonant frequency that is twice the QVCO's frequency. This forms a filter that improves the phase-noise of the oscillator. Moreover, removing the tail current source eliminates one of the largest sources of flicker noise, effectively reducing the $1/f^3$ phase-noise [56]. By coupling the two tail inductors in an inverting transformer structure, the required anti-phase coupling is achieved. A simple, and area-efficient way to implement the transformer is through the use of a single symmetric inductor [49]. Unlike the basic LC QVCO, this coupling method does not inherently shift the oscillation frequency away from the tank center frequency. Hence, the maximum tank Q is utilized, leading to a good phase-noise performance. The drawback, however, is that lower oscillation amplitudes can result in even-mode operation leading to in-phase operation (instead of

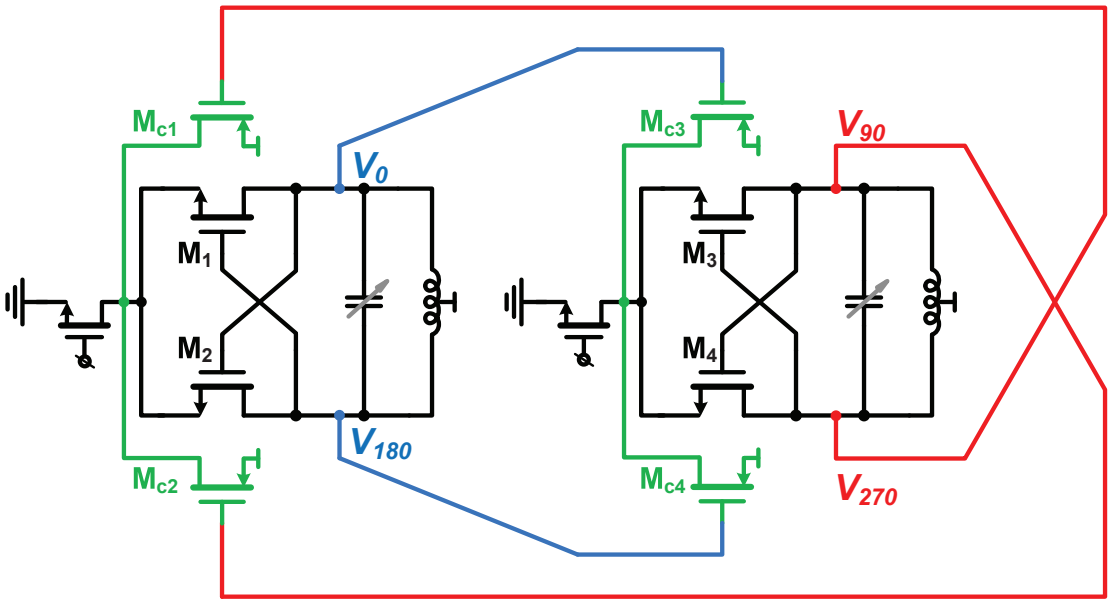

Figure 3.10: Simplified schematic of frequency doubler based super-harmonic QVCO

quadrature). While this can be mitigated by ensuring a large oscillation amplitude [49], it can put a limit on the minimum achievable frequency at constant power (amplitude decreases as frequency decreases for constant power in an LC VCO).

An alternative implementation of the super-harmonic coupling concept is shown in Fig. 3.10 [50]. At a first glance, it looks very similar to the basic LC QVCO of Fig. 3.1. A careful look, however, shows three distinctive differences: the coupling transistors are PMOS as opposed to NMOS, the drains of the coupling transistors are tied together to the common-source nodes of each of the two LC VCOs, and the sources of the coupling transistors are tied to the supply. In fact, each of the coupling transistor pairs (M_{c1}-M_{c2} and M_{c3}-M_{c4}) forms a frequency doubler. The outputs of each of the two LC VCOs are frequency-doubled, and the doubled output is fed to the common-sources of the two LC VCOs in anti-phase. This avoids the use of passive transformers, which saves area. Moreover, using PMOS transistors for coupling makes them nominally off (both gate and source are at supply voltage under no oscillation) leading to a class-C operation which

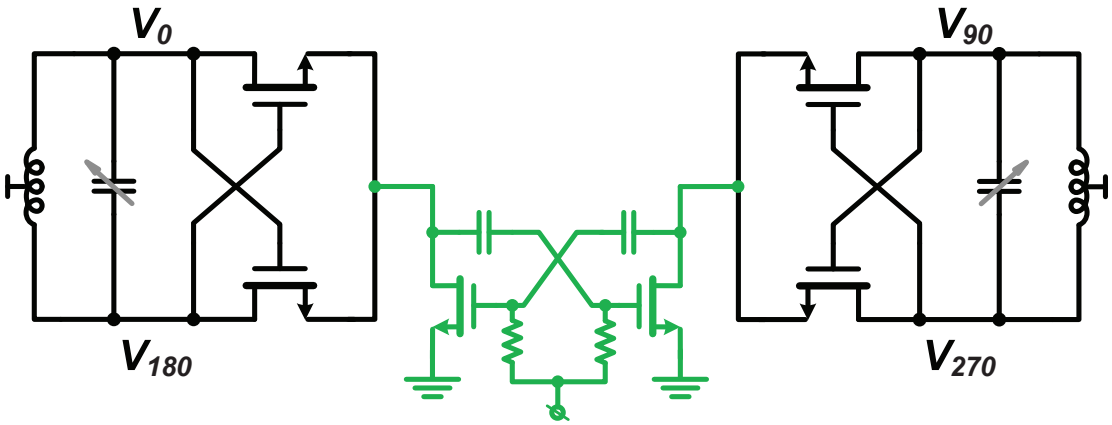

Figure 3.11: Simplified schematic of super-harmonic QVCO based on cross-coupled tail transistors

reduces the power overhead associated with the use of active components. In addition, the cycling switching of the transistors reduces their inherent $1/f$ noise content [50]. Again, the drawback is the need for high oscillation amplitude for strong coupling. Moreover, the use of active devices, while reducing area, adds more noise. Besides, active devices add extra loading which reduces the tuning range (tuning-range reduction will depend on the ratio of the active device capacitance to the total tank capacitance).

Fig. 3.11 shows another implementation of the super-harmonic coupling concept [51]. Here, the anti-phase coupling is ensured by cross-coupling of the tail current sources. This ensures that the drains of the tail current-sources (which are the common-source nodes of the VCOs) are out of phase. Again, the swing needs to be high to ensure proper quadrature coupling [51]. Another drawback is that the cross-coupling structure places a large capacitive load at the common-source node. While this is beneficial in reducing the phase-noise due to the tail current source, it can cause an effective de-Q'ing of the tank [56].

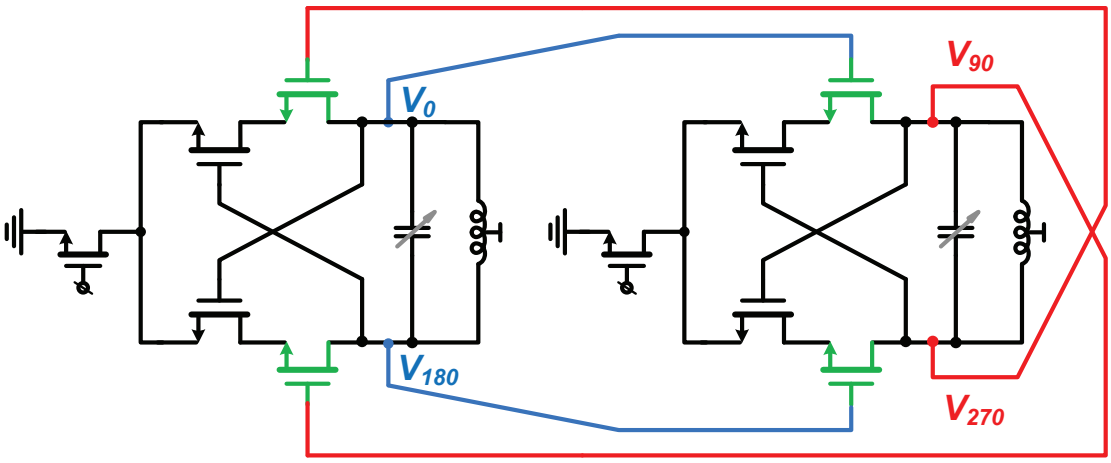

Figure 3.12: Top series-coupled LC QVCO

3.2.3 Alternative direct-coupling

In this category of QVCOs, direct coupling is performed using configurations different than that in Fig. 3.1. For instance [31] uses series transistors, instead of a parallel differential pair, to perform direct coupling. As shown in Fig. 3.12, the coupling transistors are placed in series with, and on top of, the negative-g_m cross-coupled transistors. This configuration breaks the trade-off between phase-noise and quadrature accuracy, allowing relatively constant phase accuracy regardless of the coupling transistor sizes [31]. Besides, the series placement means that the coupling transistors can reuse the current in the negative-g_m transistors, leading to power saving. Nevertheless, for optimum phase-noise performance, relatively large coupling transistor sizes are needed (in the order of five times the size of the g_m transistors in [31]). The relatively large sizing (needed for stacking as well as phase-noise performance) adds large loading to the QVCO, limiting the maximum achievable tuning-range. Moreover, transistor stacking limits the achievable amplitude and makes supply scaling difficult. Bottom series coupling (where coupling devices are placed below the negative-g_m devices) is also possible [52].

Another modified direct-coupling scheme is shown in Fig. 3.13 [53]. This scheme

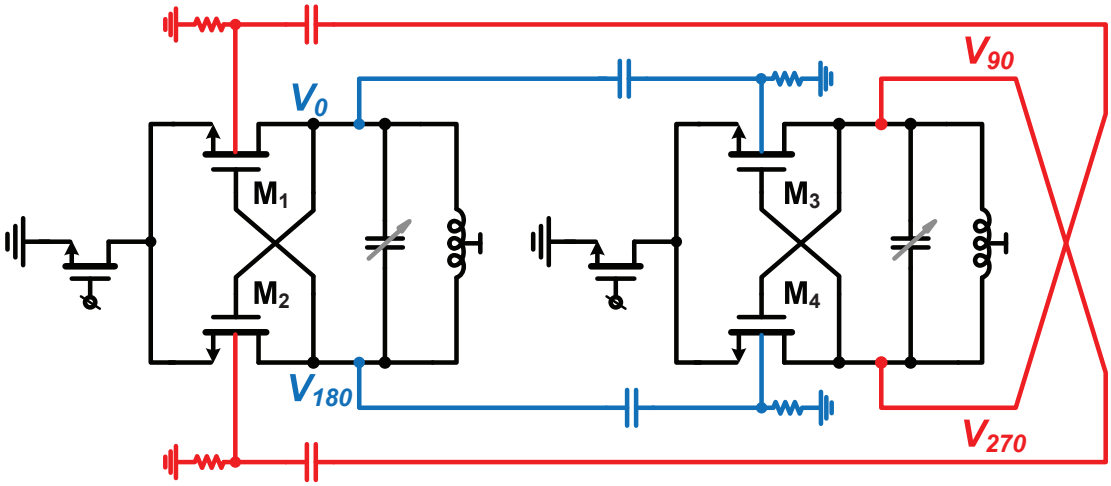

Figure 3.13: Back-gate coupled LC QVCO

exploits the fourth terminal (the bulk contact) of the g_m-cell transistor for coupling, eliminating the need for an additional coupling transistor. In addition to reducing the power consumption, this also removes the additional noise contributed by the coupling transistors. To allow this scheme, the transistor has to be a triple-well transistor to allow for a separate bulk terminal (not tied to the substrate). Note that AC-coupling is used, where resistors are used to dc-bias the bulk terminal at its nominal ground potential. While triple-well devices are available in most of the RF technologies, they are not a standard option for a plain vanilla CMOS technology. Moreover, injecting the signal into the bulk incurs the risk of forward-biasing the bulk terminal, which is directly loading the tank. Hence, the Q of the tank can be reduced by the forward biased junction leading to a phase-noise degradation.

In [54], transformer coupling is used for injection instead of active devices as shown in Fig. 3.14. This is done by using transformer coupling between the sources of one stage, and the drains of the next stage. Hence, active coupling devices are eliminated together with their noise effect. Moreover, transformers do not limit the swing allowing for low supply voltages to be used. However, the operating frequency does not coincide

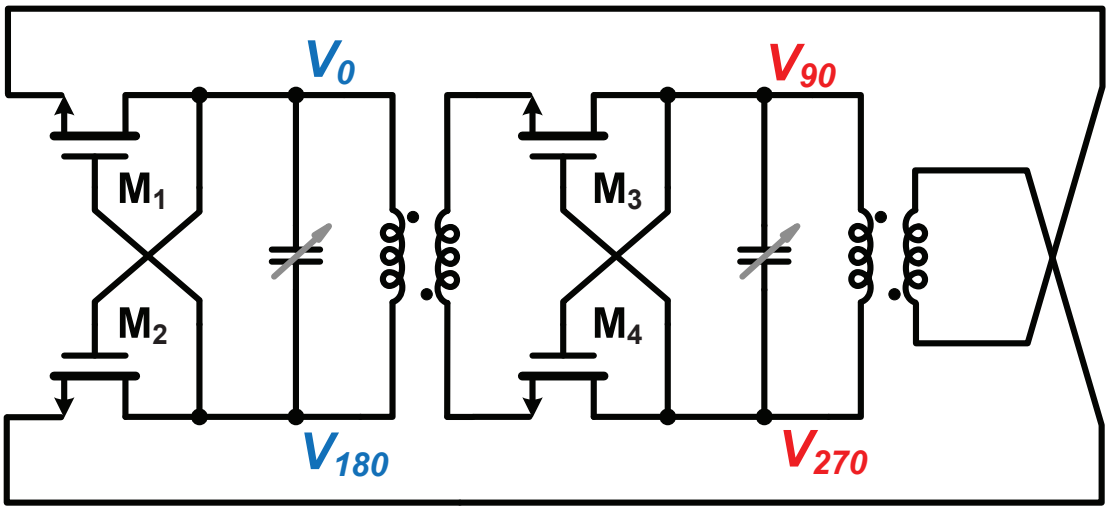

Figure 3.14: Simplified schematic of transformer-coupled QVCO

with the tank center frequency (similar to the basic QVCO). Hence, phase-noise is degraded due to this phase-shift effect [54]. This issue is addressed in [55], which uses a similar structure with two differences. First, no cross-coupling is used in the individual VCOs, forming a ring-oscillator structure instead of two coupled VCOs. [1] Second, each transformer forms a coupled resonator. With proper tuning of the coupling factor (k), the phase shift of the coupled resonator structure can be made to be 90° making the tank resonance and the QVCO frequency the same and hence improving the Q and the phase-noise performance. The drawback, however, is that relatively small coupling factors (in the order of 0.2 or less) are needed complicating the transformer design and requiring relatively tight control on the coupling factor value.

[1] A ring oscillator is a cascade of amplifiers whose gain is at least unity, and whose phase is zero, at the frequency of oscillation. The individual amplifiers do not oscillate on their own. In the other discussed QVCOs, the individual VCOs oscillate on their own (no cascade is needed) but are coupled through a network to generate quadrature phases.

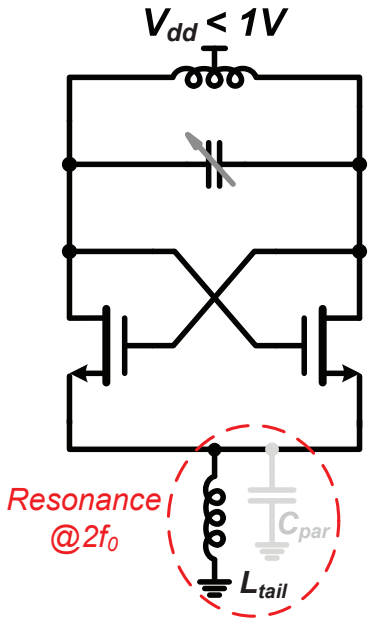

Figure 3.15: Core VCO for the proposed architecture

3.3 Proposed architecture

3.3.1 Motivation

In this section, we propose a new architecture for LC QVCOs, based on the phase-shifting concept outlined in section 3.2.1. The motivation is achieving a QVCO architecture that is:

1. simple and robust
2. achieves good phase-noise performance
3. does not limit the tuning range
4. operates with low-supply voltage (1V or less)

The QVCO developed for this work is targeted for use in a wideband phased-array receiver that covers the band from 7–9 GHz (instantaneous bandwidth is 2GHz). To

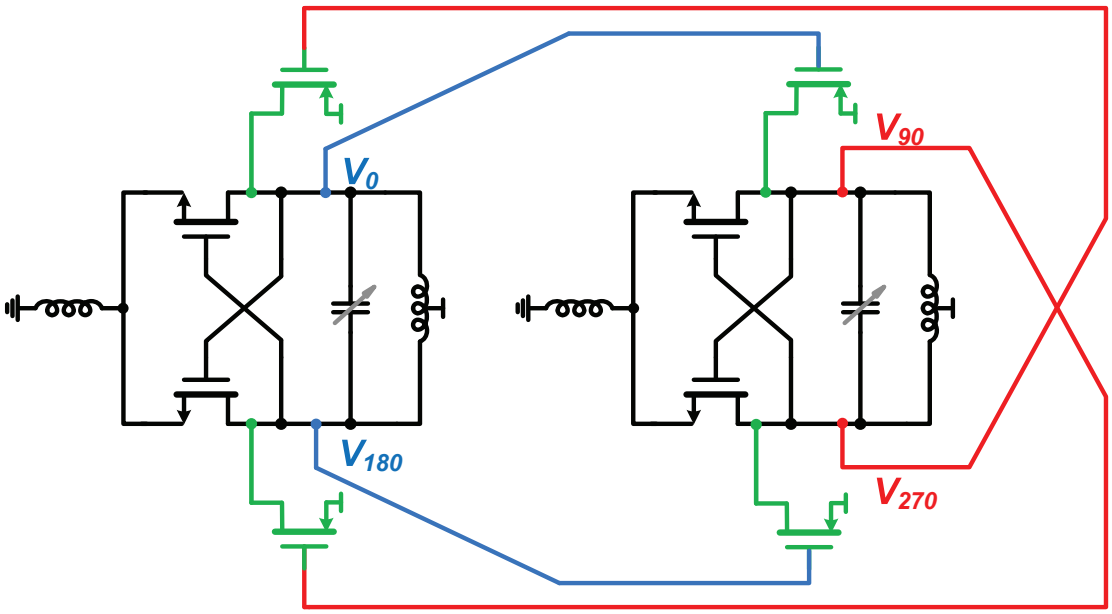

Figure 3.16: Schematic of the proposed QVCO

accommodate possible process shifts, the design target is to achieve a 6–10 GHz tuning range. Moreover, the technology in use is TSMC 65nm CMOS technology with a nominal supply voltage of 1V requiring the QVCO to operate at, or below, 1V.

3.3.2 Core VCO choice

The core VCO is a simple cross-coupled LC VCO, with the tail source removed as shown in Fig. 3.15. An inductor is placed at the common-source which forms a resonant circuit with the total parasitic capacitance at that node (C_{par}), at twice the oscillation frequency $2f_0$. In addition to allowing for a larger swing, removing the tail source also greatly reduces the $1/f^3$ noise [42, 56]. With large oscillation swings, the cross-coupled g_m transistors go into triode region for a considerable part of the cycle. The resonant circuit adds a high impedance in series with the low-resistance switch, avoiding Q factor degradation at high swing and, thus, improving the overall phase-noise performance [56].

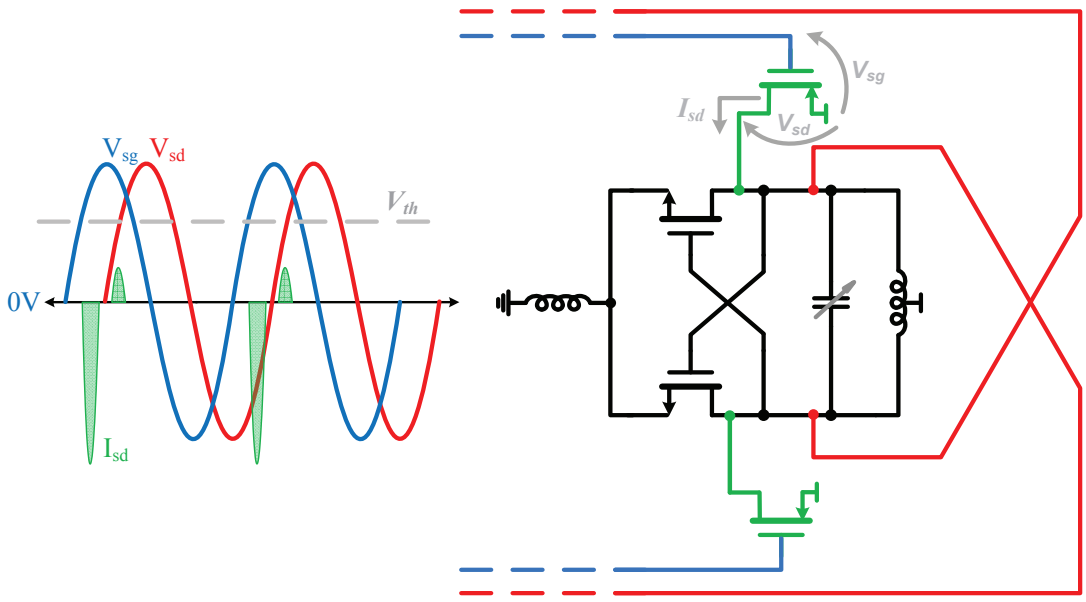

Figure 3.17: Coupling transistor current and voltage waveforms for proposed architecture

3.3.3 Full QVCO

The schematic of the proposed QVCO is shown in Fig. 3.16. The QVCO is formed by coupling two of the core VCOs in Fig. 3.15. The proposed QVCO resembles the direct-coupled QVCO of Fig. 3.1 with one difference; the coupling transistors are PMOS instead of NMOS transistors. While this might seem to only shift the injection current by 180° making the proposed QVCO very similar to the basic QVCO, the direct intuition is not correct. The use of complementary devices for coupling the two core VCOs[2] , results in a phase-shifting effect that pushes the injection current away from the voltage zero-crossing points of the oscillator's output. Thus, this architecture can be classified under the "Phase-shift based" category. Unlike the architectures presented in section 3.2.1, however, the phase-shift is not performed by passive devices (which are frequency-sensitive), nor does it need a special coupling network that might de-Q the

[2] This means that if NMOS devices are used for the g_m-cell, PMOS devices are used for coupling and vice-versa

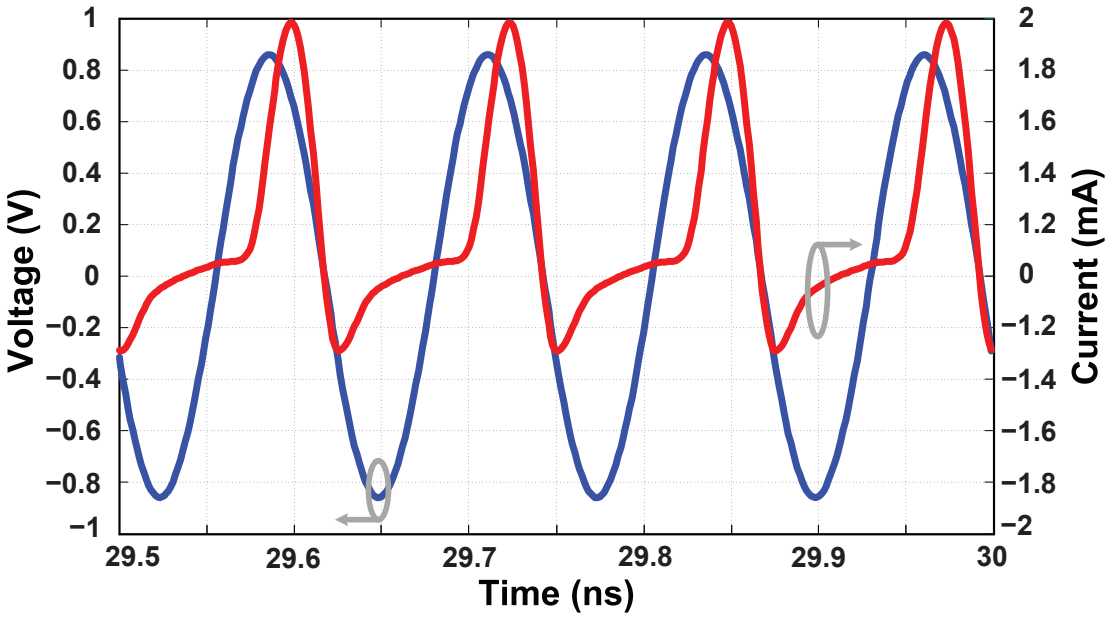

Figure 3.18: Simulated injection current and output voltage for PMOS coupling tank (as in [48]).

To understand why the proposed QVCO is different from a direct-coupled QVCO, the large-signal voltage and current waveforms of the coupling transistors have to be studied. Towards this end, consider Fig. 3.17 which depicts the large-signal time-domain waveforms of the coupling transistors. Due to the use of PMOS (or more generally: complimentary coupling), the coupling transistor is nominally off; both the source and gate voltages sit at the supply value in absence of oscillation setting V_{sg} to zero. Similarly, the source and drain voltages sit at the supply value making for a zero V_{sd}.

In the oscillation mode, the V_{sg} and V_{sd} voltages are in quadrature as they represent the single-ended quadrature outputs of the oscillator. When the V_{sg} voltage of the coupling transistor is at its peak (where it should be the most conductive), the V_{sd} voltage is zero, thus forcing the I_{sd} current to zero. *Hence, injection current is forced to be zero at the zero-crossings of the oscillator.* Away from the zero crossings, current

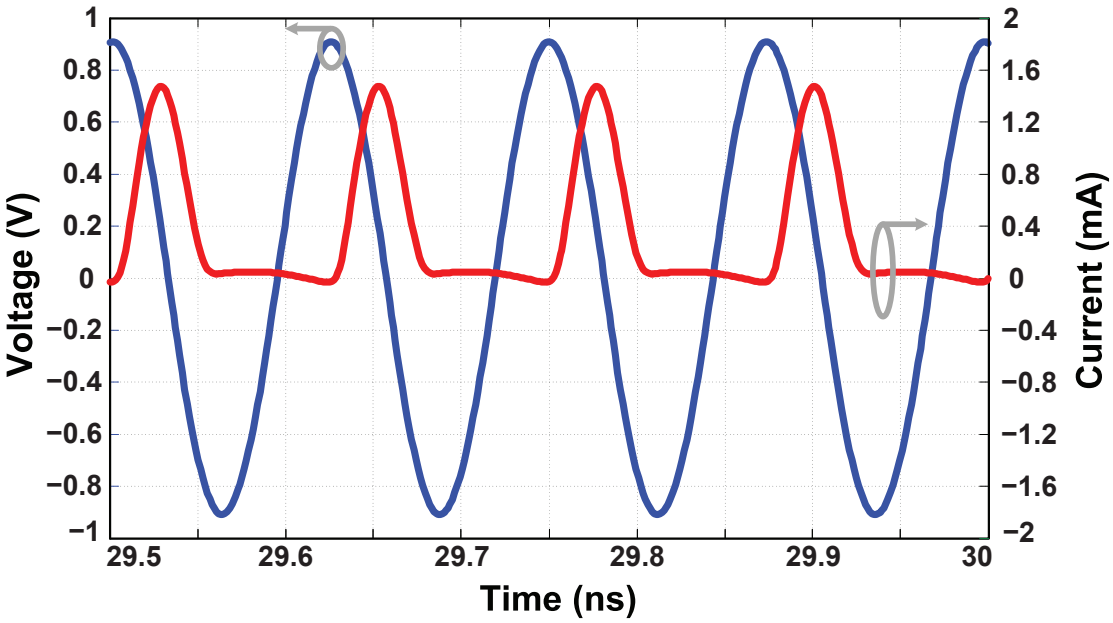

Figure 3.19: Simulated injection current and output voltage for NMOS coupling

is injected when $V_{sg} > V_{th}$ and V_{sd} is non-zero (positive or negative). As shown in Fig. 3.17, this results in two current pulses during each oscillation cycle, with one pulse (corresponding to a higher $|V_{sd}|$) much higher than the other. Interestingly, both current pulses are injected significantly far from the zero-crossing point.

This in effect creates a phase-shift that reduces phase-noise, without resorting to frequency-sensitive passives, or the use of coupling networks that might reduce the tank Q, allowing for a wide-tuning-range QVCO with robust active injection. As an added advantage, PMOS devices have inherently lower flicker noise than their NMOS counterparts due to the buried nature of the channel. The drawback, however, is that PMOS devices need to be larger than equivalent NMOS devices for equal injection strength. This becomes a problem only when the active devices constitute a large percentage of the total tank capacitance.

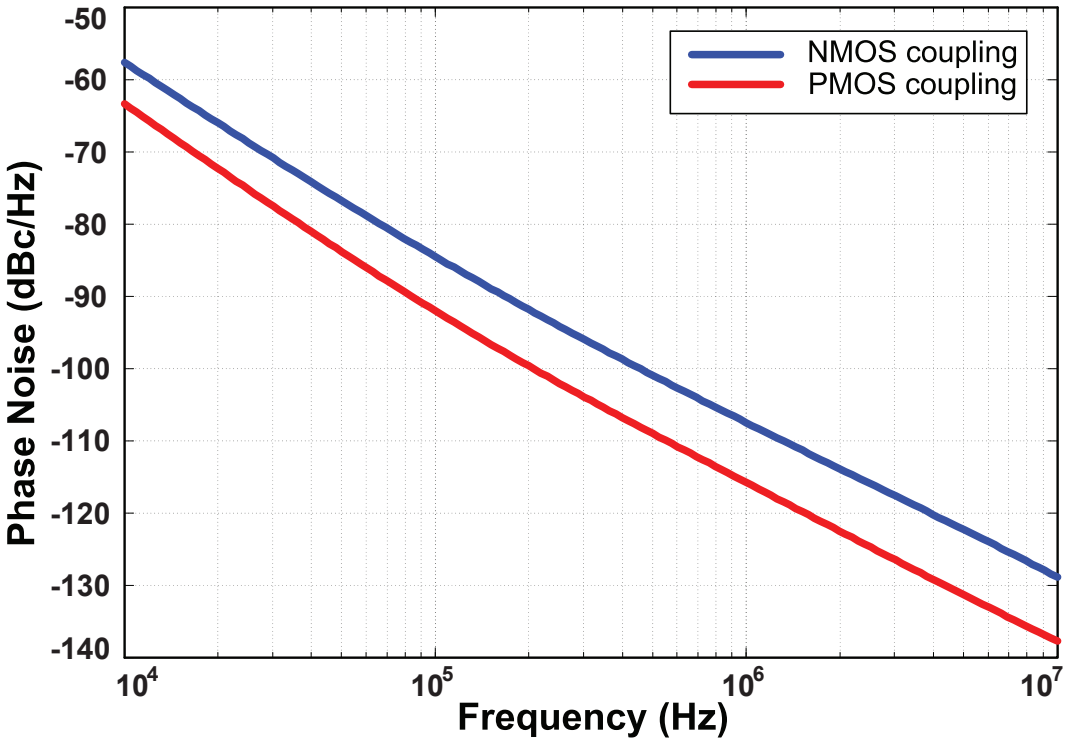

Figure 3.20: Phase-noise performance of PMOS and NMOS coupled QVCOs

Comparison: Normal and Complimentary coupling

To evaluate the effectiveness of the proposed scheme, simulations are made to compare the performance of the proposed QVCO (of Fig. 3.16), with a similar QVCO that has the PMOS coupling transistors (green transistors in Fig. 3.16) replaced with NMOS transistors. Since NMOS transistors have higher mobility than PMOS transistors, and to ensure a fair comparison, the NMOS transistors are sized such that their total injected charge (integration of the injected current over time) is equal to their PMOS counterparts. Both oscillators are tuned to operate at the same frequency of 8GHz.

Fig. 3.18 shows the injection current waveform overlapped with the output voltage waveform for PMOS coupling. The trends suggested in Fig. 3.17 can clearly be observed; the injection current is very small at the voltage zero-crossings, and goes to a maximum

away from the crossing. In fact, the peak current is shifted from the voltage zero-crossing by around 55°, with no explicit phase-shifting network employed. The same waveforms for the NMOS case are shown in Fig. 3.19, showing that the injection current peak almost coincides with the output voltage zero-crossing. The peaks are not perfectly aligned; there is a finite phase-shift of around 10°. Nevertheless, PMOS coupling adds significantly higher shift, moving the injection current peaks more towards the voltage peaks.

To assess the impact of the phase-shifting effect on the noise performance, phase-noise simulation is done for both PMOS coupling and NMOS coupling. As mentioned before, both NMOS and PMOS coupled QVCOs are sized to have equal injected charge, and are tuned to oscillate at the same frequency of 8GHz. As evident from Fig. 3.20, the PMOS coupled QVCO has a significantly better phase noise performance than its NMOS counterpart over three decades of frequency offset. The PMOS coupled version is better by 6dB in the $1/f^3$ region, and the improvement goes up to 8dB in the $1/f^2$ region. Clearly, PMOS coupling is advantageous to NMOS coupling in terms of phase-noise.

3.4 Prototype design

Based on the proposed complimentary coupling architecture, a prototype QVCO is designed in TSMC 65nm CMOS technology. Targeted at a wideband phased-array application, the design aims at achieving a center frequency of 8GHz with a tuning range of 6-10 GHz (to cover the band from 7GHz to 9GHz with margin for process shifts). Injection locking is used in the phased-array receiver, requiring the QVCO to have only discrete tuning i.e. no varactor tuning is needed. To increase the injection current, the PMOS coupling transistors are AC coupled and DC-biased at mid-supply so that their quiescent current is non-zero as shown in Fig. 3.21. Hence, the PMOS

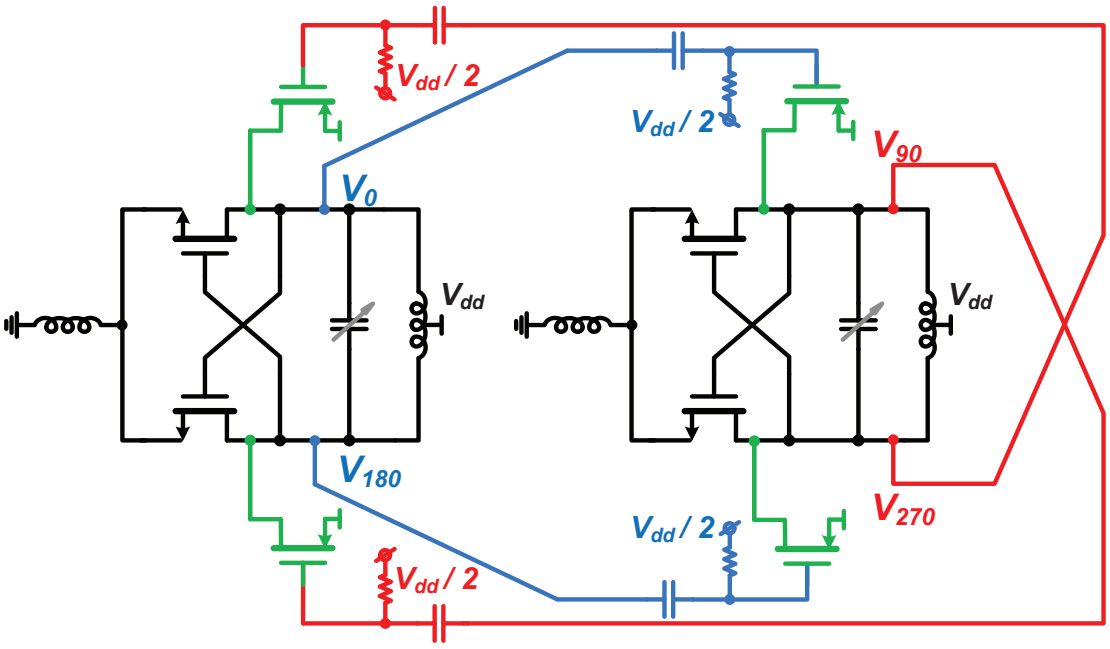

Figure 3.21: Schematic of designed prototype with class-AB complimentary coupling

coupling transistors operate in a class-AB mode instead of class-C operation.

A 4-bit binary-weighted MIM-capacitor bank is used for tuning, with the same bias scheme shown previously in Fig. 2.14. To ensure operation at the intermediate point between current-limited and voltage-limited regimes (for best phase-noise performance [57]), the QVCO operates at a supply voltage of 0.55V. The capacitor bank switches, however, are operated at the full supply voltage of 1V to ensure the lowest possible on-resistance for a given switch size.

Extracted simulation results of the discrete tuning characteristics of the designed prototype are shown in Fig. 3.22. The QVCO can be tuned from 5.5GHz at the lowest frequency end (larger tuning word and capacitance value) to 10.1GHz at the highest frequency end (where the load capacitance is purely from parasitics). Hence, the proposed VCO achieves a frequency tuning range (FTR) of approximately 59%, where FTR is defined as:

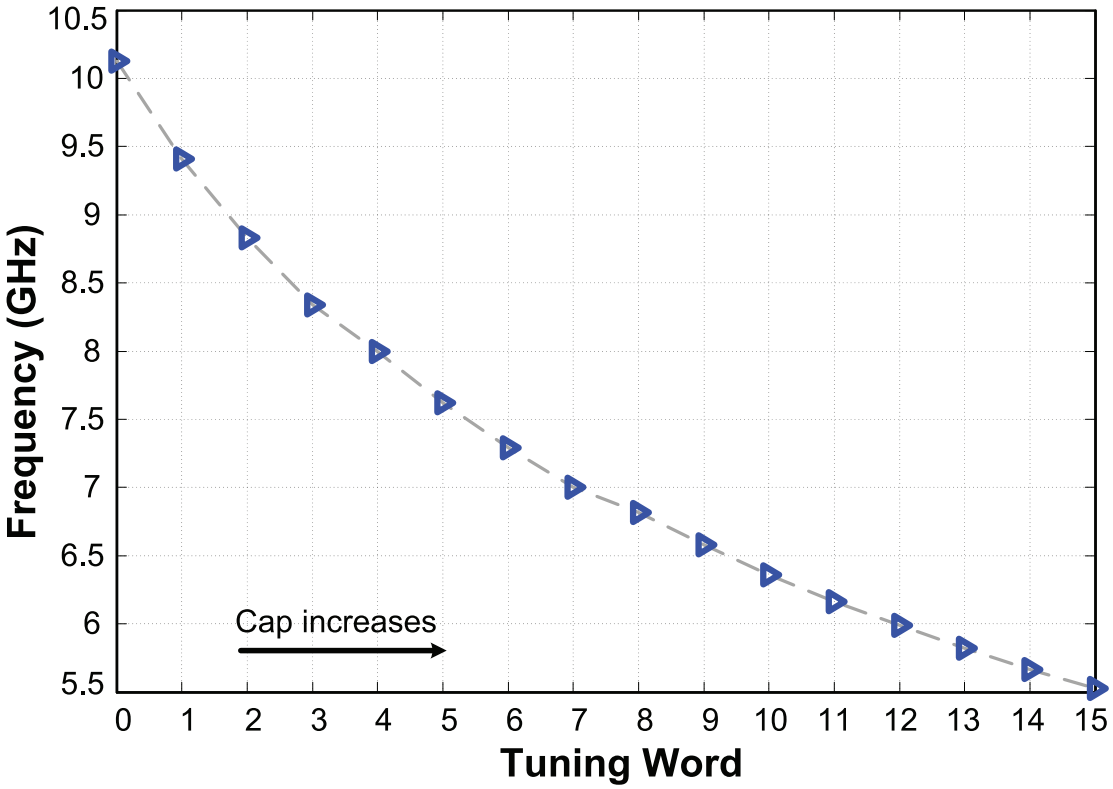

Figure 3.22: Output frequency of the QVCO prototype versus tuning word

$$FTR = \frac{2\left(f_{\max} - f_{\min}\right)}{f_{\max} + f_{\min}} \tag{3.3}$$

The power consumption of the proposed QVCO versus tuning word is shown in Fig. 3.23. As the load capacitance increases (i.e. as frequency decreases), the power consumption increases. Intuitively, this can be explained as follows: with an almost constant tank-Q, the tank's equivalent parallel resistance R_p can be given by:

$$R_p = Q\omega L = Q\sqrt{\frac{L}{C}} \tag{3.4}$$

Since power consumption is inversely proportional to R_p (larger R_p requires smaller

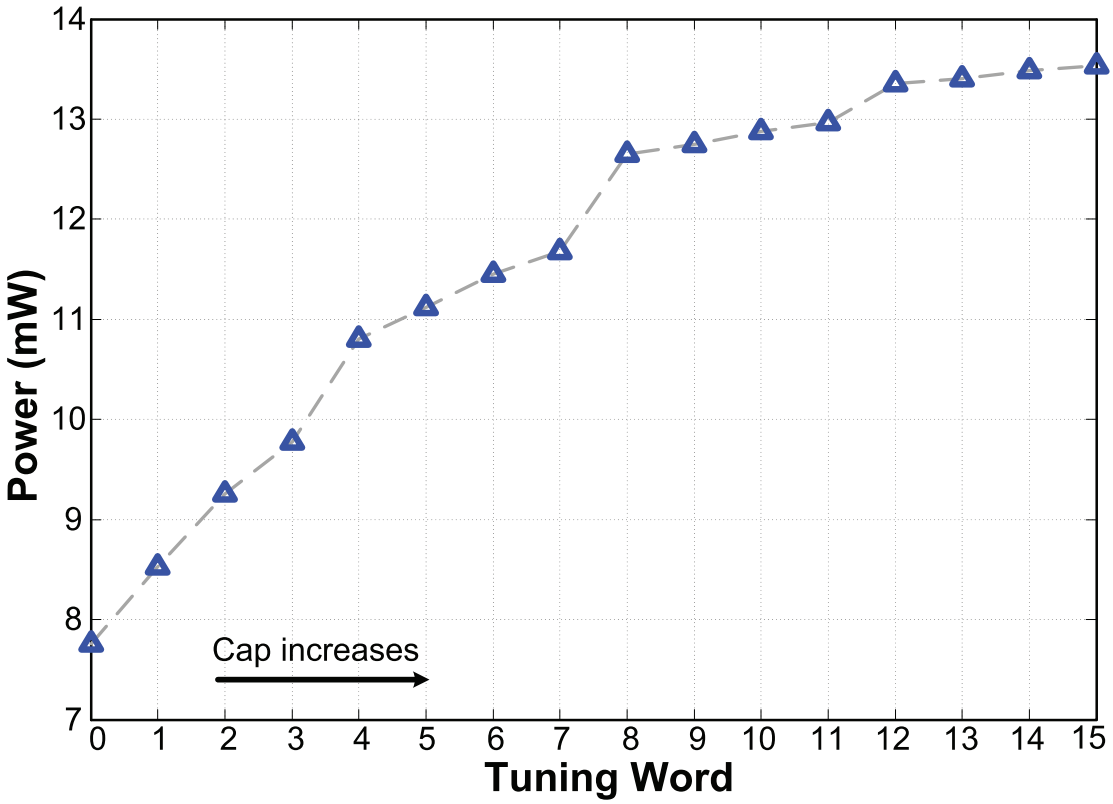

Figure 3.23: Power consumption of the QVCO prototype versus tuning word

drive current for the same swing and vice-versa), this makes power consumption proportional to $\sqrt{(C)}$ (assuming a fixed voltage swing). In our case, swing also varies with frequency so the $\sqrt{(C)}$ dependence is not strictly valid. The trend, however, of higher power consumption for higher capacitance is still valid.

The phase-noise of the proposed QVCO is shown in Fig. 3.24, at two offsets: 1MHz and 10MHz (extracted simulations). To get the best phase-noise performance at each discrete tuning-frequency, the supply voltage has to be changed to ensure that the QVCO is at the transition point between current-limited and voltage-limited regimes at that frequency. This was not done in simulation, however, to keep the results close to an actual practical scenario. Nevertheless, very good phase-noise performance is observed.

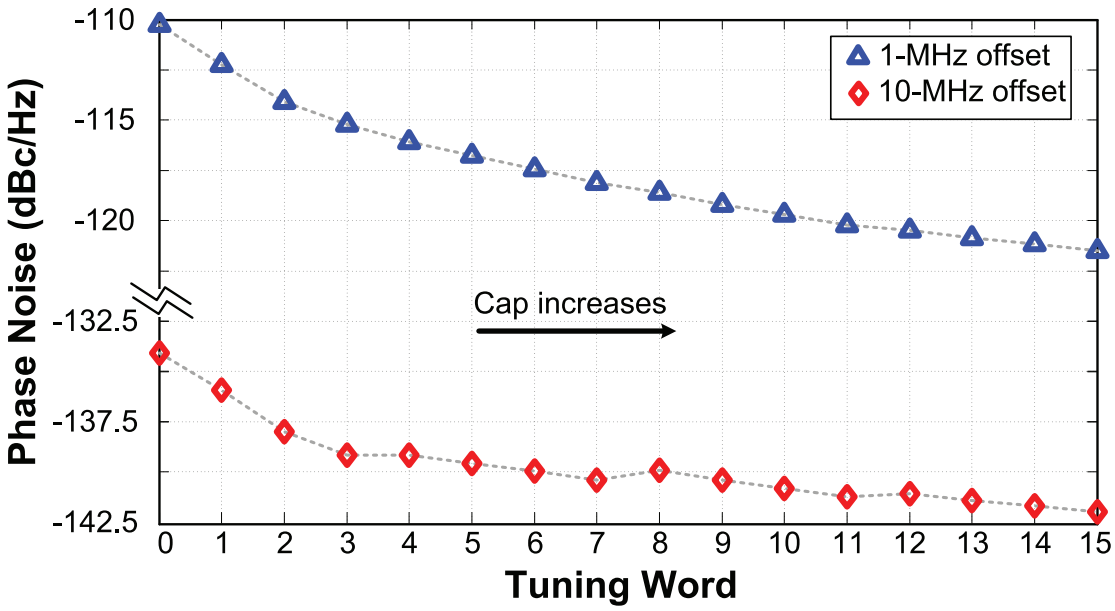

Figure 3.24: Phase-noise of the QVCO prototype versus tuning word

Since oscillator design entails a fundamental trade-off between frequency of operation, phase-noise, and power consumption, it is important to consider all these factors when evaluating the performance of an oscillator. A popular figure-of-merit (FOM) that serves this purpose can be given by [56]:

$$FOM = -\mathcal{L}\left(f_m\right) + 20Log\left(f_o/f_m\right) - 10.Log\left(\frac{P_{dc}}{1mW}\right) \tag{3.5}$$

where f_o is the VCO's center frequency, f_m is the offset frequency at which phase-noise is measured, P_{dc} is the power consumption, and $\mathcal{L}\left(f_m\right)$ is the phase-noise at offset f_m in dBc/Hz. This figure of merit does not capture an important design parameter: the VCOs tuning range. To capture the tuning range, another figure of merit is defined: the tuning-range figure-of-merit (FOMT), which can be given by [58]:

$$FOMT = FOM + 20.Log\left(\frac{FTR}{10}\right) \tag{3.6}$$

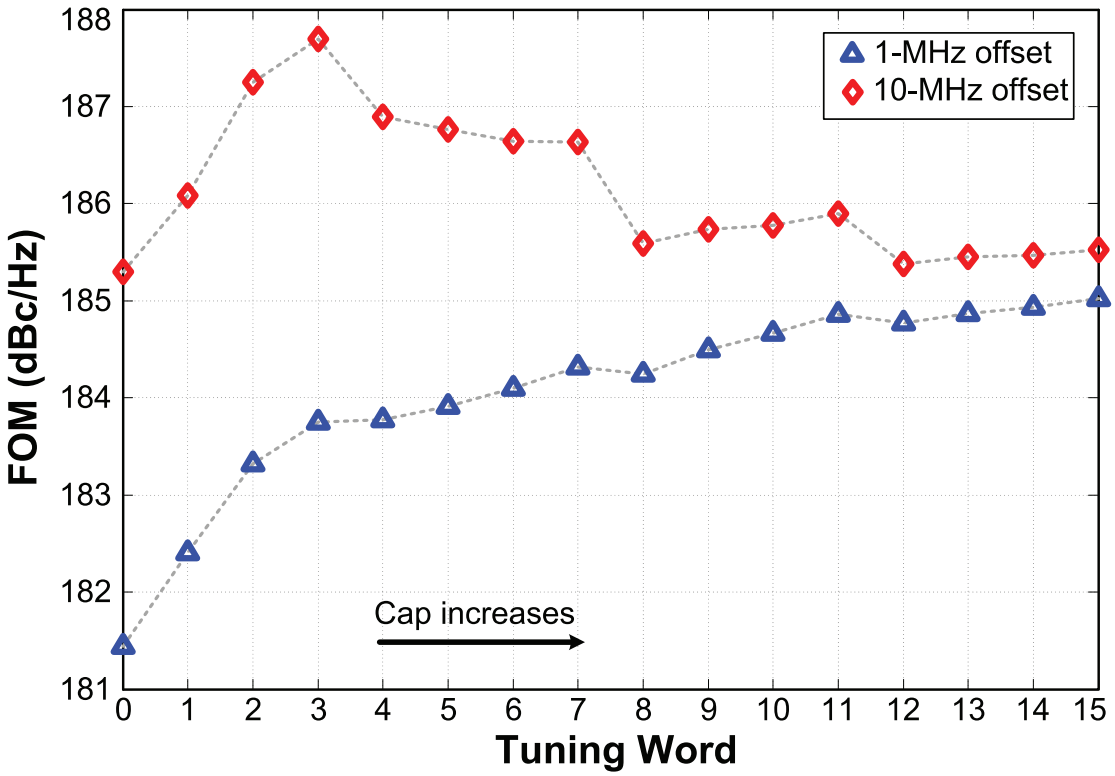

Figure 3.25: FOM of the QVCO prototype versus tuning word

The FOM, for 1MHz and 10MHz offset frequencies, is shown in Fig. 3.25. The FOM at 1MHz offset has a minimum value of 181dBc/Hz, with an FOM that decreases at higher frequencies (lower tuning word). As mentioned earlier, this is attributed to the use of a constant supply to emulate a practical working environment where it would be difficult/impractical to tune the supply voltage for each frequency point. With a wide FTR of 59%, the FOMT is 196.4dBc/Hz and 200.4dBc/Hz (worst-case) at 1MHz and 10MHz offsets, respectively. This is at par with state-of-the-art validating the usefulness of the proposed complimentary coupling technique.

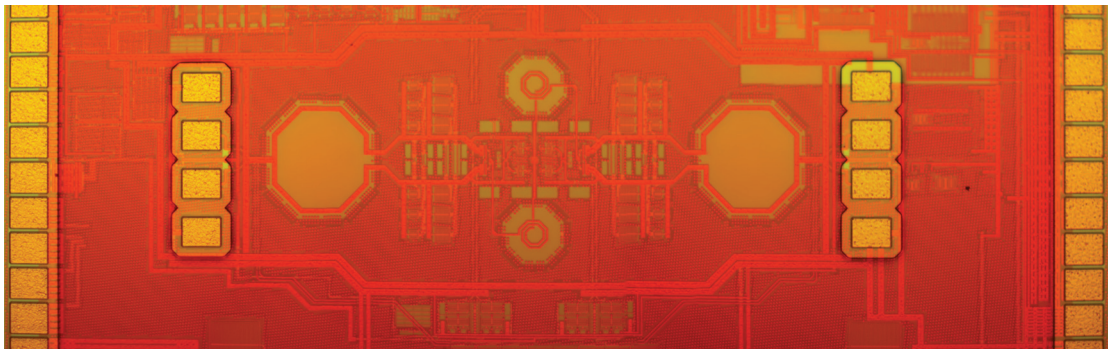

Figure 3.26: Chip micrograph

3.4.1 Measurement results

A prototype was fabricated in TSMC 65nm CMOS process. The design occupies an active area of 0.67mm^2. The buffered QVCO outputs are connected to GSSG pads for on-chip probing, using 50Ω buffers. The chip micrograph is shown in Fig. 3.26.

The fabricated QVCO can operate down to a 0.42V supply. The QVCO is tested at three different supply voltages: 0.42V, 0.5V, and 0.6V. In all cases, however, the supply voltage used for the switches in the capacitor array is kept at 1V. The supply voltage is varied by means of an off-chip linear regulator. The output of the GSSG probe is connected to an off-chip balun for differential to single-ended conversion and the single-ended output is fed to a R&S FSW43 spectrum analyzer for frequency and phase-noise measurement. The output frequency versus tuning word for the QVCO is shown in Fig. 3.27 for the 0.5V supply.

Due to a problem with EM extraction, extra inductive parasitics were not accounted for leading to a frequency shift from the original design. Nevertheless, the QVCO can be tuned from 4.59GHx to 7.82GHx achieving an FTR of 52%. Inspite of the shift, the tuning range is large enough to allow proper operation of the QVCO in the overall system. Similar results are obtained for the 0.42V, and the 0.6V, supplies. The output frequency for 0.42V supply ranges from 4.57GHz at the lowest end to 7.84GHz at the

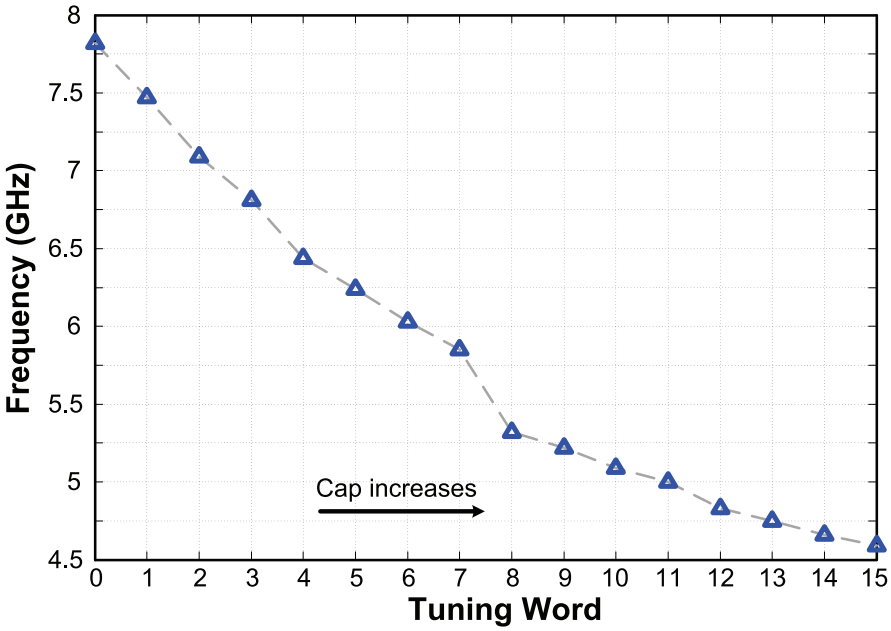

Figure 3.27: Measured frequency at 0.5V supply

highest end, achieving an FTR of 52.7%. For the 0.6V supply, the tuning range is from 4.61GHz to 7.89GHz with an FTR of 52.5%.

The measured power consumption of the QVCO versus the tuning word is shown in Fig. 3.28 for the 0.5V supply. Power consumption decreases for higher output frequencies (lower tank capacitance), and vice versa. The power consumption ranges from 7.36mW at the highest frequency, to 10.98mW at the lowest. Power consumption also varies with the supply voltage; power consumed at 0.42V supply ranges from 4.56mW to 6.6mW, whereas power consumed at 0.6V supply ranges from 16.46mW to 23.04mW. To illustrate the relative magnitudes of the power consumptions at the different supplies, Fig. 3.29 shows the power consumption for the three different supply voltages on the same plot.

The measured phase-noise of the QVCO at 0.5V, and tuning word equal to "5" (corresponding to 6.24 GHz, which is the mid-point of the tuning-range), is shown in

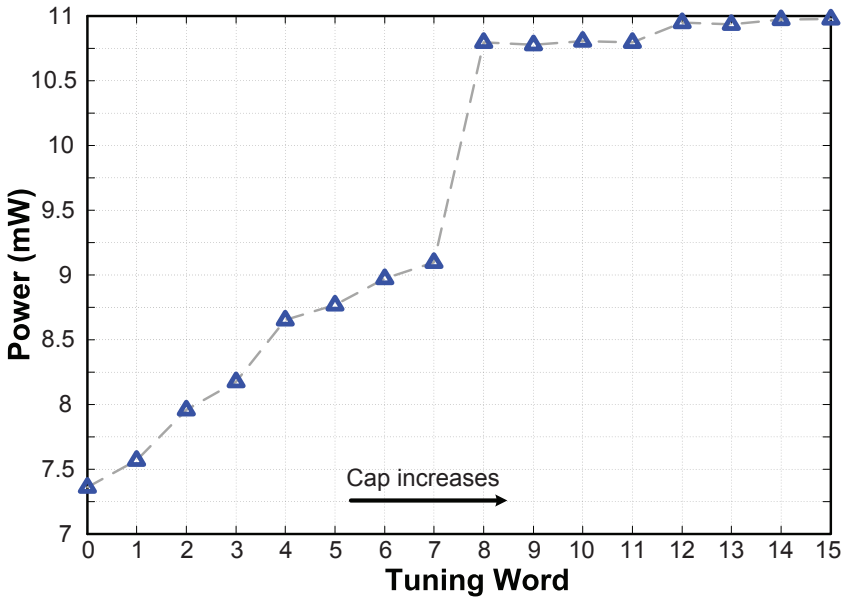

Figure 3.28: Measured power consumption at 0.5V supply

Fig. 3.30. The frequency offset is swept from 300kHz to 100MHz.

The phase-noise at 1MHz and 3MHz offsets, across the tuning range, is shown in Fig. 3.31 for 0.5V supply. At 3MHz offset, phase-noise ranges from -123.5dBc/Hz to -128.5dBc/Hz across the tuning-range, while the phase-noise at 1MHz offset ranges from -111.5dBc/Hz to -117.8dBc/Hz across the tuning-range. For the 0.42V supply, phase-noise at 3MHz offset ranges from -121.7dBc/Hz to -127.3dBc/Hz across tuning range whereas the phase-noise at 1MHz offset ranges from -110.5dBc/Hz to -115.87dBc/Hz across tuning-range. On the other hand, the 0.6V supply translates to a phase-noise of -123.26dBc/Hz to -130.26dBc/Hz, and -110.5dBc/Hz to -119.8dBc/Hz, at 3MHz and 1MHz offsets, respectively.

The FOM at 0.5V supply (for 3MHz offset) is shown in Fig. 3.32. The FOM touches 185.4dBc/Hz at its peak, and goes down to 181.6dBc/Hz at its minimum. The average FOM across the tuning range is 182.9dBc/Hz. With a 52% FTR, the average FOMT is 197.3dBc/Hz (the peak is 199.7dBc/Hz). Similarly, for 0.42V supply the average FOM

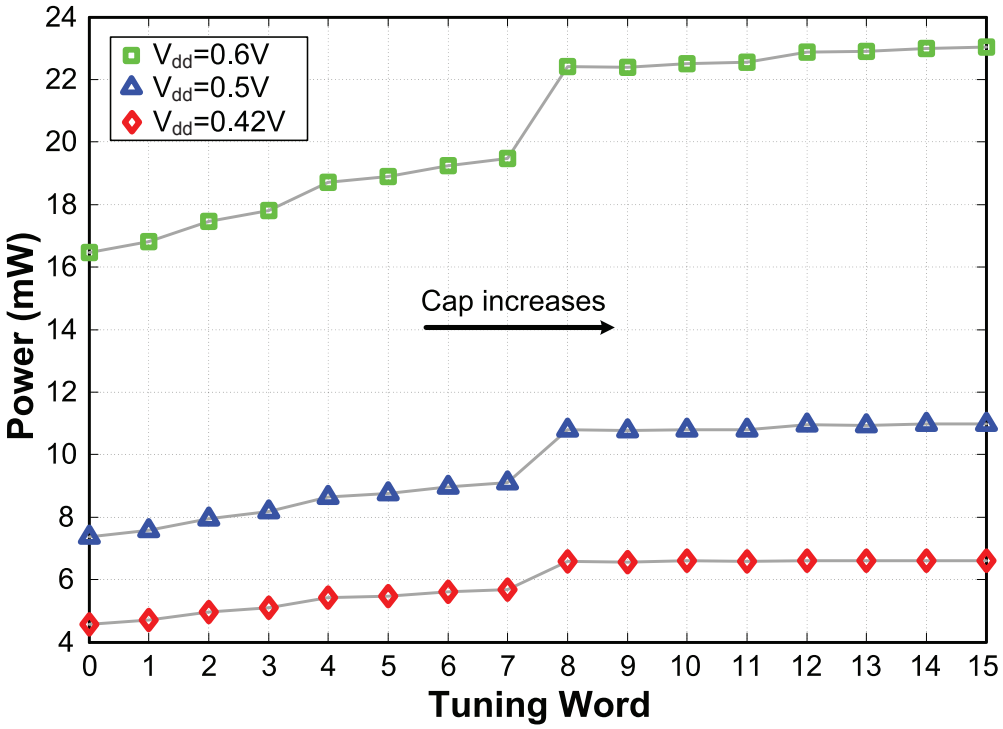

Figure 3.29: Measured power consumption at the three tested supply voltages

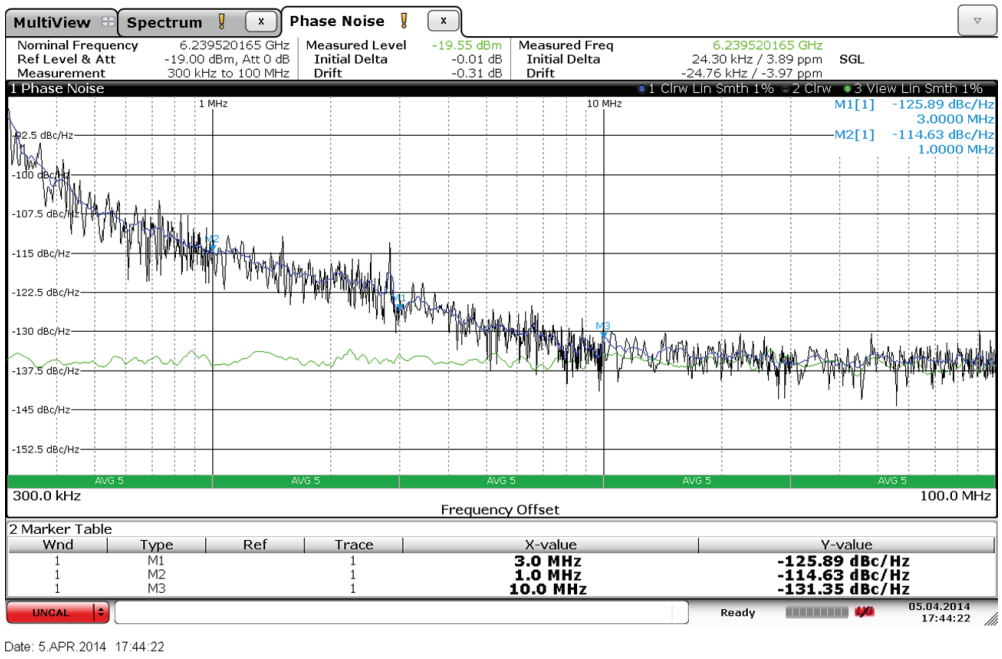

Figure 3.30: Measured phase-noise at 0.5V supply, and tuning-word="5"

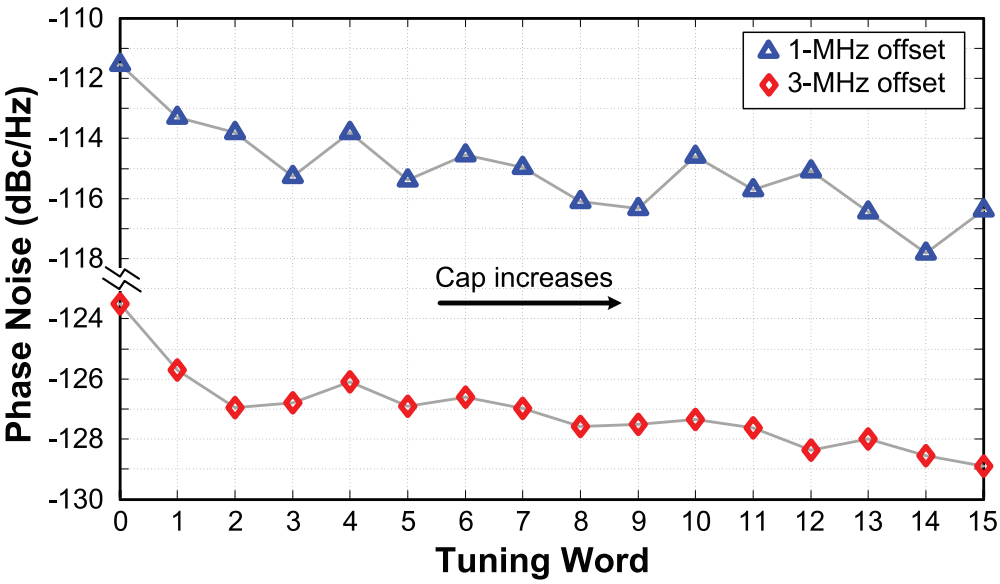

Figure 3.31: Measured phase-noise at 0.5V supply for 1MHz and 3MHz offsets

is 182.7dBc/Hz with a maximum and minimum values of 184.7dBc/Hz and 180.3dBc/Hz respectively. The average, and peak, FOMT is 197.2dBc/Hz and 199.2dBc/Hz respectively. At 0.6V supply, the average FOM degrades to 180.1dBc/Hz with a maximum and minimum value of 181.6dBc/Hz and 179.2dBc/Hz respectively. The average, and peak, FOMT is 194.5dBc/Hz and 196dBc/Hz resepctively. The degradation at higher supplies comes from an increased power consumption without an equivalent phase-noise improvement.

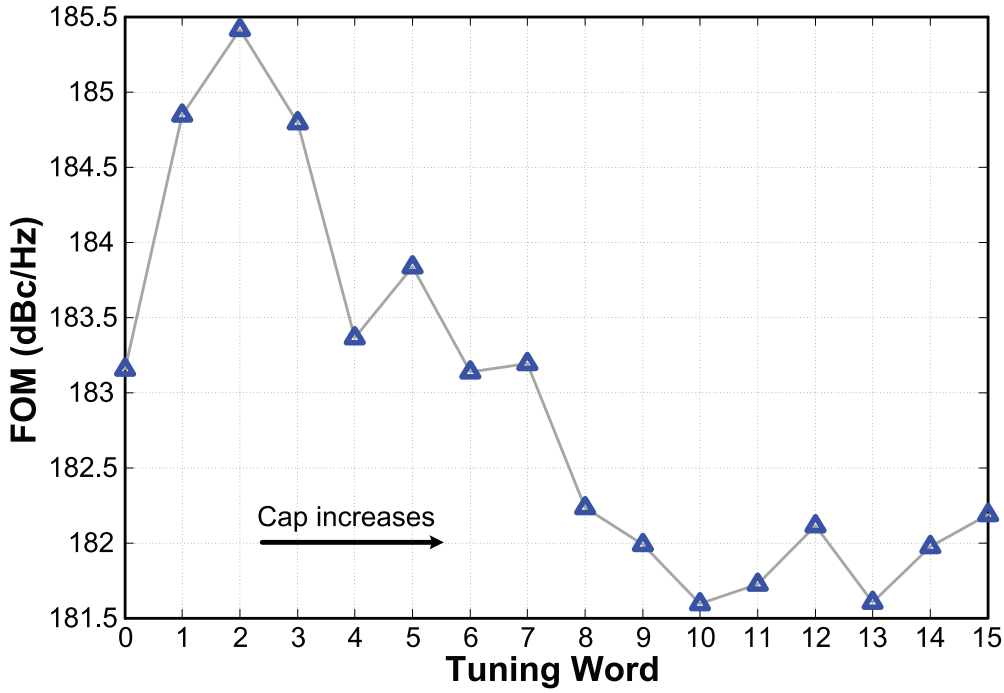

Figure 3.32: Measured FOM at 0.5V supply for 3MHz offset

The key performance aspects of the QVCO, at the three different supply voltages, are summarized in Table. 3.1. The power consumption and phase-noise numbers are those obtained at a tuning-word of "5" which corresponds to the mid-point of the tuning curve. Phase-noise values are those obtained at 3MHz offset. The FOM and FOMT values are the average across the tuning range. Optimal FOM can be observed both

at the 0.42V and the 0.5V supplies. The 0.5V supply, however, has the advantage of a lower phase-noise - without FOM degradation (i.e. extra power is justified for the phase-noise advantage). At 0.6V supply, however, phase-noise performance is similar, whereas power consumption increases drastically, resulting in a lower FOM. With all the three supply voltages achieving almost the same FTR, the FOMT of the 0.6V supply is also lower. Hence, the design-value 0.5V supply is the optimum performance point in terms of achieving the best phase-noise performance without excessive power consumption, while covering the desired tuning range.

Table 3.1: Measured QVCO performance summary

Supply(V)	FTR(%)	Power(mW)	PN(dBc/Hz)	FOM(dBc/Hz)	FOMT(dBc/Hz)
0.42	52.7	5.5	-124.3	182.7	197.2
0.5	52	8.8	-126.9	182.9	197.3
0.6	52.5	17.8	-126.6	180.1	194.5

3.5 Conclusions

In this chapter, a novel coupling technique for QVCOs is presented. Using a modification of the conventional active coupling, robust quadrature coupling together and low-phase noise are simultaneously achieved. The proposed technique, in essence, can be classified under the phase-shifting category. Nevertheless, no passive phase-shifting networks are used, hence the phase-noise advantage of phase-shifted coupling is achieved without the usual drawback of frequency sensitivity, and reduced tuning range. Furthermore, the architecture proposed is well-suited for low-voltage operation.

The performance of the fabricated prototype is compared with similar QVCOs in published literature, in Table 3.2. The phase-noise values reported are those at 3MHz offsets. If data at 3MHz offset was not available, it was extrapolated with a 20dB/decade profile. The supply used for the core of the QVCO in this work is 0.5V, but the switched

Table 3.2: Comparison with literature

Ref	V_{dd}(V)	f_o(GHz)	FTR(%)	P_{dc}(mW)	PN(dBc/Hz)	FOM	FOMT
[60]	1.7	20.9	3.1	6.3	-126.5	195.6	185.4
[47]	2	1.57	24	30	-147.5	187.1	194.7
[49]	2.5	4.9	12.2	22	-134.5	185	186.7
[31]	2	1.8	18.3	25	-140	181.6	186.8
[53]	1.8	1.1	28	5.4	-137	181	190
[54]	1	17	16.5	5	-119.5	187.6	192
[59]	1.2	4.8	67	6-20	-123.6	176.5	193
This Work	0.5	6.25	52	7.4-11	-126.6	181.6-185.4	196-199.7

capacitor tuning uses 1V supply.

This work achieves the highest FOMT amongst similar work. It also has the second highest tuning-range, next to [59]. It is to be noted, however, that the large tuning range in [54] is achieved through the use of transformers; the tuning range in this work is achieved through the use of simple conventional tanks with no specially designed transformers. Moreover, the average FOM, as well as FOMT, of this design is higher. Furthermore, the achieved FOM is close to similar designs. Designs in [47,49,60] achieve higher FOM, but also use much higher supplies. The design in [54] achieves a higher FOM with the small supply voltage of 1V but, again, at the cost of the added design complexity of using special coupling transformers.

In summary, the proposed technique provides state-of-the-art FOM performance with robust, simple design that uses conventional tank-circuits. Moreover, it achieves state-of-the-art tuning-range, with best-in-class FOMT performance.

Chapter 4

mm-Wave QVCO

4.1 Introduction

With the ever-rising demand for high data rates in wireless consumer products, there is an increasing demand for wider RF bandwidth. Millimeter-wave bands meet these demands by providing wide RF bandwidths, allowing for Gb/s data rates. With 9-GHz of ISM (unlicensed) bandwidth between 57GHz and 66GHz, new standards have emerged to exploit the available bandwidth for high data rate applications leading to the development of the IEEE 802.11ad standard [61][1] ; a WLAN standard complimenting the, currently popular, 802.11a/b/g/n for short range, very high data rate (up to 6.75Gb/s) applications. For long-range communications, such as wireless back-haul, the E-band spanning 71-76 GHz and 81-86 GHz allows 1Gb/s transmission over a distance of 2-3 km [62]. Besides communications applications, the millimeter wave band is ideal for radar applications. Two bands for vehicular radar are allowed by regulatory agencies: the 24GHz and the 77GHz bands [63]. The 77GHz band[2] offers higher radar performance due to smaller antenna sizes, better angular resolution, smaller fractional

[1] In US, only 7GHz of bandwidth are available spanning 57GHz - 64GHz.
[2] This band spans 76 - 77 GHz in US, and 77 - 81 GHz in Europe

bandwidth (hence easier passive component integration), as well as higher allowable transmit power (which translates to a longer range operation) [63]. CMOS technology has proven its viability for millimeter wave applications [16, 64–66], allowing for high degree of integration and cost reduction of millimeter wave systems.

4.2 Motivation

Conventional quadrature generation techniques, namely polyphase filtering and divide-by-2 frequency dividers, are impractical for millimeter wave applications. Divide-by-2 quadrature generation requires the system's oscillator to operate at double the desired output frequency, which is impractical or impossible for 60GHz (and above) frequencies. Polyphase filtering requires the use of very small values for resistors and capacitors, making them very sensitive to parasitics and mismatch effects. Quadrature generation, however, can be done by using 90° hybrids [64, 67], or quadrature VCOs [16, 65, 68]. Due to the passive nature of hybrids, however, their output suffers attenuation [67]. Quadrature VCOs are, thus, well-suited to millimeter-wave requiring less power for signal generation and buffering.

Several millimeter-wave QVCO designs are present in literature. In [69], the basic LC QVCO structure of Fig. 3.1 is used. A major drawback is the use of active coupling transistors that load the tanks, leading to a reduced tuning range. The "varactor-like" effect is used for additional tuning, by varying the tail current of the coupling transistors. While this adds a degree of freedom in tuning the oscillator, it comes at the cost of either a larger quadrature error (if the tail current is reduced to reduce the frequency) or a higher phase-noise (if the tail current is increased to increase the frequency). Thus, the optimal trade-off point between phase-noise and quadrature accuracy cannot be maintained across the whole tuning range. The QVCO has a center frequency of 48GHz with a tuning range of 8GHz achieving an FTR of 16.67%.

In [70], the basic LC QVCO structure is again used. To cover the 57-66GHz communications band, however, two QVCOs with overlapping frequency ranges are used. This incurs an area penalty, due to the replication of the QVCO as well as the replication of the VCO buffers. Nevertheless, a single QVCO just covers the desired 57-66GHz band. The dual QVCO structure, however, allows an overall tuning range of roughly 57-72GHz. Furthermore, the phase-noise performance is relatively poor which is characteristic of the conventional QVCO as discussed in section 3.1.

In [55], a ring structure is used with transformer-based inter-stage coupling. The coupling factor is designed to induce a 90° phase-shift in-between stages to improve phase-noise as explained in section 3.2.1. Although it achieves a very good phase-noise performance, the QVCO has a limited tuning range of 4.35GHz falling short of covering the 57-66GHz band. Moreover, the transformers require a low-coupling factor to achieve the desired phase-shift, resulting in relatively complicated transformer design as well as signal loss.

In [71], the conventional QVCO structure is used along with transformer-coupling. Tuning is done through changing the tail current. The bi-modal operation of a QVCO is exploited to increase the tuning range. This is done by adding a switchable stage of 90° phase-shift. When the phase-shift stage is off, the QVCO operates in the "normal" mode corresponding to a center frequency higher than the tank's resonance frequency [40]. A major drawback is the dependence on a frequency-sensitive LC structure for the bi-modal operation, making the QVCO prone to mismatches and process variations (with no tracking between the main tank's LC and the phase-shift network's LC). Nevertheless, the QVCO achieves a tuning range of 13GHz, covering the frequency range of 49-62GHz with good phase noise performance.

In [48], the frequency independent phase-shift network shown in Fig. 3.7(b) is used to achieve good phase-noise performance over a wide tuning range. The QVCO can be

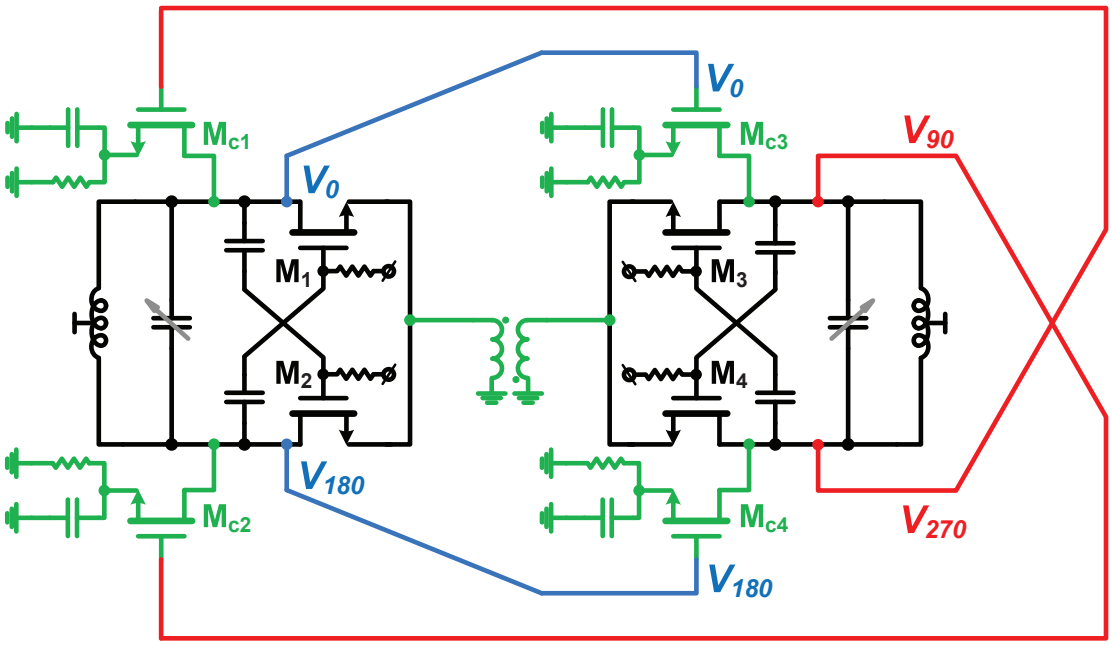

Figure 4.1: Proposed millimeter-wave QVCO

tuned from 58-68GHz. While the QVCO achieves a good phase-noise performance with relatively low power, the tuning range barely covers the desired 57-66GHz band leaving little room for process shifts.

This work aims at achieving a wide-tuning range quadrature VCO that is well-suited to millimeter-wave operation, achieves reasonable phase noise and power numbers and, simultaneously achieving a tuning range that covers the 57-66GHz communications band with enough room for process shifts. Moreover, it is also desirable to achieve a tuning range that would allow the QVCO to be used in multiple millimeter-wave bands such as the 57-66GHz ISM band, the 71-76GHz E-band and the 76-77GHz vehicular radar band.

4.3 Proposed QVCO

In the absence of parasitics, the ratio between the maximum and the minimum oscillation frequency of an LC oscillator would be given by:

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{C_{\max}}{C_{\min}}} \tag{4.1}$$

where f_{max} is the maximum oscillation frequency, f_{min} is the minimum oscillation frequency, C_{max} is the maximum capacitance, and C_{min} is the minimum capacitance. Practically, the tank capacitance has a relatively large percentage of parasitics (C_{par}). If switched-capacitor tuning is used, then a part of the parasitic capacitance (C_{fixed}) will be due to cross-coupled pair, the parasitic capacitance of the tank inductor, input capacitance of the QVCO buffers, as well as any deliberate fixed capacitance connected to the tank. Another parasitic component will arise from the parasitic top and bottom plate capacitances associated with the switched-capacitor bank. If the parasitic capacitance for each switched capacitor of value C is given by αC, where $\alpha < 1$, then the total parasitic capacitance can be given by:

$$C_{par} = C_{fixed} + \alpha.C_{\max} \tag{4.2}$$

Now the ratio of f_{max} to f_{min} becomes:

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{C_{\max} + C_{par}}{C_{\min} + C_{par}}} \tag{4.3}$$

Clearly, the presence of the parasitic tank capacitance reduces the ratio of f_{max} to f_{min}. Note that in the limit that $C_{par} \gg C_{max}$, this ratio tends to one. This means that for larger C_{par}, the ratio of f_{max} to f_{min} diminishes, severely limiting the tuning range. This becomes specially important at millimeter-wave frequencies, since the design value of the tank capacitances is intrinsically low (due to the high frequency

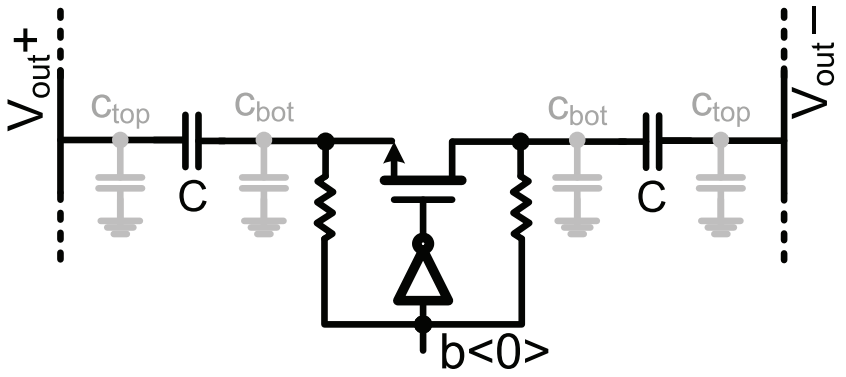

Figure 4.2: A single bit slice of the capacitor bank, and associated parasitics

requirement), making the tuning range more sensitive to parasitics. It is, therefore, of utmost importance that the quadrature coupling technique used adds as little parasitic capacitance as possible (ideally no parasitics at all).

Based on the previous discussion, the proposed QVCO architecture is shown in Fig. 4.1. To reduce parasitic loading, super-harmonic transformer coupling at the tail is used as explained in section 3.2.2. Since the transformer based super-harmonic coupling technique requires larger QVCO swings [49], it is more effective at the higher frequency bands where the amplitude is larger. To ensure proper coupling at the lower frequency bands, RC phase-shifting with small coupling transistors is used to assist the coupling operation at lower amplitudes (lower frequencies). The coupling transistors are almost seven times smaller than the cross-coupled g_m transistors, adding very small parasitic loading. The gates of the cross-coupled g_m transistors are AC-coupled, with separate gate biasing allowing a larger output-swing before the g_m transistors go into the linear region, and hence improving phase-noise performance [72].

Besides the parasitics from the coupling transistors, the capacitor bank parasitics become important, specially when a large tuning range is desired. Fig 4.2 shows one slice of the switched capacitor bank. Note that there are parasitic capacitances associated with both the top (C_{top})and bottom (C_{bot}) plates of the capacitor. There are also

parasitics originating from the MOS switch (C_{sw}). When the switch is off, the top plate, bottom plate, and switch parasitics appear in parallel (assuming $C \ll C_{top,bot,sw}$). This lowers the maximum oscillation frequency as it increases the tank capacitance at the highest frequency setting (when all bank capacitors are disconnected). On the other hand, when the switch is on it has a finite resistance r_{on}. This finite resistance puts an upper limit on the capacitor's quality factor, thus reducing the quality factor of the tank for lower frequencies, and *increasing* the lower frequency limit. *Hence, in the capacitor bank the capacitor and switch parasitics limit the upper frequency limit whereas the switch on-resistance restricts the lower frequency limit.*

4.3.1 Prototype Design

Based on the architecture proposed in Fig. 4.1, a prototype was designed in IBM's 32nm SOI process. Only discrete capacitor tuning is used, with 6-bits of binary-weighted tuning: 3-bits of coarse tuning (a 15fF unit capacitor), and 3-bits of fine tuning (a 3fF unit capacitor). The high-Q capacitor available in the process is a Metal-Oxide-Metal (MOM) capacitor, which is formed by inter-digitated fingers of metal layers. The drawback of the MOM capacitor is its large parasitic capacitance, which is equal for both top and bottom plates. Parasitics are large due to the use of metal layers close to the substrate, and are equal on both top and bottom plates due to the structure used as shown in Fig. 4.3(a). This MOM capacitor uses three metal layers: Metal-6 through Metal-8.

To reduce parasitics, a custom capacitor is designed as shown in Fig. 4.3(b). The custom capacitor employs only Metal-8 and Metal-9; these metals are further away from the substrate reducing the parasitic component. Furthermore, significant reduction in top plate parasitic is achieved by keeping the interdigitated structure only on the upper metal layer. The lower metal layer is a single metal sheet, with no interdigitation. The

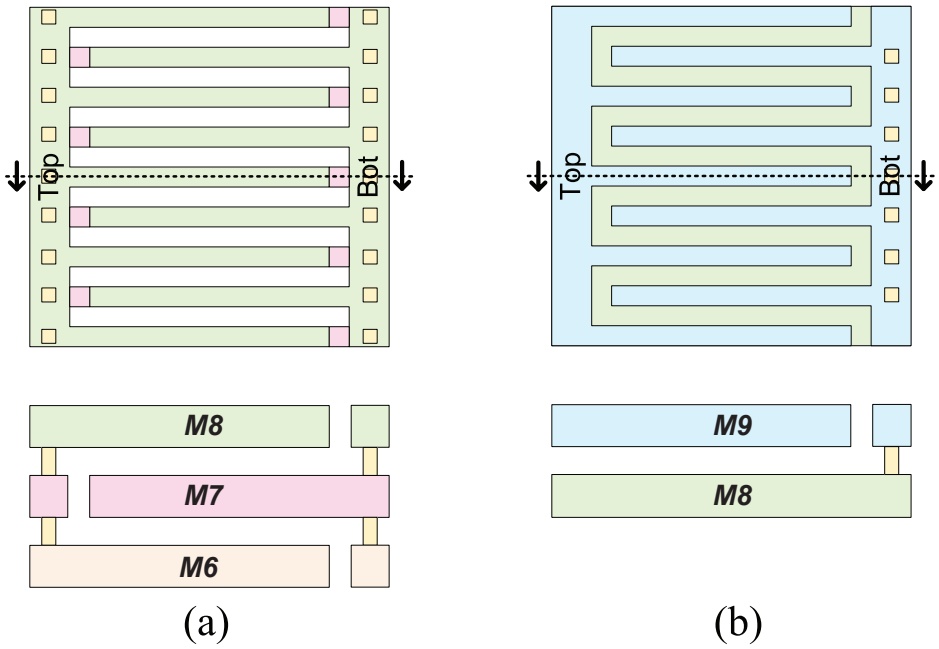

Figure 4.3: Capacitor structures (a) MOM-capacitor and (b) Custom Capacitor

capacitor's top plate thus has lower parasitics to ground than the bottom plate, since the bottom plate shields the top plate from the substrate. The drawback, however, is a lower capacitance density resulting in larger capacitor area for the same capacitor value. The two unit capacitors (15fF and 3fF) are designed and simulated using 3D electromagnetic simulation through Integrand's EMX® EM-simulation tool [36].

The tail transformer is designed as a two-turn symmetric inductor with a ground connection at the center tap, as shown in Fig. 4.4. Due to the physical layout constraints, relatively long leads have to be used. The whole structure (transformer + leads) is EM-simulated, and is designed such that it resonates with the capacitance at the common sources of each of the two oscillators forming the QVCO (CS1 and CS2 nodes), with the resonance occurring at double the oscillation frequency [49].

The tank inductor is a symmetrical single-turn inductor with a differential capacitance of 60pH. Due to the large size of the capacitor bank (caused by both large capacitor

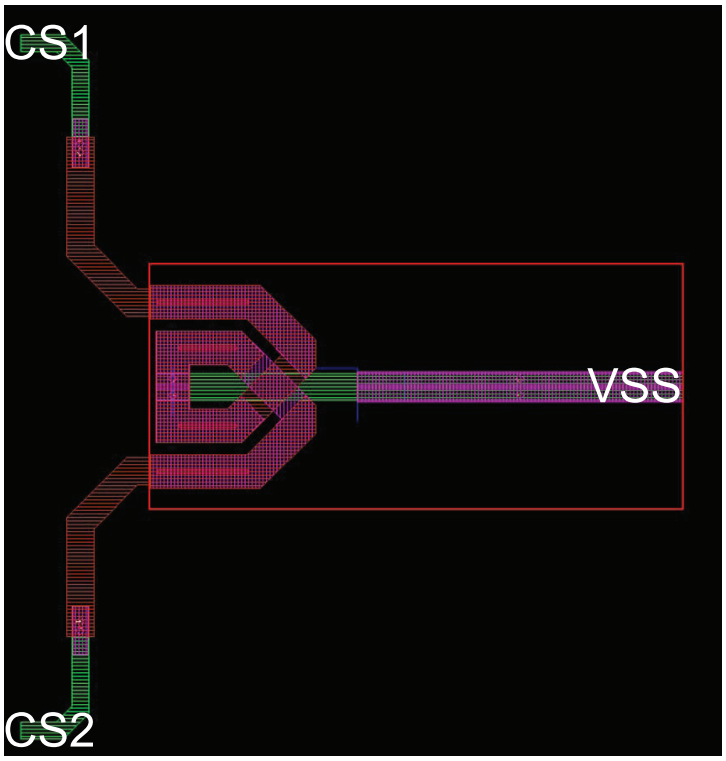

Figure 4.4: Tail transformer layout

areas, and a large number of bits), the interconnects add significant inductance. Hence, the tank inductance and the capacitor array are EM-simulated as a single structure to ensure the most accurate results. The full layout of the QVCO is shown in Fig. 4.5. The g_m-cell for each VCO is placed as close as possible to the tank inductor. Smaller capacitors are placed closer to the g_m-cell, and the larger capacitors are placed further away. This improves the tuning range by keeping the "effective" capacitance of the smaller capacitors in the capacitor bank almost unchanged (small lead inductance), while increasing the "effective" capacitance of the larger ones [73].

The QVCO is buffered using 50Ω buffers, and the I and Q outputs are downconverted using mixers with an external input. The 50Ω buffers are made up of the same tank as the QVCO, with only coarse tuning retained. A cascoded g_m-cell is used at the

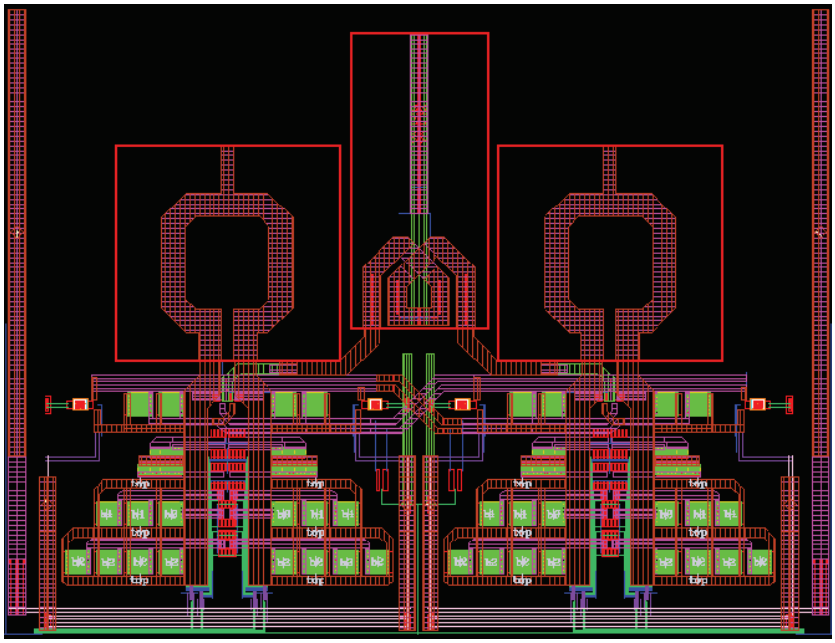

Figure 4.5: Full layout of the proposed QVCO

input, and a differential 100Ω resistor is used for 50Ω matching. The buffer outputs are connected to GSSG probes for on-chip probing. A GSG pad is used for providing the external input. The block diagram of the entire system (QVCO+buffer+mixers) is shown in Fig. 4.6.

The QVCO is simulated with full EM-extraction of the tank structure, as well as the tail transformer. A supply of 1V is used, with 600mV of gate-bias. The frequency of the QVCO versus the tuning word is shown in Fig. 4.7. With 3-bits of coarse tuning, eight different tuning "bands" can be distinctively identified. Within each band, eight different discrete frequencies can be observed corresponding to the 3-bits of fine tuning. The QVCO can be tuned in 63 discrete tuning steps, ranging from 53.84GHz to 73.59GHz with a maximum frequency step size of around 700MHz. *The QVCO has thus 19.75GHz of frequency range, with a center frequency of 63.72GHz corresponding to an FTR of 31%.* This frequency range covers the 57-66GHz band with ample room

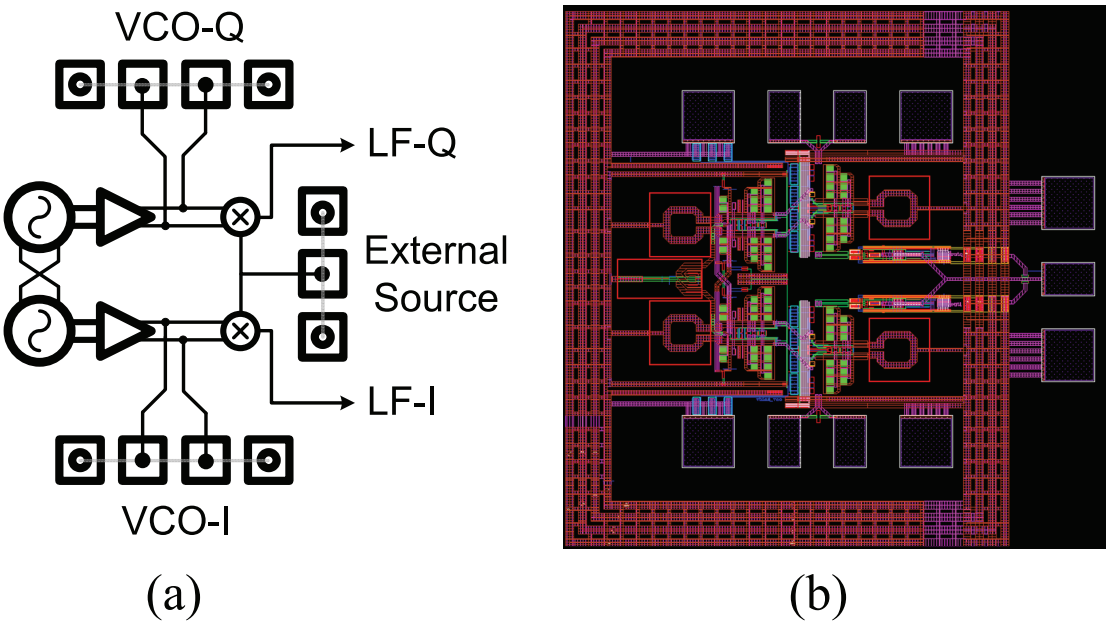

Figure 4.6: Entire system (a) Block Diagram, and (b) Layout

for process shifts. With a little shift in frequency (for instance via reducing the tank inductance), it can be made to cover the 71-76GHz E-band as well.

The power consumption of the proposed QVCO versus tuning word is shown in Fig. 4.8. The power consumption ranges from 23mW at the highest frequency, to around 29mW at the lowest frequency.

The phase-noise performance of the QVCO is also shown in Fig. 4.9, at 1MHz and 10MHz offsets from the carrier. The phase-noise at 1MHz offset is comparable to the state-of-the-art performance in [48, 55, 69–71]. Except for [71], the QVCO's which have significantly better phase-noise have relatively low tuning ranges (maximum of 16.6%) which allows for better phase-noise optimization. In [71], phase-noise at similar frequencies is very close to this work. Better phase-noise numbers are achieved at lower frequencies, as the design in [71] extends over the lower frequency range of 48.8-62.3GHz. It is also to be noted that the phase-noise value at 10MHz offset in Fig. 4.9 is almost

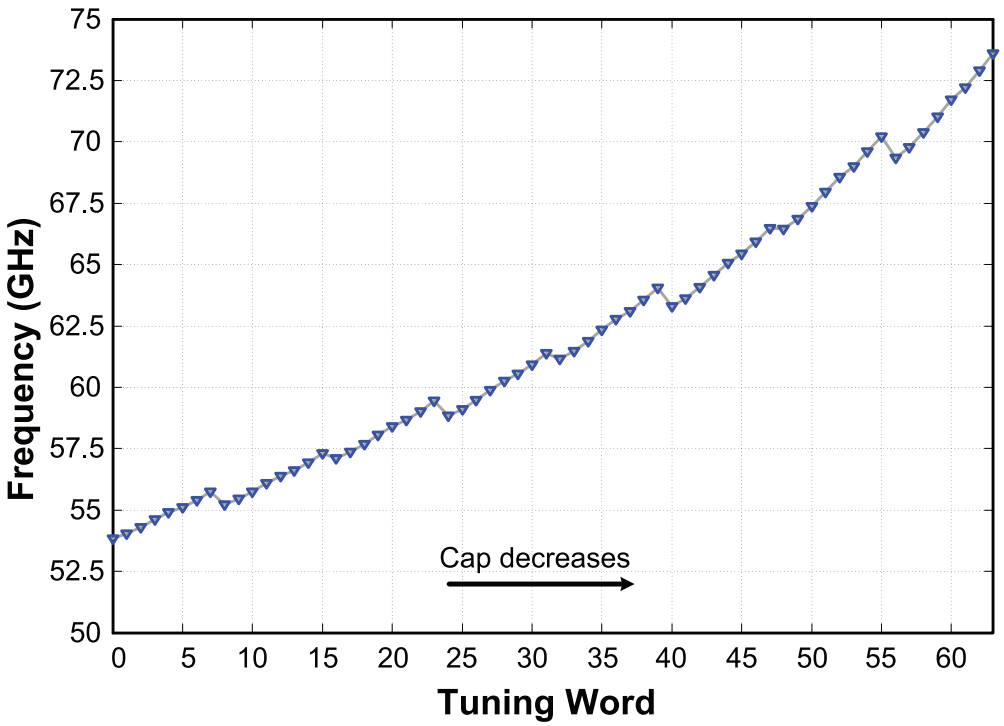

Figure 4.7: Output frequency of the proposed QVCO versus tuning word

30dB lower than the value at 1MHz offset, indicating a $\frac{1}{f^3}$ noise profile. This can be attributed to the relatively small transistor sizes used in the g_m-cell.

The figure of merit (FOM) of the QVCO, for phase-noise at 1MHz and 10MHz offsets, is shown in Fig. 4.10. At 1MHz offset, the FOM ranges from 165 to 173 dBc/Hz. While the 173dBc/Hz FOM benchmark is lower than (or equal to) the FOM achieved in [48,55,69–71], the achieved 19.75GHz tuning range (and the corresponding 31% FTR) is larger resulting in an FOMT of 183dBc/Hz which is at par with state-of-the-art. The 10MHz offset FOM ranges from 176dBc/Hz to 180dBc/Hz, with a corresponding FOMT of 190dBc/Hz.

Table 4.1 shows a performance comparison of this work with state-of-the-art millimeter-wave QVCO designs. Amongst the designs presented in this comparison, the QVCO proposed in this work achieves the highest center frequency, and the highest tuning

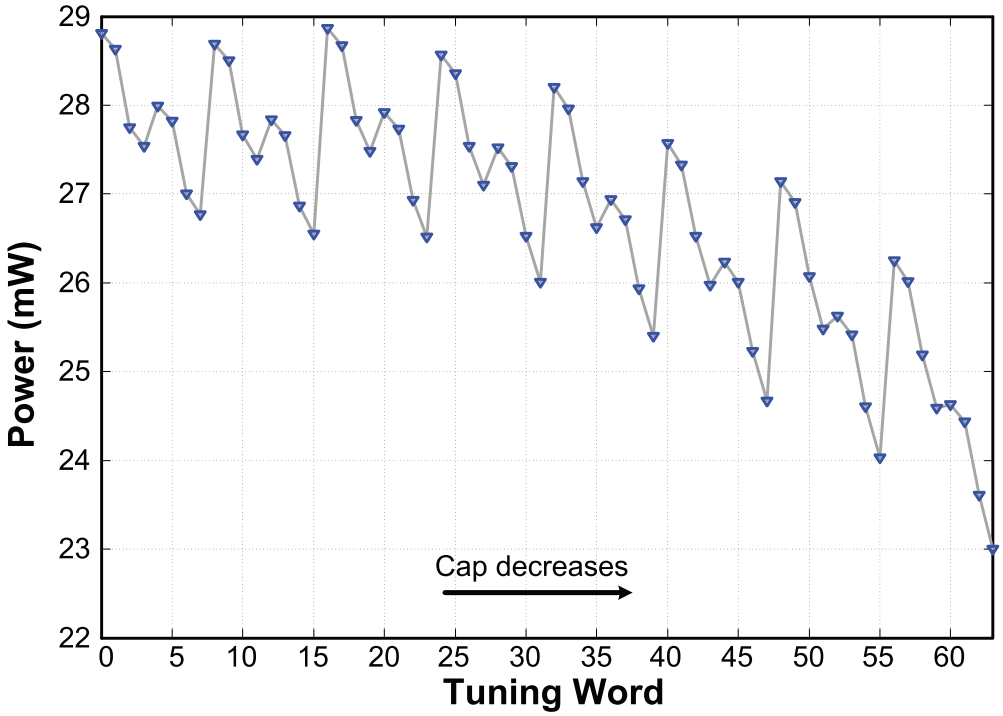

Figure 4.8: Power consumption of the proposed QVCO versus tuning word

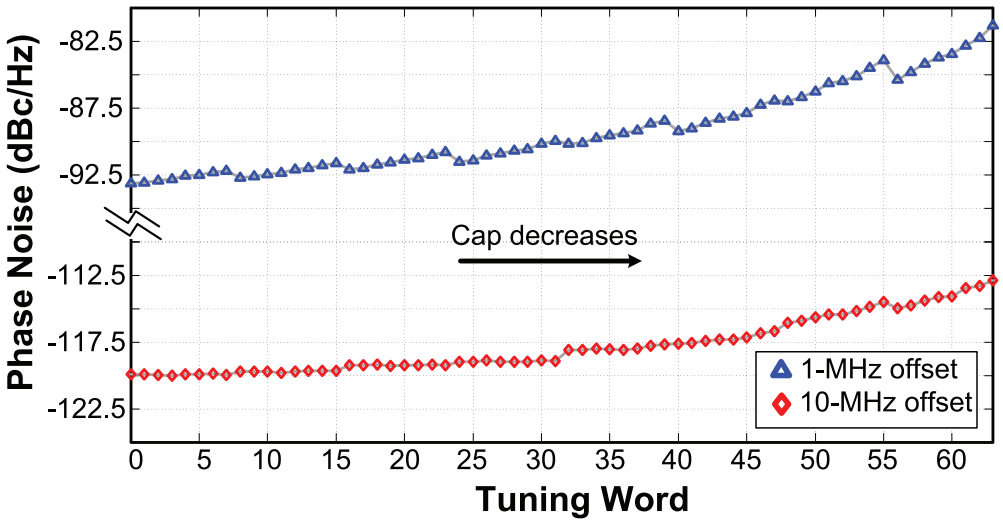

Figure 4.9: Phase-noise of the proposed QVCO

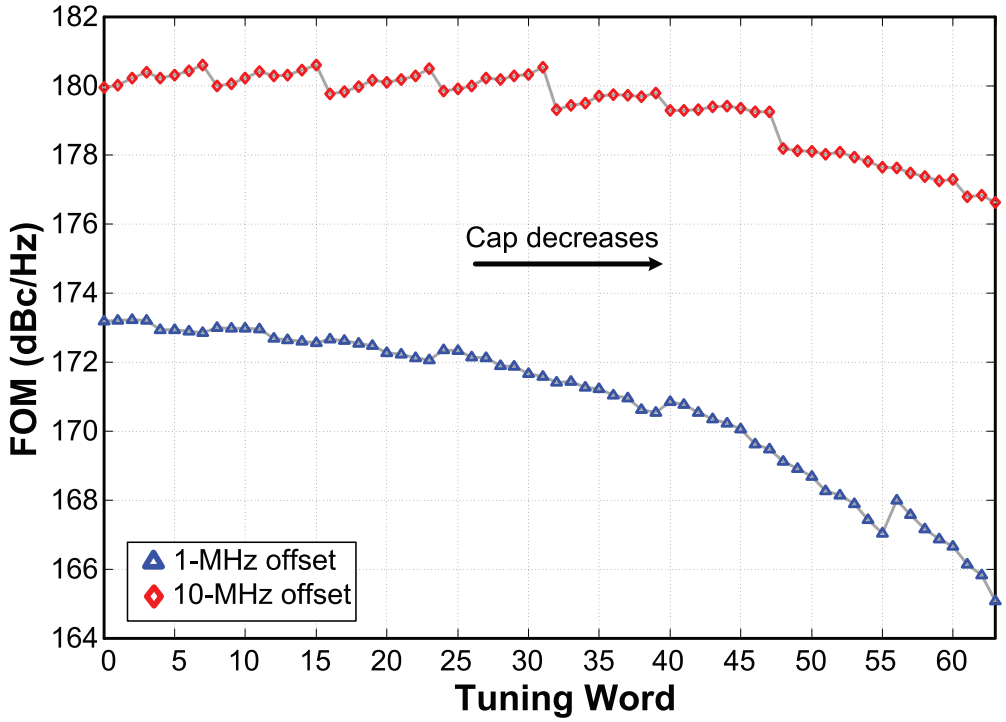

Figure 4.10: Figure of merit of the proposed QVCO

Table 4.1: Performance Comparison

Ref	f_o (GHz)	FTR	PN(dBc/Hz)	FOM(dBc/Hz)	FOMT(dBc/Hz)	Power (mW)
[48]	63.1	16.6%	-95	179	184	11.4
[55]	58.2	7.5%	-97	179	177	22
[71]	55.5	24.3%	-94	176	184	15.6-30
This Work	63.7	31%	-92.5	173	183	23-29

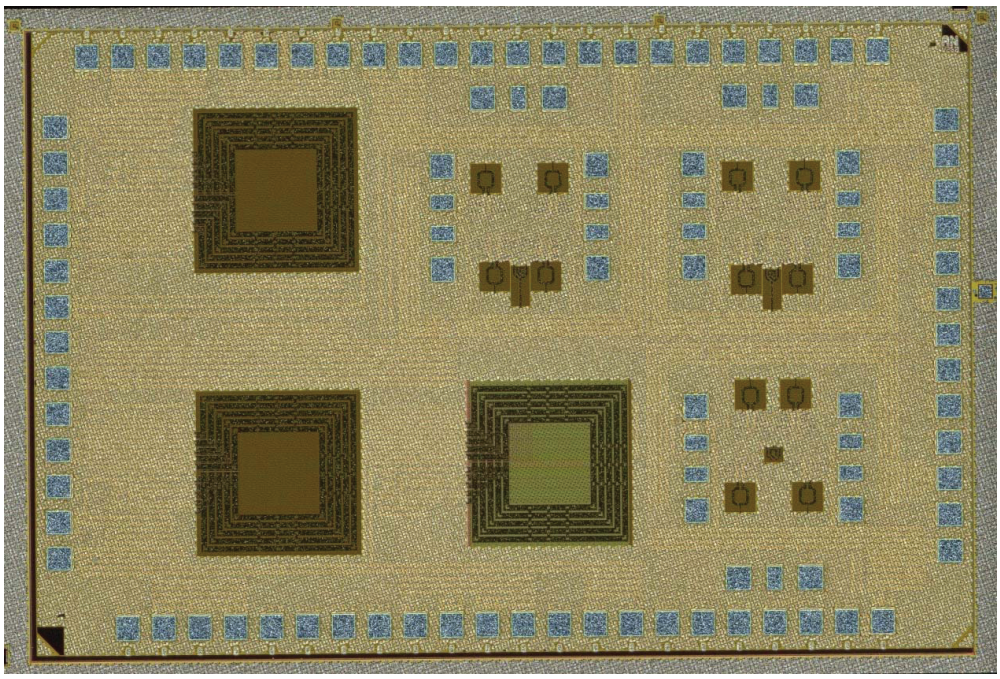

Figure 4.11: Chip micrograph

range (in absolute and relative terms) while achieving competitive phase-noise, FOM and FOMT numbers. Moreover, the presented design is the only one that covers the entire 57-66GHz band, while also covering a considerable part of the 71-76GHz E-band. In fact, with modification of the tank inductance the proposed QVCO can be made to simultaneously cover the whole 57-66GHz, as well as the whole 71-76GHz E-band, a feature not achieved by the other presented work.

4.3.2 Measurements

The micrograph of the fabricated chip is shown in Fig. 4.11. The three large inductors are *not* a part of the design. Three different prototypes of the QVCO were placed on chip, two with 6-bits of tuning and different placement of the g_m-cell, and a third one with only 3-bits of coarse tuning.

Although the three designs were simulated using full 3D EM-simulation, neither of the oscillators started up in actual measurements. The most likely reason is the lack of RF models in this specific process; the SOI process files available were mostly tailored for a digital/mixed-signal design flow. These lacked the essential modeling to account for the high-frequency non-quasistatic effects that would limit the performance at millimeter wave frequency. No capability was present to generate the high frequency models from measurements, and hence, the process files provided by the fab were used. Moreover, unexpected metal fill was performed by the fab on the top-most metal layer in the chip; this is a metal layer that is higher than the actual top-most metal used in the design. The effects of this metal fill had not been taken into account in the actual design (they mostly lead to increased loss and reduced quality factor).

Chapter 5

Research Contributions & Future Work

In this thesis, the following contributions are made:

- A flexible injection-locking based LO generation scheme, with quadrature outputs, for frequency-channelized transceivers. The scheme results in smaller number of harmonics than SSB implementations. It also allows small frequency separations at higher center frequencies, making it well-suited for mm-wave operation. Design, and implementation, of the scheme is discussed. Phase-noise and spurious performances are also analyzed.

- A robust coupling scheme for a QVCO is presented. The complimentary-coupling scheme is well suited for the lower supplies of scaled sub-micron technologies. It also allows better (lower) phase-noise, without the need for reducing the size of the coupling transistors. Moreover, the coupling scheme does not employ frequency-sensitive coupling networks, making it a good candidate for wide-tuning-range applications. Design, and implementation, of the suggested scheme is discussed.

The phase-noise advantage, compared to conventional coupling, is explained and verified.

- A wide tuning-range mm-Wave QVCO which combines two coupling schemes, together with custom-designed metal capacitors and inductors, to achieve the 31% tuning range at 63.7GHz center frequency. The achieved tuning range allows the QVCO to span multiple mm-wave bands, opening the possibility for a mm-wave SDR receiver.

5.1 Future Work

With the quest for software-defined-radio, frequency channelization holds the potential of realizing a system that is as close as possible to Mitola's architecture [10]. The major premise of Mitola's architecture is implementing an ADC with a bandwidth wide enough to accomodate the entire RF bands of interest. With current technology, direct implementation of such an ADC is an impossible feat. Nevertheless, proper extension of frequency channelization schemes can potentially achieve an affordable realization of the SDR. This venue of research includes finding the proper bandwidth to strike a balance between the overhead of the extra RF power needed for channelization and the total power consumption of the reduced sampling rate ADCs. Significant research is also required for multiple, simultaneous LO and clock generation schemes for channelization, as well as the potential issues of cross-talk and frequency pulling resulting from implementing multiple LOs on the same chip.

While frequency-channelization can bring the far-fetched Mitola's architecture closer to reality, the current approach to SDR involves relatively smaller instantaneous bandwidths transcievers, with tunable LOs. Pertinent to this SDR realization is the use of wide-tuning range QVCOs [11]. The ideas and schemes presented in this work can be

built upon to enable robust quadrature LO generation, with the wider tuning ranges enabling a smaller number of QVCOs hence reducing the area requirements as well as the design and calibration complexity. Furthermore, mm-Wave SDR design remains an unexplored territory, and wide-tuning range mm-Wave QVCO's can present a starting point for such research, further extending the possible scope of applications of SDR.

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