

CHARACTERIZATION OF STREPTAVIDIN-  
SEMICONDUCTOR INTERFACES FOR THE DEVELOPMENT  
OF A BIOSENSOR

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# **CONTENTS**

## **1 MOSFET**

- 1.1 Development of Field Effect Transistor **3**
- 1.2 MOS Capacitor **4**
- 1.3 MOSFET Operation **6**

## **2 MODIFIED MOSFET**

- 2.1 Idealized Sensor Characteristics **10**
- 2.2 Ambient-Oxide Interface Sensing **11**
- 2.3 Surface Interface Challenges in Modified FET **11**
  - 2.3.1 Oxide Interface Properties **12**
  - 2.3.2 Reduction of Electrical Drift **14**
  - 2.3.3 Device Packaging **15**
- 2.4 ISFET **15**
- 2.5 BioFET **17**

## **3 DEVICE PROCESSING TECHNIQUE**

- 3.1 Overview of MOS Device Fabrication **18**
- 3.2 MOSFET Fabrication **18**
  - 3.2.1 Mask Creation **19**
  - 3.2.2 Wafer Cleaning and Preparation **22**
  - 3.2.3 Field Oxide Growth **23**
  - 3.2.4 Photolithography **23**
  - 3.2.5 Source and Drain Diffusions **25**
  - 3.2.6 Gate Oxide Growth **25**
  - 3.2.7 Aluminum Evaporation and Contact Formation **26**
- 3.3 Device Insulation **27**

## **4 BIOFET**

- 4.1 Introduction **28**
- 4.2 Experimental Methods and Techniques **29**
- 4.3 Experimental Results **30**
- 4.4 Experimental Analysis **33**
- 4.5 Conclusions **34**

## **WORKS CITED 35**

## **LIST OF FIGURES AND EQUATIONS**

Figure 1.1	Inversion layer resulting from field effect	3
Figure 1.2	Surface Charge Density vs. Surface Potential	5
Figure 1.3	Equilibrium MOS Interface	5
Figure 1.4	Inversion at MOS Interface	6
Figure 1.5	Cross section of MOSFET	6
Figure 1.6	Band Diagram for n-channel MOSFET	7
Figure 1.7	MOSFET I-V relationship	7
Equation 1.1	Source-Drain Current in Linear Region	8
Equation 1.2	Source-Drain Current in Saturation Region	8
Figure 1.8	Discrete Circuit Model of MOSFET	9
Equation 2.1	Theshold Voltage	12
Figure 2.1	Molecular SiO <sub>2</sub> --Ideal and Non-ideal Structures	13
Figure 2.2	SiO <sub>2</sub> interface with adsorbed protons and hydroxides	14
Figure 3.1	Overlay of the four-step mask layout for a single die	20
Figure 3.2	Devices and test structures in center region of die	21
Figure 3.3	Wet bench for wafer cleaning	22
Figure 3.4	Furnace tubes for performing wafer oxidation and diffusion	23
Figure 3.5	Step by step photolithography process for oxide etching	24
Figure 3.6	Silicon orientation and oxidation specific prefactors	25
Equation 3.1	Arrhenius equation	25
Equation 3.2	Deal Grove Model	26
Equation 3.3	Deal Grove Model Correction for Dry Oxidation	26
Figure 3.7	Final MOSFET, following aluminum contact definition	27
Figure 4.1	FET 4 BSA Receptor	30
Figure 4.2	FET 5 BSA Receptor	30
Figure 4.3	FET 6 BSA Receptor	31
Figure 4.4	FET 4 Streptavidin Receptor	31
Figure 4.5	FET 5 Streptavidin Receptor	32
Figure 4.6	FET 6 Streptavidin Receptor	32
Figure 4.7	Device channel geometries	33
Equation 4.1	Change in charge over gate area	34
Figure 4.8	Charges per molecule at pH 7.4	34

## Chapter 1 MOSFET

### 1.1 Development of Field Effect Transistor

A capacitor forms when two conducting bodies, regardless of shape and size, are separated by an insulated (dielectric) medium. When a bias is applied across the conductors charge of equal and opposite polarity is transferred to the surfaces of the conductors. Electrostatic fields result from this distribution of charge across the parallel plates.

Brattain, Bardeen, and Shockley used this concept, along with their knowledge of semiconductors, to demonstrate the field effect in an electronic device now known as the transistor. They believed that a metal plate and a semiconductor substrate could act as the opposing plates of a parallel capacitor. It was believed that the field effect resulting from the charged metal plate would cause charge from the semiconductor bulk to be drawn to the surface of the material, resulting in a depleted region within the semiconductor.

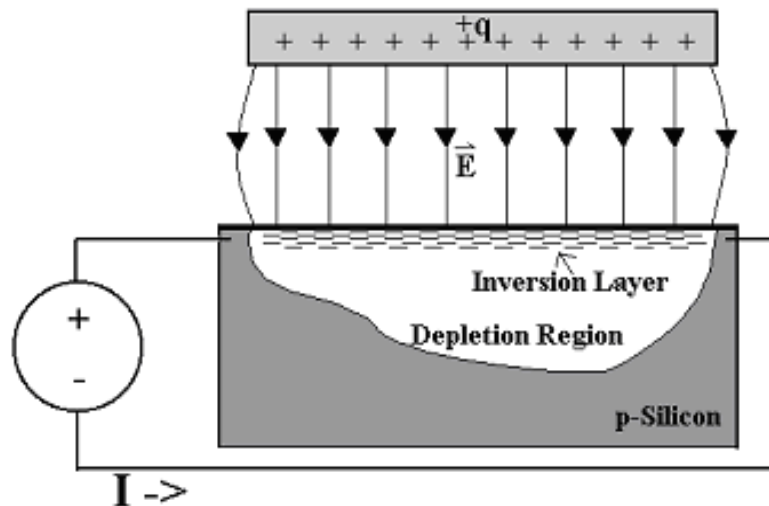


Figure 1.1 Inversion Layer resulting from field effect

Their attempts to demonstrate the FET experimentally in 1948 led to the serendipitous discovery of the bipolar junction transistor (BJT). At this time, the quality of

semiconductor processing techniques and attention to important surface properties were underdeveloped and prevented the further development of the FET for several decades. Despite their shortcomings in the development of a successful FET, their ideas set the groundwork for further development. After the problem of surface states was resolved by growing an oxide insulator on Si, the first metal-oxide-semiconductor FET (MOSFET) was successfully demonstrated in 1960 by Kahng and Atalla. This MOSFET was founded on the field effect concept first proposed by Shockley, where the conduction was controlled with the MOS capacitor.

## **1.2 MOS Capacitor**

Charge above the insulating oxide interface causes an equal and opposite amount of charge to be drawn from the bulk of the semiconductor to the semiconductor/oxide interface. This distribution of charge at the interface causes band bending within the semiconductor. The band structure of the semiconductor near the semiconductor-oxide interface would bend proportionally to the potential of the metal, resulting in the accumulation or depletion of charge carriers at the interface. The potential of the metal, which is described as the surface potential when seen from the semiconductor side, results in a variable charge density at the semiconductor/oxide interface. Figure 1.2 shows the surface charge density as a function of the surface potential.

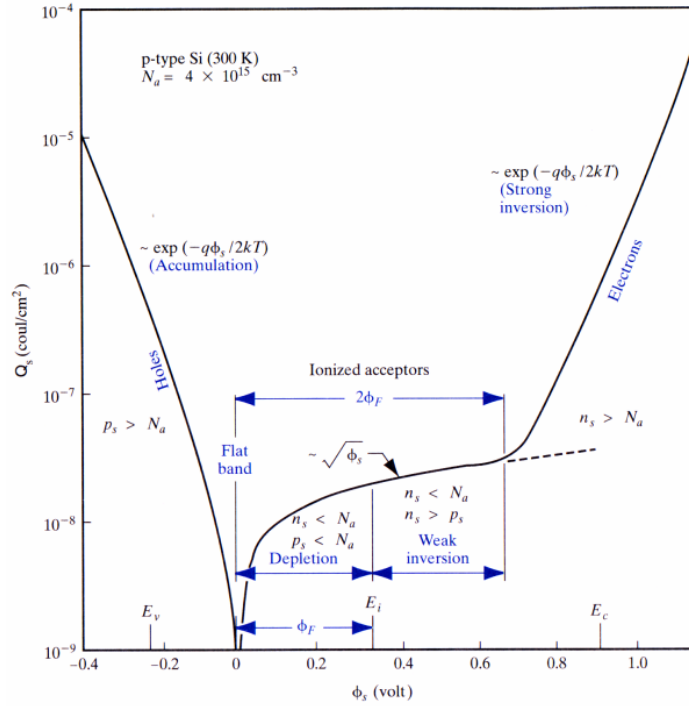


Figure 1.2 Surface Charge Density vs. Surface Potential [Streetman]

When the applied potential exceeds twice the flatband potential, the Fermi level exceeds the intrinsic level near the interface, resulting in the development of an inverted charge layer commonly known as the inversion layer. The inversion layer, as the name suggests, exhibits charge properties which were inverted relative to the equilibrium properties of the semiconductor. The band levels at equilibrium and inversion are shown below.

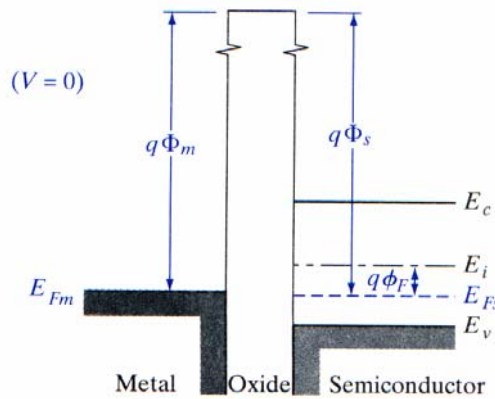


Figure 1.3 Equilibrium MOS Interface

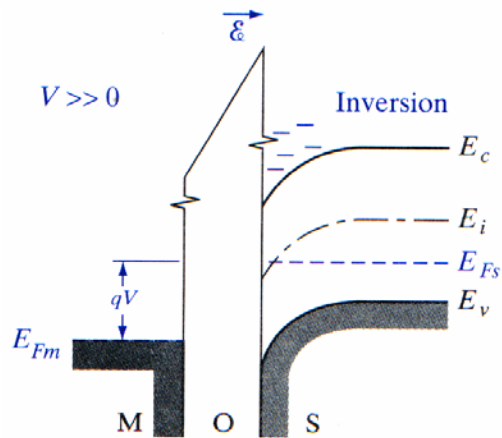


Figure 1.4 Inversion at MOS Interface

### 1.3 MOSFET Operation

The MOSFET is essentially a transistor, or controllable switch, that is controlled by field effects. The MOSFET is a three terminal device based on the MOS capacitor, where the charge collected at the semiconductor/oxide interface of the MOS capacitor serves as a channel for current flow between the source and drain. The current that flows from source to drain is controlled by the charge present on the metal gate. The MOSFET, while maintaining the three terminal setup originally displayed by the bipolar junction transistor (BJT), displays many favorable features, such as non-parasitic electrical behavior in circuits, high input impedance, and stable operating characteristics.

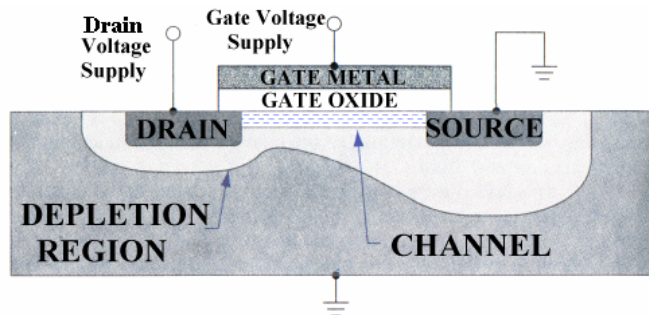


Figure 1.5 Cross section of MOSFET

The electron band diagram given in Figure 1.6 illustrates the MOSFET design further. With n-channel MOSFET, the n-type nature arises from the inversion layer formed from the gate potential. This n-type inversion layer, which forms over the channel of the MOSFET, can be seen as the lowering of the band in the channel region. This flattening of the conduction band between source and drain results in a decreased resistance of electron flow, or increased conduction.

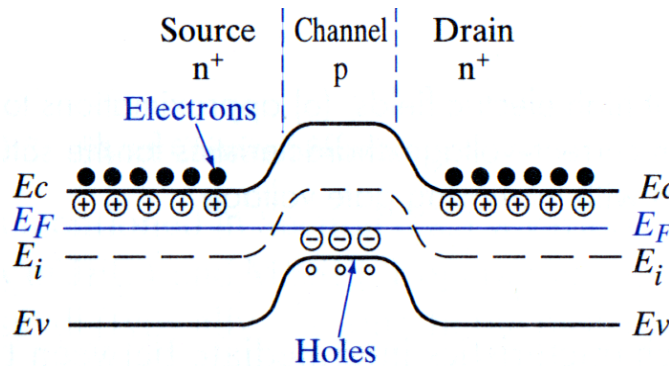


Figure 1.6 Band Diagram for n-channel MOSFET

The current-voltage (I-V) relationship for MOSFETs is described by Figure 1.7. Notice that the four curves correspond to four separate gate voltages. The linear regime of operation is described by the portions of the curve that exist before the pinch-off the channel. Once pinch-off occurs, the MOSFET is in the saturation regime. The current equations for the linear and saturation regime are described in Equations 1.1 and 1.2, respectively.

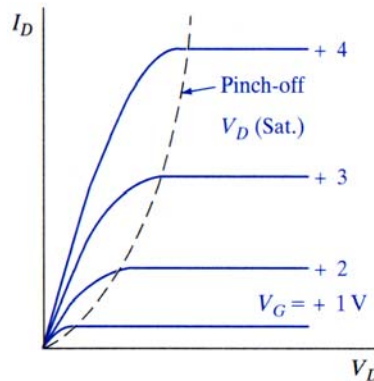


Figure 1.7 MOSFET I-V relationship



The resulting current-voltage (I-V) properties of the device are given by the I-V curves above. The four curves each correspond to a different applied gate voltage. The portion of the curves that exist before the pinch-off of the channel, describe the device operation in the linear regime. While the onset of saturation regime operation begins once pinch-off is achieved. The mathematical equations describing these two operation regimes are given by:

$$I_{DS \text{ linear}} = \left( \frac{\mu Z C_i}{L} \right) \left[ (V_g - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad \text{Equation 1.1}$$

$$I_{DS \text{ saturation}} = \left( \frac{\mu Z C_i}{2 L} \right) \left[ (V_g - V_t)^2 \right] \quad \text{Equation 1.2}$$

where

$V_g$  = Gate voltage (volts)

$V_t$  = Threshold voltage (volts)

$V_{ds}$  = Drain to source voltage (volts)

$\mu$  = Surface electron mobility ( $\text{cm}^2/\text{V-s}$ )

$C_i$  = Insulator capacitance ( $\text{F}/\text{cm}^2$ )

$Z$  = Width of the channel (cm)

$L$  = Length of the channel (cm)

The MOSFET can be represented as a discrete circuit model with capacitive and resistive components as shown in Figure 1.8. Notice the current source is controlled by the gate voltage. In a common-source configuration, the source and the substrate contacts are at the same potential. The substrate contact is required to maintain proper bias of the bulk substrate, which allows for the formation of a repeatable depletion width. Without a substrate contact the depletion width would become variable and can affect the charge at the semiconductor/oxide interface and, subsequently, the current flowing from source to drain.

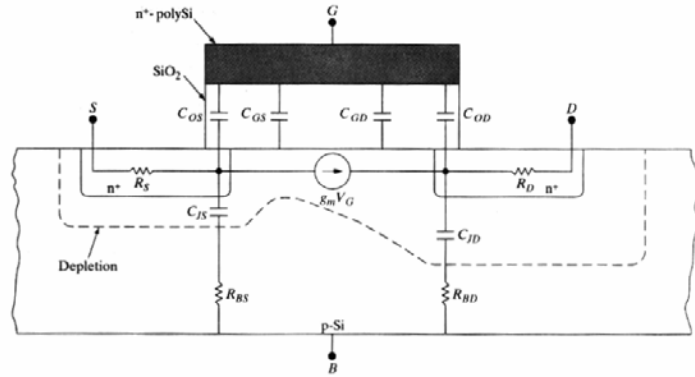


Figure 1.8 Discrete Circuit Model of MOSFET

It is important to remember that control of this device is done so through the charge applied across the metal/oxide interface, which thus changes the surface potential of the semiconductor. Referring back to Figure 1.2, which describes the surface charge density as a function of surface potential, it can be seen that small amounts of charge on the gate metal, with space charge densities of  $10^{-7}$  coulombs, can lead to observable changes in the operating characteristics. From this observation we derive the notion of the MOSFET serving as a biological or chemical sensor platform.

## **2 MODIFIED MOSFET**

### **2.1 Idealized Sensor Characteristics**

The MOSFET platform offers many characteristics that are ideal for sensing applications. The MOSFET is a well-characterized device which has stable operation. As mentioned in the previous section, the MOSFET is highly sensitive to charge present on the gate. Lastly, modern processing techniques have allowed for these devices to be relatively inexpensive (when considered on a per device basis).

The stability of the MOSFET is exemplified by its ability to operate over a wide range of temperatures, thus allowing it to be used for sensing in temperature ranges common to biological environments. Furthermore, the MOSFET has no moving parts, which allows for consistent operating parameters that do not change with time. The semiconductor industry has demonstrated the repeatable production of these devices. The mass production of MOSFETs allows for small and inexpensive sensor platforms.

The MOSFET, with its built in transducer-like functionality and amplification, allows for high sensitivity and a moderate dynamic range. With surface charge densities on the range of  $10^{-9}$  to  $10^{-5}$  C/cm<sup>2</sup> present over an area of  $10^{-4}$  cm<sup>2</sup>, the drain-source current for a MOSFET can vary between 0 to 1000 microamperes. The MOSFET can provide a sufficiently large current output such that it can be provided directly to other devices. In other words, the output signal is only (and proportionally) amplified by the presence of charge at the gate.

Selectivity is a critical sensor parameter which must be addressed with the MOSFET. In order for the MOSFET to respond to charge on the gate region, special surface preparations must be made to allow for the detection of a specific sensing target. From the selectivity of surface components that promote (or prohibit) charge transfer, the MOSFET can become selective. The long-term challenge that needs to be addressed is how to promote the selective sensing at the gate oxide interface.

## **2.2 Ambient-Oxide Interface Sensing**

The MOSFET is controlled by the electric potential applied to the metal electrode of the MOS junction/capacitor. In order to achieve sensor functionality, the MOSFET must be modified to allow other charges to access the metal side of the metal-oxide junction. This can be achieved by removing the metal gate electrode, which forms an ambient-oxide interface. Charge can come in direct contact with the gate oxide to allow for charge collection at the semiconductor/oxide interface. The charge present on the ambient-oxide interface can be calculated from the source/drain currents measured from the FET. Thus, we need to give much consideration to the ambient-oxide interface since sensing functionality is based upon interactions occurring at this surface. This is the fundamental idea for using the modified FET for sensing applications.

The charge that forms in the semiconductor as a result of charge at the ambient oxide interface is affected by the physical and chemical state of the oxide interface. The oxide interface can have charged species which provide a shielding (canceling) effect to the perceived charge in the ambient-oxide interface. As a result, the physical and chemical preparation of the semiconductor interface will have a significant impact on determining the sensor's capabilities and present challenges in the development of modified FETs.

## **2.3 Surface Interface Challenges in Modified FETs**

Many of the benefits which are inherent to the MOSFET sensor platform come at a high price and create immense challenges for the creation of a workable biological/chemical sensor. As D.M. Wilson stated, "FETs, of course, can be fabricated in standard CMOS and other microfabrication processes and conversion of the electronic FET to an effective chemical sensor requires, in theory, only replacement of the gate with a suitable chemically sensitive material. The impact of the environment, materials compatibility, and other fabrication issues, however, make the integration of the CHEMFET with standard FET architectures significantly more complicated than the theory and has

generated a broad range of CHEMFET architectures and design methodologies directed at solving practical, portable chemical sensing problems.” [5] The challenges that arise are often as unique as the invention itself; however, there are common challenges in the FET-based sensor design which include the following: control of the oxide interface properties, elimination of electrical drift and noise due to environmental factors, the characterization techniques which can be used, and device isolation and packaging. These challenges will be discussed in the following paragraphs.

### 2.3.1 Oxide Interface Properties

The oxide interface properties are critical in device fabrication. Interface states that exist between the oxide and semiconductor can prove damaging to a device’s performance. Interface states arise from additional charges that may originate from a variety of sources which include contamination from mobile ions, such as sodium ions in the oxide layer. Charges trapped in the oxide layer can also be due to impurities that existed during formation of the oxide. Localized states caused by trapped charge can also result from imperfections in the semiconductor interface or interface states which exist due to chemical reactions at the interface, such as of dopant atom constituents from the semiconductor, or adsorbate specific local chemical bonding. [1] These charges can accumulate at the oxide-semiconductor interface and have significant effects on the threshold voltage of the FET. The threshold voltage signifies the enable point and is associated with the onset of strong inversion operation. [2] A more accurate definition of the threshold voltage is shown in Equation 2.1

$$V_t = 2\phi_F + \phi_{MS} - (Q_f + Q_{ot} + Q_m + Q_{b \max}) / C_o \quad \text{Equation 2.1}$$

where

$\phi_F$  = Fermi level to Intrinsic Level offset (volts)

$\phi_{MS}$  = Metal-Semiconductor Work Function (volts)

$Q_f$  = Oxide fixed charge (C/cm<sup>2</sup>)

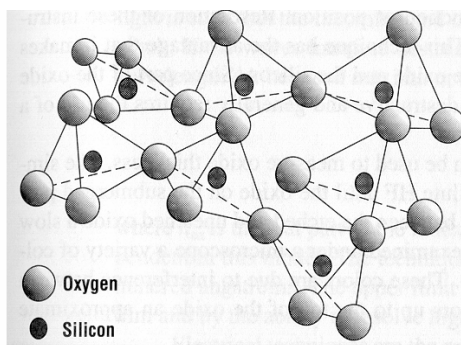
$Q_{ot}$  = Oxide trapped charge (C/cm<sup>2</sup>)

$Q_m$  = Mobile Ionic charge (C/cm<sup>2</sup>)

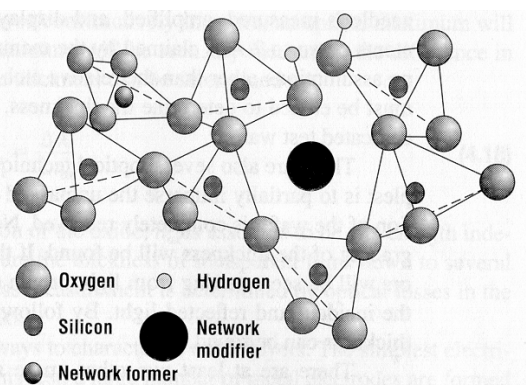
$Q_{b \max}$  = Bound Charge in the depletion region (C/cm<sup>2</sup>)

$C_o$  = Accumulation Capacitance (Farads/ cm)

Modern processing techniques have allowed for low trapped charge densities on the order of  $10^{10}$  charges/cm<sup>2</sup> .[9] Despite such low values, these charges act as a charge sink, which essentially means that more charge is required on the ambient-oxide interface in order for it to be sensed. Imperfections, such as dangling charges, can also have an impact at the ambient-oxide interface. Dangling H<sup>+</sup> and OH<sup>-</sup> bonds can exist at the interface where the chemistry of interest occurs. Such bonding imperfection arise for several reasons. Excess water (or other impurities) during oxide growth can cause dangling hydrogen bonds. Chemical processing (etching) during fabrication can cause OH<sup>-</sup> to form on the oxide surface. Dangling bonds such as these can severely affect device operation as they reduce the effective charge being detected and thus lower the device sensitivity. Furthermore, such dangling bonds can serve as a collection spot for contaminants or other unwanted species.

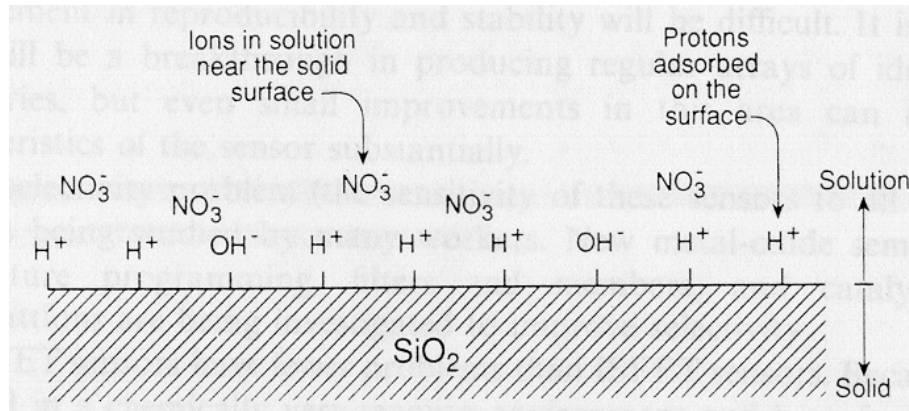


**Figure 4.7** The physical structure of SiO<sub>2</sub> consists of silicon atoms sitting at the center of oxygen polyhedra.



**Figure 4.8** Schematic of impurities and imperfections in SiO<sub>2</sub>.

**Figure 2.1:** Molecular SiO<sub>2</sub>--Ideal and Non-ideal Structures.



**Figure 2.2:**  $\text{SiO}_2$  interface with adsorbed protons and hydroxides

As a result of the ambient-oxide interface, the oxide is susceptible to hydration found in the ambient environment or solutions. Such hydration encourages oxide growth, which changes oxide thickness and the associated device capacitance. As a result, the device operating characteristics, like the threshold voltage, can alter through operation. A popular solution used to prevent further insulator growth and to make the surface more chemically stable would be to apply an over-layer of  $\text{Si}_3\text{N}_4$ . Further work needs to be done in order to fully characterize the performance of such insulator covering layers.

### 2.3.2 Reduction of Electrical Drift

Development of portable sensor structures based on the FET requires the reduction of electrical drift and noise due to environmental factors. The collection of contaminant particles by the oxide surface is undesired and represent a large challenge for such sensors. Charged dust particles or even chemically similar substances to the sensor's target particle can bond to the surface and cause a faulty detection. Isolation from contaminants is hard to achieve in most environments outside the cleanroom, and failure to do so will lead to the degradation in device performance. Furthermore, electrical drift becomes a problem due to semiconductor device's inherent dependence on operating temperature. It would be very challenging to adjust sensor readings in a way that takes temperature into account.

### **2.3.3 Device Packaging**

Device isolation and packaging is critical to realizing modified FETs in portable sensing applications. The source and drain metallization must be isolated in order to ensure stable device performance. Without proper isolation the electrical operation or user's safety may be compromised. The packaging must also provide chemical isolation of the sensor's components, which can be achieved with different dielectric overlayers. Optical isolation would prevent noise created from optically induced electron-hole pair formation. Temperature control would lead to predictable device performance. [4] Since an inexpensive polymer would be an ideal isolation layer for cheap, reusable sensors, there are a number of material integration questions that need to be addressed. From the standpoint of commercial applications, the packaging of these devices will be a significant part of design.

## **2.4 ISFET**

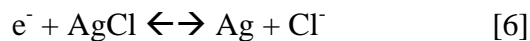
In 1970 Bergveld realized the value of the MOSFET structure as a sensor and proposed a modified MOSFET structure called the ion-sensitive FET (ISFET). Bergveld reasoned that free-charge over the gate dielectric could be used to control device operating properties. When this cause effect relationship was reversed, it was realized that output properties of the MOSFET could be used to characterize the ion-concentration, or pH, of a liquid. The ISFET was later incorporated in a broad category of FETs known as the CHEMFET. The CHEMFET could be used, in theory, to detect the presence of gasses or ionized liquids.

With the removal of the metal gate electrode and subsequent placement of ion-containing liquids over the gate region, a conductive channel could be induced between source and drain, allowing the device output to be controlled by the pH of a solution. The traditional substrate contact is replaced by a reference electrode in order to provide a reference. This reference electrode needs to be selected carefully based on the solution/ambient being sensed. In creating a high quality ISFET sensor, the selection of a reference electrode



material is critical. “A reference electrode is an electrode that accurately reflects the potential in the solution independent of changes in the dissolved species or in the pH of the solution.” [6] Two views currently exist on the fabrication and use of the electrode structure.

Using the more traditional ISFET design, the reference electrode should be freely exposed to the gas or liquid environment and made of a material which allows the electrode to associate with the solution of interest. For instance:



describes a classic chlorine gas sensor which requires a silver electrode in order to provide the current needed by the reference electrode for proper sensor operation.

The second philosophy for ISFET design incorporates the reference electrode as a chemically sensitive conductive gate material. This electrode supports a reduction/oxidization reaction which causes a difference in work function between the redox material and the conductive gate. [3] This idea is currently under development for a number of sensors because the geometry and placement of the conductive gate is in accordance to traditional planar processing.

Uncertainty surrounds the chemical reactions these devices attempt to perform. For example, the reaction of the palladium-gated hydrogen sensor is explained by two mechanisms. In the first mechanism, Pd migrates to the Pd/SiO<sub>2</sub> interface, which causes a dipole layer to form. The threshold voltage of the device, which is equivalent to modifying the amount of charge on the gate of the FET, is affected by the change in work function between Pd and SiO<sub>2</sub>. The second mechanism suggests that the work function difference is caused by a palladium hydride phase at the interface. Such uncertainties in the development of these sensors are due to the interface charge states which can be altered during the lifetime of the device and the time of reaction.

Reversibility in reaction is another issue as there is often a trade-off between a sensor being sensitive and reusable. The more sensitive chemical reactions available for use

here are not reversible. The ISFET is moderately stable, but suffers drawbacks due to ambient temperature affects and integrity of the insulating layer. Sensitivity of the ISFET is relatively high due to the field effect. Selectivity of the device, however, is considered to be moderate. For ion-sensing applications, the ISFET offers a relatively predictable and controllable reaction mechanism.

## **2.5. BioFET**

The union of transistor technology and biology provides a new and exciting alternative to conventional sensing devices. More specifically, the replacement of the metal gate on a field effect transistor (FET) with a film of biological receptors (BioFET) promises to improve the sensitivity and specificity of such devices. When the BioFET is in the presence of the agent to be detected, there is an ensuing chemical reaction that alters the net charge of the film that will affect the ability for current to flow from source to drain. The nature of this phenomenon is well understood. However, the properties of such protein-semiconductor interfaces have remained unexplored.

### **3 DEVICE PROCESSING TECHNIQUE**

#### **3.1 Cleanroom environment**

Microelectronic devices are very sensitive to contamination. Small quantities of unwanted material can lead to uncontrolled changes in device properties or even device failure. Semiconductor device fabrication occurs in a cleanroom environment in order to improve the yield, reliability, and integrity of results.

The cleanroom typically has extremely low-level particulate contamination. In MOS processing, devices are especially sensitive to human-introduced contamination such as sodium ions found in the breath or from oils and perspiration on the skin. Therefore special care will be taken prevent contamination of these types.

The cleanroom in which device fabrication will take place uses HEPA filtration to maintain specified particle standards. The cleanroom in which photolithography is performed is specified to be at least class 100. Other rooms are specified to be at least class 1000, while the service corridors are specified to be at least 10,000.

Human beings are a major source of contamination in the cleanroom. Suits and gloves are worn at all times in order to minimized particles released by the body. Also, tweezers will be used to handle wafers in order to further prevent contamination.

#### **3.2 MOSFET Fabrication**

The semiconductor devices will be fabricated using Silicon Planar Technology. Each die, as will be described further in Section 3.2.1, contains 6 traditional MOSFETs and 24 modified MOSFETs. Test structures, including a MOS capacitor, a van der Pauw structure for measuring sheet resistance, and a TLM structure for measuring specific contact resistance, will be used for device characterization.

### 3.2.1 Mask Creation

MOSFET fabrication is a multi-step process where each step adds an element of functionality to the final device. After calculating device operating properties, device parameters are fitted to layout geometries defined by photomasks. The masks are used to protect or expose certain regions of the silicon wafer to a given process step. This allows for a bottom-up fabrication of the device. Design of the masks is done using computer aided drawing (CAD). Process error is accounted for by the layout tolerance specifications, which designate how much error can be allowed for each layer while still allowing for the creation of functional devices.

The mask layout used in this process contains four repeating units known as dies. An example of a die is shown in Figure 3.1. Due to the small scale of the devices relative to the entire die, a close up view of the device region is shown in Figure 3.2. The 6 traditional MOSFETs are in the central region of Figure 3.2 and are easily noticeable due to their metal gates. The 24 modified MOSFETs line the perimeter of Figure 3.2. The gate oxide region of these devices are left exposed for wet biomaterial application. To prevent shorting in such wet environments, the metal contacts for the modified MOSFETs extend beyond the insulating layer.

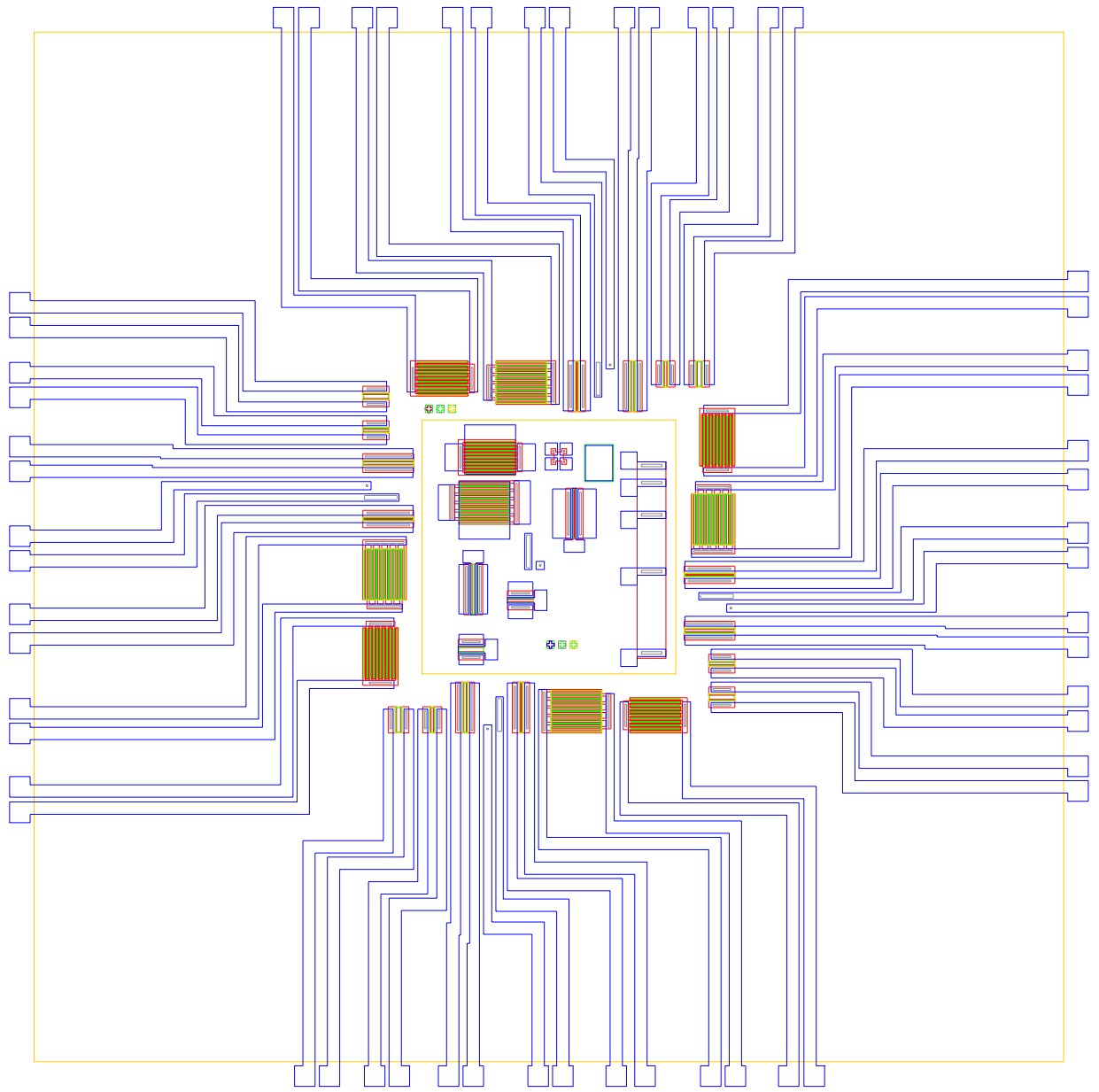


Figure 3.1 Overlay of the four-step mask layout for a single die

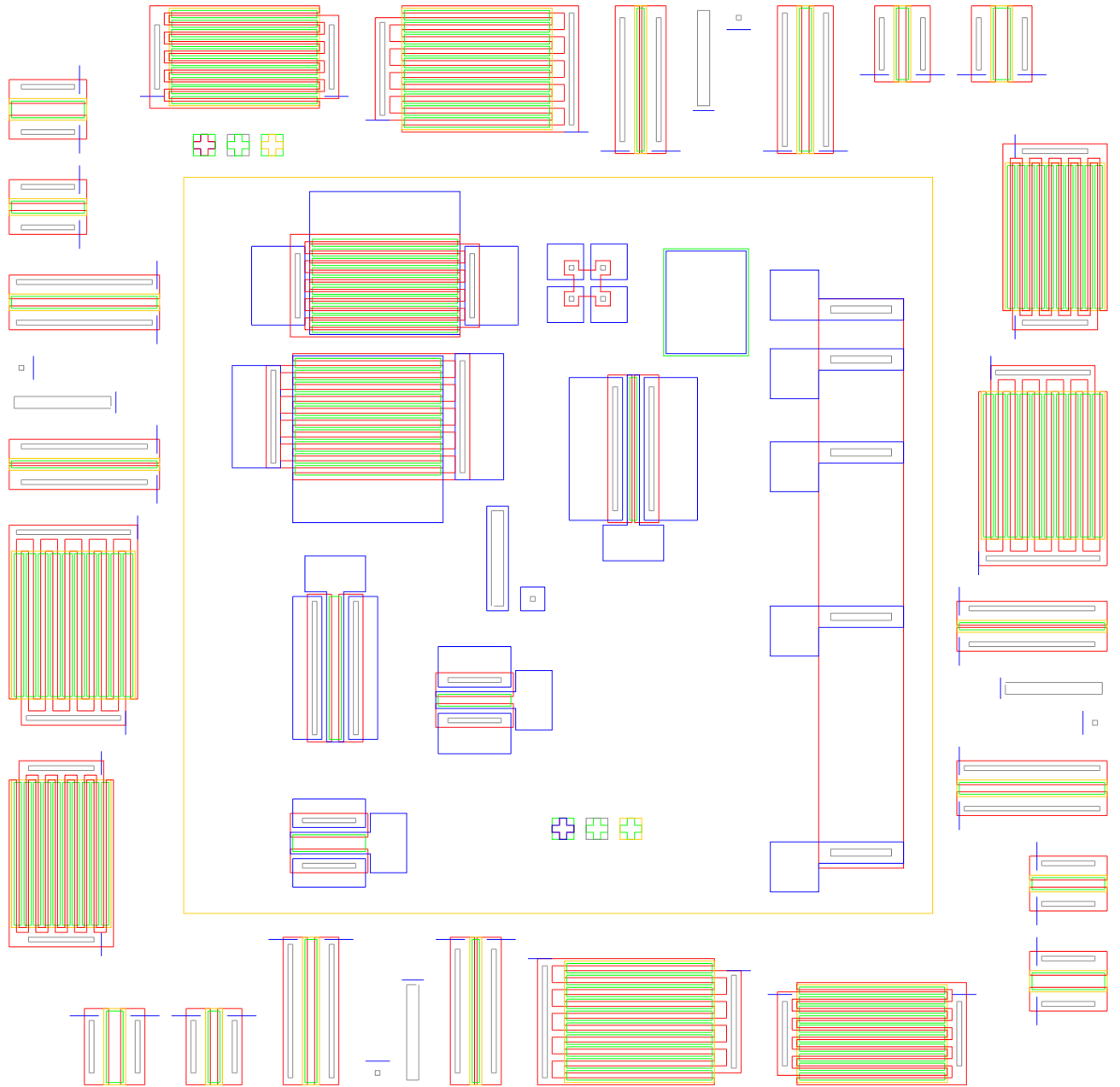


Figure 3.2 Devices and test structures in center region of die

### 3.2.2 Wafer Cleaning and Preparation

The first step in the fabrication process involves an initial degrease and clean to remove contamination (mobile sodium ions, dirt, oils) from the silicon substrate. The degrease removes oil and dirt residues. The wafer is rinsed in successive, five minutes ultrasonic baths containing TUD detergent, acetone, and methanol, where each step is followed by a five minute rinse in deionized water. The initial clean removes microscopic surface contamination and involves a standard clean 1 (SC1), standard clean 2 (SC2), and an oxide etch. SC1 contains a solution of ammonium hydroxide, hydrogen peroxide, and deionized water in a 1:1:5 proportion. The SC1 solution is heated up to about 70° C before addition of the hydrogen peroxide and the wafer is submersed for ten minutes. A rinse in deionized water follows SC1. SC2 contains hydrochloric acid, hydrogen peroxide, and deionized water in a 1:1:5 proportion. The SC2 solution is heated up to about 70° C before addition of the hydrogen peroxide and the wafer is submersed for ten minutes. A rinse in deionized water follows SC2. An oxide etch is performed to remove any native oxide formed. The wafers are immerse for 1 minute in a solution containing deionized water and hydrofluoric acid in a 1:1 proportion, followed by a rinse in deionized water.



**Figure 3.3:** Wet bench for wafer cleaning

### 3.2.3 Field Oxide Growth

The clean silicon wafer is placed in an oxidation furnace to perform wet oxidation, a process which involves introducing water vapor into a 1100° C furnace tube during a one hour oxidation period. The oxide is grown to a thickness of about 0.5 μm, which can be determined by visual inspection of the wafer's color. The oxide is then patterned using a photolithography step with an oxide etch.



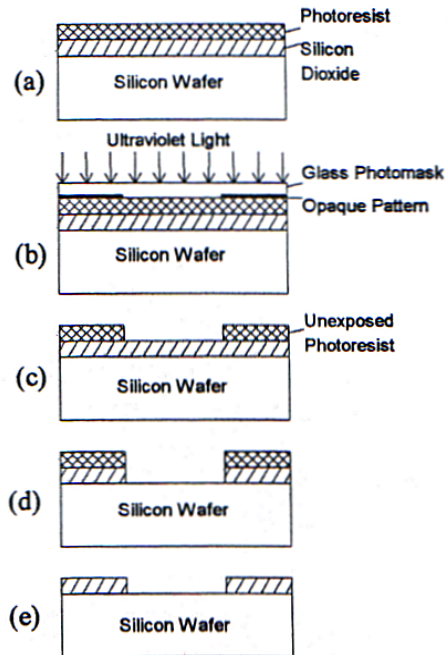
**Figure 3.4:** Furnace tubes for performing wafer oxidation and diffusion

### 3.2.4 Photolithography

Photolithography involves the application and patterning of photoresist. Patterned photoresist can be used to protect and expose regions of a device for different processing steps. Liquid HMDS, an intermediate binding agent which promotes the adhesion of photoresist to the wafer surface, is applied to a wafer and spun to an even thickness. The photoresist, Shipley 1818, is then applied and spun to an even thickness. A soft bake is then performed where the photoresist is solidified by heating the wafer to 95° C on a hotplate for one minute. A mask aligner is used to position the photomask to the alignment marks of existing device layers on a silicon wafer. The mask aligner contains an ultraviolet source for exposing the regions of the wafer not covered by the photomask. The wafer is then placed in a developer solution that removes the exposed portions of the photoresist (positive photoresist). A hard bake is then performed at 110 °C to harden the photoresist. The process of chemically hardening the photoresist allows the wafer to



undergo chemical processing steps where only the uncovered regions of the devices will be affected. This process is summarized in Figure 3.5.



**Figure 3.5:** Step by step photolithography process for oxide etching

The step by step photolithography process for oxide etching is further described below. Note that this process can be generalized to other steps.

Step A:

- Application of HMDS and photoresist
- Photoresist softbake

Step B:

- Mask alignment
- Ultraviolet exposure

Step C:

- Develop exposed photoresist
- Hard Bake remaining photoresist

Step D:

- Chemical oxide etch with buffered HF
- Deionized water rinse to stop etching

Step E:

- Acetone bath removes photoresist
- Deionized water rinse

### 3.2.5 Drain and Source Diffusions

The source and drain wells are provided by the deposition and diffusion of phosphorus, an n-type dopant, into the p-type silicon substrate. The phosphorous is deposited in a furnace filled with highly toxic phosphine gas. The phosphorous coats the entire surface of the wafer and is then diffused into the silicon during the “drive-in” step, which occurs in the nitrogen ambient furnace. These source and drain wells also serve as the ohmic contact for the aluminum contacts used for making electrical connection to the final device.

### 3.2.6 Gate Oxide Growth

The gate oxide growth is the most critical step in MOSFET formation, since the oxide must be free of structural defects and charged contaminants. To achieve this, a more controlled process known as dry oxidation is implemented. The furnace for dry oxidation is scoured with hydrochloric acid in vapor form in order to prevent metal ions from being trapped in the gate oxide. The furnace is filled with O<sub>2</sub> and the temperature is maintained at 1100°C. The time needed to grow 0.1 μm of dry oxide on a <100> wafer can be calculated using the Deal Grove and Arrhenius equations.

$$B \text{ or } (B/A) = D_o \exp\left\{\frac{-E_a}{k_B T}\right\}$$

	<b>B</b>		<b>B/A</b>	
	<i>D<sub>o</sub></i> (μm <sup>2</sup> /hr)	<i>E<sub>a</sub></i> (eV)	<i>D<sub>o</sub></i> (μm/hr)	<i>E<sub>a</sub></i> (eV)
(100) wet	386	0.78	9.70 x 10 <sup>7</sup>	2.05
(100) dry	772	1.23	3.71 x 10 <sup>6</sup>	2.00
(111) wet	386	0.78	1.63 x 10 <sup>8</sup>	2.05
(111) dry	772	1.23	6.23 x 10 <sup>6</sup>	2.00

**Figure 3.6 and Equation 3.1:** Arrhenius equation with silicon orientation and oxidation specific prefactors.

Where:

$K_b$  = Boltzman's constant =  $8.617 \times 10^{-5}$  eV/K

T = Temperature (Kelvin)

$$t = \frac{x_o^2}{B} + \frac{x_o}{B/A} - \tau$$

**Equation 3.2: Deal Grove Model**

$$\tau = \frac{x_i^2}{B} + \frac{x_i}{B/A}$$

**Equation 3.3: Deal Grove Model Correction for Dry Oxidation**

Where:

t = Time for oxidation (hours)

B = Parabolic Rate Coefficient ( $\mu\text{m}^2/\text{hr}$ )

B/A = Linear Rate Coefficient( $\mu\text{m}/\text{hr}$ )

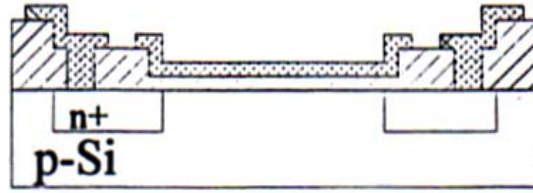
$X_i$  = 0.025  $\mu\text{m}$

$X_o$  = Desired oxide thicknes ( $\mu\text{m}$ )

From the Deal Grove Model, the time required for oxidation is approximately 50 minutes for the formation of a 0.1  $\mu\text{m}$  thick gate oxide.

### 3.2.7 Aluminum Evaporation and Contact Formation

Electron beam evaporation of an aluminum source is used to deposit an even layer of aluminum on the substrate. The deposition is performed in a vacuum chamber where the pressure is reduced to  $10^{-6}$  Torr, allowing the mean free path of the evaporated aluminum to be unhindered and deposited evenly over the wafer surface to a thickness of 0.6  $\mu\text{m}$ . Photolithography is used to define the aluminum contact pads. Following the patterning of the photoresist, an aluminum etch solution containing 15:1:1:1 phosphoric acid, nitric acid, acetic acid, and deionized water is used to etch the aluminum. The time required to etch is variable and therefore is often performed on a sample wafer first to gauge the time necessary. The definition of the aluminum pads for a MOSFET is shown in Figure 3.7.



**Figure 3.7** Final MOSFET, following aluminum contact definition

### **3.3 Device Insulation**

To obtain maximum process reliability, the substrate surface should be clean and dry prior to applying SU-8 photoresist. Substrate pretreatment includes an acetone rinse followed by a deionized water rinse. To dehydrate the surface, the substrate is baked at 200°C for 5 minutes on a hotplate. The SU-8 is then applied and spun using recommended conditions. After the resist has been applied to the substrate, a pre-bake set at 65°C is performed for 3 minutes, followed by a soft-bake set at 95°C for 9 minutes. After a 30 minute cooling period, the resist is exposed. A post exposure bake 1 is performed at 65°C for 1 minute, followed by a post exposure 2 performed at 95°C for 7 minutes. The substrate is allowed to cool down for 30 minutes. The resist is then developed, rinsed, and dried.

## **4 BIOFET**

### **4.1 Introduction**

A biosensor is a device that consists of a molecular identification element (MIE) and a transducer or transistor. The concept of a biosensor was initially designed for use in medical applications. However, the potential applications of biosensing devices in areas of environmental, agricultural, and military concern have generated a continued interest in the development of this biologically based technology. Despite past efforts, there are distinct limitations in biosensor technology that makes it imperative to move forward in research efforts. Such research endeavors can generally be divided into three realms including the identification and fabrication of molecular identification elements (MIE's), improvement of existing processing techniques, and characterization of the resulting biosensor systems. The research on MIE's involves the identification or fabrication of a MIE compound (including enzymes, microbes, organelles, plant or animal cells, antibodies, receptors, or nucleic acids) for a specific analyte (chemical or biological compound to be detected) and is evaluated based on specificity (MIE affinity to analyte) and storage, operational, and environmental stability. Furthermore, the evolution of microfabrication processes has made the development of biosensors economically feasible as sensor devices can be mass produced and are both small and portable. Despite the latter advance, there is still room for advancement of device fabrication and optimization. The latest approach in optimizing biosensing devices is to create a number of small sensors based on a modified field effect transistor (FET). The MIE would vary between a set of sensors and would produce a unique response to a particular chemical or biological agent. More specifically, a MIE/analyte reaction will yield a product with a net charge and will alter the voltage across the FET. This phenomenon can be attributed to the fact that the FET is charge sensitive and the flux of current flow from source to drain is directly related to voltage across the gate. This makes it possible to sense biological or chemical agents.

The BioFET is based on the naturally selective binding of biological elements during which charge exchange occurs. The FET is implemented as a biosensor by treating the exposed gate oxide with the biological components Streptavidin, Biotin-HRP, and BSA.

Streptavidin and Biotin-HRP form a receptor-ligand pair and can be detected using the charge sensitive properties of the FET. Biotin is conjugated with horse radish peroxidase (HRP) to form Biotin-HRP. Bovine Serum Albumin (BSA) prohibits the binding of the ligand, Biotin-HRP, to the gate surface.

## **4.2 Experimental Methods and Techniques**

The surface treatments can be separated into two categories (1) BSA receptor and (2) Streptavidin receptor. In each case Biotin-HRP is the target molecule applied to the receptor layer.

The BSA receptor treatment is used to provide an experimental control, since Biotin-HRP is prohibited from binding and exchanging charge. Therefore the BioFET's change in drain-source current should be negligible for this case. The Streptavidin receptor treatment provides a surface where affinity binding events to Biotin-HRP should occur and the largest drain-source current change should result.

Each target and receptor biomaterial treatment is immobilized using adsorption. The gate oxide surface is exposed to a solution of the biologically active material for a period of time, then the surface is washed to remove the loosely bound material and the biosensor is ready to be used. The biologically active material is held to the surface by a combination of various forces, including van der Waals forces, hydrophobic forces, hydrogen bonds, and ionic forces. This wide variety of molecular forces is due to the complex, large structures of the biological materials. The advantage of adsorption is that the forces binding the biologically active material are relatively gentle and are not likely to distort the active conformation of the molecules, which can denature the materials. One disadvantage to adsorption is that the molecules are weakly bound to the transducer. A change in temperature, pH, or ion concentration can desorb the biologically active material. Another operational problem is that it is difficult to quantify the amount of material that has been adsorbed by the transducer.

### 4.3 Experimental Results

An I-V measurement is first performed on the FET before treatment, after receptor treatment, and after target treatment. The drain-source current was monitored as a function of the drain-source voltage, swept from 0 to 5.0 volts.

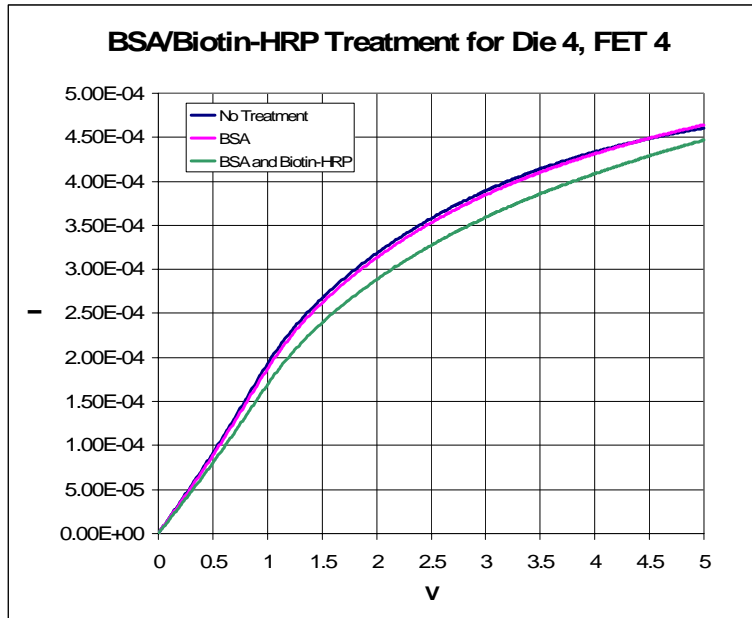


Figure 4.1 FET 4 BSA Receptor

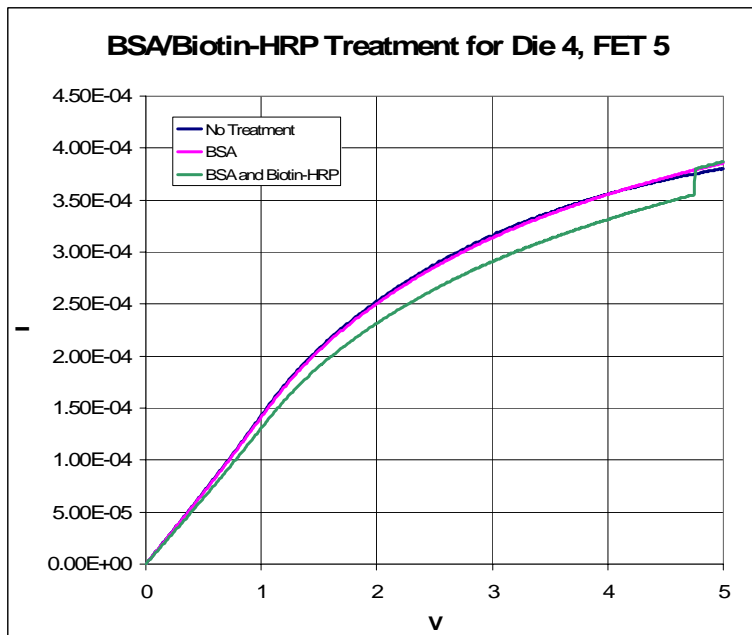


Figure 4.2 FET 5 BSA Receptor

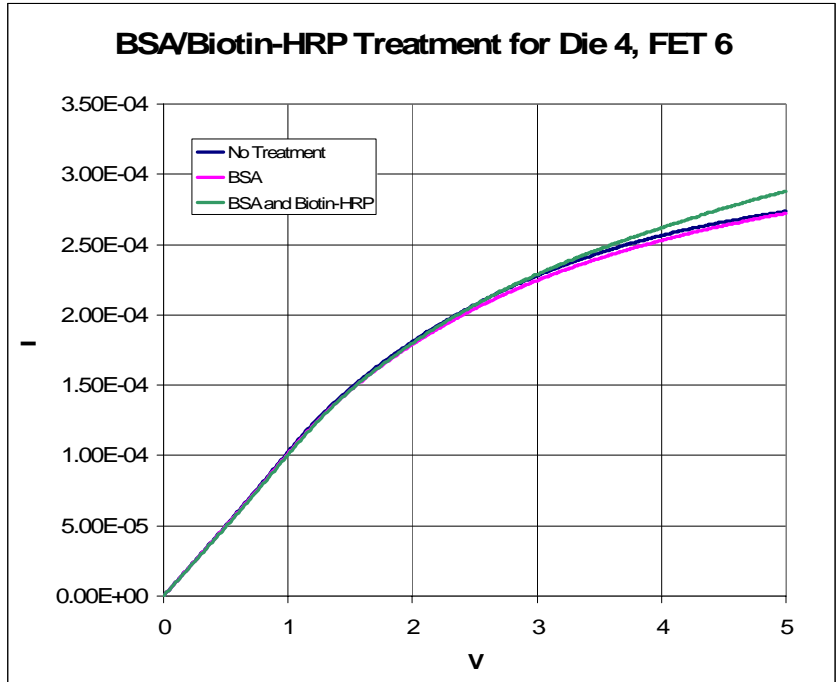


Figure 4.3 FET 6 BSA Receptor

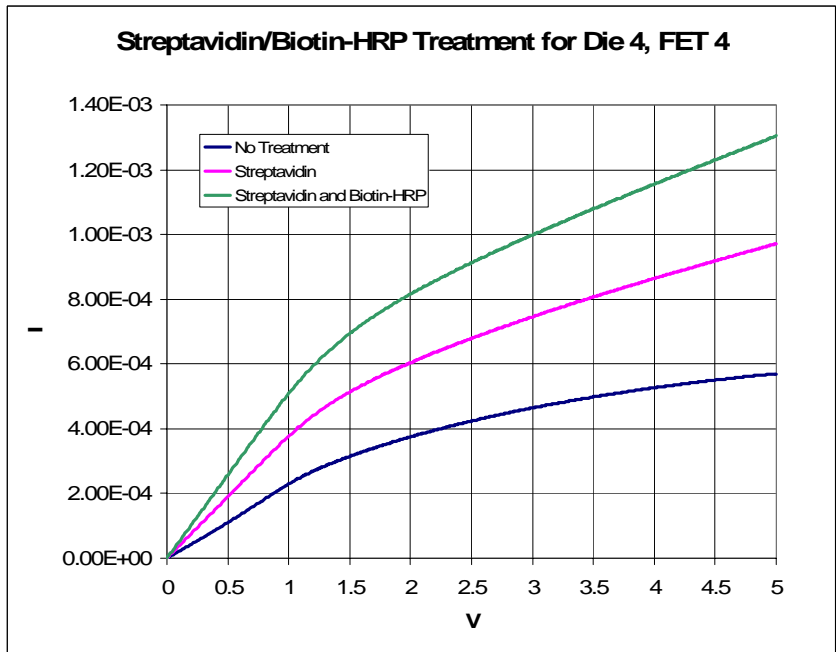


Figure 4.4 FET 4 Streptavidin Receptor



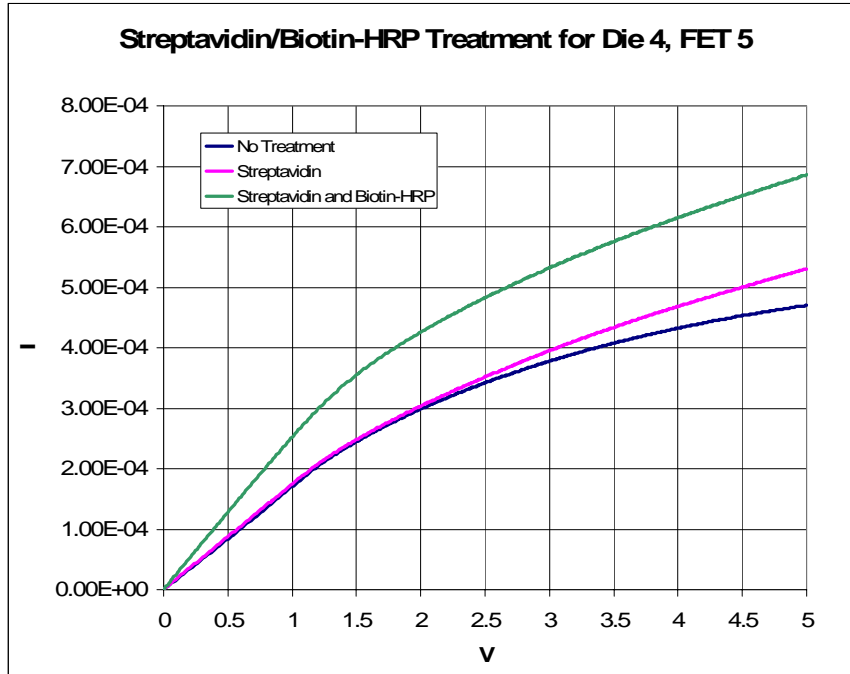


Figure 4.5 FET 5 Streptavidin Receptor

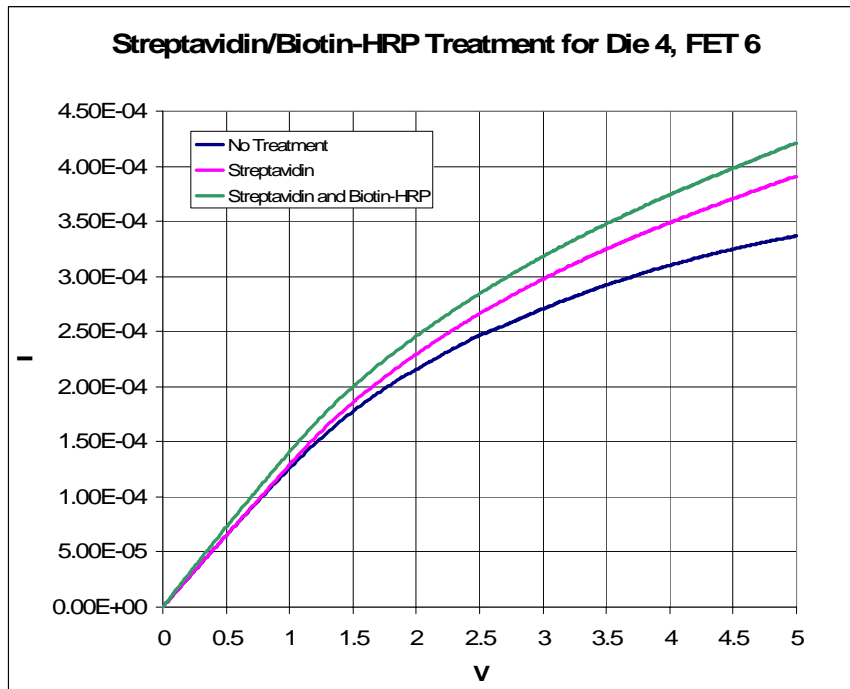


Figure 4.6 FET 6 Streptavidin Receptor

#### 4.4 Experimental Analysis

The resulting current-voltage (I-V) properties of the device are given by the I-V curves in Section 4.3. The three curves each correspond to specific type of treatment. The mathematical equation describing the saturation regime is given by Equation 1.2

$$I_{D\text{saturation}} = \left(\frac{\mu Z C_i}{2L}\right) [(V_g - V_t)^2]$$

where

$V_g$  = Gate voltage (volts)

$V_t$  = Threshold voltage (volts)

$V_{ds}$  = Drain to source voltage (volts)

$\mu$  = Surface electron mobility ( $\text{cm}^2/\text{V-s}$ )

$C_i$  = Insulator capacitance ( $\text{F}/\text{cm}^2$ )

$Z$  = Width of the channel (cm)

$L$  = Length of the channel (cm)

The specific channel geometries for the three types of FETs are shown in Figure 4.7. The largest  $Z/L$  ratios provide the greater amplification properties. Therefore, FET 4 provides the largest change in current output for a specific change in “gate voltage”.

FET	Z ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
4	600	50
5	300	70
6	300	50

Figure 4.7 Device channel geometries

The BSA receptor treatment will be discussed first, as this experiment acted as a control. Referring to Figure 4.1, FET 4 sensed 10 uA change between no treatment and the BSA treatment at 2.5V. Biotin-HRP application causes a 25 uA decrease in output properties at 2.5 V. The biosensing property was weakly demonstrated here, which agrees with our expectations. Remember that BSA acts as a block and prevents Biotin-HRP binding and subsequent charge transfer.

Referring to Figure 4.4, FET4 sensed a 250 uA change between no treatment and streptavidin treatment at 2.5 V. Biotin-HRP application causes a 230 uA decrease in output properties at 2.5 V;. Here the biosensing property has been strongly demonstrated.

Rearranging Equation 1.2, the change in current can be related to the change in effective charge sensed by BioFET. Using this equation the charge transfer per molecule can be calculated and compared to the theoretical values shown in Figure 4.8.

$$\left(\frac{\Delta I_{DS} 2L}{\mu Z C_I}\right) = \left(\frac{\Delta Q_{Eff}}{C_I}\right)^2 - 2V_T \frac{\Delta Q_{Eff}}{C_I} \quad \text{Equation 4.1}$$

BSA	-16 charges/molecule
Streptavidin	-0.83 charges/molecule
Biotin-HRP	-1.82 charges/molecules

Figure 4.8 Charges per molecule at pH 7.4

The depletion mode MOSFET should experience a decrease in output current for negative charges applied to the gate. Successful recognition of the Biotin-HRP treatment with Streptavidin increases the output current. This can be attributed to charging effects still being studied.

## 4.5 Conclusions

The BioFET demonstrated stable, sensitive, and selective operating parameters. Effective charge transfer due to streptavidin/biotin-HRP binding events were monitored using the current output of the modified FET. Furthermore, charge transfer is largely dependent on binding events. Further work will be done to uncover what is going on at a molecular level. The efficiency of charge transfer, for example, could be a function of protein structure. Studying the charge transfer of a variety of proteins with matched charges can help provide a model for charge redistribution at the molecular level.

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