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Second Ripple Current Suppression by Two Band-Pass Filters and Current Sharing Method for Energy Storage Converters in DC Microgrid

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***Abstract*—With the increasing of AC loads injected into DC microgird (MG) through the inverters, the second ripple current (SRC) in the front-end energy storage converter (ESC) and circulating current among the ESCs in DC MG become more and more serious. In this paper, the SRC suppression method by introducing two band-pass filters (BPFs) into the output voltage and inductance current feedback of the ESC is proposed. Compared with the traditional dual-loop control method, the proposed method effectively reduces the SRC and improves the dynamic performance in case of a lower cut-off frequency in the outer voltage loop. Simultaneously, an adaptive droop control method by introducing the fine tuning virtual resistances is adopted to reduce the output voltage deviation of parallel ESCs and improve the output current sharing among the ESCs. Considering the allowed range of the deviation between the output voltage and rated voltage for each ESC, the impacts of the line power loss and circulating current power loss caused by the introduced virtual resistances are analyzed in detail. While the sum of the line power loss and circulating current power loss reaches the minimum value, the appropriate control parameters are obtained. Simulation and experimental results verify the validity of the proposed method.**

***Index Terms*—DC microgrid (MG); energy storage converter (ESC); second ripple current (SRC); band-pass filter (BPF); current sharing; virtual resistance**

I. Introduction

With the increasingly serious energy crisis and environmental pollution, renewable energy distributed generation (DG) has been widely concerned and researched, and MG has also been proposed [1]-[4]. Compared to AC MG, DC MG can shorten the energy conversion chain by reducing the number of DC/AC or AC/DC converters. Meanwhile, they also feature the advantages of higher efficiency, enhanced reliability, lower control complexity, etc. [5]-[6]. Moreover, DC MG can overcome some disadvantages of AC systems, such as transformer inrush current, frequency synchronization, reactive power flow, power quality issues, etc. [7]-[8], and DC MG is developing rapidly.

The low-voltage DC MG is mainly composed of DGs, energy storages (ESs), power converters and AC and DC loads, as shown in Fig. 1. When single-phase inverters with AC loads are injected into DC MG, instantaneous output power of single-phase inverters ripples at double output voltage frequency, which leads to generate the SRC in the front-end ESC. If the peak-to-peak value of the SRC is above 8% of the rated current, it would not only lead to damage to the electrode and electrolyte of the batteries [9], but also reduce the efficiency and lifespan of the batteries [10]. Simultaneously, the SRC also wastes the capacity of the ESCs, influences the lifespan of the power converters [9], and increases the current stress and power loss of the power switching devices [11]. So, it is necessary to suppress the SRC.

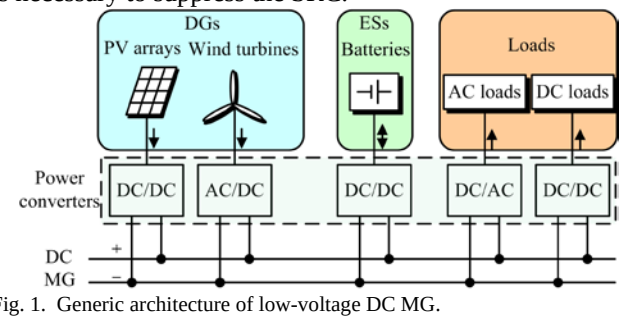

Fig. 1. Generic architecture of low-voltage DC MG.

Considering the impacts of PV converters in MPPT modes, when there is sufficient power and energy reserve within the ESs, the ESs terminals assume DC bus regulation responsibility [12]. The ESCs have three operation modes: buck modes, boost modes and non-working modes. If the load power consumption is below the output power of PV arrays when PV converters are in MPPT modes, the superfluous energy will charge the ESs and the ESCs will work in buck modes. If the load power

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consumption is above the output power of PV arrays when PV converters are in MPPT modes, the ESs will be discharged to provide the power deficit and the ESCs will work in boost modes. If the load power consumption is equal to the output power of PV arrays when PV converters are in MPPT modes, the ESs and the ESCs will not work. In these three operation modes, the SRC will penetrate into the PV converters and ESCs. References [13]-[15] have addressed the solutions for the SRC issue in PV converters which realize MPPT of PV arrays, and the SRC in the PV converters is well suppressed. If the existing SRC suppression methods for PV converters which realize MPPT of PV arrays are adopted and the loop gain of the ESCs is relatively high, most of the SRC will penetrate into the ESCs which regulates DC bus voltage. Therefore, when analyzing the SRC alone in the low-voltage standalone DC MG, PV converters in MPPT modes can be omitted [16].

A variety of approaches in reducing the SRC has been proposed in previous publications. A boost DC/DC converter topology with the novel capability has been proposed in [17] to cancel the input current ripple at an arbitrarily preselected duty cycle, which is accomplished without increasing the count of the number of components. In [18], a coupled inductor and an auxiliary inductor are utilized to obtain ripple-free input current and achieve zero-voltage-switching (ZVS) operation of the main and auxiliary switches. A novel high step-up converter has been proposed for a front-end photovoltaic system [19], which not only reduces the current stress through each power switch, but also constrains the input current ripple.

Another approach is to force the SRC in the front-end ESC to flow through DC bus capacitor. In [20], an advanced active control technique has been proposed to incorporate a current control loop in the DC/DC converter for ripple reduction, but the dynamic performance needs to be further improved. The inductance current feedback control method by single BPF has been proposed in [21], which can reduce the closed-loop impedance of the ESC at non-double output voltage frequency and improve the dynamic performance of the system at the load mutation by the BPF, but due to select range limitation of the quality factor, the closed-loop impedance of the ESC at double output voltage frequency in [21] is lower than that in [22]. So, the SRC is less reduced. The capacitance voltage feedback control method by single BPF has been proposed in [22], it effectively reduces the SRC, but there is no single BPF in the inductance current feedback, the closed-loop impedance of the ESC at non-double output voltage frequency in [22] is higher than that in [21], weakening the dynamic performance of the system at the load mutation.

In addition, the circulating current issue will arise if there is a mismatch in the output voltage deviation of parallel ESCs. To solve this problem, a modified droop control method by utilizing the information of no-load circulating current has been proposed in [23] to overcome the effect of error in nominal voltages and reduce the circulating current. References [24]-[25] present a hierarchical control method for the DC/DC converters to suppress the circulating current and improve the system performance. In [26], the droop controller is employed to achieve independent operation and the average voltage and current controllers are used in each converter to simultaneously enhance the current sharing accuracy and restore DC bus voltage. Distribution voltage control using adaptive droop coefficient in local controller has been proposed to obtain a better voltage regulation in [27]. An adaptive droop scheme is proposed for multiterminal DC grids in [28] to share the load according to the available headroom of converters. An adaptive droop resistance technique can compensate for the adaptive voltage positioning control in a boost DC/DC converter in [29]. But the impact of the output power caused by the line impedance and equivalent output impedance has not been considered in the above methods.

In this paper, the SRC suppression by two BPFs and current sharing method for the ESCs in DC MG is proposed. The paper is organized as follows. The circulating current, SRC are analyzed, and the whole control method for parallel ESCs is proposed in Section II. Section III presents an adaptive droop control method by introducing the fine tuning virtual resistances in series. Section IV shows the SRC suppression method by two BPFs for the ESC. Finally, simulations and experiments are illustrated and discussed in Section V. Some conclusions are given in Section VI.

II. CIRCULATING CURRENT, SRC ANALYSIS AND PROPOSED CONTROL METHOD FOR PARALLEL ESCS

A. *Analysis of the circulating current among the ESCs*

Diagram of parallel ESCs in DC MG with AC loads is shown in Fig. 2. The buck-boost converter named the ESC achieves the bi-directional energy flow between the batteries and DC bus of DC MG. The single-phase full-bridge inverters with LC filters can effectively reduce high-frequency harmonic current. The load is simulated by the DC/AC inverters.

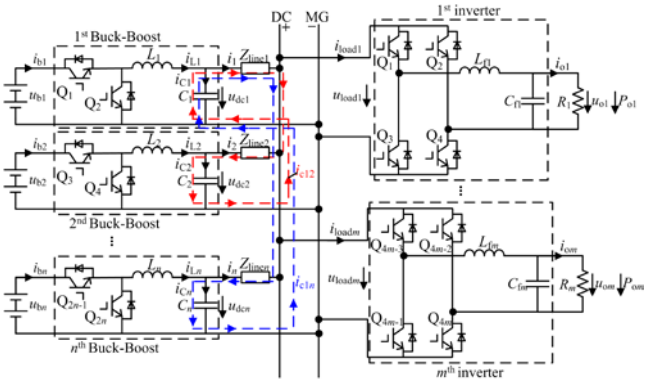

Fig. 2. Diagram of parallel ESCs in DC MG with AC loads.

In Fig. 2, u_{bj} and i_{bj} are the output voltage and current of the j^{th} ($j=1, 2, \cdots, n$) batteries, respectively. L_j and C_j are the inductance and capacitance of the j^{th} ESC, respectively. i_{Lj} and i_{Cj} are separately the currents flowing through L_j and C_j. u_{dcj} and i_j are the output voltage and current of the j^{th} ESC. i_{c1j} is the circulating current flowing from the 1st ESC to the j^{th} ESC. u_{loadh} and i_{loadh} are the input DC-link voltage and current of the h^{th} ($h=1, 2, \cdots, m$) inverter, respectively. L_{fh} and C_{fh} are the filter inductance and capacitance of the h^{th} inverter with AC loads R_h, respectively. u_{oh} and i_{oh} are the output voltage and current of the h^{th} inverter, respectively. P_{oh} is the output active power of AC

loads R_h. The line impedance is $Z_{linej} = r_{linej} + jX_{linej}$. Since the line resistance is much larger than the line reactance in the low-voltage system [2], $Z_{linej} = r_{linej}$ is assumed and selected in this paper.

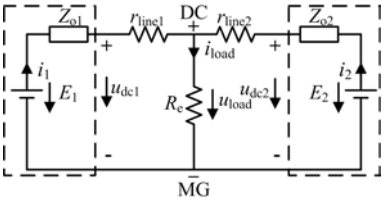

Fig. 3. Simplified diagram of parallel ESCs.

Simplified diagram of parallel ESCs is shown in Fig. 3, where E_j ($j = 1, 2$) is the output voltage without the load, Z_{oj} ($Z_{oj} = r_{oj} + jX_{oj}$) is the equivalent output impedance, and R_e is the equivalent resistance of AC loads connected to DC bus through the inverters. i_1 and i_2 can be expressed as

$$\begin{cases} i_1 = \dfrac{(r_{line2} + R_e)u_{dc1} - R_e u_{dc2}}{r_{line1}r_{line2} + r_{line1}R_e + r_{line2}R_e} \\ i_2 = \dfrac{(r_{line1} + R_e)u_{dc2} - R_e u_{dc1}}{r_{line1}r_{line2} + r_{line1}R_e + r_{line2}R_e} \end{cases} \tag{1}$$

The circulating current flowing from the 1st ESC to the 2nd ESC i_{c12} can be defined as

$$i_{c12} = -i_{c21} = \frac{u_{dc1} - u_{dc2}}{r_{line1} + r_{line2}} = \frac{i_1 r_{line1} - i_2 r_{line2}}{r_{line1} + r_{line2}} \tag{2}$$

Since R_e is much larger than the line resistance r_{line1} and r_{line2}, $r_{line1}r_{line2}$ can be ignored, and i_1 and i_2 can be simplified to

$$\begin{cases} i_1 = \underbrace{\dfrac{r_{line2}u_{dc1}}{r_{line1}R_e + r_{line2}R_e}}_{i'_1} + \underbrace{\dfrac{u_{dc1} - u_{dc2}}{r_{line1} + r_{line2}}}_{i_{c12}} \\ i_2 = \underbrace{\dfrac{r_{line1}u_{dc2}}{r_{line1}R_e + r_{line2}R_e}}_{i'_2} + \underbrace{\dfrac{u_{dc2} - u_{dc1}}{r_{line1} + r_{line2}}}_{i_{c21}} \end{cases} \tag{3}$$

where i'_1 and i'_2 are the currents flowing from the 1st ESC and the 2nd ESC to the equivalent load R_e, respectively.

As a result, the total circulating currents of the nth ESCs i_{cn} can be expressed as

$$\begin{bmatrix} i_{c1} \\ \vdots \\ i_{cn} \end{bmatrix} = \begin{bmatrix} \sum_{m\neq 1}^{n}\left(\dfrac{1}{r_{line1} + r_{linem}}\right) & \cdots & \dfrac{-1}{r_{line1} + r_{linen}} \\ \vdots & \ddots & \vdots \\ \dfrac{-1}{r_{linen} + r_{line1}} & \cdots & \sum_{m\neq n}^{n-1}\left(\dfrac{1}{r_{linen} + r_{linem}}\right) \end{bmatrix} \begin{bmatrix} u_{dc1} \\ \vdots \\ u_{dcn} \end{bmatrix} \tag{4}$$

where i_{cn} is the sum of the circulating currents flowing from the nth ESC to other ESC.

B. Mechanism of the SRC for the ESC

The output voltage of the hth inverter is supposed to be ideally sinusoidal. For a linear load, the output voltage and current of the hth inverter can be expressed as

$$\begin{cases} u_{oh} = U_{oh}\sin(\omega_o t) \\ i_{oh} = I_{oh}\sin(\omega_o t - \varphi) \end{cases} \tag{5}$$

where U_{oh}, I_{oh} and ω_o are separately the output voltage amplitude, output current amplitude and angular frequency of the hth inverter, and φ is the load impedance angle.

From (5), instantaneous output power of the hth inverter can be expressed as

$$p_{oh} = u_{oh}i_{oh} = \frac{1}{2}U_{oh}I_{oh}(\cos\varphi - \cos(2\omega_o t - \varphi)) \tag{6}$$

Supposing the efficiency of the inverter is η. Since the ripple of DC bus voltage Δu_{dc} is very small, DC bus voltage $u_{dc} = U_{dc}$. The total instantaneous output power of the inverters can be also expressed as

$$\sum_{h=1}^{m} p_{oh} = \eta\sum_{h=1}^{m} p_{inh} = \eta U_{dc}\sum_{j=1}^{n} i_j \tag{7}$$

where p_{inh} is instantaneous intput power of the hth inverter. So, the output current of the jth ESC can be expressed as

$$\begin{aligned} i_j &= \lambda_j \frac{1}{\eta}\sum_{h=1}^{m}\left[\frac{1}{2U_{dc}}U_{oh}I_{oh}(\cos\varphi - \cos(2\omega_o t - \varphi))\right] \\ &= I_{dcj} + i_{2ndj} \end{aligned} \tag{8}$$

where λ_j is the proportion coefficient of instantaneous output power of the jth ESC, $\sum_{j=1}^{n}\lambda_j = 1$.

According to (8), the output current i_j is mainly composed of two components. One is DC component I_{dcj}, and the other is the SRC i_{2ndj}. I_{dcj} and i_{2ndj} can be expressed as

$$\begin{cases} I_{dcj} = \lambda_j \dfrac{1}{2U_{dc}\eta}\sum_{h=1}^{m}(U_{oh}I_{oh}\cos\varphi) \\ i_{2ndj} = \lambda_j \dfrac{1}{2U_{dc}\eta}\sum_{h=1}^{m}(U_{oh}I_{oh}\cos(2\omega_o t - \varphi)) \end{cases} \tag{9}$$

Equivalent circuit diagram of the single ESC is shown in Fig. 4. It is obvious that i_{2ndj} will flow into the inductance L_j and capacitance C_j of the jth ESC. So, there will be the SRC in i_{Lj} and i_{Cj}. The SRC in i_{Lj} increases the current stress and power loss of the power switching devices. Therefore, it is necessary to suppress the SRC in the inductance current.

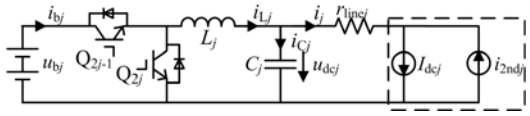

Fig. 4. Equivalent circuit diagram of the single ESC.

C. Proposed control method for parallel ESCs

As shown in Fig. 5, the SRC suppression method by introducing two BPFs into the output voltage and inductance current feedback of the ESC is proposed, and an adaptive droop control method by introducing the fine tuning virtual resistances is adopted to sharing currents among the ESCs. R_{droopj} and R'_{droopj} are separately the non-fine-tuning and fine-tuning virtual resistances of the jth ESC. $u^*_{dc\_ref}$ is the output voltage reference of the ESC when the fine tuning virtual resistances are introduced into the output voltage and inductance current feedback of the ESC. i^*_{Lj} is the inductance current reference of the jth ESC. $G_u(s)$ is the transfer function of

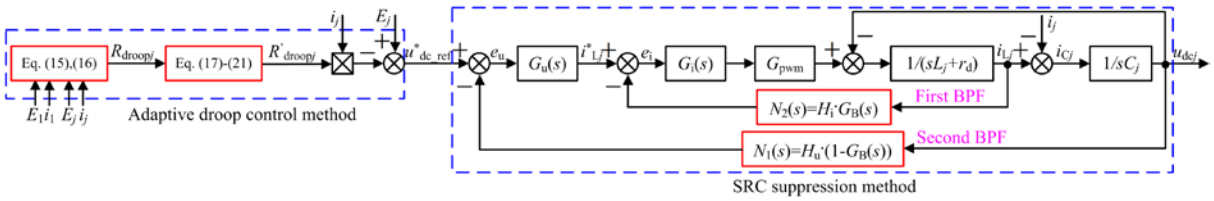

Fig. 5. Proposed control method for parallel ESCs.

PI controller in the outer voltage loop. $G_i(s)$ is the transfer function of P controller in the inner current loop. G_{pwm} is the gain of the ESC. $G_B(s)$ is the transfer function of the BPF. $N_1(s)=H_u(1-G_B(s))$ and $N_2(s)=H_iG_B(s)$ are separately the feedback coefficients of the capacitance voltage and inductance current. H_u and H_i are separately the sensor coefficients of the capacitance voltage and inductance current. r_d is the equivalent resistance connected to the inductance in series.

III. The Adaptive Droop Control Method for Parallel ESCs

To reduce the output voltage deviation of parallel ESCs and improve the output current sharing among the ESCs, an adaptive droop control method by introducing the fine tuning virtual resistances is adopted as shown in Fig. 5. Simplified diagram of parallel ESCs with the virtual resistances is shown in Fig. 6. The droop control with the virtual resistances can be expressed as

$$\begin{cases} u_{dc1\_ref} = E_1 - i_1 Z_{o1} - i_1 R_{droop1} \\ u_{dc2\_ref} = E_2 - i_2 Z_{o2} - i_2 R_{droop2} \end{cases} \tag{10}$$

where u_{dc1_ref} and u_{dc2_ref} are separately the output voltage references when the virtual resistances are introduced into the 1st ESC and the 2nd ESC.

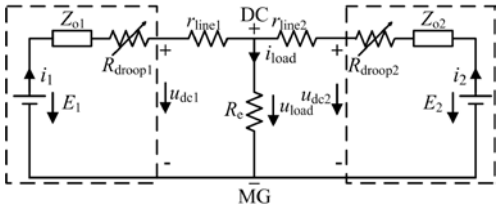

Fig. 6. Simplified diagram of parallel ESCs with the virtual resistances.

Since the equivalent output reactance can be ignored, the equivalent impedances are expressed as $Z_{o1}=r_{o1}$ and $Z_{o2}=r_{o2}$ under the DC component. The relationship between the virtual resistances can be expressed as

$$R_{droop1}/R_{droop2} = R_1/R_2 \tag{11}$$

where $R_1=r_{o1}+r_{line1}$, and $R_2=r_{o2}+r_{line2}$.

Considering the line resistances, the line power loss of the ESC can be expressed as

$$P_{line} = i_1^2 r_{line1} + i_2^2 r_{line2} \tag{12}$$

The output currents of the 1st ESC i_1 and the 2nd ESC i_2 can be expressed as

$$\begin{cases} i_1 = \dfrac{(C+R_e)AE_2 - R_eE_2}{X} \\ i_2 = \dfrac{(BC+R_e)E_2 - R_eAE_2}{X} \end{cases} \tag{13}$$

where $A=E_1/E_2$, $B=R_1/R_2$, $C=R_2+R_{droop2}$, and $X=BC^2+(1+B)CR_e$.

Therefore, the circulating current i_{c12} can be expressed as

$$i_{c12} = -i_{c21} = E_2 \cdot \frac{Dr_{line1} - Fr_{line2}}{X(r_{line1}+r_{line2})} \tag{14}$$

where $D=AC+(A-1)R_e$, and $F=BC+(1-A)R_e$.

The circulating current power loss can be expressed as

$$P_{c12} = E_2^2 \cdot \frac{D^2 r_{line1}^2 - 2DFr_{line1}r_{line2} + F^2 r_{line2}^2}{X^2(r_{line1}+r_{line2})} \tag{15}$$

Using (12) and (13), the line power loss can be expressed as

$$P_{line} = E_2^2 \cdot \frac{D^2 r_{line1} + F^2 r_{line2}}{[BC^2+(1+B)CR_e]^2} \tag{16}$$

From Fig. 5, the input variables E_j (j = 1, 2) and i_j can obtain the line power loss P_{line} and circulating current power loss P_{c12} by using (15) and (16). The relationship curves between the line power loss P_{line}, the circulating current power loss P_{c12}, $P_{line}+P_{c12}$ and R_{droop2} are shown in Fig. 7, where P_{line} increases and P_{c12} decreases continuously with increase in R_{droop2}. Considering the allowed range of the deviation between the output voltage and rated voltage for each ESC, while the sum of P_{line} and P_{c12} reaches the minimum value, the appropriate R_{droop2} is obtained.

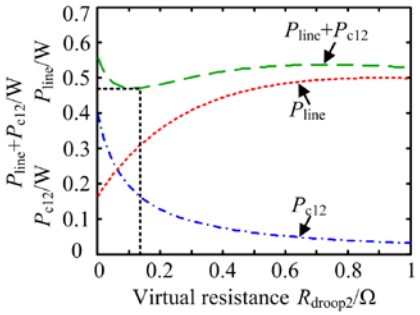

Fig. 7. Relationship curves between the line power loss P_{line}, the circulating current power loss P_{c12}, $P_{line}+P_{c12}$ and R_{droop2}.

The output voltages of parallel ESCs may have a certain deviation when the virtual resistances are introduced into parallel ESCs. So, the virtual resistances have to be fine tuned to make the output voltages of parallel ESCs equivalent. Droop characteristics of the fine tuning virtual resistances are shown in Fig. 8, where m_1 and m_2 are the droop control curves of the 1st ESC and the 2nd ESC with the non-fine-tuning virtual resistances, respectively, m_3 and m_4 are the droop control curves of the 1st ESC and the 2nd ESC with the fine-tuning virtual resistances, respectively, and Δu_1 and Δu_2 are the variations of the voltages u_{dc1} and u_{dc2} of the 1st ESC and the 2nd ESC from introducing the non-fine-tuning virtual resistances to fine-tuning virtual resistances, respectively.

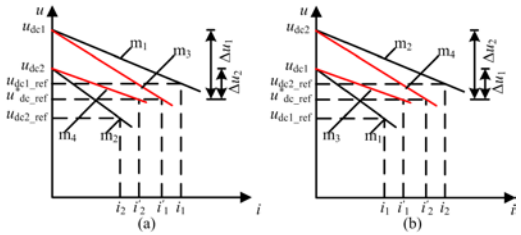

Fig. 8. Droop characteristics of the fine tuning virtual resistances. (a) $(u_{dc1}-u_{dc2})>0$. (b) $(u_{dc1}-u_{dc2})<0$.

From Fig. 8(a), if $(u_{dc1}-u_{dc2})>0$, the fine tuning virtual resistances R'_{droop1} and R'_{droop2} can be expressed as

$$\begin{cases} R'_{droop1} = R_{droop1} + k_1 i_{load} \\ R'_{droop2} = R_{droop2} - k_2 i_{load} \end{cases} \tag{17}$$

where k_1 and k_2 are the droop correction parameters. $k_2 > k_1$ is selected in order to make the drop-out values of the output voltages of parallel ESCs within a certain range.

Using (10) and (17), if $(u_{dc1}-u_{dc2})>0$, the droop correction parameters k_1 and k_2 can be expressed as

$$\begin{cases} k_1 = (X\varepsilon_u - DE_2 R_{droop1})/DE_2 i_{load} \\ k_2 = (FE_2 R_{droop2} - X\varepsilon_u)/FE_2 i_{load} \end{cases} \tag{18}$$

where ε_u is the half of the allowed maximum output voltage deviation of parallel ESCs.

From Fig. 8(b), if $(u_{dc1}-u_{dc2})<0$, the fine tuning virtual resistances R'_{droop1} and R'_{droop2} can be expressed as

$$\begin{cases} R'_{droop1} = R_{droop1} - k_2 i_{load} \\ R'_{droop2} = R_{droop2} + k_1 i_{load} \end{cases} \tag{19}$$

Using (10) and (19), if $(u_{dc1}-u_{dc2})<0$, the droop correction parameters k_1 and k_2 can be expressed as

$$\begin{cases} k_1 = (X\varepsilon_u - FE_2 R_{droop2})/FE_2 i_{load} \\ k_2 = (DE_2 R_{droop1} - X\varepsilon_u)/DE_2 i_{load} \end{cases} \tag{20}$$

While $(u_{dc1}-u_{dc2})=0$, the fine tuning virtual resistances R'_{droop1} and R'_{droop2} can be expressed as

$$\begin{cases} R'_{droop1} = R_{droop1} \\ R'_{droop2} = R_{droop2} \end{cases} \tag{21}$$

From Fig. 5, the virtual resistances R_{droopj} can change into the fine tuning virtual resistances R'_{droopj} by using (17) to (21). Meanwhile, the output voltages of parallel ESCs are equivalent when the fine tuning virtual resistances are introduced into parallel ESCs. So, the adaptive droop control method eliminates the circulating current and improves the output current sharing between parallel ESCs.

IV. The SRC Suppression Method by Two BPFs for the ESC

A. The SRC suppression method by two BPFs and its dynamic performance analysis

The equivalent transformation diagram of the SRC suppression method is shown in Fig. 9. The feedback of the inductance current i_{L1} is moved back to the output of PWM from the input of P controller in the inner current loop. The virtual impedance $Z_s(s)$ can be expressed

$$Z_s(s) = N_2(s)G_i(s)G_{pwm} \tag{22}$$

Different feedback coefficients of the SRC suppression method are given out in Tab. I. The impacts of the SRC suppression and dynamic performance caused by the feedback coefficients are analyzed, and the appropriate control parameters are selected while the SRC suppression and dynamic performance are the best.

TABLE I
DIFFERENT FEEDBACK COEFFICIENTS OF THE SRC SUPPRESSION METHOD

Feedback coefficients	$N_1(s)$	$N_2(s)$
Case I	H_u	H_i
Case II	H_u	$H_iG_B(s)$
Case III	$H_u(1-G_B(s))$	H_i
Case IV	$H_u(1-G_B(s))$	$H_iG_B(s)$

From Fig. 9(b), the SRC in the inductance current i_{L1} depends on the capacitance C_1 connected to the closed-loop impedance Z_L in parallel. Assumed that the capacitance C_1 is constant, the closed-loop impedance Z_L increases in order to decrease the SRC in the inductance current i_{L1}. The closed-loop impedance Z_L can be expressed as

$$Z_L = \frac{sL_1 + r_d + Z_s(s)}{1 + G_u(s)G_i(s)G_{pwm}N_1(s)} \tag{23}$$

The outer voltage loop gain can be expressed as

$$T_u(s) = \frac{G_u(s)G_i(s)G_{pwm}N_1(s)}{sC_1(sL_1 + r_d + Z_s(s)) + 1} \tag{24}$$

The transfer function of the closed-loop of the system can be expressed as

$$\Phi(s) = G_u(s)G_i(s)G_{pwm}/M \tag{25}$$

where $M=sC_1(sL_1+r_d+Z_s(s))+G_u(s)G_i(s)G_{pwm}N_1(s)+1$.

Bode diagrams of the closed-loop impedances are shown in Fig. 10. The closed-loop impedance presents high impedance at the whole output voltage frequency in the case I. So, the SRC suppression and dynamic performance of the system at the load mutation need to be improved. Compared to the cases I and II, the amplitude of the closed-loop impedance reaches the

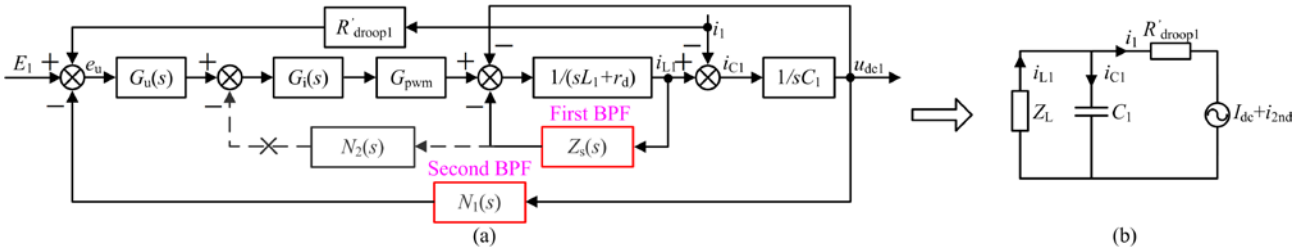

Fig. 9. The equivalent transformation diagram of the proposed SRC suppression method. (a) Control diagram of the equivalent transformation. (b) Construction circuit of the SRC

maximum value at double output voltage frequency in the cases III and IV, which effectively reduce the SRC.

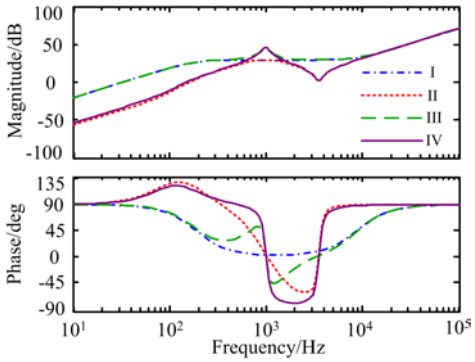

Fig. 10. Bode diagrams of the closed-loop impedances.

Magnitude-frequency curves of the outer voltage loop gains are shown in Fig. 11, where f_o is the frequency of the output voltage for the h^{th} inverter. The instantaneous output power of the h^{th} inverter ripples at double output voltage frequency, which leads to generate the SRC with the same frequency in the ESC. Compared to the cases I and III, the cut-off frequencies in the outer voltages loop are increased in the cases II and IV, which improve the dynamic performance in case of a very low cut-off frequency in the outer voltage loop in the case I.

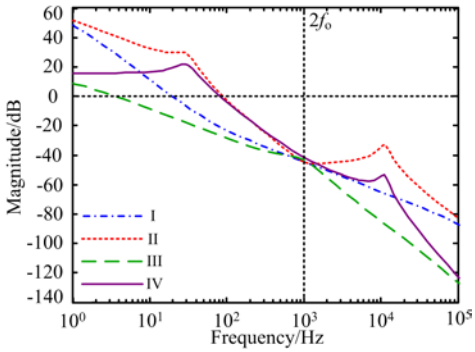

Fig. 11. Magnitude-frequency curves of the outer voltage loop gains.

Unit step dynamic responses of the ESC are shown in Fig. 12. Compared to the cases I and III, the regulation time and overshoot are the minimum value in the cases II and IV, which improve the dynamic performance of the system at the load mutation. So, the SRC suppression method by two BPFs not only effectively reduces the SRC, but also improves the dynamic performance of the system at the load mutation.

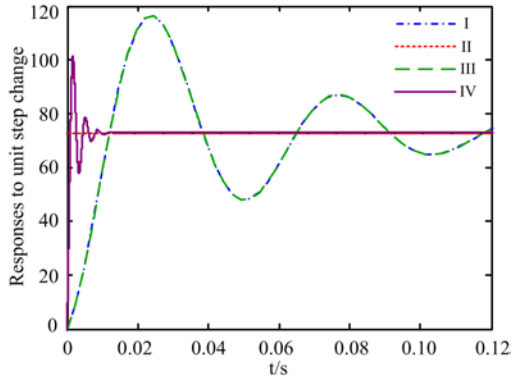

Fig. 12. Unit step dynamic responses of the ESC.

B. The control parameters selection and stability analysis

The transfer function of the BPF $G_B(s)$ can be expressed as

$$G_B(s)=\frac{2\omega_o s/Q}{s^2+2\omega_o s/Q+(2\omega_o)^2} \tag{26}$$

where Q is the quality factor of the BPF.

Bode diagrams of the BPF with Q = 0.25, 1, 2 are shown in Fig. 13. The function of the BPF is that the signals are allowed to pass within a certain range of the transmission band. Meanwhile, the signals that are lower than the minimal limit frequency and higher than the maximal limit frequency are attenuated and inhibited. The larger value of Q is, the better wave-passed characteristic is, but the smaller range of the frequency is. System responses to unit step change with Q = 0.25, 1, 2 are shown in Fig. 14. The regulation time and overshoot increase when Q enlarges, which can influence the dynamic performance of the ESC at the load mutation. So, Q = 1 is selected when the wave-passed characteristic and dynamic performance are considered.

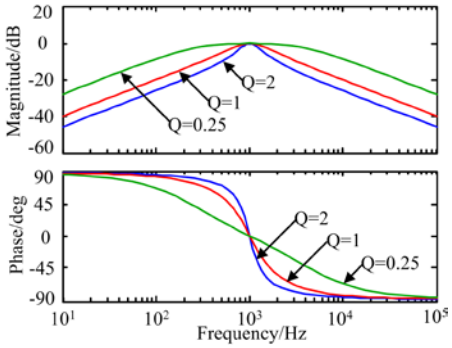

Fig. 13. Bode diagrams of the BPF with Q = 0.25, 1, 2.

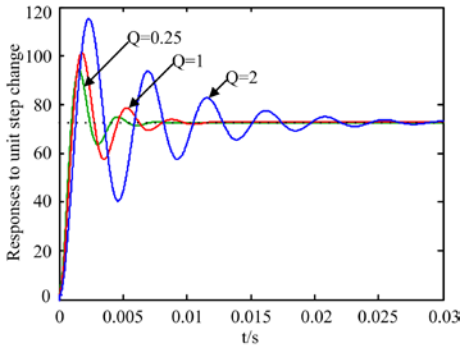

Fig. 14. System responses to unit step change with Q = 0.25, 1, 2.

Using (25), the characteristic root equation of the closed-loop transfer function of the system can be expressed as

$$T_1s^5+T_2s^4+T_3s^3+T_4s^2+T_5s^1+T_6s^0=0 \tag{27}$$

where

$$\begin{cases} T_1=QL_1C_1 \\ T_2=2\omega_o L_1C_1+QC_1r_d \\ T_3=(2\omega_o)^2QL_1C_1+2\omega_oC_1(r_d+r_s)+Q(k_pG_{pwm}H_u+1) \\ T_4=(2\omega_o)^2QC_1r_d+Qk_iG_{pwm}H_u+2\omega_o \\ T_5=(2\omega_o)^2Q(k_pG_{pwm}H_u+1) \\ T_6=(2\omega_o)^2Qk_iG_{pwm}H_u \end{cases}$$

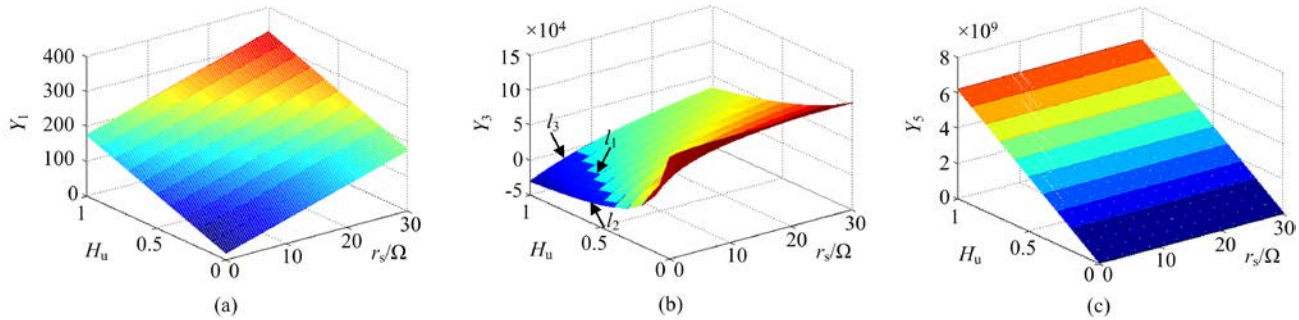

Fig. 15. Relationship among the virtual resistance r_s, feedback coefficient H_u and the first array coefficients in the routh table. (a) The first array coefficient Y_1. (b) The first array coefficient Y_3. (c) The first array coefficient Y_5.

k_p and k_i are the parameters of PI controller in the outer voltage loop, r_s is the virtual impedance $Z_s(s)$ when the feedbacks are not added into the BPF, and $r_s = H_i G_i G_{pwm}$.

TABLE II
ROUTH TABLE OF THE CLOSED-LOOP SYSTEM

Rank	Routh array		
s^5	T_1	T_3	T_5
s^4	T_2	T_4	T_6
s^3	$Y_1=(T_2T_3-T_1T_4)/T_2$	$Y_2=(T_2T_5-T_1T_6)/T_2$	0
s^2	$Y_3=(Y_1T_4-T_2Y_2)/Y_1$	$Y_4=T_6$	0
s^1	$Y_5=(Y_3Y_2-Y_1Y_4)/Y_3$	0	0
s^0	$Y_6=T_6$	0	0

Routh table of the closed-loop system is shown in Tab. II. The first array coefficients of the routh table must be positive in order to meet the steady condition of the closed-loop system. In other words, the characteristic roots are all in the left-half plane of s. Relationship among the virtual resistance r_s, feedback coefficient H_u and the first array coefficients in the routh table are shown in Fig. 15. From Fig. 15(a), Y_1 is always above zero with changes in the virtual resistance r_s and feedback coefficient H_u. From Fig. 15(b), when the feedback coefficient H_u is constant, Y_3 increases continuously with increase in the virtual resistance r_s. When the virtual resistance r_s is constant, Y_3 decreases continuously with increase in the feedback coefficient H_u. The part surrounded by the curves l_1, l_2 and l_3 indicates Y_3 is below zero. From Fig. 15(c), Y_5 is always above zero with changes in the virtual resistance r_s and feedback coefficient H_u. Therefore, when the virtual resistance r_s and feedback coefficient H_u are not in the part surrounded by the curves l_1, l_2 and l_3, the closed-loop system is steady.

C. Impact of the equivalent output resistance of the proposed control method

Under the DC component and the SRC, the equivalent output impedance of each ESC is designed to the larger resistance in order to effectively eliminate the effect of the different line resistances, suppress the circulating current and realize the output current sharing among the ESCs.

Bode diagrams of the equivalent output impedances under the different control methods are shown in Fig. 16. The control method without the virtual resistance and SRC suppression is defined as "the control method A". The control method with the virtual resistances but not introducing the SRC suppression is defined as "the control method B". The control method with the adaptive droop control method but not introducing the SRC suppression is defined as "the control method C". The proposed control method is defined as "the control method D".

Using the control method A, the equivalent output impedance Z_{o1} can be expressed as

$$Z_{o1} = \frac{L_1 s^2 + (r_d + r_s)s}{A_3(s)s^3 + A_2(s)s^2 + A_1(s)s + A_0(s)} \tag{28}$$

where

$$\begin{cases} A_3(s) = L_1 C_1 \\ A_2(s) = C_1(r_d + r_s) \\ A_1(s) = 1 + k_p G_i G_{pwm} H_u \\ A_0(s) = k_i G_i G_{pwm} H_u \end{cases}$$

The control method B and C are similar. So, taking the control method C as the study object, the equivalent output impedance Z'_{o1} can be expressed as

$$Z'_{o1} = R'_{droop1} + Z_{o1} \tag{29}$$

Using the proposed control method, the equivalent output impedance Z''_{o1} can be expressed

$$\begin{aligned} Z''_{o1} = (B_5(s)s^5 + B_4(s)s^4 + B_3(s)s^3 + B_2(s)s^2 + \\ B_1(s)s^1 + B_0(s)) / (D_5(s)s^5 + D_4(s)s^4 + \\ D_3(s)s^3 + D_2(s)s^2 + D_1(s)s^1 + D_0(s)) \end{aligned} \tag{30}$$

where

$$\begin{cases} B_5(s) = R'_{droop1} Q L_1 C_1 \\ B_4(s) = Q L_1 + R'_{droop1} C_1 (2\omega_o L_1 + Q r_d) \\ B_3(s) = 2\omega_o L_1 + Q r_d + R'_{droop1}\{Q + Q k_p G_i G_{pwm} H_u \\ \qquad + C_1[(2\omega_o)^2 Q L_1 + 2\omega_o (r_d + r_s)]\} \\ B_2(s) = (2\omega_o)^2 Q L_1 + 2\omega_o (r_d + r_s) \\ \qquad + R'_{droop1}[2\omega_o + Q k_i G_i G_{pwm} H_u + (2\omega_o)^2 Q r_d C_1] \\ B_1(s) = (2\omega_o)^2 Q r_d + R'_{droop1}(2\omega_o)^2 Q(1 + k_p G_i G_{pwm} H_u) \\ B_0(s) = R'_{droop1}(2\omega_o)^2 Q k_i G_i G_{pwm} H_u \end{cases}$$

$$\begin{cases} D_5(s) = Q L_1 C_1 \\ D_4(s) = C_1(2\omega_o L_1 + Q r_d) \\ D_3(s) = Q(1 + k_p G_i G_{pwm} H_u) + C_1[(2\omega_o)^2 Q L_1 + 2\omega_o (r_d + r_s)] \\ D_2(s) = 2\omega_o + Q k_i G_i G_{pwm} H_u + (2\omega_o)^2 Q r_d C_1 \\ D_1(s) = (2\omega_o)^2 Q(1 + k_p G_i G_{pwm} H_u) \\ D_0(s) = (2\omega_o)^2 Q k_i G_i G_{pwm} H_u \end{cases}$$

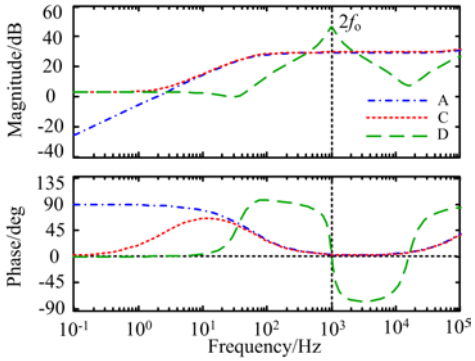

Fig. 16. Bode diagrams of the equivalent output impedances under the different control methods.

From Fig. 16, compared to the control method A, the equivalent output impedance Z'_{o1} is the larger resistance in the low frequency range in the control method C, which decreases the effect of the different line resistances, but the influence of the SRC is not considered. Compared to the control method C, the proposed control method not only has the advantages of the control method C, but also makes the equivalent output impedance Z''_{o1} be resistive and the larger amplitude at double output voltage frequency, which is in favor of the circulating current suppression among the ESCs, realizes the output current sharing and effectively reduces the SRC.

V. Simulation and Experiment

The In order to verify the validity of the proposed control method, the simulation model of parallel ESCs in the low-voltage DC MG is built by using PSIM 9.0 based on the Fig. 2. System parameters are shown in Tab. III.

TABLE III
System Parameters

Parameters	Value	Parameters	Value
U_{dc}/V	41	R_{droop1}/mΩ	140
U_o/V	22	R_{droop2}/mΩ	168
U_m/V	2	k_p	1.5
L_1/mH	1.2	k_i	0.01
L_2/mH	1.2	k	0.95
C_1/μF	8000	H_u	0.137
C_2/μF	8000	H_i	0.1
L_f/mH	5	k_1	0.001
C_f/μF	3.3	k_2	0.02
r_d/Ω	3	f_s/kHz	12.8
r_{line1}/mΩ	100	f_o/Hz	500
r_{line2}/mΩ	120	f_r/kHz	1.24

The single group of single-phase AC loads is injected into DC MG, and its active power is approximately equal to 200W. The simulation results of the output voltage u_{dcj}, output current i_j, circulating current i_{c1j}, output power P_j and inductance current i_{Lj} under different control methods with single group AC loads are shown in Fig. 17. From Fig. 17(a), during time

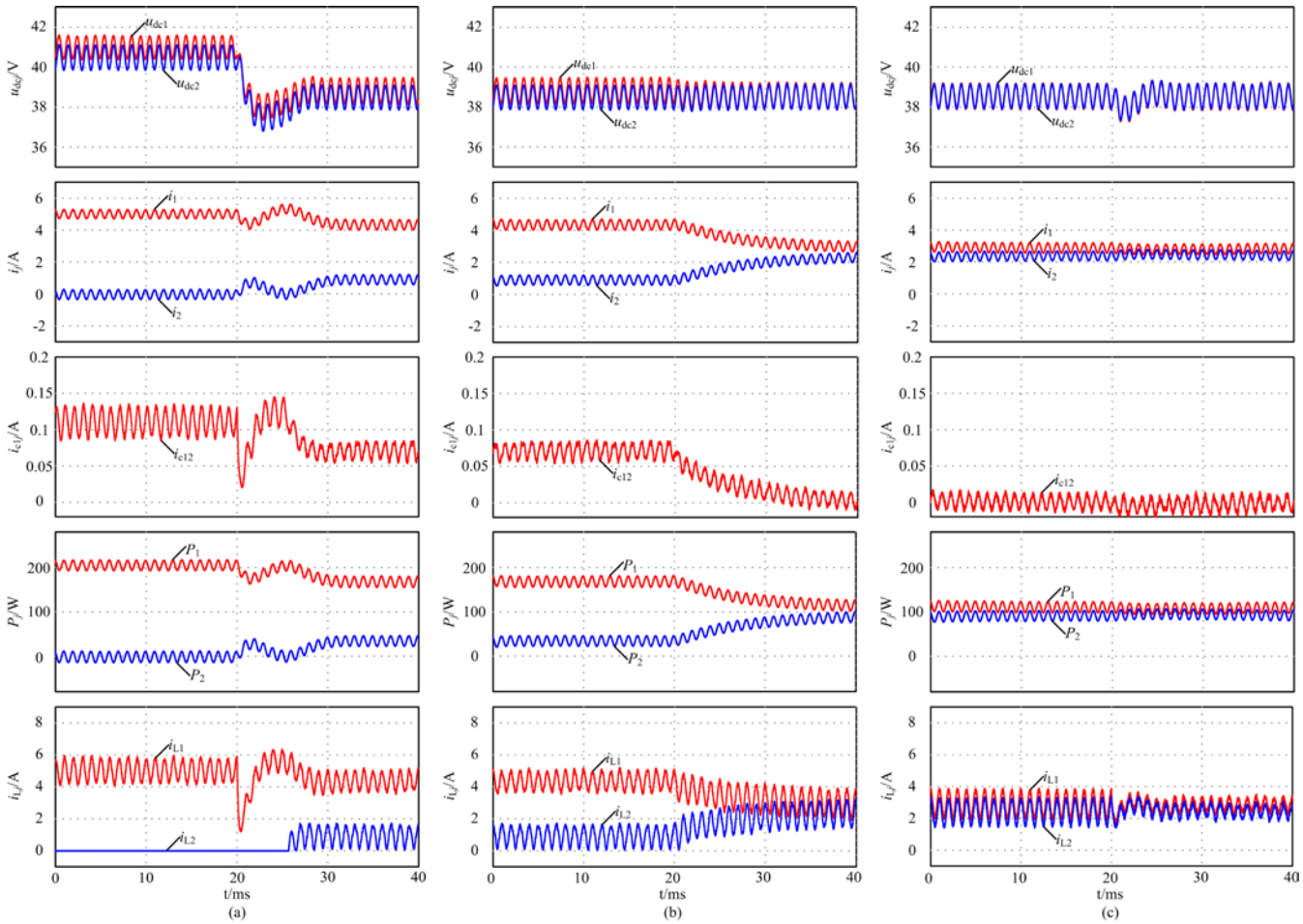

Fig. 17. Simulation results of the output voltage u_{dcj}, output current i_j, circulating current i_{c1j}, output power P_j and inductance current i_{Lj} under different control methods with single group AC loads. (a) the control method A and B. (b) the control method B and C. (c) the control method C and D.

0-20 ms, the control method A is used to simulate for each ESC. During time 20-40 ms, the control method B is used to simulate for each ESC. Initially, up to 20 ms, the output voltage of the 2nd ESC is decreased by 1% of its nominal value 41V. At time 30 ms, the deviation between the output voltage and the rated voltage for each ESC is 5% within the acceptable range, but the output voltages of parallel ESCs may have a certain deviation. Compared to the control method A, the control method B reduces the output voltage deviation of parallel ESCs and suppresses the circulating current.

From Fig. 17(b), during time 0-20 ms, the control method B is used to simulate for each ESC. During time 20-40 ms, the control method C is used to simulate for each ESC. Initially, up to 20 ms, the deviation between the output voltage and the rated voltage for each ESC is 5% within the acceptable range, but the output voltages of parallel ESCs may have a certain deviation. At time 30 ms, the output voltage of the 2nd ESC is equal to the output voltage of the 1st ESC. Compared to the control method B, the control method C makes the output voltages of parallel ESCs equivalent, eliminates the circulating current and improves the output current sharing between parallel ESCs.

From Fig. 17(c), during time 0-20 ms, the control method C is used to simulate for each ESC. During time 20-40 ms, the control method D is used to simulate for each ESC. Initially, up to 20 ms, the peak-to-peak of the SRC is 1 A. At time 25 ms, the peak-to-peak of the SRC is 0.4 A. Compared to the control method C, the control method D not only makes the output voltages of parallel ESCs equivalent, eliminates the circulating current and improves the output current sharing between parallel ESCs, but also effectively reduces the SRC.

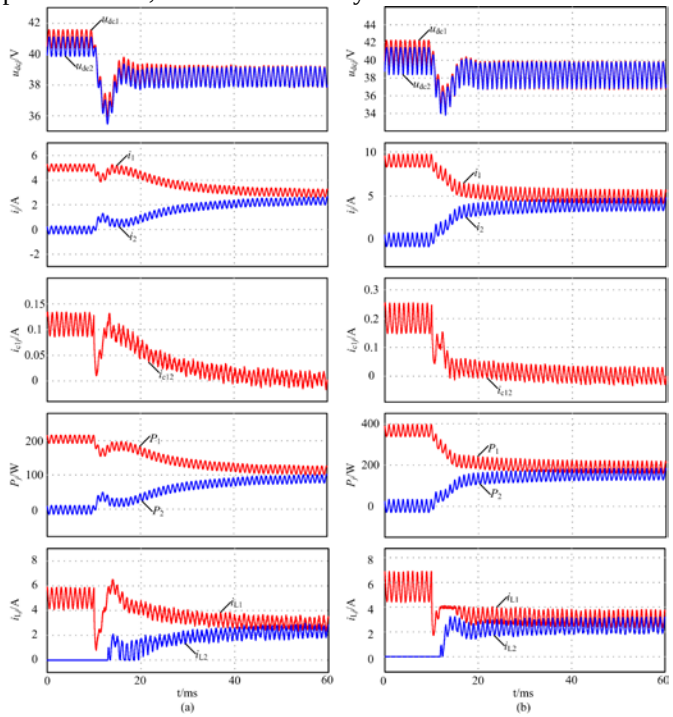

Fig. 18. Simulation results of the output voltage u_{dcj}, output current i_j, circulating current i_{c1j}, output power P_j and inductance current i_{Lj} under the different control method A and D with the number of AC loads. (a) single group AC loads with P_{o1}=200W. (b) two groups of AC loads with P_{o1}= P_{o2}= 200W.

With the number of single-phase AC loads increasing, the comparative simulation results of the output voltage u_{dcj}, output current i_j, circulating current i_{c1j}, output power P_j and inductance current i_{Lj} under the control method A and D are shown in Fig. 18. In Fig 18(a), single group AC loads is injected into DC MG, and its active power is approximately equal to 200W. The control method A is used to simulate for each ESC during time 0-10 ms, and the control method D is used to simulate for each ESC during time 10-60 ms. Initially, up to 10 ms, the output voltage of the 2nd ESC is decreased by 1% of its nominal value 41V, and the peak-to-peak of the SRC is 1 A. At time 40 ms, the output voltage of the 2nd ESC is equal to the output voltage of the 1st ESC and the peak-to-peak of the SRC is 0.4 A. Compared to the control method A, the control method D not only makes the output voltages of parallel ESCs equivalent, eliminates the circulating current and improves the output current sharing between parallel ESCs, but also effectively reduces the SRC.

In Fig 18(b), two groups of single-phase AC loads are injected into DC MG, where active power of each group AC loads is approximately equal to 200W. The procedure is the same as the one described above. Compared to the control method A, except the peak-to-peak of the SRC increasing continuously with increase in the number of single-phase AC loads, other conditions are equal to Fig. 18(a). Therefore, when the number of single-phase AC loads increases, the proposed control method is still applicable.

In order to verify the simulation results, the experimental platform of parallel ESCs in the low-voltage DC MG is built in Fig. 19, which is mainly composed of the batteries, ESCs, DC/AC inverters, LC filters and loads. The proposed control method is implemented by using TMS320F2812. Detailed system parameters are shown in Tab. III.

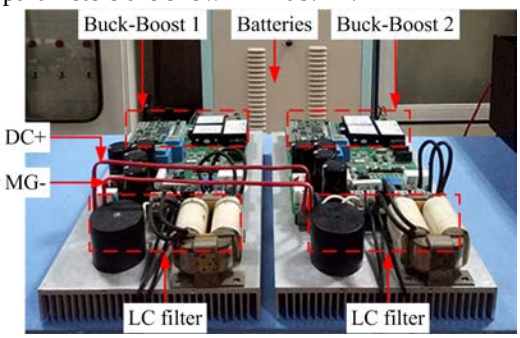

Fig. 19. Experimental platform of parallel ESCs.

The comparative experiments under different control methods including cases I, II, III and IV are shown in Fig. 20 and 21. Fig. 20 shows the experimental results of the ripple of DC bus voltage Δu_{dc}, ripple of the inductance current Δi_{L1} and output current of the inverter i_o. Seen from Fig. 20(a) and 20(b), the peak-to-peak of the SRC is 1 A in the case I and II, and the proportion is about 20.5%. But from Fig. 20(c) and 20(d), the peak-to-peak of the SRC is 0.3A in the case III and IV, which accounts for 6.15%. Therefore, the SRC in the inductance current is smaller in the case III and IV, which effectively reduce the SRC.

Fig. 21 shows the experimental results of the ripple of DC

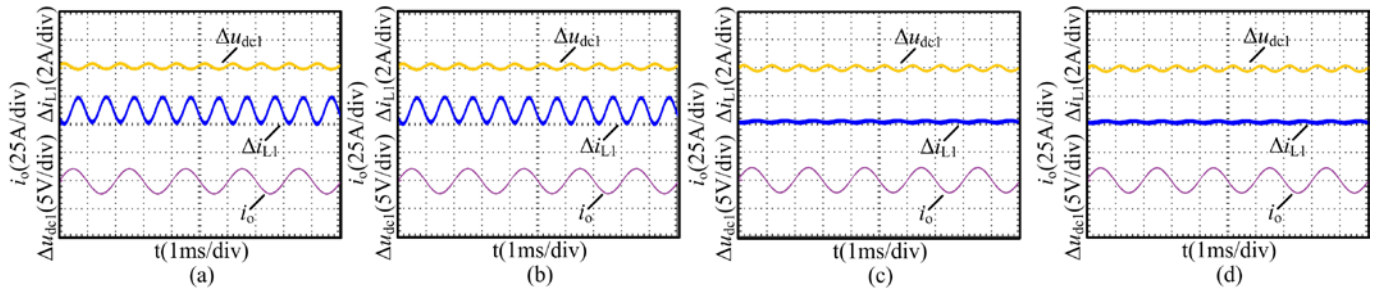

Fig. 20. Experimental results of the ripple of DC bus voltage Δu_{dc}, ripple of the inductance current Δi_{L1} and output current of the inverter i_o under different methods. (a) Case I. (b) Case II. (c) Case III. (d) Case IV.

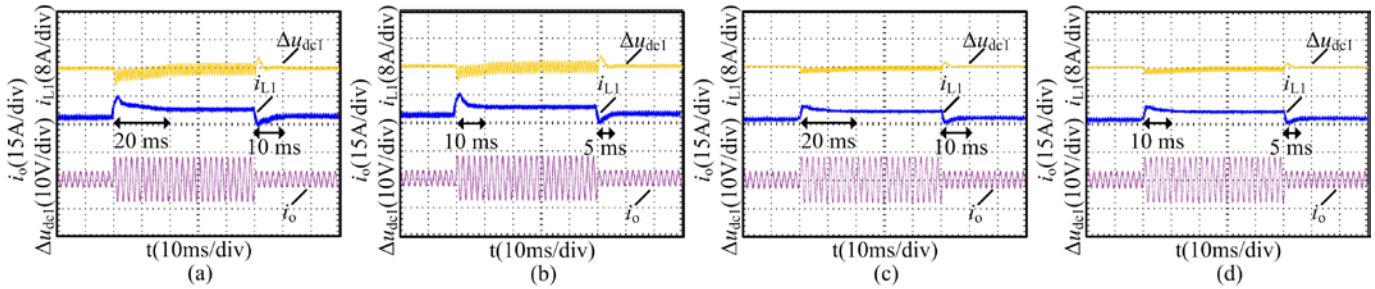

Fig. 21. Experimental results of the ripple of DC bus voltage Δu_{dc}, inductance current i_{L1} and output current of the inverter i_o with the loads suddenly changing under different methods. (a) Case I. (b) Case II. (c) Case III. (d) Case IV.

bus voltage Δu_{dc}, inductance current i_{L1} and output current of the inverter i_o when the loads suddenly increase from 33% to 100% or suddenly decrease from 100% to 33%. Seen from Fig. 21(a) and 21(c), the regulation time is 20 ms at the loads increased suddenly and the regulation time becomes 10 ms at the loads decreased abruptly in the case I and III. But from Fig. 21(b) and 21(d), the regulation time is 10 ms at the loads increasing suddenly, and the regulation time becomes 5 ms at the loads decreasing abruptly in the case II and IV, which improve the dynamic performance of the system at the load mutation. Therefore, the case IV not only effectively reduces the SRC, but also improves the dynamic performance of the system at the load mutation.

The single group of single-phase AC loads is injected into DC MG, and its active power is approximately equal to 200W. The experimental results of the output voltage u_{dcj} and circulating current i_{c1j} under different control methods with single group AC loads are shown in Fig. 22. From Fig. 22(a), during time 0-20 ms, the control method A is used to simulate for each ESC. During time 20-40 ms, the control method B is used to simulate for each ESC. Initially, up to 20 ms, the output voltage of the 2nd ESC is decreased by 1% of its nominal value 41V and the amplitude of the circulating current is about 1.2 A. At time 30 ms, the deviation between the output voltage and the rated voltage for each ESC is 5% within the acceptable range, but the output voltages of parallel ESCs may have a certain deviation. And the amplitude of the circulating current is about 0.7 A. Compared to the control method A, the control method B reduces the output voltage deviation of parallel ESCs and suppresses the circulating current.

From Fig. 22(b), during time 0-20 ms, the control method B is used to simulate for each ESC. During time 20-40 ms, the control method C is used to simulate for each ESC. Initially, up to 20 ms, the deviation between the output voltage and the rated voltage for each ESC is 5% within the acceptable range, but the output voltages of parallel ESCs may have a certain deviation. And the amplitude of the circulating current is about 0.7 A. At time 30 ms, the output voltage of the 2nd ESC is equal to the output voltage of the 1st ESC and the amplitude of the circulating current is about 0.1 A. Compared to the control method B, the control method C makes the output voltages of parallel ESCs equivalent, eliminates the circulating current and improves the output current sharing between parallel ESCs.

From Fig. 22(c), during time 0-20 ms, the control method C is used to simulate for each ESC. During time 20-40 ms, the control method D is used to simulate for each ESC. The control

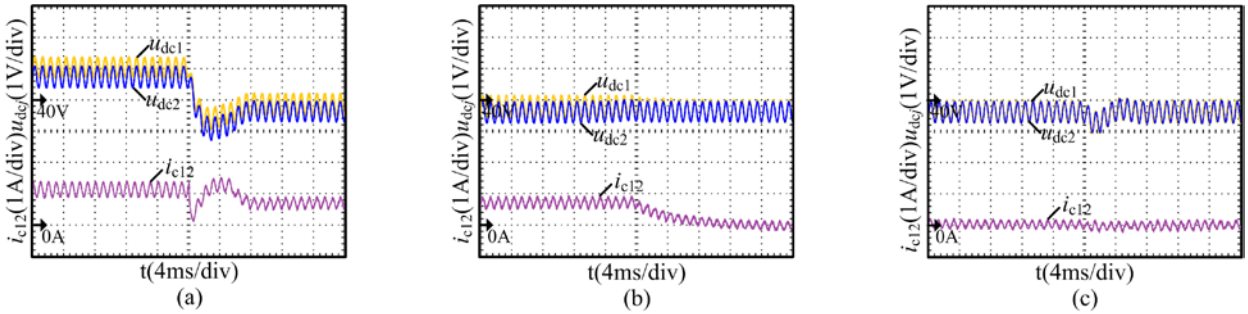

Fig. 22. Experimental results of the output voltage u_{dcj} and circulating current i_{c1j} under different control methods with single group AC loads. (a) the control method A and B. (b) the control method B and C. (c) the control method C and D.

method D has the advantages of the control method C. From Fig. 20 and Fig. 21, the SRC suppression method by two BPFs not only effectively reduces the SRC, but also improves the dynamic performance of the system at the load mutation. So, the control method D not only makes the output voltages of parallel ESCs equivalent, eliminates the circulating current and improves the output current sharing between parallel ESCs, but also effectively reduces the SRC.

With the number of single-phase AC loads increasing, the comparative experimental results of the output voltage u_{dcj} and circulating current i_{c1j} under the control method A and D are shown in Fig. 23. In Fig. 23(a), single group AC loads is injected into DC MG, and its active power is approximately equal to 200W. In Fig 23(b), two groups of single-phase AC loads are injected into DC MG, where active power of each group AC loads is approximately equal to 200W. The control method A is used to simulate for each ESC during time 0-10 ms, and the control method D is used to simulate for each ESC during time 10-60 ms. Obviously, with the number of the same AC loads increasing, initially, up to 10 ms, the output voltage of the 2nd ESC is decreased by 1% of its nominal value 41V and the amplitude of the circulating current is about 1.2 A in Fig. 23(a) and 2.2 A in Fig. 23(b). At time 40 ms, the output voltage of the 2nd ESC is equal to the output voltage of the 1st ESC in Fig. 23(a) and Fig. 23(b). Therefore, when the number of single-phase AC loads increases, the proposed control method is still applicable.

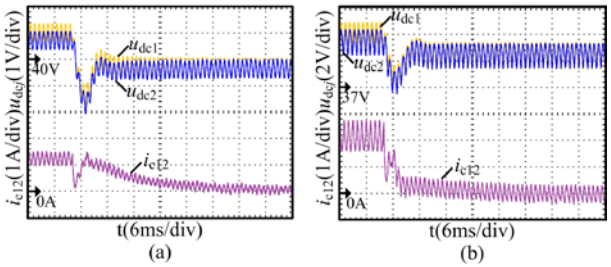

Fig. 23. Experimental results of the output voltage u_{dcj} and circulating current i_{c1j} under the control method A and D with the different number of AC loads. (a) single group AC loads. (b) two groups of AC loads.

VI. Conclusion

In DC MG, when single-phase inverters with AC loads are injected to DC MG, instantaneous output power of single-phase inverters ripples at double output voltage frequency, which leads to generate the SRC. Meanwhile, the circulating current issue will arise if there is a mismatch in the output voltage deviation of parallel ESCs. In this paper, the SRC suppression by two BPFs and current sharing method is proposed, and conclusion is summarized as follow: The SRC suppression method by two BPFs for the ESC not only effectively reduces the SRC, but also improves the dynamic performance of the system at the load mutation. Thus the lifespan of the power converters are improved, and the current stress and conduction loss of the power switches are decreased. An adaptive droop control method by introducing the fine tuning virtual resistances is adopted to reduce the output voltage deviation of parallel ESCs and effectively suppress the circulating current.

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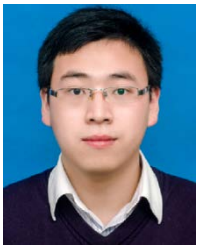

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