

Aalborg Universitet

Reliability-Oriented Optimization of the LC Filter Design of a Buck DC-DC Converter

Liu, Yi; Huang, Meng; Wang, Huai; Zha, Xiaoming; Gong, Jinwu; Sun, Jianjun

Published in: **IEEE Transactions on Power Electronics**

DOI (link to publication from Publisher): 10.1109/TPEL.2016.2619690

Publication date: 2017

Document Version Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):

Liu, Y., Huang, M., Wang, H., Zha, X., Gong, J., & Sun, J. (2017). Reliability-Oriented Optimization of the LC Filter Design of a Buck DC-DC Converter. *IEEE Transactions on Power Electronics*, 32(8), 6323 - 6337. https://doi.org/10.1109/TPEL.2016.2619690

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- ? Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- ? You may not further distribute the material or use it for any profit-making activity or commercial gain ? You may freely distribute the URL identifying the publication in the public portal ?

Take down policy

If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

Downloaded from vbn.aau.dk on: November 29, 2020

Reliability-Oriented Optimization of the LC Filter in a Buck DC-DC Converter

Yi Liu, Student Member, IEEE, Meng Huang, Member, IEEE, Huai Wang, Member, IEEE, Xiaoming Zha, Member, IEEE, Jinwu Gong, and Jianjun Sun, Member, IEEE

Abstract-Lifetime is an important performance factor in the reliable operation of power converters. However, the state-of-the-art LC filter design of a buck DC-DC converter is limited to the specifications of voltage and current ripples and constrains in power density and cost without reliability considerations. This paper proposes a method to optimize the design of the LC filters from a reliability perspective, besides other considerations. An enhanced model is derived to quantify the lifetime of the capacitor in the filter considering the electro-thermal stress on it. Furthermore, the influence of different design aspects like the value of capacitance, the value of inductance, type of the capacitor have been discussed, focusing on their impacts on the key design objectives which are the cut-off frequency, lifetime and volume. Based on the analysis, an optimized design is proposed among different parameter sets. A 1 kW converter prototype is applied to verify the theoretical analysis and simulation.

Index Terms—DC-DC converter, buck converter, LC filter, reliability, capacitor

I. Introduction

DC-DC converters play vital roles in renewable energy, smart grid, aeronautical and navigational electronics [1]. LC filter is a key part in buck type DC-DC converters for reducing the switching harmonics appeared in the output voltage and current [2]. The design of LC filter therefore has a considerable impact on the performance of the converters in terms of functionality, cost, and power density. In [3], multiple objective functions and constraints of the output side capacitors in a buck converter is investigated, including EMC, output voltage ripple, and the number of capacitors connected in parallel. In [4], the load transient specification is further considered and an acceptable boundary curves for buck

Manuscript received April 5, 2016; revised July 12, 2016; accepted October 7, 2016. This work is supported by the National Natural Science Foundation of China (No. 51507118, 51637007), the Hubei Provincial Science and Technology Support Program (No. 2015BAA109), and the Fundamental Research Funds for Central Universities Program (No. 410500078), and was presented in part at the 2015 IEEE Energy Conversion Congress and Exposition (ECCE 2015), Sept. 20--24, 2015, Montreal, Canada.

Y. Liu, M. Huang, X. Zha, J. Gong and J. Sun are with the School of Electrical Engineering, Wuhan University, Wuhan 430072, China (e-mail: aaronlau@whu.edu.cn; meng.huang@whu.edu.cn; xmzha@whu.edu.cn; gongjinwu@whu.edu.cn; jjsun@whu.edu.cn).

H. Wang is with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: hwa@ et.aau.dk).

converter output filter design is obtained. All these design methods concentrate on the filtering function and the electrical aspect performance of the filter.

1

Reliability is an important performance factor especially for power converters in reliability and safety critical applications, such as renewable energy systems under harsh environment [5] and military systems [6]. Therefore, it is highly recommended that reliability can be treated properly since the beginning of the power converter design [7]. For DC-DC converters, semiconductors are vulnerable to electric stress, however these weaknesses can be enhanced by certain protect circuits and control strategy [8]-[9]. With respect to the wear out, the capacitors are considered to be reliability-critical, which may be influenced by the stresses of voltage, current, temperature, humidity, etc. For inductors, it is widely assumed more reliable compared to capacitors. However, the state-of-the-art studies presented in [3]-[4] are limited to design an LC filter by compromising the static and dynamic performance. Other considerations have been investigated in some specific applications. In [10], a hybrid LC filter is designed for motor application based on the frequency behavior estimation. In [11], the EMI suppression of input LC filter in a DC-DC converter and the relevant stability are analyzed. Volume and cost of the components are also considered in the design of LC filter. In [12]-[13], additional circuits are applied to the buck converter in order to minimize the size of output capacitor. In [14], a cost-effective design of inverter output filters is proposed based on the analysis of filter component prices, motor, inverter parameters, and filtering requirements. However, all these design considerations are lack of evaluation on the reliability of the LC filters.

Since the reliability is a critical design objective, methods to enhance the reliability of DC-link capacitors have also been investigated in the previous studies. Some methods have been developed using additional components or circuits to protect the fragile electrolytic capacitor. In [15], film capacitor is paralleled with electrolytic capacitor to relieve the current stress by utilizing their different frequency characteristics. After paralleling a 2 mF film capacitor, the current stress on a 40 mF electrolytic capacitor bank is decreased to 75% of that comparing to the scenario without the film capacitor. Another solution adds an auxiliary circuit working as a regulator to reduce the energy storage requirement of capacitors [16]. In [17]-[18], a bi-directional converter and a transformer are connected in series with the DC-link capacitor to boost up the

capacitor voltage in order to reduce the capacitance or even the removal of the electrolytic capacitor by film capacitor. Instead of using additional components and circuits, it is more easily and cost effective to design the capacitor circuit with higher reliability from the beginning of the design.

An optimized LC filter design is needed with the consideration of reliability aspect performance, especially the lifetime of the capacitors. There are various design variables, such as the values of the capacitance and inductance, the physical formation of a capacitor bank, the selection of the capacitors from product portfolios, which affect the electro-thermal stresses and therefore the reliability of the capacitors. It is worth an effort to identify the influences of those design variables and achieve a compromised design accordingly [19].

Without exceeding the design constraints of electrical specification, volume, and cost, the reliability performance should be considered. Multi-objective design tools can be applied to deal with the problems that concentrate on one or more specific features together with the basic specifications. In [4], the method of acceptability boundary curves is proposed. Acceptability boundary curves are the curves bounding the regions restricted by design objectives which are voltage ripple, load-transient behavior and volume. In [20], ρ – η Pareto optimization is conducted in the trade-off design of six specifications in a three phase AC inverter. The six specifications are output voltage slew rate, transient output voltage dip, bridge-leg output current ripple, output voltage ripple, capacitive reactive power, and EMI. Evolutionary algorithms are also applied in the multi-objective optimization of LC filter design. In [21], the Genetic Algorithms (GA) is used to acquire appropriate parameter values to meet the desired power factor (PF) and Total Harmonic Distortion (THD).

In this paper, a reliability-oriented design for the LC filter in a buck DC-DC converter is proposed with multi-objective optimization. The design methodology is firstly presented in Section II. In Section III, the ripple current spectrum of the output capacitors is analyzed under both continuous current mode (CCM) and discontinuous current mode (DCM) operation, allowing the thermal stress analysis and lifetime prediction of the capacitors. Section IV evaluates the impact of design parameters to three design objectives which are cut-off frequency, capacitor lifetime and total volume. Section V demonstrates a study case of the LC filter design for a 1 kW DC-DC converter, followed by the experimental verification in Section VI and conclusions.

II. RELIABILITY-ORIENTED DESIGN CONCEPT FOR LC FILTER OF BUCK DC-DC CONVERTER

To better take into account both electrical aspect and reliability aspect specifications of DC-DC converters, a reliability-oriented design procedure for LC filter in buck DC-DC converter is proposed as shown in Fig. 1 [19]. It is composed of four major design steps. The first step is to obtain the minimum required values of the inductor and capacitor and

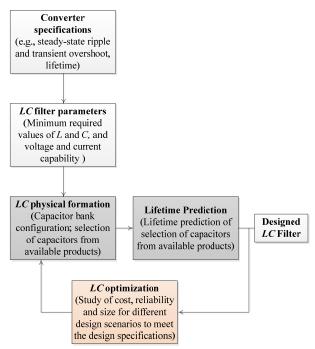


Fig. 1. A reliability-oriented design procedure for *LC* filter of buck DC-DC converter.

the associated voltage and current capability to ensure the basic functionality and fulfill the electrical specifications. The outcome of the first step provides a basis for the physical formation of the LC filter in the second step. Different possible design solutions can be obtained in terms of the chosen values of L and C, the physical capacitor bank configuration, and the choices of those capacitors and inductors from available products in the market. The third step focuses on the corresponding lifetime prediction of the capacitor of various design scenarios. In the final step, the trade-off study among cost, reliability and size of the LC filter is performed to fulfill the specified lifetime at optimal cost and size.

III. LIFETIME PREDICTION OF CAPACITORS IN LC FILTER

Fig. 2 shows a buck converter with input voltage V_{in} and switch function s(t). The voltage across the diode is $v_D = V_{in} \cdot s(t)$. According to superposition theorem, the circuit in the blue block of Fig. 2 is equivalent to a DC voltage source paralleled by AC harmonic voltage sources. As the ESR of capacitor is negligible compared to the load resistance, for sake of simplicity, it is assumed that all the harmonic components go through the capacitor branch and only the DC component of the voltage sources feeds the load. A simplified equivalent capacitor model is also shown in Fig. 2. The ESR of capacitor varies with frequency. The ESR decreases with increasing frequency first and then increases with frequency.

DC sawtooth PWM is one of the main modulation strategies in DC-DC converters. It is implemented by comparing DC modulation wave and high-frequency sawtooth carrier. According to [22], an equivalent element can be used to describe the implementation of DC saw-tooth PWM in one duty cycle. Based on the calculation process of Double Fourier Series, the general expression of switching function can be

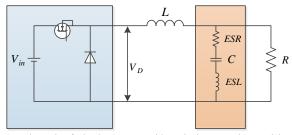


Fig. 2. Schematic of a buck converter with equivalent capacitor model.

written as

$$s(t) = D + \sum_{k=1}^{\infty} \left(s_k^* \cdot \sin(\omega_k t) \right)$$
 (1)

where duty cycle D is the DC component of switching function, and the second part is the AC component at ω_k which is k times of carrier angular frequency. s_k^* is the amplitude of k order harmonic component of switching function. s_k^* of CCM and DCM buck can be derived as

CCM:
$$s_k^* = \frac{2}{\pi k} \sin(\pi k D) \tag{2}$$

DCM:

$$s_{k}^{*} = \frac{2}{\pi k} \sqrt{\frac{\sin^{2}(\pi k D) - \frac{M}{2} \sin(2\pi k D) \sin(\frac{2\pi k D}{M})}{+ M^{2} \sin^{2}(\frac{\pi k D}{M}) - 2M \sin^{2}(\pi k D) \sin^{2}(\frac{\pi k D}{M})}}$$
(3)

where
$$M = \frac{2}{1 + \sqrt{1 + \frac{4V_{in}(V_{in} - V_o)}{V_o^2}}}$$
, $D = \sqrt{\frac{2LfV_o^2}{RV_{in}(V_{in} - V_o)}}$, L is

inductance of the LC filter, R is the load resistance, T is the switching period.

With the harmonic voltage source $v_{hk} = V_{in} \cdot s_k^* \sin(\omega_k t)$ applying on the circuit individually, the root-mean-square (RMS) of harmonic current on the capacitor I_{hk} is

$$I_{hk} = \frac{\sqrt{2} \cdot V_{in} \cdot s_k^*}{2\left(\omega_k L - \frac{1}{\omega_k C}\right)} \tag{4}$$

The internal thermal power of the capacitor consumed on the LC filter is

$$P_T = \sum_{k=1}^{\infty} I_{hk}^2 R_{fk}$$
 (5)

where f_k (k=1, 2, ..., n) is the frequency k times of switching frequency, R_{fk} is the ESR at frequency f_k . Since the amplitude of high order harmonics are insignificant [22], only the first 4 polynomials, which are representing 1st to 4th order harmonics, are considered in the calculation process of (5).

The productions of both electrolytic capacitor and film capacitor can be regard as the parallel-connection of capacitance per unit area. So the ESR of capacitor is inversely proportional to capacitance at the same frequency and voltage level, theoretically. The R_{fk} in (5) can be written as

$$R_{fk} = \frac{K_{Cfk}}{C} \tag{6}$$

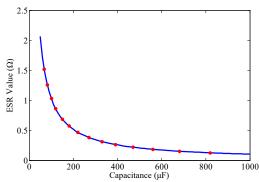


Fig. 3. The relationship of capacitance and ESR at 120 Hz for 400 V CD294 Series from Jianghai Capacitor.

where $K_{C/k}$ is a constant number depending on the frequency, voltage level and the craftsmanship of manufacturers. Fig. 3 plots the relationship of capacitance and ESR at 120 Hz from a 400V CD294 series, and the $K_{C/k}$ of this product is 1.035×10^{-4} (Ω ·F) using the curve fitting.

After the calculation of internal power dissipation, the internal temperature rise of capacitor can be obtained by

$$\Delta T = R_{th} \cdot P_T \tag{7}$$

where R_{th} is the thermal resistance from capacitor core to the case.

The lifetime model of the capacitors varies with manufacturers. The following one is widely used that can represent a wide range of both electrolytic capacitors, and film capacitors for buck DC-DC converter applications [23].

$$L_{x} = L_{o} \cdot \left(\frac{V}{V^{*}}\right)^{-n} 2^{\frac{T_{o} - T_{x}}{10}} \cdot 2^{-\frac{\Delta T}{K_{T}}}$$
(8)

where L_x is the lifetime of capacitor, L_o is the lifetime of capacitor when it is working at the rated upper operational temperature and rated voltage, V and V^* are working voltage and rated voltage respectively, for electrolytic capacitors, the exponent n is from around 3 to 5 among different manufacturers [7], T_o and T_x are the limit working temperature and environmental temperature respectively, ΔT is the temperature rise inside the capacitor. K_T is a constant from 5 to 12 depending on the products from different manufactures [7].

By solving equation (1) to (8), the lifetime of the capacitor of a LC filter in buck converter can be obtained.

ESR and thermal resistance R_{th} are temperature dependent [24]. Fig. 4 plots the relationship of ESR and frequency under different temperature levels, as well as the relationship of thermal resistance and temperature under different wind velocity. It can be seen from Fig. 4 that the temperature have nearly no impact thermal resistance. Hence, all the thermal resistance value treated as constant in this paper, and the value with no wind velocity is applied. Considering the temperature have certain influence on ESR, a more precise internal temperature rise can be obtained by the method defined in Fig. 5 with datasheets from the manufacturers. If the manufacturers can provide the function of ESR and temperature, solving following equation (9) can also obtain the inherent temperature rise of with improved accuracy.

TPEL-Reg-2016-04-0629 4

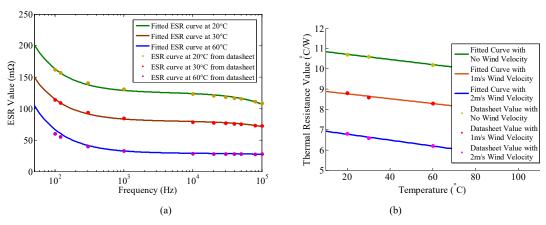


Fig. 4. (a) ESR value at different temperature with corresponding fitting curves for 400 V CD294 Series from Jianghai Capacitor. (b) Thermal resistance value at different wind velocity with corresponding fitting curves for 400 V CD294 Series from Jianghai Capacitor.

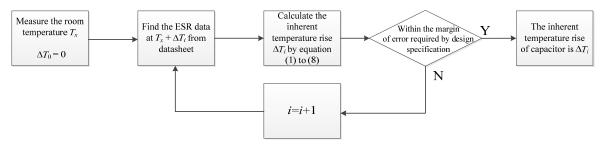


Fig. 5. The process of obtaining the capacitor internal temperature rise by datasheet.

 PARAMETER USED IN THE STUDY CASE

 Parameter
 Value

 V_{in} 285 V

 V_{out} 114 V

 f_s 10 kHz

 R 13 Ω

 Range of L 150 μH-3 mH

 Range of C 150 μF-3000 μF

$$R_{\theta} \sum_{k=1}^{\infty} R_{fk} (T_x) \cdot i_{ck}^2 = T_x - T_R$$

$$\tag{9}$$

where T_x and T_R are capacitor inherent temperature rise and room temperature, respectively. In (9), R_{fk} is the function of T_x , and T_x changes on both sides of equation (9) at the same time. Iterative algorithm, such as Newton's method, can be applied to solve (9) [25].

As shown in Fig. 5, an initial ESR value is firstly obtained based on a specific temperature level, then the internal temperature raise and hotspot temperature of the capacitor can be calculated, which is corresponding to an updated ESR value. The error indicated in Fig.5 is defined as the difference between the estimated hotspot temperatures based on this updated ESR value and the initial ESR value. The "margin of error" is the selected maximum error allowed in the hotspot temperature estimation (a margin of error of 0.1 °C is used in the specific case study). The iteration process continues until the error is within the selected "margin of error".

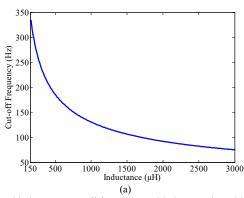
IV. THE INFLUENCE OF DESIGN PARAMETERS ON THE DESIGN OBJECTIVES

The impact of the LC filter design parameters (i.e., inductance, capacitance and ESR value) on the design objectives (i.e., cut-off frequency, lifetime, power density and cost) is discussed in this section. In order to illustrate the objectives from a practical design-point of view, a 1 kW buck converter is taken as an example. The key specifications of the buck converter are shown in Table I. The peak current on the filter inductor is 28 A when the inductance is 150 µH. Since the iron dust core will be easily saturated with a higher peak current over 30 A, an inductance of 150 µH is selected as the minimum inductance in the parameter range. With the inductance fixed at the minimum value of 150 µH, a minimum capacitance of 150 μF can be adopted for the requirement of cut-off frequency 1 kHz. So the minimum capacitance is selected as 150 μF. The upper ranges of inductance and capacitance can be selected as 3 mH and 3000 µF with the consideration of volume and cost.

As the Partial Differentiation is a common tool to evaluate the influence of parameters [26], an operator *S*, which is with respect to each design objective, is defined as following formula to reflect the sensitivity of the parameters on the design objectives.

$$S(Object) \mid_{Parameter} = \ln \left| \frac{\partial F_O(p)}{\partial p} \right|$$
 (10)

TPEL-Reg-2016-04-0629 5



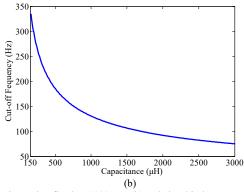


Fig. 6. (a) Relationship between cut-off frequency and inductor value with capacitor value fixed at $1000~\mu F$; (b) Relationship between cut-off frequency and capacitor value with inductor value fixed at $1000~\mu H$.

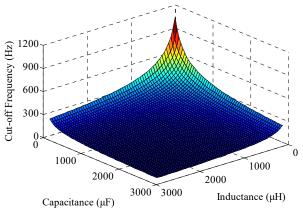


Fig. 7. The relationship of cut-off frequency, capacitance and inductance.

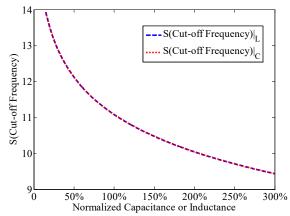


Fig. 8. The relationship between filter capability-operator and each parameter.

where $F_O(p)$ is the function of the objective, and p is the investigated parameter, such as L, C, and ESR. The value of L, C and ESR can be varying due to different design or different working conditions. In this value interval, the values of the partial derivative are very large, so using the logarithm operation can simplify the calculation and comparison. As ceramic capacitors and film capacitors can be applied in the DC-link filters, a comparison of different capacitors is given in the final part of this section.

According to the dielectric, industrial electrical capacitors

TABLE II ELECTROLYTIC CAPACITOR PARAMETERS USED IN THE LC FILTER

Parameter	Value
Capacitance	$150~\mu F - 3000~\mu F$
Rated Lifetime	1000 hours
T_{O}	105 °C
T_x	25 °C
K_T	5
$K_{C 10 \mathrm{kHz}}$	3.708×10^{-4}
$K_{C20\mathrm{kHz}}$	3.642×10^{-4}
$K_{C30\mathrm{kHz}}$	3.624×10^{-4}
$K_{C40\mathrm{kHz}}$	3.577×10^{-4}

are categorized into electrolytic capacitor, film capacitor, ceramic capacitor and other solid dielectric capacitors (e.g., tantalum capacitors). However, the cost of the solutions based on ceramic capacitors and tantalum capacitors could be significantly higher by considering the capacitance requirements of the analyzed buck converter. What is more, there are limited capacitance value for a single ceramic capacitor or capacitor module (e.g., 20 μF for Ceralink capacitors from TDK-EPCOS), and limited voltage rating of tantalum capacitors (e.g., up to 150 V for commercialized products) which requires also relatively large voltage de-rating. Therefore, in the presented study case, aluminum electrolytic capacitors and film capacitors are considered as the candidates as the major capacitive components.

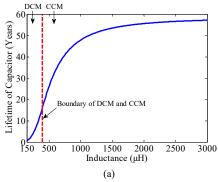
A. Cut-off frequency

The ability of a filter to reduce harmonics depends on the designed cut-off frequency which is described as follow

$$f_C = \frac{1}{2\pi\sqrt{LC}} \tag{11}$$

where L and C are inductance and capacitance of the filter respectively.

Fig. 6 and Fig. 7 plot the relationship between cut-off frequency and inductor value, capacitor value in 2D and 3D, respectively. The relationships of sensitivity-operator S-(Cut-off frequency) and parameters (L and C) are plot in Fig. 8. The x-axis is the percentage of investigated parameter value out of the reference parameter value of 1 mH inductance and 1000 μ F capacitance. The percentage is applied in the aim of



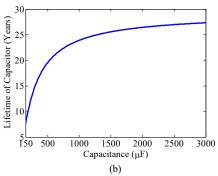


Fig. 9. (a) The lifetime variation according to different inductor values where capacitor value fixed at 1000 μF. (b) The lifetime variation according to different capacitor values where inductor value fixed at 1 mH.

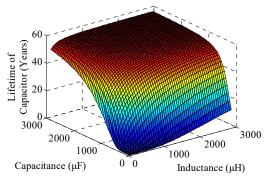


Fig. 10. The relationship of capacitor lifetime, capacitance, and inductance.

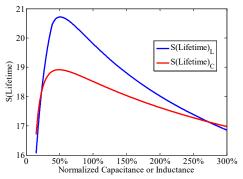


Fig. 11. Relationship between the lifetime-operators and the design parameters (L, C).

comparing different parameters, and y-axis is S-(Cut-off frequency) calculated from (11). Take the calculation of the operator S-(Cut-off frequency)|L for an instance,

$$S(Cut - off \ frequency)|_{L} = \ln \left| \frac{\partial F_{O}(L)}{\partial L} \right|$$

$$F_{O}(L) = \frac{1}{2\pi\sqrt{LC^{*}}}$$
(12)

$$F_O(L) = \frac{1}{2\pi\sqrt{LC^*}} \tag{13}$$

where C^* is the reference capacitor value fixed at 1000 μ F. When substituting $F_0(L)$ into the equation (12), the operator S-(Cut-off frequency) $|_L$ will be

$$S(Cut - off \ frequency)|_{L} = \ln \frac{1}{4\pi\sqrt{L^{3}C^{*}}}$$
 (14)

In a likewise method, the operator S-(Cut-off frequency) $|_{\mathbb{C}}$ can be calculated. The curves of inductor and capacitor are overlapped in Fig. 8, which indicating that the inductance and the capacitance have the same impact on the cut-off frequency.

B. Lifetime

The lifetime of the LC filter can be quantified by the means of predicting the lifetime of output capacitor which is calculated from equations (1) to (8) in Section III. Fig. 9 plots the relationship between lifetime of capacitors and each parameter. For example, in Fig. 9 (a), the capacitor is fixed at 1000 µF. Therefore, the lifetime of the LC filter can be calculated by switching function from equation (2) or (3) according to different operation modes depending on the inductor values. The calculated relationship can be shown in Fig. 9 (a). In a likewise method, the Fig. 9 (b) can be plotted according to the designed capacitance. Fig. 10 shows the 3D plot of the relationship of lifetime and design parameters.

Fig. 11 shows the sensitivity of each parameter on the lifetime of LC filter. In the calculation of operator S-(Lifetime) $|_{L}$, $F_O(L)$ is lifetime calculated in DCM or CCM according to different inductance. After submitting lifetime model into (10), operator S-(Lifetime)|_L will be calculated. In a similar way, S-(*Lifetime*) $|_C$ can be obtained.

In Fig. 11, both the operator S-(Lifetime) $|_L$ and S-(Lifetime) $|_C$ increase rapidly with the inductance first, then decrease in a relatively slowly speed. Unlike the design of cut-off frequency, the value of S-(Lifetime) $|_L$ and S-(Lifetime) $|_C$ not always the same in the design of reliability. As S-(Lifetime) $|_L$ valued higher than S-(Lifetime) $|_C$ after experience a comparative range, the inductor value plays a more significant role in the design of reliability.

C. Volume

1) Inductor

The following formula is a definition of inductance value widely used in industrial application

$$L = A_l \cdot N^2 \tag{15}$$

where N is the number of windings, A_l is the inductance factor defined as follow

$$A_{l} = \frac{\mu_0 \mu_r S_C}{l_m} \tag{16}$$

where S_C is the cross-sectional area of the ferrite core, l_m is the length of magnetic path, μ_0 and μ_r are permeability of vacuum and relative permeability respectively.

Fig. 12 shows a toroidal core of which OD and ID are outer

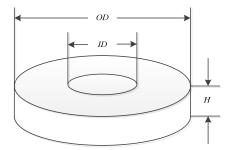


Fig. 12. Toroidal core of an inductor.

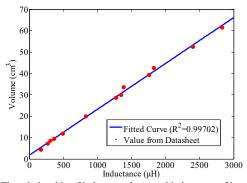


Fig. 13. The relationship of inductor volume and inductance of iron dust core from Pocomagnetic NPS series [27].

diameter and inner diameter respectively, and H is the height. To stay away from the saturation point and simplify the craftsmanship, the inductors are often manufactured compacted one layer. Then the number of windings N can be calculated as

$$N \approx \pi \frac{ID - WD}{WD} \tag{17}$$

where WD is the diameter of the wire. Substituting (17) and (18) into (16), the general expression of inductance will be

$$L = \mu_0 \mu_r H \cdot \left(\frac{ID - WD}{WD}\right)^2 \left(\frac{OD - ID}{OD + ID}\right)$$
 (18)

Ignored the volume of wire, the space volume of the inductor is

$$V_{L-space} = \pi \cdot OD^2 \cdot H \tag{19}$$

Fig. 13 shows a fitting curve of a series of inductor product with μ_r fixed at 160 and WD fixed at 1 mm. The minimum inductance is selected as 150 μ H in the consideration of core saturation. Also, the volume of the inductor could be large in order to avoid the magnetic saturation. But in fact, it is not necessary to use very large volume for a specific practical converter. Here, the 1 kW converter is considered, and the peak inductor current would not exceed 30 A. The inductor can be designed within this range and it can be seen that $V_{L-space}$ and inductance are in accordance with the linear relationship

2) Capacitor

Commonly, electrolytic capacitor is parallel-plate capacitor rolled up by winding technology. Fig. 14 shows the winding process. The capacitance of parallel-plate capacitor is defined as

$$C = \frac{\varepsilon_0 \varepsilon_r S}{d} \tag{20}$$

where ε_0 and ε_r are vacuum permittivity and relative permittivity respectively, S is the area of plate, d is the length

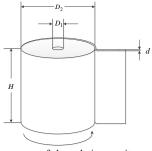


Fig. 14. The winding process of electrolytic capacitor.

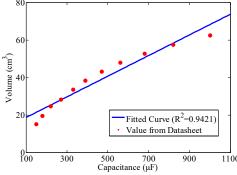


Fig. 15. The relationship of capacitor volume and capacitance of 400V CD294 series capacitor from Jianghai Capacitor [28].

between two plates.

In electrolytic capacitor, the dielectric is Al_2O_3 and the ε_r is between 8-10, and d is the thickness of the two aluminum foils, S is the area of aluminum foil. After corrosion, it is very hard to get the precise value of S. Assuming the corrosion of aluminum is uniform, then the area of aluminum foil S will be multiple of the area of plate S_p . If S is k_1 times of S_p , (20) will be

$$C = k_1 \frac{\varepsilon_0 \varepsilon_r S_p}{d}$$

From the Fig. 14, S_p can be calculated as $S_p = \frac{\pi (D_2^2 - D_1^2)H}{4d}$

and thickness d is proportional to rated voltage V_{C0} . As D_1 is very small relative to D_2 , the capacitance of electrolytic capacitor can be written as

$$C \approx \frac{k_1 \varepsilon_0 \varepsilon_r \pi D_2^2 H}{4d^2} = \frac{k_1 \varepsilon_0 \varepsilon_r V_{C-space}}{4k_2^2 V^{*2}}$$
 (21)

where $V_{C\text{-space}}$ and k_2 are capacitor volume and proportionality coefficient of d and V^* respectively. So in industrial products, the volume of capacitor can be expressed as following formula

$$V_{C-space} = k_{C-space} CV^{*2}$$
 (22)

where $k_{C\text{-space}}$ is the coefficient described the linear relationship. $k_{C\text{-space}}$ is hard to be calculated theoretically, but (16) provides a formula for curve fitting. Fig. 15 plots the fitting curve of capacitor volume and capacitance. The dotted points in Fig. 15 are from 400V CD294 series product.

3) Total Volume

According to (19) and (22), the total volume of the LC filter can be obtained. Fig. 16 shows the 3D plot of total volume, capacitance and inductance. As the inductance and capacitance are linear to volume, the operator S-(Volume) $|_L$ and S-(Volume) $|_C$ are constant.

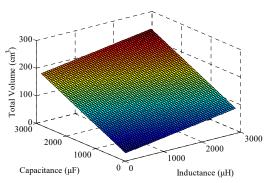


Fig. 16. The relationship of total volume, capacitance and inductance.

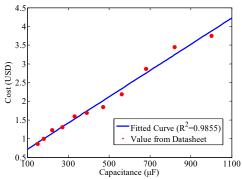


Fig. 17. The relationship of inductor cost and inductance of 400V CD294 series capacitor from Jianghai Capacitor [28].

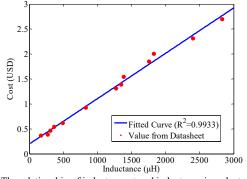


Fig. 18. The relationship of inductor cost and inductance iron dust core from Pocomagnetic NPS series [27].

D. Cost

The cost of a given series of electrolytic capacitor scales with the rated store energy. The cost model of capacitor is defined as follow in [30].

$$Cost_C = a_C CV^{*2} + b_C V^*$$
 (23)

where a_C and b_C are two constants obtained from curve fitting of cost data. V^* is the rated voltage.

For inductors, a large fraction of the total cost can be explained by the material and labor cost. The cost model can also be found in [30]

$$Cost_{L} = Cost_{mat} + Cost_{lab}$$
 (24)

where

$$Cost_{mat} = \sigma_{Core-price}W_{Core} + \sigma_{Winding-price}W_{Winding} + Cost_{mat.x}$$
(25)

$$Cost_{lab} = \sigma_{lab-price} W_{Winding} + Cost_{lab.x}$$
 (26)

TABLE III
FILM CAPACITOR PARAMETERS USED IN THE STUDY CASE

Parameter	Value
Rated Voltage	400 V
Capacitance	150 μF-3000 μF
Rated lifetime	100000 hours
T_{O}	70 °C
T_x	25 °C
K_T	10
$K_{C 10 \mathrm{kHz}}$	2.276×10^{-6}
$K_{C20\mathrm{kHz}}$	2.486×10^{-6}
$K_{C30\mathrm{kHz}}$	2.707×10^{-6}
$K_{C ext{ 40kHz}}$	2.872×10^{-6}

 $\sigma_{Core-cost}$, $\sigma_{Winding-cost}$ and $\sigma_{lab-cost}$ are specific cost per weight W_{Core} , $W_{Winding}$ of the core and winding. Like the discussions of inductor volume, very expensive material and complex structure would not be necessary for a simple DC-DC converter. Here, the iron dust core from NPS series is used and a peak current of 30 A is considered. The cost of the inductor also has a linear relationship with the inductance.

Since the inductance and capacitance are linear related to the cost, the operator S-(Cost) $|_L$ and S-(Cost) $|_C$ are constants.

E. Film Capacitor vs. Electrolytic Capacitor

1) Lifetime of Film Capacitor

The lifetime model of film capacitor follows the formula of (8), the exponent n is typically from around 7 to 9.4 used by leading capacitor manufacturers [31]. Unlike the aging mechanism of electrolytic capacitor, the aging extent of solid electrode brought by temperature is a slower process than the evaporation of electrolyte [31]. This contributes to a higher constant value of K_T in (8). The other significant difference of film capacitor is its lower ESR value, implying larger ripple current capability.

Table III has the parameters of the investigated film capacitor. Fig. 19 shows the variation of lifetime. 3-D figure is also plotted in Fig. 20, from which the distribution of parameters and the lifetime can be seen.

2) Film Capacitor Volume and Cost

Winding technology is also applied in the manufacturing of high-capacitance film capacitor. Similar to electrolytic capacitor, the volume of film capacitor will be

$$V = \frac{Cd^2}{\varepsilon_0 \varepsilon_r} \tag{27}$$

where V is the volume of capacitor, ε_0 and ε_r are vacuum permittivity and relative permittivity respectively, d is the thickness between two films.

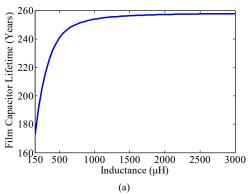
In film capacitors, the dielectric is polypropylene (PP), and ε_r is 2.2. The thickness of film is 3-6 μm . However, in the winding process, the gap brought by winding machine is very hard to calculate. So the curve method is also applied in the discussion of film capacitor volume.

In [30], the cost model of capacitor is defined as follow

$$Cost_{FilmC} = a_{FilmC} + b_{FilmC}C + c_{FilmC}V^*$$
 (28)

where a_{FilmC} , b_{FilmC} and c_{FilmC} are the constants obtained from curve fitting of cost data, and V^* is the rated voltage.

Fig. 21 plots the relationship of the capacitance and volume of capacitor. Unlike the electrolytic capacitor, the dielectric is



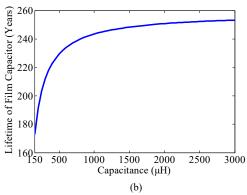


Fig. 19. (a) The relationship of film capacitor lifetime and inductance with capacitance fixed at 150 μ F. (b) The relationship of film capacitor lifetime and capacitance with inductance fixed at 150 μ H.

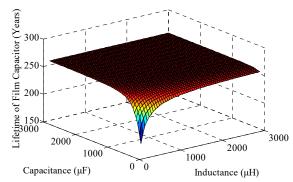


Fig. 20. The relationship of film capacitor lifetime and design parameters.

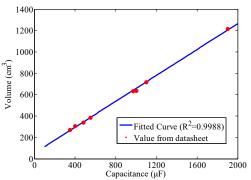


Fig. 21. The relationship of film capacitor volume and capacitance of 400V customized MKP-FS series film capacitor from CSD Capacitor [29].

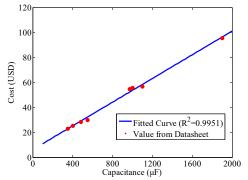


Fig. 22. The relationship of film capacitor cost and capacitance of 400V customized MKP-FS series film capacitor from CSD Capacitor [29].

well-distributed in film capacitor, and the relationship of film capacitor and its volume is more linear. Fig. 22 plots the

relationship of the capacitance and cost of film capacitor.

Compared to electrolytic capacitor, film capacitor can extend capacitor lifetime significantly. However, the volume and cost are enormous. It is not advisable to use film capacitor in this application for its low power density.

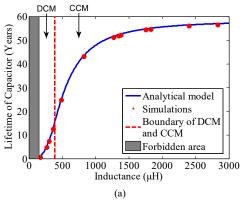
V. RELIABILITY-ORIENTED DESIGN OF LC FILTERS OF A 1 KW BUCK CONVERTER

In this section, the study case of a 1 kW buck converter is implemented to verify previous analysis. The design specifications are list as Table I in Section IV. The design parameters are the same as Table I. For the simulation study, the considered inductance values for CCM and DCM operation are from 390 μ H to 3000 μ H and from 150 μ H to 390 μ H, respectively. The main design objectives in this study case are the cut-off frequency, the total volume of LC and the lifetime, as shown in Table IV.

It is worth mention that the capacitor lifetime in Table IV is based on the continuous operation scenario of the analyzed buck converter. For a given application with long-term operation profile (i.e., loading levels with time), it could take into account the interruptions and loading variations. But there is still lifetime consumption on the capacitors when the converter is in standby mode or fully shutdown mode due to thermal-related wear out mechanisms. Therefore, for the sake of simplicity, we focus on the design methodology based on the rated operation load without considering the interruptions. Moreover, the lifetime model applied for the capacitors is B10 lifetime, which is the time when 10% of the items of interest fail [32]. It is reasonable to set the B10 lifetime target over 15 years for a B10 lifetime target of 5 to 10 years in applications, since other components contribute to the converter level failure as well.

From Section IV, it can be noted that both volume and cost are conformed to linear relationship and share the same trend. So in this Section, only the objective of "Total volume" is analyzed. In the end of this section, the cost of different parameter sets will be represented with other objectives. As the film capacitor is not favorable in this application, only electrolytic capacitor is analyzed in this section.

When the buck converter is operating, the RMS value of capacitor currents at each carrier band I_C , and the corresponding



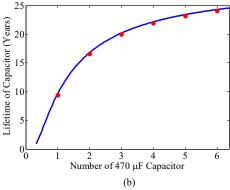


Fig. 23. Lifetime calculated from the analytical model and simulations. (a) Capacitor lifetime under different inductor value when C=1410 μ F. The forbidden area indicates the inductor value that cannot meet design spec. (b) Lifetime under different Nc when L= 620 μ H.

Design Objectives	Design Requirements
Cut-off Frequency	≤ 250 Hz
Capacitor Lifetime	≥ 15 Years
Total Volume	$\leq 120 \text{ cm}^3$

TABLE V COMPARISON OF THE EXPERIMENTED AND CALCULATED AMPLITUDE OF CAPACITOR CURRENT

	DCM(L =200 μ H, N_c =3)		CCM(L =500 μ H, N_c =3	
Frequency (Hz)	$I_{C}\left(\mathbf{A}\right)$	$Ic^*(A)$	$I_{C}\left(\mathbf{A}\right)$	$Ic^*(A)$
10k	12.60	12.97	5.31	5.53
20k	1.41	1.43	0.81	0.85
30k	0.45	0.47	0.36	0.38
40k	0.82	0.86	0.32	0.34

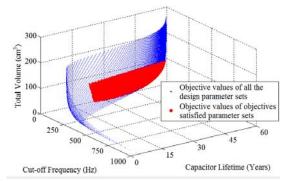


Fig. 24 The distribution of design objective points.

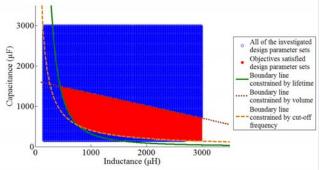


Fig. 25 The distribution of design parameters with boundary referred to each design objective.

calculated ones I_C^* are shown in Table V. It can be noted that the differences between I_C and I_C^* are negligible.

Based on the capacitor current, it can be inferred from Section IV that the lifetime of the output capacitor is influenced by the value of both inductor and capacitor. Fig. 23 plots the relationship of capacitor lifetime and inductance, capacitance according to the capacitor current value. In Fig. 23, the blue curve is lifetime calculated by I_C from (4), the red points are lifetime calculated by I_C^* from the simulation.

From Fig. 23, it can be noted that there is a tradeoff between the capacitor lifetime and the volume or cost of the inductor and capacitor. With large value of inductor and large number of capacitors, the fragile capacitor can achieve a long lifetime. However, the cost and volume of system should be taken into consideration. Therefore, it is worth designing the LC filter carefully to achieve an optimized choice for the parameters of LC filter.

The design requirements are shown in Table IV, which are cut-off frequency lower than 250 Hz, lifetime more than 15 years, and total volume less than 70 cm³. Based on the parameter analysis in Section IV, the distribution of the satisfied points among all the investigated ones is plotted in Fig. 24. A surface vertical to numbers will have a design object which is represented by the cut-off frequency, volume, and lifetime. All these results are shown as the blue dots in Fig. 24, as the "investigated design parameter sets". However, only parts of the design sets are satisfying the design objective. The "objects satisfied design parameter sets" can be easily found from the figure, which are painted by the red color. It is shown that, considering lifetime constrains, the inductor and capacitor values should be chose more carefully to achieve good performance and long lifetime.

The relationship can be seen more clearly and directly from Fig. 25 with inductor and capacitor values. The corresponding parameter sets are shown in Fig. 25. The possible inductor and capacitor values are shown in this figure. However, the boundary of the value can be given through cut-off frequency, volume and lifetime constrains, which are shown as the red, yellow and green curves in the figure. The boundary lines referred to each objective are also plotted in Fig. 25, which can explain how each object constrains the design parameters.

TABLE VI DESIGN PARAMETERS OF THE STUDY CASE

Design Parameter	Range
L	200 μΗ-800 μΗ
<i>C</i>	470 μF-2820 μF

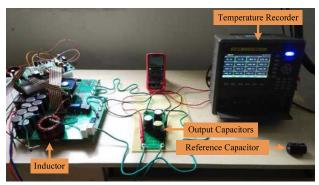


Fig. 26. Experimental prototype of a 1 kW buck converter.

VI. EXPERIMENT VERIFICATIONS

A 1 kW buck converter with the same parameters in Table VI is implemented to verify the analysis. The ranges of investigated inductance and capacitance are selected from the range of inductance in Table I. As the inductance over $800 \mu H$ has slight impact on cut-off frequency and capacitor lifetime, the range of inductance is selected as $200 \mu H$ -800 μH . For simplicity, only 400 V $470 \mu F$ CD294 type electrolytic capacitor is considered. Different capacitance is realized by different numbers of capacitors. The investigated number of $470 \mu F$ capacitors N_c connected in parallel is from 1 to 5. The

Iek Stop Noise Filter Off $I_L = 10 \, A \, / \, div$ Time Scale: $40 \, \mu \text{S/div}$ [a) Noise Filter Off $I_L = 10 \, A \, / \, div$ Time Scale: $40 \, \mu \text{S/div}$ Time Scale: $40 \, \mu \text{S/div}$ [a) Noise Filter Off $I_L = 10 \, A \, / \, div$

prototype used in the experiment is shown in Fig. 26.

Three design parameter sets are implemented to verify the previous analysis, which are shown in Table VII. 2 sets (Set A and Set B) are from design requirements unsatisfied parameter sets and 1 set (Set C) is from requirements satisfied sets in Fig. 25.

Thermocouple is used to measure the internal temperature rise of the output capacitor. As shown in Fig. 26 a capacitor with thermocouple is set as a reference to measure the room temperature. Temperatures are recorded by the temperature recorder every 30 seconds. Fig. 27 and Fig. 28 plot the waveform, FFT results and the temperature variation of the 3 investigated parameter sets. Table VIII shows the objectives of each parameter set. It can be seen that the inside temperature of capacitor is reduced significantly with the requirements satisfied LC sets.

More experimental results can be seen in Fig. 29 and Table IX to Table XI. Fig. 29 represents the inherent temperature rise of different parameter sets. Table IX shows the influence of inductance on design objectives. Four objectives, which are output ripple voltage, inherent capacitor temperature rise, total volume and cost are compared quantitatively.

Table X records the experimental results in the same way. The calculated temperature rise is based on ESR at 20 °C. As ESR decrease with temperature and the room temperature is 20 °C, the calculated temperature rise is higher than real. This can be modified by solving (9) with iterative algorithm.

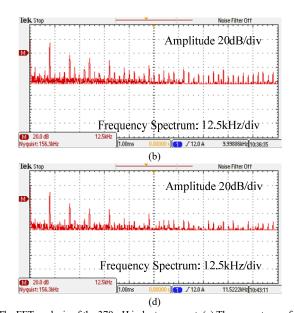


Fig. 27. Experimental results: (a) The current waveform of 370 μ H inductor; (b) The FFT analysis of the 370 μ H inductor current. (c) The current waveform of 620 μ H inductor; (d) The FFT analysis of the 620 μ H inductor current.

Table VII
INVESTGATED DESIGN PARAMETER SETS

	Design Parameter Set A	Design Parameter Set B	Design Parameter Set C
Inductance	370 μΗ	370 μΗ	620 μΗ
Number of 470 µF capacitors	1	6	3

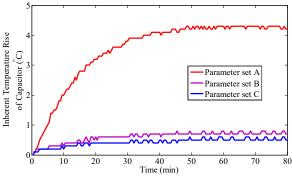


Fig. 28. Experimental results: The internal temperature rise recorded by temperature recorder.

Table VIII
OBJECTIVE VALUES OF THE INVESTIGATED PARAMETER SETS WITH CALCULATED AND MEASURED INTERNAL TEMPERATURE RISE.

Parameter Set	Cut-off Frequency (Hz)	Capacitor Lifetime (Years)	Total Volume (cm ³)	Calculated Internal Temperature Rise (°C)	Measured Internal Temperature Rise (°C)
A	381	1.3	48	4.48	4.2
В	156	17	178	0.75	0.7
C	170	20	106	0.53	0.5

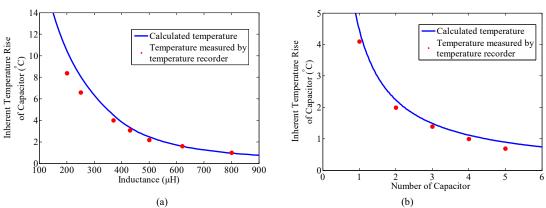


Fig. 29. Experiment results: Internal temperature rise of capacitor measured by the temperature recorder. (a) Temperature under different inductance with one 470 μF capacitors. (b) Temperature under different number of capacitor with inductance fixed at 370 μH.

 $Table\ IX$ Experiment Results: The Performance of the Converter under Different Inductance Value with One 470 μF Capacitor.

	Output Voltage Ripple (V)	Internal Temperature Rise of Capacitor (°C)	Total Volume of Inductor and Capacitors (cm ³)	Total Cost (USD)
200 μΗ	0.3	8.4	45.24	2.40
250 μΗ	0.24	6.6	46.31	2.44
370 μΗ	0.16	4.0	48.87	2.55
430 μΗ	0.14	3.1	50.16	2.60
500 μΗ	0.13	2.2	51.66	2.67
620 μΗ	0.11	1.6	54.24	2.78
800 μΗ	0.07	1.0	58.09	2.94

Table X Experiment Results: The Performance of the Converter under Different Number of 470 μ F Capacitors with Inductance Fixed at 370 μ H

	Output Voltage Ripple (V)	Internal Temperature Rise of Capacitor (°C)	Total Volume of Inductor and Capacitors (cm ³)	Total Cost (USD)
1	0.3	4.2	48.87	2.55
2	0.15	2.0	74.80	4.20
3	0.11	1.4	100.73	5.84
4	0.07	1.0	126.65	7.50
5	0.05	0.7	152.58	9.13

Table XI Experiment Results: The Performance of the Converter under Different Inductance Value with One 470 μ F FILM Capacitor.

Inductance	Output Voltage Ripple (V)	Internal Temperature Rise of Capacitor (°C)	Total Volume of Inductor and Capacitors (cm ³)	Total Cost (USD)
200 μΗ	0.3	0.2	780.72	30.24
370 μΗ	0.11	0.1	868.68	31.10

As film capacitor has lower ESR than Electrolytic Capacitor of same capacitance, the impedance of film capacitor is smaller. After paralleling the film capacitor, electrolytic capacitor branch shares less current, this can reduce the internal temperature of the capacitor to a certain extent. Table XI shows the performance of converter after paralleling the film capacitor to circuit. It can be seen that the inside temperature rise of film capacitor is tiny compared to electrolytic capacitor. However, film capacitors of high capacitance are of large volume and expensive.

VII. CONCLUSION

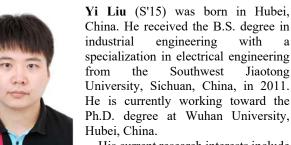
In this paper, a method to optimize the design of the LC filters from a reliability perspective, besides other considerations is presented. A lifetime model of capacitor based on electro-thermal stresses analysis of different design parameters is proposed. The influence of design parameters on cut-off frequency, lifetime and volume are analyzed. The distribution of design objectives of a 1 kW buck converter under different parameter sets is plotted, and the study reveals the design trade-offs to fulfill a specific lifetime requirement of the applied capacitors. The theoretical analysis and simulation results are verified by a 1 kW buck prototype.

REFERENCES

- [1] J. W. Kolar, T. Friedli, F. Krismer, A. Looser, M. Schweizer, R. A. Friedemann, P. K. Steimer, and J. B. Bevirt, "Conceptualization and Multiobjective Optimization of the Electric System of an Airborne Wind Turbine," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 73-103, Jun. 2013.
- [2] P. Pelletier, J. M. Guichon, J. L. Schanen, "Optimization of a DC capacitor tank," *IEEE Transactions on Industry Applications*, vol. 45, no. 20, pp. 880-886, Mar.-Apr. 2009.
- [3] Johanson Dielectrics INC. Technical Note *DC-DC* converter trends and output filter capacitor requirements, 2006.
- [4] A. D. Nardo, N. Femia, G. Petrone, G. Spagnuolo, "Optimal buck converter output filter design for point-of-load applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1330-1341, Apr. 2010.
- [5] K. Ma, M. Liserrer, F. Blaabjerg, "Lifetime estimation for the power semiconductors considering mission profiles in wind power converter," in Proc. IEEE Energy Conversion Congress and Exposition, 2013, pp. 2962-2971.
- [6] E. J. Yoo, T. Y. Lee, W. Y. Choi, Y. W. Park, "Low temperature evaluation of commercial DC/DC converters for military applications," in Proc. TENCON 2010 IEEE Region 10 Conference, 2010, pp. 1247-1250.
- [7] H. Wang, F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—an overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569-3578, Sep.-Oct. 2014.
- [8] D. P. Sadik, J. Colmenares, G. Tolstoy, D. Peftitsis, M. Bakowski, J. Rabkowski, and H. P. Nee, "Short-Circuit Protection Circuits for Silicon-Carbide Power Transistors," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 4, pp. 1995-2004, Sep. 2016.
- [9] T. Horiguchi, S. Kinouchi, Y. Nakayama, T. Oi, H. Urushibata, S. Okamoto, S. Tominaga, and H. Akagi, "A High-Speed Protection Circuit

- for IGBTs Subjected to Hard-Switching Faults," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1774-1781, Mar.-Apr. 2015.
- [10] V. Dzhankhotov and J. Pyrhönen, "Passive LC Filter Design Considerations for Motor Applications," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 1430–1443, Oct. 2011.
- [11] M.Iftikhar, D. Sadarnac, C.Karimi, "Conducted EMI Suppression and Stability Issues in Switch-mode DC-DC Converters," in Proc. IEEE Multitopic Conference, INMIC '06., 2006, pp. 389-394.
- [12] D. Lu, J. Liu, F. Poon, and B. Pong, "A single phase voltage regulator module (VRM) with stepping inductance for fast transient response," *Transactions on Power Electronics*, vol. 22, no. 2, pp. 417–424, Mar. 2007.
- [13] T. Senanayake and T. Ninomiya, "An improved topology of inductor-switching DC–DC converter," *Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 869–878, Jun. 2005.
- [14] J. Salomaki, M. Hinkkanen, and J. Luomi, "Cost-Effective Design of Inverter Output Filters for AC Drives," in Proc. IEEE Industrial Electronics Conference, 2007, pp. 1220-1226.
- [15] M. A. Brubaker, D. E. Hage, T. A. Hosking, H. C. Kirbie, and E. D. Sawyer, "Increasing the life of electrolytic capacitor banks using integrated high performance film capacitors," in Proc. Europe Power Conversion Intelligent Motion (PCIM), 2013.
- [16] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4778–4794, Jul. 2015.
- [17] R. Wang, F. Wang, D. Boroyevich, P. Ning, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1430–1443, May. 2011.
- [18] P. Krein, R. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.
- [19] Y. Liu, M. Huang, H. Wang, X. Zha, J. Gong and J. Sun, "Reliability-oriented design of LC filter in buck DC-DC converter," in Proc. IEEE Energy Conversion Congress and Exposition, 2015, pp 1427-1433.
- [20] D. Boillat, F. Krismer, and J. Kolar, "Design Space Analysis and ρ-η Pareto Optimization of LC Output Filters for Switch-Mode AC Power Sources," *Transactions on Power Electronics*, vol. 30, no. 12, pp. 6906–6923, Dec. 2015.
- [21] Y. Chen, "Passive Filter Design Using Genetic Algorithms," Transactions on Industrial Electronics, vol. 50, no. 1, pp. 202–207, Feb. 2003.
- [22] B. P. McGrath, and D. G. Holmes, "A General Analytical Method for Calculating Inverter DC-Link Current Harmonics," *IEEE Transactions* on *Industrial Application*, vol. 45, no. 5, pp. 1851–1859, Sep. 2009.
- [23] R. Jánó, and D. Pitică, "Accelerated Ageing Tests for Predicting Capacitor Lifetimes," in Proc. of 17th International Symposium for Design and Technology in Electronic Packaging (SIITME), 2011, pp. 63-68, 2011.
- [24] M. A. Vogelsberger, T. Wiesinger, and H. Ertl, "Life-Cycle Monitoring and Voltage-Managing Unit for DC-Link Electrolytic Capacitors in PWM Converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 493-503, Feb. 2011.
- [25] V. Khuu, M. Osterman, A. B. Cohen, and M. Pecht, "Experimental application of a quadratic optimal iterative learning control method for control of wafer temperature uniformity in rapid thermal processing," *IEEE Transactions on Device and Materials Reliability*, vol. 9, no. 3, pp. 379-391, Sep. 2009.
- [26] S. Barmada, A. Musolino, M. Raugi, and M. Tucci, "Analysis of Power Lines Uncertain Parameter Influence on Power Line Communications," *IEEE Transactions on Power Dlievery*, vol. 22, no. 4, pp. 2163-2171, Oct. 2007.

- [27] Characteristic Specifications for NPS Series Iron Core. Pocomagnetic, Shenzhen, China, Dec. 2015. [Online].
- [28] Technical Notes and Guidelines for Aluminum Electrolytic Capacitor. Jianghai Capacitor, Jiangsu, China, May 2014. [Online]
- [29] Series for Alternative Energy and Industrial Applications. CSD Capacitor, Shenzhen, China, Sep. 2015.
- [30] R. Burkart, J. Kolar, "Component Cost Models for Multi-Objective Optimizations of Switched-Mode Power Converters," in Proc. IEEE Energy Conversion Congress and Exposition, 2013, pp. 2139-2146.
- [31] Emerson Network Power, Capacitors age and capacitors have an end of life, White Paper.
- [32] E. Baygildina, L. Smirnova, P. Peltoniemi, O. Pyrhönen and K. Ma, "Power semiconductor lifetime estimation considering dynamics of wind turbine," in Proc. Power Electronics and Machines for Wind and Water Applications (PEMWA), 2014 IEEE Symposium, Milwaukee, WI, 2014, pp. 1-6.



His current research interests include reliability of power electronics, failure mechanism of capacitors and semiconductor devices and reliable design of power converters.



Meng Huang (S'11–M'13) received the B.Eng. and M.Eng. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2006 and 2008, respectively, and the Ph.D. degree from the Hong Kong Polytechnic University, Hong Kong, in 2013. He is currently an Associate Professor of the School of Electrical Engineering, Wuhan University,

Wuhan, China.

His research interests include nonlinear analysis of power converters and power electronics reliability.



Huai Wang (S'07–M'12) is currently an Associate Professor and a research trust leader with the Center of Reliable Power Electronics (CORPE), Aalborg University, Denmark. His research addresses the fundamental challenges in modelling and validation of the failure mechanisms of power electronic components, and application issues in system-level predictability, condition

monitoring, circuit architecture, and robustness design. He has contributed a few concept papers in the area of power electronics reliability, filed four patents in capacitive DC-link inventions, and co-edited a book.

Dr. Wang received the PhD degree from City University of Hong Kong, Hong Kong, in 2012, and B. E. degree from Huazhong University of Science and Technology, Wuhan, China, in 2007. He was a Visiting Scientist with the ETH Zurich, Switzerland, from Aug. to Sep. 2014, and with the Massachusetts Institute of Technology (MIT), USA, from Sep. to Nov. 2013. He was with the ABB Corporate Research Center, Switzerland, in 2009. Dr. Wang received the IEEE PELS Richard M. Bass Outstanding Young Power Electronics Engineer Award, in 2016, for the contribution to the reliability of power electronic conversion systems. He has been an Associate Editor of IEEE Transactions on Power Electronics since 2015.



Xiaoming Zha (M'02) was born in Huaining, Anhui Province, China, in 1967. He received B.S., M.S., and Ph.D. degrees in electrical engineering from Wuhan University, Wuhan, China, in 1989, 1992, and 2001. He was a postdoctoral fellow in University of Alberta, Canada from 2001 to 2003.

He has been a faculty member of Wuhan University since 1992, and

became a professor in 2003. He is now deputy dean in the school of electrical engineering from Wuhan University, Wuhan, China. His research interests include power electronic converter, the application of power electronics in smart grid and renewable energy generation, the analysis and control of microgrid, the analysis and control of power quality, and frequency control of high-voltage high-power electric motors.



Jinwu Gong received the B.Eng. and Ph.D. degrees in electrical engineering from Wuhan University, Wuhan, China, in 2004 and 2012, respectively. He is currently an Associate Professor of the School of Electrical Engineering, Wuhan University.

His research interests include high power converters such as motor drives, static synchronous compensators,

active power filters and digital control technique.



Jianjun Sun (M'13) was born in 1975. He received the B.Eng. degree from Wuhan University of Hydraulic and Electrical Engineering, Wuhan, China, in 1997, and then he received the M.Eng. and Ph.D. degrees from Wuhan University, Wuhan, China, in 2000 and 2007, respectively. He is now working in the School of electrical engineering of Wuhan University as an associate professor and the deputy director of

Motor and Power Electronics Center. He is also an associate director of Wuhan power supply society.

His current research interests include modeling and analysis of high-power power-electronic system, operation and control of microgrid, and power quality analysis and compensation.