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Performance Comparison for Virtual Impedance Techniques Used in Droop Controlled Islanded Microgrids

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***Abstract*—Droop control has limitations with respect to current sharing since the output current delivered by the inverters depends on their output impedance ratios. In addition, harmonic voltage drops due to the flow of harmonic currents induce voltage distortion at the point of common coupling (PCC). Virtual impedance loops were proposed in literature to improve the current sharing between the inverters by normalizing the output impedance of the inverters. However, virtual impedance loops have constraints in this respect since the improvement in the current sharing occurs through redistribution of the current harmonics which can add to the voltage distortion at the PCC. This paper compares the performance of resistive, inductive, inductive-resistive and resistive-capacitive virtual impedance loops with respect to current sharing and voltage harmonic distortion at the PCC. Simulation results are given for a single phase microgrid setup to achieve a fair performance comparison of the different virtual impedance techniques.**

***Index Terms*—microgrids, droop control, voltage harmonics, current sharing, islanded operation, virtual impedance loop**

I. Introduction

Although the droop control algorithm is suitable to share the fundamental active power between the VC-VSIs, it has limitations when it comes to reactive power sharing (i.e. mismatches in the fundamental current component) and harmonic current sharing. These limitations arise since the current sharing depends on the output impedance of the inverters and the line impedances in the microgrid. The inverter output impedance is typically considered to be inductive when viewed from the perspective of the point of common coupling (PCC). This assumption is justified by a high line inductance or due to a large output filter inductor. However, the closed-loop output impedance also depends on the primary control algorithms which are implemented in the respective inverters. In addition, component tolerances and different power line lengths imply that impedance mismatch is guaranteed and therefore current sharing cannot be achieved. In addition, the inverter output harmonic currents induce harmonic voltage drops across their respective filter inductors. Assuming that the inverter output voltages are purely sinusoidal, the harmonic voltage drop causes voltage harmonic distortion at the PCC [1]. These voltage harmonics may cause stability issues due to resonances present on the microgrid [2] and thus harmonic damping techniques must be considered.

Primary control algorithms can be implemented in the microgrid inverters to improve the harmonic current sharing while reducing the voltage distortion that would result due to harmonic loads at the PCC during islanded operation. The virtual output impedance loop consists of a fast control loop which could be employed to obtain a consistent output impedance for the inverters. Various authors have proposed different virtual impedance loops to improve the current sharing [1], [3]–[8] and also to improve the voltage total harmonic distortion (THD) at the PCC [1], [8]. These virtual impedance loops can be used to change the output impedance of all the inverters in the microgrid into an arbitrary impedance which is independent from the original output impedance of the respective inverter. Therefore the output impedance matching can be improved using this technique, which implies that the current sharing can also be improved. However, the performance achieved by primary control techniques has limitations in this respect [1]. The concept of virtual impedance loops has been reported in various literature where resistive [6], inductive [3] and resistive-inductive [7] virtual impedances were designed and implemented to improve the current sharing. In [1], [8], [9], the authors propose a resistive-capacitive virtual impedance loop which improves the voltage harmonic distortion at the PCC while also improving the current sharing between the inverters. The main limitation of virtual impedance techniques employed for islanded operation of microgrids is that the harmonic currents required by the harmonic loads must still be supplied by the inverters. Therefore, the harmonic current outputs of the respective inverters cannot be eliminated completely but redistribution of the current harmonics occurs which enables to achieve a compromise between both of these requirements. The redistribution of the current harmonics also affects the voltage harmonics at the PCC which can lead to better/worse voltage THD.

This paper compares the performance achieved by the resistive, inductive, inductive-resistive and resistive-capacitive virtual impedances. Simulations are performed for a single

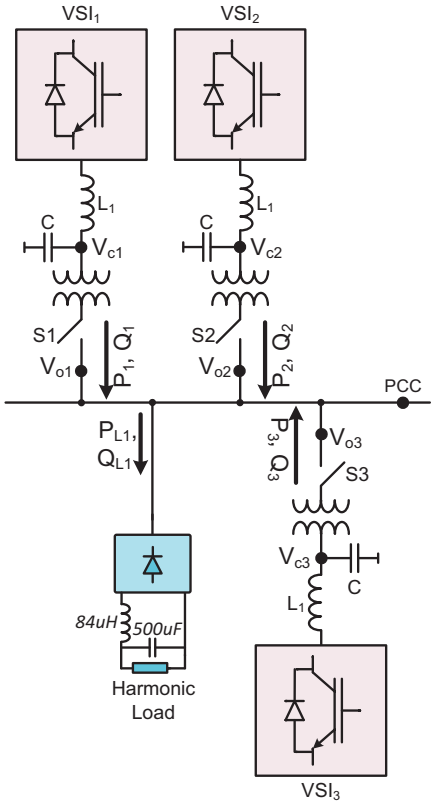


Fig. 1. Block diagram of the considered islanded microgrid setup consisting of three single phase inverters and a harmonic load.

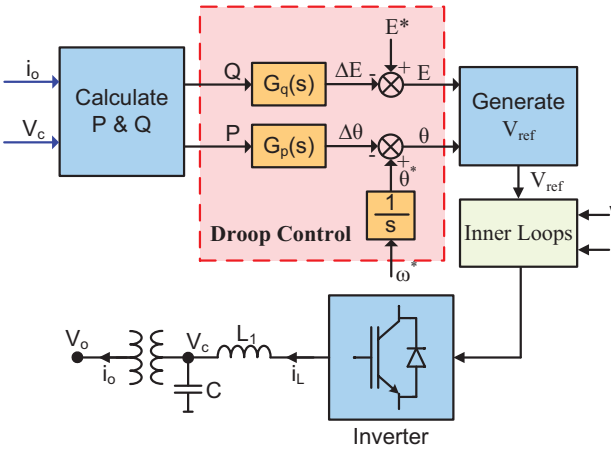


Fig. 2. Block diagram of the inverter primary control loops. The real and reactive power are determined from the capacitor voltage (V_c) and the output current (i_o). The voltage reference V_{ref} applied to the inner control loops is determined via the droop control algorithm.

phase microgrid setup to verify the fundamental current and harmonic current sharing capabilities of these techniques. In addition, the voltage harmonic distortion which occurs at the PCC of the microgrid during each scenario shall also be analyzed. The paper is structured as follows. In Section II, a description of the considered microgrid setup and primary control loops is given. Section III contains a description of the virtual impedance concept and a concise description of the considered virtual impedance loops. Section IV compares the simulation results of the considered virtual impedance loops with respect to the current sharing achieved by the inverters together with the resulting voltage harmonic distortion at the PCC.

II. Simulated Microgrid Architecture

The islanded microgrid setup consists of three single phase inverters having LC output filters together with 1:1 isolation transformers connected at their output. A block diagram of the setup is given in Fig. 1. A local harmonic load is also connected to the microgrid, which consists of a rectifier with a smoothing capacitor. Switches S1 to S3, connected at the output of the inverters, enable to connect/disconnect the inverters to the microgrid.

During islanded operation, the inverters regulate autonomously the local voltage and frequency of the microgrid through the droop control algorithm, implemented in the respective primary control loops of the inverters. Real power is supplied to the loads by using real power against frequency (P-ω) droops while the reactive power is supplied to the loads by using reactive power against voltage (Q-E) droops. The block diagram of the primary control loops implemented in the microgrid inverters is shown in Fig. 2.

The measured real and reactive power are input into the droop controller and the voltage reference determined by the droop control algorithm is then applied to the input of the inner control loops. Considering that $G_q(s)$ and $G_p(s)$ are the droop controller transfer functions, the droop control functions in islanded mode can be mathematically expressed as:

$$\theta = \theta^* - G_p(s)P = \theta^* - \left(m_p + \frac{m}{s}\right)P \quad (1)$$

$$E = E^* - G_q(s)Q = E^* - (sn_d + n)Q \quad (2)$$

where $\theta^* = \frac{\omega^*}{s}$ and ω^* is the nominal frequency (50Hz) of the microgrid; $\theta = \frac{\omega}{s}$ and ω is the droop frequency; m and n are the P-ω and Q-E droop gains respectively, m_p is the proportional gain of the P-ω droop and n_d is the Q-E derivative gain. The designed droop gains for all the inverters were m = 0.03rad/W.s and n = 0.06V/VAr respectively while m_p and n_d were designed to be equal to $0.002 rad/W.s^2$ and 0.005V/VAr.s respectively.

A. Inner Control Loops

The inner controllers that were considered for the single phase inverters consist of a voltage loop and an inner current loop. The block diagram of the inner control loops is shown in Fig. 3. Both control loops are based on the stationary reference frame and Proportional-Resonant (PR) controllers were used for both loops. The transfer functions of the voltage and current controllers can be given by [1], [10]:

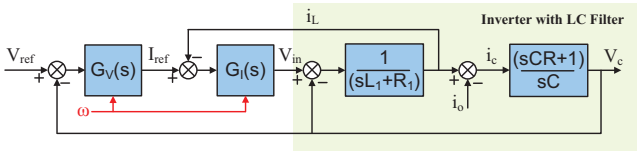


Fig. 3. Block diagram of the inner control loops where V_{ref} is the voltage reference that is determined by the droop control loop, i_L is the current through inverter-side inductor L_1, i_o is the current through the output transformer, C is the filter capacitance, R_1 is the inverter side choke resistance and R is the damping resistor.

$$G_V(s) = K_{pV} + \sum_{h=1,3,5,7} \frac{k_{iVh}s}{s^2 + \omega_{cVh}s + \omega_h^2} \quad (3)$$

$$G_I(s) = K_{pI} + \sum_{h=1,3,5,7} \frac{k_{iIh}s}{s^2 + \omega_{cIh}s + \omega_h^2} \quad (4)$$

where K_{pV} and K_{pI} are the proportional gains, k_{iVh} and k_{iIh} are the harmonic gains, ω_{cVh} and ω_{cIh} determine the bandwidth and ω_h is the resonant frequency which is an odd multiple of the droop fundamental frequency. Due to the selective harmonic control terms, the voltage and current controllers are capable of regulating the fundamental frequency components, the 3^{rd}, the 5^{th} and also the 7^{th} harmonic voltages and currents.

The bode plot of the CLTF $V_c(s)/V_{ref}(s)$ for the nested inner loops is shown in Fig. 4. The inner loops exhibit a bandwidth of 40Hz at the fundamental frequency while the selective harmonic control components introduce bandpass characteristics at 150Hz, 250Hz and 350Hz in addition to the fundamental frequency. The designed PR controller gains are: $K_{pV} = 0.1$, $K_{pI} = 2$, $k_{iV} = 0.4\omega_h$, $k_{iI} = 0.4\omega_h$, $\omega_{cVh} = 0.002\omega_h$ and $\omega_{cIh} = 0.002\omega_h$. The design and stability analysis of the inner control loops was described in detail by the authors in [1], [10].

III. Virtual Impedance Loops

The basic principles behind the resistive, inductive, inductive-resistive and resistive-capacitive virtual impedance

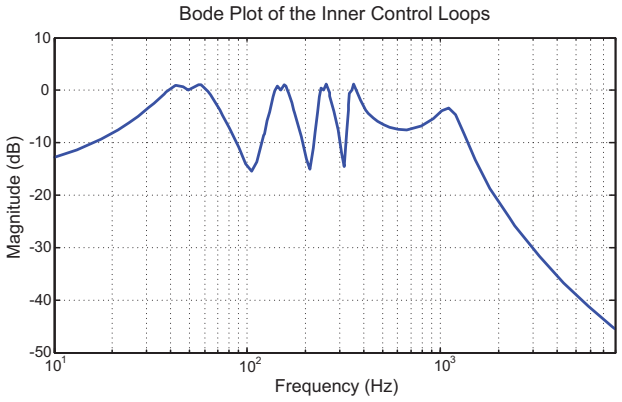


Fig. 4. Magnitude response of the inner loops closed loop transfer function $V_c(s)/V_{ref}(s)$ for the following output filter parameters: $L_1 = 1mH$, $R_1 = 0.065\Omega$,$R = 1\Omega$ and $C = 23\mu F$.

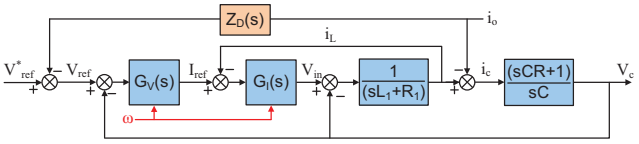


Fig. 5. Block diagram of the inner loops with the additional virtual impedance transfer function $Z_D(s)$.

loops shall be described in this section. Fig. 5 shows the interaction between the virtual impedance $Z_D(s)$ and the inner control loops of the inverter. The virtual impedance causes $i_o(s)$ to become an additional input of the inner loops which in turn enables to control the respective inverter output impedance. The capacitor voltage demand changes to $V_{ref}(s) = V^*_{ref}(s) - i_o(s)Z_D(s)$ when the virtual impedance loop is added to the inner control loops.

A. Virtual Inductive Impedances

A virtual inductive loop can be used to increase the output impedance of the inverters such that it becomes predominantly inductive thereby improving the power sharing accuracy of the droop control algorithm. The arbitrary inductive impedance can also reduce the effect of mismatches thereby improving the current sharing. A virtual inductive output impedance can be implemented by [3]:

$$Z_D(s) = sL_v \quad (5)$$

where L_v is the virtual inductance. L_v is chosen arbitrarily and is typically selected such that it dominates the output impedance of the inverters. A low pass filter must be included in series with the virtual inductance to eliminate the noise generated by the derivative term. Hence, in practice the virtual inductive transfer function can be rewritten as:

$$Z_D(s) = sL_v \frac{\omega}{(s+\omega)} \quad (6)$$

B. Virtual Resistive Loop

Similarly to the previous case, a virtual resistive loop can also be used to increase the output impedance of the inverters such that it becomes more resistive. The final result is that the effect of mismatches is also reduced thereby improving the current sharing. A virtual resistance allows sharing of linear and nonlinear loads in microgrid applications without introducing additional losses in the network and improves the stability of the microgrid [6], [11]. A virtual resistive output impedance can be implemented simply by:

$$Z_D(s) = R_v \quad (7)$$

where R_v is the virtual resistance. R_v is chosen arbitrarily and is typically selected such that it dominates the output impedance of the inverter.

C. Inductive-Resistive Virtual Impedance Loop

The resistive-inductive virtual impedance loop improves the fundamental current sharing by achieving a predominantly inductive impedance due to the inductive term while the harmonic current sharing can be improved by the additional selective resistive virtual impedances [7]. The inductive-resistive virtual impedance transfer function can be represented as:

$$Z_D(s) = sL_v \frac{\omega}{(s+\omega)} - \sum_{h=3,5,7} \frac{R_H \omega_{ch} s}{s^2 + \omega_{ch} s + \omega_h^2} \quad (8)$$

where R_H is the resistive virtual impedance at the respective harmonic frequency. R_H and L_v are chosen arbitrarily and these are both typically selected such that the resulting impedance dominates over the output impedance of the inverter.

D. Resistive-Capacitive Virtual Impedance Loop

The resistive-capacitive virtual impedance loop improves the current sharing between the inverters while reducing the voltage harmonics at the PCC [1], [8]. The general capacitive virtual impedance transfer function can be represented as:

$$Z_D(s) = R_v - \sum_{h=3,5,7} \frac{\omega_{ch}(k_{ph} s + k_{ih})}{s^2 + \omega_{ch} s + \omega_h^2} \quad (9)$$

where k_{ph} is the proportional gain and k_{ih} is the integral gain at the respective harmonic. k_{ph} and k_{ih} can be obtained by equating $|Z_D(s)|$ to $|Z_{Trafo}(s)|$ while $\angle Z_D(s)$ must be equal and opposite to $\angle Z_{Trafo}(s)$ to cancel the voltage drop across the transformer self-inductance. Details on the design of the capacitive virtual impedance are given in [1], [8] and [9].

IV. Simulation Results

The aim of this section is to compare the performance of the virtual impedance loops described in the previous section. The considered performance criteria are the fundamental and harmonic current sharing and also the resulting voltage harmonic distortion at the PCC. The three inverters are connected to the microgrid each with the corresponding $Z_D(s)$ in its inner control loops. The inverters were required to supply a local single phase rectifier with smoothing capacitor as described in Section II. The total RMS current demand by the harmonic load under ideal current sharing conditions is equal to 5A. This implies that for equal current sharing, each inverter in the following tests should supply 1.67A to the load. This ideal inverter output current shall be used as a common denominator for the following tests to obtain the percentage variance with respect to the ideal conditions.

The parameters of the isolation transformers at the output of the respective inverters are given in Table I. Inverters 1 and 3 have nearly identical output impedance characteristics and can therefore accurately share the current with minimal error. On the other hand, inverter 2 cannot equally share the output current with the other two inverters due to the a large difference in its output impedance characteristics.

The real and reactive power flowing in the microgrid and the PCC voltage depend on the operation of the droop control algorithm. The only changes which were performed to obtain the following simulation results are in the implementation of the virtual impedance loop. The choice of the magnitude of the virtual impedance $|Z_D(s)|$ is selected based on a compromise between the current sharing and the voltage THD at the PCC. The gains of the virtual impedance loops were selected such that these provide an impedance of 3Ω at the fundamental frequency. This enables to achieve a fair basis for comparing the performance of the considered virtual impedance techniques.

TABLE I
MICROGRID MODEL TRANSFORMER SIMULATION PARAMETERS WHERE SUBSCRIPT P DENOTES THE PRIMARY WINDING AND S DENOTES THE SECONDARY WINDING.

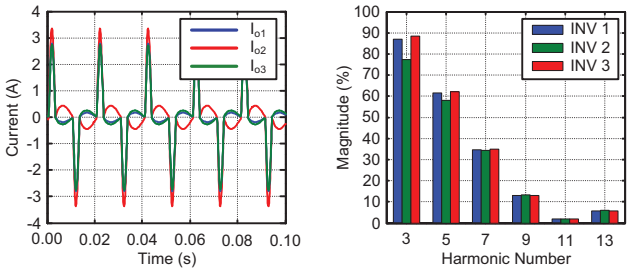
Inverter	R_{2p} Ω	R_{2s} Ω	L_{2p} mH	L_{2s} mH	L_M H	R_C Ω
VSI 1	0.392	0.392	1.75	1.75	2.70	372
VSI 2	0.256	0.256	1.20	1.20	1.20	255
VSI 3	0.385	0.385	1.80	1.80	2.75	329

A. Resistive Impedance Loop

Simulations were initially performed for a virtual resistance R_v of 3Ω implemented in each of the microgrid inverters. The steady state output currents by each of the inverters are shown in Fig. 6(a) while the harmonic components of the inverter output currents are given in Fig. 6(b). The total RMS current output by the inverters are 1.47A, 1.80A and 1.45A respectively. Therefore, for the resistive virtual impedance of 3Ω, the maximum percentage variance in the output current of the inverters from the ideal current sharing condition is found to be 13.2%. The magnitude of the voltage harmonics which occur at the PCC of the microgrid are shown in Fig. 10 where the voltage THD in this case is equal to 2.65%. Increasing the value of R_v improves the current sharing between the inverters while on the other hand the voltage THD at the PCC increases.

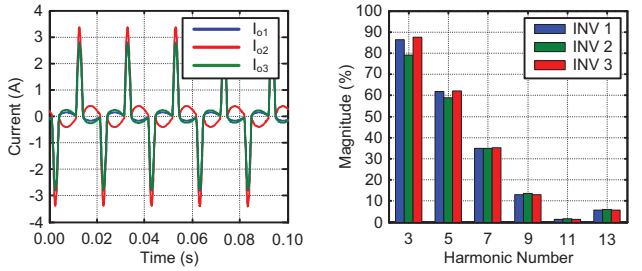
B. Inductive Impedance Loop

Additional simulations were then performed for a virtual inductance L_v of 10mH implemented in each of the microgrid inverters. The steady state output currents by each of the inverters are shown in Fig. 7(a) while the harmonic components of the inverter output currents are given in Fig. 7(b).



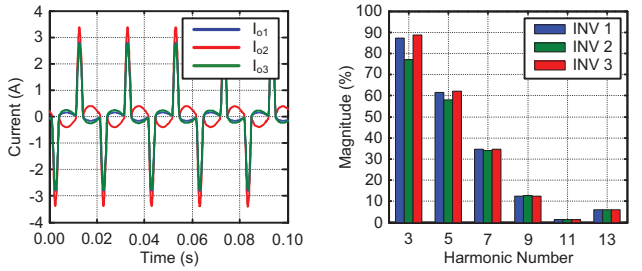
(a) Steady state output current. (b) Steady state harmonic spectrum.

Fig. 6. Current sharing between the microgrid inverters for a virtual resistance R_v of 3Ω implemented in all three inverters of the single phase microgrid while supplying the harmonic load.



(a) Steady state output current. (b) Steady state harmonic spectrum.

Fig. 7. Current sharing between the microgrid inverters for a virtual inductance L_v of 10mH implemented in all three inverters of the single phase microgrid while supplying the harmonic load.



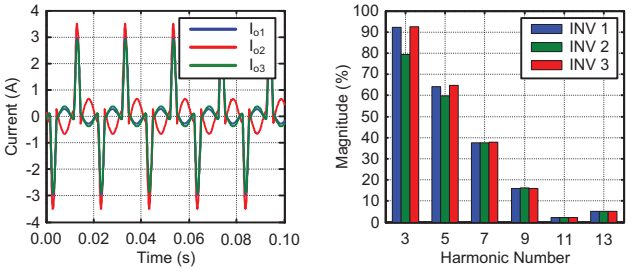
(a) Steady state output current. (b) Steady state harmonic spectrum.

Fig. 8. Current sharing between the microgrid inverters for the inductive-resistive virtual impedance for an L_v of 10mH and an R_H of 3Ω implemented in all three inverters of the single phase microgrid while supplying the harmonic load.

The resulting total RMS current output by the inverters are 1.48A, 1.81A and 1.46A respectively. Therefore, for the virtual inductance of 10mH, the maximum percentage variance from the ideal inverter output current is 12.6%. Hence, the performance with respect to the current sharing between the inverters achieved by the virtual resistance and virtual inductance loops is very similar. The magnitude of the voltage harmonics which occur at the PCC of the microgrid are shown in Fig. 10, where the voltage THD increases from the previous scenario up to 2.74%. This implies an increase of 3.5% when compared to the resistive impedance simulation results. Therefore, the virtual resistive impedance has superior performance due to its lower voltage harmonic distortion at the PCC for approximately the same current sharing percentages. In addition, similarly to the previous scenario, increasing the value of L_v improves the current sharing between the inverters while on the other hand the voltage THD at the PCC increases. Therefore in both cases, there is a compromise between the level of current sharing and the PCC voltage harmonic distortion.

C. Inductive-Resistive Impedance Loop

Consider that in addition to the virtual inductance of L_v of 10mH, the harmonic components were also compensated with additional virtual harmonic resistances of R_H of 3Ω. The steady state output currents by each of the inverters are shown in Fig. 8(a) while the harmonic components of the inverter output currents are given in Fig. 8(b). The resulting total RMS current output by the inverters are 1.48A, 1.80A and 1.46A respectively. Therefore, the maximum percentage variance from the ideal output current of the inverters is 12.5%. The combined inductive-resistive virtual impedances therefore does not provide any improvement in the current sharing between the inverters when compared to the purely inductive impedance scenario. The magnitude of the voltage harmonics which occur at the PCC of the microgrid are shown in Fig. 10 where the voltage THD becomes equal to 3.10%. This implies an increase in the voltage THD by a factor of 11.4% when compared to the resistive impedance case. This result shows that in an attempt to improve the current sharing, the voltage harmonic distortion at the PCC increases by 11.4%. Similarly to the previous scenarios, increasing the value of L_v and R_H improves the harmonic current sharing between the inverters while on the other hand the voltage THD at the PCC increases.



(a) Steady state output current. (b) Steady state harmonic spectrum.

Fig. 9. Current sharing between the microgrid inverters for the resistive-capacitive virtual impedance for an R_v of 3Ω and capacitive virtual impedance gains given in Appendix A implemented in all three inverters of the single phase microgrid while supplying the harmonic load.

D. Resistive-Capacitive Impedance Loop

Finally, simulations were also performed for the resistive-capacitive virtual impedance implemented in each of the microgrid inverters. The virtual resistance R_v was set to 3Ω as for the purely resistive case while the capacitive virtual impedance gains are given in Appendix A. These gains were obtained using the design procedure described earlier. The steady state

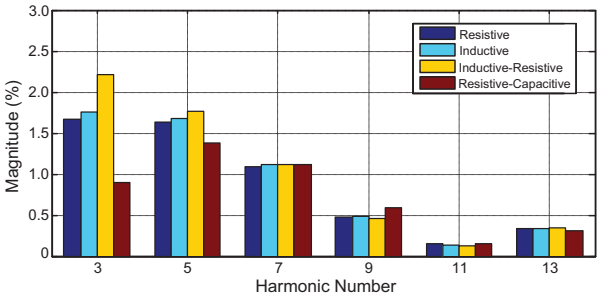


Fig. 10. Voltage harmonics at the PCC during islanded operation expressed as a percentage of the fundamental voltage component of the single phase microgrid for the considered harmonic load.

output currents by each of the inverters are shown in Fig. 9(a) while the harmonic components of the inverter output currents are given in Fig. 9(b). The resulting total RMS current output by the inverters are 1.54A, 1.84A and 1.51A respectively. Therefore, the maximum percentage variance from the ideal output current of the inverters is 10%. Therefore, the combined resistive-capacitive virtual impedances marginally improves the current sharing by 3.2% when compared to the purely resistive case. The magnitude of the voltage harmonics which occur at the PCC of the microgrid are shown in Fig. 10. The voltage THD in this case reduces to 2.11% which implies a reduction of 20.5% when compared to the purely resistive virtual impedance simulation results. This result shows that using the resistive-capacitive virtual impedance, one can achieve the same level of current sharing between the inverters as other virtual impedance techniques with an added advantage of a significantly lower voltage THD at the PCC.

V. Conclusion

Various virtual impedance techniques are found in literature which aim towards improving the current sharing between the inverters in the microgrid. The effects of the resistive, inductive, inductive-resistive and resistive-capacitive virtual impedance loops on the operation of a single phase microgrid were analyzed through simulations. Simulation results have shown that the virtual impedance loops have a compromise between current sharing and voltage harmonic distortion which occurs at the PCC when there are harmonic loads in the microgrid. Simulation results have also shown that the resistive-capacitive virtual impedance loop achieves the best compromise between current sharing accuracy and voltage harmonic distortion at the PCC. The resistive-capacitive virtual impedance loop achieves the minimum voltage THD at the PCC of 2.11% with the minimum current sharing variance of 10% from the ideal current output, thereby indicating its effectiveness when compared to other virtual impedance techniques.

Appendix A
Design Data for the Capacitive Virtual Impedance Loop

Inverter	VC-VSI 1	VC-VSI 2	VC-VSI 3
k_{p3}	3.7840 Ω	3.5120 Ω	3.7840 Ω
k_{i3}	3.2987 F^{-1}	2.2619 F^{-1}	3.2987 F^{-1}
k_{p5}	3.7840 Ω	3.5120 Ω	3.7840 Ω
k_{i5}	5.4987 F^{-1}	3.7699 F^{-1}	5.4987 F^{-1}
k_{p7}	3.7840 Ω	3.5120 Ω	3.7840 Ω
k_{i7}	7.6969 F^{-1}	5.2779 F^{-1}	7.6969 F^{-1}

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