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Comparison of Thermal Runaway Limits under Different Test Conditions Based on a 4.5 kV IGBT

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Abstract

This investigation focuses on determining the temperature-dependent leakage current limits which compromise the blocking safe operating area for silicon IGBT technologies. A discussion of a proper characterization method for selecting the maximum rated junction temperature of devices at high temperatures is given by comparing the different testing methods: static performance (including and excluding self-heating), Short Circuit Safe Operation area and High Temperature Reverse Bias. Additionally, a thermal model is used to predict the junction temperature at which thermal runaway takes place. In this paper a guideline has been proposed based on the correlation between short circuit withstanding capability and off-state leakage current guarantying reliable operation and ensuring that they are thermally stable even if they are exposed to parameter variations. This study is helpful to facilitate application engineers the in tedious task of defining the correct stability criteria and/or margins in respect of thermal runaway.

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1. Introduction

High-Voltage IGBTs are nowadays being pushed to operate closer to their SOA (Safe Operation Area) limits at ever increasing temperatures [1, 2]. With this new challenge, devices have to demonstrate their switching capability at the maximum ratings and specified junction temperature by proving their stable temperature-dependent performances [3, 4].

The definition of maximum junction temperature in power semiconductor devices is a crucial topic for device designers as well as application engineers because it limits the stable operation range of such devices. For this reason, large margins are adopted to ensure the device reliability by derating the voltage and current of the device. Thermal runaway is one of most common failure mechanisms in silicon semiconductor devices, especially at high temperatures in the off state [5]. As a rule of thumb, the leakage current for traditional-silicon devices increases by a factor of 2 when the temperature increases by 11ºC [6]. Thermal runaway is mostly related to technological issues, therefore it is worth mentioning the three leakage current main components: (a) the bulk of the chip (i.e., amplification behavior of the PNP transistor gain), (b) the chip termination design (i.e., p^+-type guard rings, variation of lateral doping), and (c) the passivation process [7].

The main part of this study is to provide a guideline to select the rating of the maximum allowed junction temperature of semiconductor devices during standard operation $T_{vj}(op)$. In order to draw this conclusion, the devices must guarantee reliable operation and ensure that they are thermally stable even if they are exposed to parameter variations. To conclude that devices can be rated for a given temperature many factors should be considered, such as: thermal coupling from neighboring components, airflow, package material and technique, ambient temperature, good current/voltage sharing in paralleled/series devices, stable blocking behavior and low leakage current. Presently, the characterization method for defining the maximum rated junction temperature is to increase the temperature of the entire setup to the targeted temperature. Nevertheless, this method may give erroneous results because static stability criterions might be violated which are not relevant to the real-world applications.

This study is exemplary based on the thermal stability limits of 4.5 kV/ 150A Soft-Punch-Through (SPT+) IGBTs by looking at thermal runaway failures. In order to closely approach the real-world applications, two static stability methods and dynamic short circuit tests are compared to find a joint correlation under different tests conditions: a guideline has been proposed based on the correlation between short circuit withstanding capability and off-state leakage current. Finally, a High Temperature Reverse Bias (HTRB) test is also carried out in order to show the long-term reliability stability. This study is helpful to facilitate application engineers the tedious task of defining the correct stability criteria and/or margins in respect of thermal runaway.

2. Static Performance up to Thermal Runaway

2.1. Device under test

Experiments have been carried out on 4.5 kV/ 50 A SPT+ IGBTs which were mounted on test-substrates similar to the one shown in Fig 1. The test-substrates consist of 4 IGBTs in parallel with two anti-parallel diodes.

2.2 Thermal Stability Testing Methods

The IGBT leakage current was measured under blocking state at several operating temperatures by directly mounting the test-substrates on a temperature-controlled heating plate.

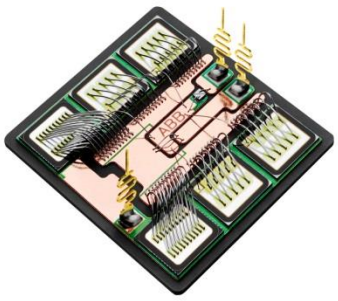
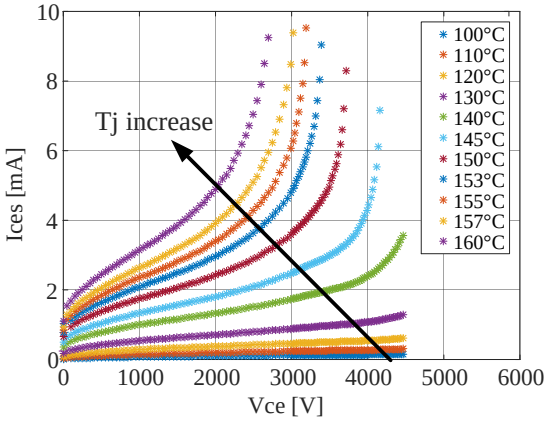
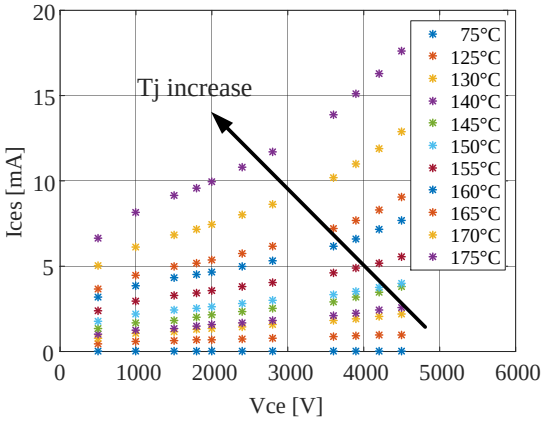


Fig. 1. 4.5 kV/ 150 A IGBT test substrate.

Two test methods have been applied with the aim of illustrating the correlation among them, namely: (i) *IV*-sweep thermal stability test, and (ii) Quasi-static thermal stability test. For the *IV*-sweep test, the leakage current is measured when the blocking voltage is swept from 0 V up to 4.5 kV. The total time for this test is 2 minutes and thus, the chip self-heating effect is evidenced. On the other hand, the quasi-static test measures the leakage current by applying a single voltage pulse which length can be programmed by the user. The voltage pulse has been selected to be 200 ms ensuring that the self-heating of the IGBT chip is negligible. If the pulse length is too short, the leakage current will be incorrectly measured due to the positive feedback between leakage current and temperature. Fig. 2 shows the IGBT leakage current values for the *IV*-sweep test and quasi-static test, for temperatures ranging from 100ºC up to 160ºC and from 75 ºC up to 175ºC, respectively. Note that the test-substrates are mounted directly to the heating plate, thus, the initial junction temperature can



(a)



(b)

Fig. 2. 4.5 kV IGBT off-state leakage current dependence with temperature: (a) *IV*-sweep test (b) quasi-static test.

assumed to be similar as the heating plate. Both testing methods are well-known between the application engineers; however, the correlation between them is usually not well-known, especially when predicting the thermal runaway limits.

A significant result comes out from Fig. 2. A correlation between off-state leakage current and junction temperature for a given blocking voltage can be made by applying the following formula [6]:

$$I_{CES}\,(T_1) = I_{CES}\,(T_0)\; x\; 2^{\frac{T_1 - T_0}{\Delta T}} \qquad (1)$$

where I_{CES} is the leakage current, T is the junction temperature of the chip and ΔT is the thermal coefficient obtained by fitting the curves in Fig. 2. ΔT is equal to 8.7 for the results from the *IV*-sweep and equal to 12.5 for the quasi-static results.

Thanks to this correlation, the leakage current can be estimated as a function of the junction temperature and included in the thermal models. Additionally, the differences between the two methods can be straightforwardly understood.

2.1 Blocking Stability Criteria

Thermal runaway occurs when the heat generated is greater than the heat dissipated. To ensure thermal stability, it is essential that the relationship in (2) is not violated [8]:

$$dP_{gen}/\,dT_j \leq dP_{dis}/\,dT_j \qquad (2)$$

The generated power P_{gen} is the one coming from the leakage current under blocking state. The dissipated power P_{dis} depends on the cooling conditions, in this study, only the junction-to-case thermal resistance should be considered (i.e., the substrate is mounted on the heat plate), which value is 0.09 K/W.

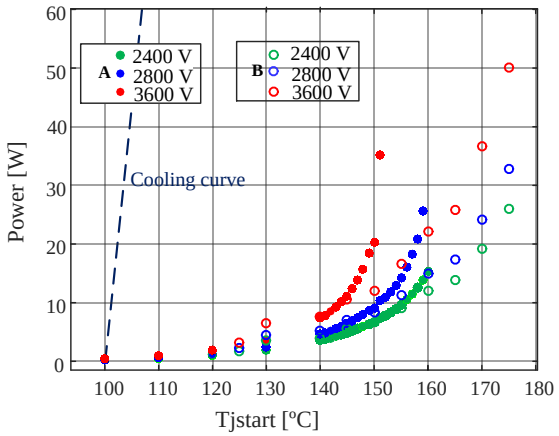


Fig. 3. Thermal runaway stability criterion: A – Static *IV*-sweep test, and B – quasi-static test.

Fig. 3 shows the power generated due to off-state leakage current together with the junction-to-case thermal resistance cooling curve. The previous stability criterion can be applied to the experimental results to establish the limits before thermal runaway takes place. An interesting observation can be made when comparing the derivatives (e.g., dP_{gen} / dT_j) of the two thermal stability test methods. The *IV*-sweep method (A in Fig. 3) shows higher derivative values than the quasi-static method (B in Fig. 3). Therefore it is advisable not to use the results from the *IV*-sweep method to formulate the stability criterion.

3. Thermal Runaway during Short Circuit

Short circuit current plays an important role for assessing the thermal stability of the device. Due to the excess energy during short circuit, the system can be easily driven into thermal runaway.

Short circuit tests have been performed using a typical short circuit type 1 configuration at a given collector-emitter voltage [9]. A variable short-circuit pulse allows the self-heating of the IGBT with the possibility to step-by-step increase the leakage current of the device in the off state. The purpose is to provide a guideline to select the maximum junction temperature of the IGBT by fulfilling the SCSOA (Short Circuit Safe Operation Area). Prior to the short circuit tests, the leakage current of four IGBTs is measured by using the quasi-static method, demonstrating that higher leakage current devices show reduced short circuit time capability. This correlation can be seen by comparing Figs. 4 and 5, the highest leakage current is observed for NRUQ23 followed by NRUQ04, NRUQ01 and NRUQ06.

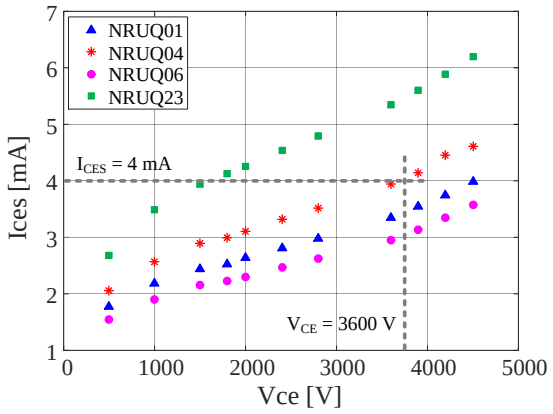


Fig.4. 4.5 kV IGBT leakage current dependence with voltage at 150ºC for 4 IGBTs from the same lot.

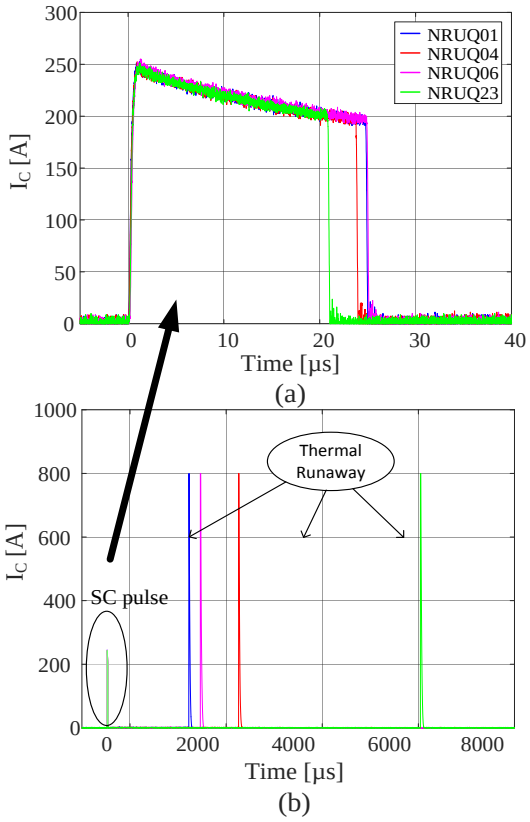


Fig. 5. Short circuit current up to thermal runaway of 4 IGBTs: (a) short circuit pulse, and (b) evidence of thermal runaway.

In agreement with the leakage current measurements, Fig. 5 shows that the first one to fail is the NRUQ23, followed by NRUQ04, NRUQ01 and NRUQ06.

Based on the results, the existing correlation between the device leakage current and the short circuit withstanding capability can be used as a method to select the maximum allowable junction temperature of the device. For this reason, short circuit tests have been done at different starting temperatures, as reported in Fig. 6. The proposed guideline lies in the following steps:

1. Select the maximum allowable leakage current that the IGBT chip should have at a given blocking voltage and starting junction temperature – in this case study, 4 mA at 3600 V and 150ºC.
2. Select the maximum allowable short circuit withstanding capability for a given voltage and starting junction temperature – in this case study, IGBTs with leakage current of 4 mA are able to survive 23 µs at 3600 V and 125ºC.

3. Extrapolate the short circuit withstanding capability at different starting junction temperatures (i.e, 16µs short circuit at 150ºC).
4. Select the maximum allowable junction temperature bearing in mind that IGBTs have to be designed to withstand at least 10µs short circuit. Additionally some margin must be given – in this case study, the maximum junction temperature can be selected as 150ºC.

Note that this procedure has been done for one single IGBT chip, without taking into account thermal coupling effects coming from the neighboring components.

4. Modelling of Junction Temperature

4.1 Electro-Thermal Model

An electro-thermal model is applied to predict the evolution of the IGBT junction temperature during and after the short circuit test. The thermal impedance from junction-to-baseplate can be estimated according to the method in [10], where the thermal impedance is modelled as a Cauer network. The thermal resistance R_{th} and the thermal capacitance C_{th} of different physical layers (e.g., IGBT chip, chip solder and substrate) can be calculated from the geometry and material properties. Table 1 reports the calculated thermal resistance and thermal capacitance values for each layer.

Table 1: Thermal impedances

Layers	R_{th} [ºC/W]	C_{th} [J/ ºC]
IGBT chip - silicon	0.036	0.084
Solder - PbSn5Ag2.5	0.014	0.028
Top copper layer	0.004	0.194
Substrate - AlN	0.033	0.447
Bottom copper layer	0.003	0.177

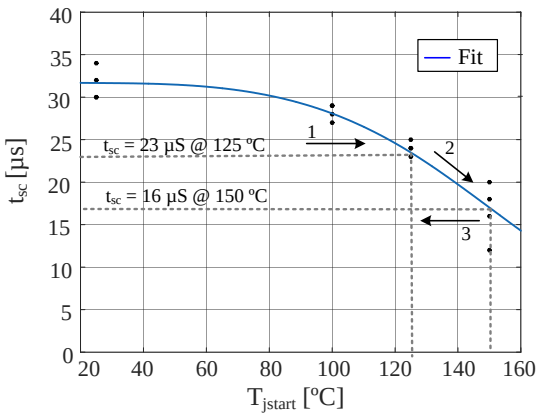


Fig. 6. Maximum short circuit time versus temperature.

4.2 Thermal Runaway Prediction

It is well-known that the minimum dissipated energy that leads to thermal runaway failure of a specific device after a single short circuit is referred as critical energy E_C [11]. The junction temperature can be predicted based on the electro-thermal by including the critical short circuit energy obtained via experiments. Nevertheless, it is not enough to understand the evolution of the junction temperature in the off state – when the failure takes place. To that end, the correlation between leakage current and junction temperature given in (1) can be calculated for each device and included in the electro-thermal model. For the test-substrate NRUQ01, the leakage current can be calculated as follows:

$$I_{CES}(T_1) = 3.35\,(T_{0=150ºC})\; x\; 2^{\frac{T_1-150}{12.7}} \qquad (3)$$

Fig. 7 shows the estimated temperature for each layer (i.e., IGBT chip, solder, top copper, AlN and bottom copper) based on the short circuit energy when the failure occurs. During the cooling phase (i.e., off-state), the junction temperature slighly decreases but after 800 µs, the dissipated power due to the leakage current is high enough to drive the IGBT into an unstable situation, causing thermal runaway.

With reference to Fig. 8, the point at which the simulated junction temperature reaches the minimum of instability is similar with the time at which thermal runaway is experimentally observed.

5. High Temperature Reverse Bias up to Thermal Runaway

One of the commonly used test for assesing the maximum allowable junction temperature of semiconductor devices is the High Temperature Reverse Bias (HTRB) test.

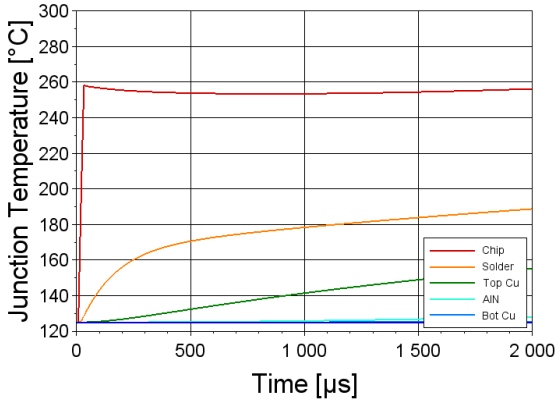


Fig. 7. Simulated junction temperature evidencing thermal runaway instability.

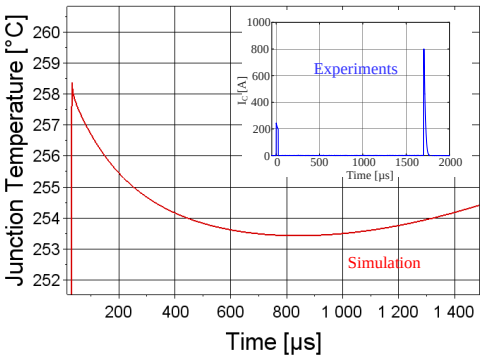


Fig. 8. Comparison between short circuit current and simulated junction temperature when thermal runaway is observed.

The device has to withstand the reverse blocking voltage at the ambient temperature for a long-term period (i.e., one day) and show a stable leakage current before the device can be qualified for that junction temperature. The test is continued until the device reaches an ambient temperature where thermal runaway takes place.

The test vehicle for running the HTRB test should be well isolated to avoid breakdown due to the high voltage applied. The isolation was not an issue in previous tests because the substrates were filled with nitrogen unlike the HTRB test. For this reason, 4.5 kV/ 150A HiPak modules have been used [12]. They are build with a half-bridge configuration having one substrate per arm - the substrate is the same as the ones used previously in this study.

Fig. 9 reports the leakage current measurements at 150ºC of the eight 4.5 kV/ 150 A power modules. The exisiting leakage current variation among them will dictate the order of failure during the HTRB test. The eight modules were placed in a temperature oven under the maximum rated blocking voltage; the temperature was increased incrementally until all of them failed. Fig. 10 shows the leakage current of each module as a function of time for three ambient temperature steps – 130ºC, 135ºC, and 140ºC. As seen in comparison with Fig. 9, the modules number 8 and 7 which are the first ones to fail, presented higher leakage current levels. On the other hand side, when the variation of leakage current measured in the static tester is very close among the modules, it is difficult to establish a correlation between leakage current level and failing point. This is because the HTRB tester fails from the following limitation: the ambient temperature inside the oven is

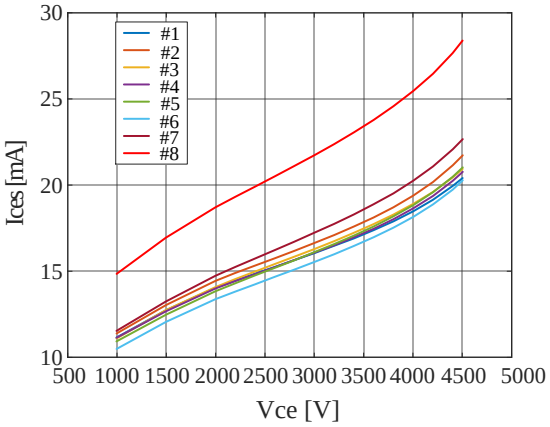


Fig. 9. Off-state leakage current measured at 150ºC.

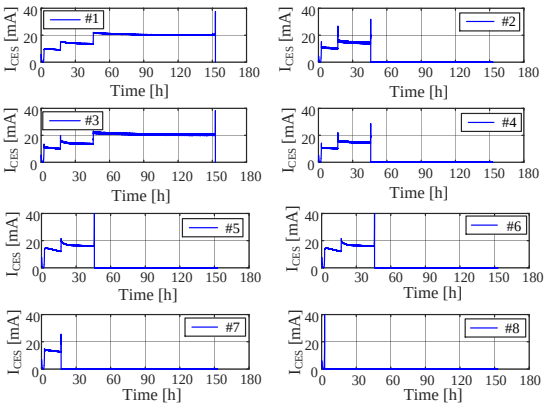


Fig. 10. HTRB results for three ambient temperature levels: 130ºC, 135ºC, and 140ºC.

not evenly uniform and thus the devices which are heated up more will be the first ones to fail.

For the sake of completeness, HTRB is a good measure to asses the long-term temperature capability of semiconductor devices, yet not enough adecuate for selecting the maximum allowable junction temperature. For instance, in the HTRB test the entire setup is increased up to the targeted temperature which may violate the thermal stability criterions not relevant to the real-world applications. Instead, the results from the off-state leakage current in Fig. 9 indicate that the modules are thermally stable at 150ºC - no avalanche breakdown is observed.

6. Conclusions

This work reports for the high-voltage IGBTs scenario, the difficulties encountered for defining the maximum rated junction temperature in semiconduc-

tor devices looking at different test setups. A comparison between the tests which are presently used to assess their temperature capability (i.e., static thermal stability, SCSOA and HTRB) has been given. The analysis has revealed a joint correlation between the short circuit withstanding capability and off-state leakage current by looking at thermal stability aspects, such as thermal runaway. This correlation can be used as a guideline to select the rating of the maximum allowed junction temperature of semiconductor devices during standard operation T_{vj}(op). Additionally, in order to compare the static and dynamic behaviour, the junction temperature after the short circuit pulse has also been modelled, evidencing that the junction temperature in the off-state suddenly increases coinciding with the thermal runaway failure observed experimentally. The proposed characterization method tries to understand the threats for the operation of HV IGBTs at high temperatures and how much devices must be over-dimensioned in order to operate safely.

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