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Silva, Filipe Miguel Faria da; Bak, Claus Leth

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Distance protection of multiple-circuit shared tower transmission lines with different voltages. Part II: Fault loop impedance

F. Faria da Silva [1*], Claus L. Bak[1]

[1] Department of Energy Technology, Aalborg University, Pontoppidanstraede 111, Aalborg, Denmark

[*] ffs@et.aau.dk

Abstract: Multiple-circuit transmission lines combining different voltage levels in one tower present extra challenges when setting a protection philosophy, as faults between voltage levels are possible.

In this paper, the fault loop impedance of combined faults is compared with the fault loop impedance of single-phase-to-ground faults and it is demonstrated that they are similar for high short-circuit powers; however, the fault loop impedance of a combined fault may increase substantially as the short-circuit power of the system decreases, a behaviour that is less noticeable for single-phase-to-ground faults. It is also demonstrated that the fault loop impedance of combined faults is more resistive, when compared with equivalent single-phase-to-ground faults.

It is concluded that the settings used to protect a line against single-phase-to-ground faults are capable of protecting the line against combined faults, being advised to increase the resistive limit of the protection zone, if the network has lower short-circuit power. It is recommended to assure that the fault can only happen for cases where the faulted phase from the higher voltage level leads the faulted phase from the lower voltage level, if the length of the line at lower voltage level is smaller than of the line at higher voltage level.

1. Introduction

This paper continues the analysis performed in Part I, by focusing on the fault loop impedances and the respective RX diagrams. The fault impedance seen by distance relays for combined faults is estimated for a simplified system, in order to demonstrate analytically that the short-circuit impedance of the grid has a large influence in the fault loop impedance of combined faults, something that does not happen for single-phase-to-ground faults (SPTG).

Several test cases, based on a Danish multiple-circuit transmission line, are simulated for different fault locations and short-circuit power levels at the busbars, with guidelines for the setting of the relays being proposed based on the theoretical analysis and simulations.

2. Test System

The simulations performed in this paper for demonstrative purposes are based on a real multiple-circuit 400kV/150kV line in Denmark. Figure 1 shows the single-line diagram of the line, Figure 2 shows the tower layout and the position of the phases in the tower [1]. Reference [1] presents also fault recorded data from a real combined fault in the line.

The distance of the different sections is:

- LAG to MAL: 78.21km of OHL
- LAG to KNA: 20.16km of OHL and 1.1km of cable section
- KNA to HAT: 1.23km of cable section and 24.21km of OHL
- HAT to MAL: 33.84km of OHL

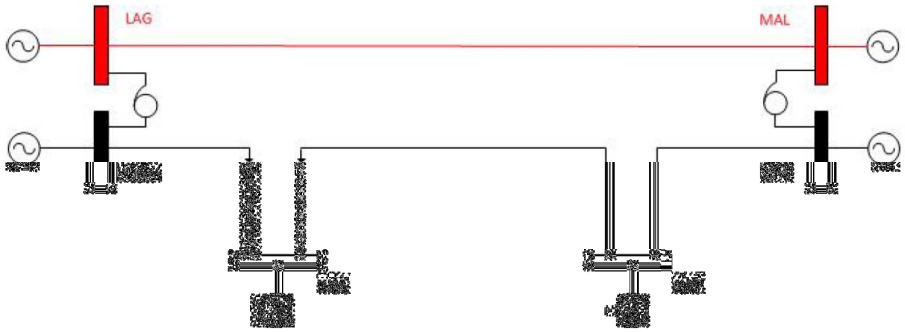

Figure 1 – Single-line diagram of the combined multiple-circuit line. Red: 400kV; Black 150kV. Solid line: OHL; Dashed line: underground cable [1]

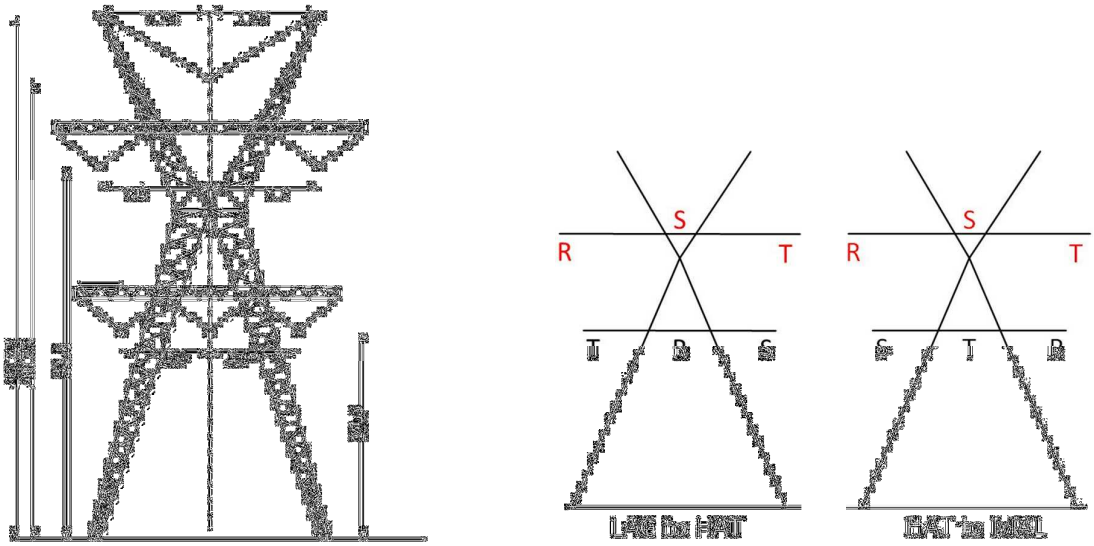

Figure 2 – Left: Double circuit tower: 400kV in delta at the top and 150kV in flat formation at the bottom. Right: Position of the different phases in the tower. Refer to Figure 1 for clarification of LAG, HAT and MAL [1]

3. RX diagrams

3.1. Theoretical expectations

Part I of the paper demonstrated that the fault current magnitude is expected to be up to 20% larger for combined faults than single-phase-to-ground (SPTG) faults. However, distance relays use fault loop impedance measurements for fault discrimination, which depend on current and voltage phasors during fault. The latter decreases when the short-circuit power decreases and thus, it is not possible to say immediately that the larger current of combined faults is sufficient for the faulted condition to fall within the pre-set protection zone and to trigger the distance relay; moreover, variations in the phase angle will occur due to the fault changing the location of the fault in the RX diagram and may lead to a fault condition outside of the protection zone.

Two aspects should be analysed first: SPTG faults are characterised by a mostly inductive current, in part because the ground impedance is mostly inductive. Combined faults are expected to be between different phases, because of the layout of the towers, as previously explained. The phase angle difference of approximately 120˚ between the faulted phases also influences the locus of the fault loop impedances and it should be considered.

Starting with the former, using the theoretical analysis done in Part I and comparing the equation for a combined fault (1) with that for a SPTG fault (2), which are repeat here for convenience, one can conclude that the phase angle of the fault current should not be much affected by the fact that the fault current does

not flow in the ground. This was confirmed by simulating a combined fault between equal phases from different voltage levels.

$$I^{+}_{400\_CF} = \frac{E_{400} - E_{150}}{Z^{+}_{400} + Z^{+}_{150} + Z^{-}_{400} + Z^{-}_{150} + Z^{0}_{400} + Z^{0}_{150} + 3\left(Z_F + Z_{G400} + Z_{G150}\right) - 2\times\left(3Z_M\right)} \quad (1)$$

$$I^{+}_{400\_SPTGF} = \frac{E_{400}}{Z^{+}_{400} + Z^{-}_{400} + Z^{0}_{400} + 3\left(Z_F + Z_{G400}\right)} \quad (2)$$

The second factor influencing the measured impedance is the phase angle between faulted phases. It was previously assumed that the phase angle between faulted phases from different voltage level is always approximately ±120˚. The fault current depends on the subtraction of the voltage phasors from the two faulted phases (1), as these are the driving electromotive forces for the fault current in the sequence component equivalent scheme (Figure 4 in Part I). If the two circuits have the same voltage level, this corresponds to a variation of 30˚ in the fault loop impedance when compared with the one from a SPTG fault; for the expected case of phases with different voltages, it will depend on the nominal voltages, being the variation of the fault loop impedance slightly bigger than 15˚ for the reference system used in this paper. Thus, it is expected that the fault current of a combined fault shows a less inductive behaviour, but one cannot say that it will show a 15˚ phase difference for all cases.

The distance relay is installed in the line feeder and the voltage it sees depends on the network's short circuit power. If the network is strong the fault loop impedance seen by the distance relay for a combined fault shows an approximate deviation of 15˚ when compared with the fault loop impedance for a SPTG fault. For weak networks the deviation is much larger and it is even possible that a distance relay sees faults as mostly resistive and capacitive, instead of mostly inductive. This happens because there is a large voltage drop at the short-circuit equivalent circuit, if it is much larger than the line impedance, a situation that occurs for weak networks.

Figure 3 shows a simplified single-line diagram used to explain these variations, where Z_{TH_400} and Z_{TH_150} are the Thévenin impedances of the higher and lower voltage levels, respectively.

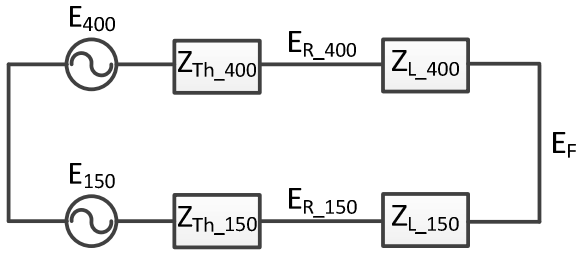

Figure 3 – Simplified single-lime diagram for a fault between different voltage levels

The impedance seen by the distance relay of the higher voltage level (E_{R_400}) is defined in (3) and it can be simplified into (4).

$$Z_{R\_400} = \frac{E_{R\_400}}{I_F} \Leftrightarrow Z_{R\_400} = \frac{E_{R\_400}}{\frac{E_{400} - E_{150}}{Z_T}} \quad (3)$$

where, $Z_T = Z_{Th\_400} + Z_{Th\_150} + Z_{L\_400} + Z_{L\_150}$

$$Z_{R\_400} = \frac{E_{400}}{E_{400} - E_{150}} Z_T - Z_{Th\_400} \quad (4)$$

The combined faults between voltage levels are between different phases and (5) is obtained for a combined fault involving 400kV and 150kV lines, where the sign of the imaginary part depends on the higher voltage level leading or lagging the lower voltage level.

$$\frac{E_{400}}{E_{400} - E_{150}} = 0.78 \pm j0.21 \quad (5)$$

Considering that the X/R the short-circuit equivalent and lines is equal, (4) can be written as (6) for a combined fault between 400kV and 150kV, where x is the relation between the Thévenin impedance of the 400kV level and the total impedance. To consider the X/R equal is a simplification for demonstration proposes, as the X/R of the lines has a high variability, but overhead lines are mostly inductive, which is the most important aspect in this demonstration.

$$Z_{R\_400} = (0.78 \pm j0.21)(a + j \cdot b) - x(a + j \cdot b) \quad (6)$$

Equation (6) is rewritten as (7), by considering X/R=10. The value of x is close to 0 for strong networks and close to 1 for weak networks.

$$\begin{aligned} & Z_{R\_400} = a\left((0.78 \pm j0.21)(1 + j \cdot 10) - x(1 + j \cdot 10)\right) \\ \Leftrightarrow\ & Z_{R\_400} = a\left((0.78 \mp 2.1 - x) + j(7.8 \pm 0.21 - 10x)\right) \end{aligned} \quad (7)$$

The variable a is the summation of the real parts of the Thévenin equivalent from the 400kV network and remaining impedances from Figure 3. Therefore, the weaker the network the bigger the value of a and x. Applying this relation in (7), conclusions can be made regarding the real and imaginary parts of the fault loop impedance seen by the relay of the higher voltage level (400kV in this example) during a combined fault. Starting with the imaginary part, if the network is strong the network is inductive. As the network becomes weaker, x increases and the imaginary part reduces to values closer to 0, until it becomes negative and the loop impedance seen by the relay becomes capacitive; after this point, as the network becomes weaker the fault loop impedance becomes more capacitive as both a and x continue increasing. Simulations performed next (Figure 4-Figure 9) demonstrate this behaviour.

Applying the same analysis to the real part of (7), two different situations may occur depending on the phases involved in the combined fault. If the value 2.1 from (7) adds, the real part of the loop impedance increases with positive sign when the network becomes weaker, because a increases and x is always smaller than 1; i.e., while the variation in x reduces the real part of the loop impedance when the network becomes weaker, the value is still positive and the increase in a results in an increase of the real part of the fault loop impedance, meaning that the fault loop impedance seen by the distance relay becomes more resistive. If the value 2.1 from (7) subtracts, the real part of the loop impedance is negative and the weaker the network the more negative it is, as both x and a increase the absolute value. Thus, the distance relay installed at the higher voltage level will in this case see the real part of the loop impedance as negative.

Combined faults will be between different phases, as previously explained. Therefore, the real part of the fault loop impedance seen by the distance relays of the higher voltage level are positive if the higher voltage level leads the lower voltage level (e.g., a fault between phase C of the higher voltage level and phase A of the lower voltage level), being negative if the lower voltage level leads the higher voltage level

(e.g., a fault between phase A of the higher voltage level and phase C of the lower voltage level). The opposite happens to the distance relays of the lower voltage level. Table 1 summarises these conclusions.

A special reference should be given to the strong network cases, as these are expected to be the most common ones. A comparison of a combined fault and SPTG fault in these conditions shows that the angle of the fault loop impedance varies approximately 15˚, with the direction of the angle rotation depending on the phases involved in the combined fault.

Table 1 – Expected behaviour for a combined fault when the faulted phase from the higher voltage level leads the faulted phase from the lower voltage level

	Higher voltage leads
Higher voltage level	Sees fault in forward direction
Lower voltage level	Sees fault in reverse direction
Impedance real part (HV relay)	More resistive as short-circuit power decreases
Impedance imaginary part (HV relay)	Inductance decreases and eventually capacitive as short-circuit power decreases

This theoretical study indicated that the fault loop impedance may have negative resistance or capacitive impedance for combined faults, depending on the phases involved and network's short circuit power. Moreover, the short-circuit power at the busbars has a substantial influence in the fault loop impedance, something that it is not so relevant in SPTG faults. The question to be answered via simulations is if these changes are sufficient for having the loop impedance falling outside of the pre-set zones, i.e., Z_{1B}.

3.2. Validation via simulations

The first case is a fault between phase C from the higher voltage level and phase A from the lower voltage level, which should result in a fault loop impedance with positive resistance when seen by the distance relays at the higher voltage level. Figure 4 shows the RX diagrams for a fault in the system described in section 2 at 10km from substation MAL. The current in the 400kV line pre-fault is 620A, the fault impedance is 2Ω and the groundings are all 1Ω. The k0 values used to estimate the fault loop impedance are those that would be used for SPTG faults. The same system and data is used in the rest of the simulation done in this paper, with the changes being only in the fault location and involved phases.

The red stars correspond to a SPTG fault for all short-circuit power combinations, and the remaining colours to a combined fault for different short-circuit power at the 400kV MAL substation (blue: 6000MVA; green: 2000MVA and black: 500MVA), with the short-circuit powers at the other substations varying between these values for each of these three colours. The horizontal blue line shows Z_1 extended

protection zone for the reactance, corresponding to 120% of the line reactance, as autoreclosure is normally the first step when protecting overhead lines against faults. The vertical blue lines correspond to the resistance, which is set considering a R/X relation of 1; this relation can be larger and up to 2 for overhead lines below 100km [3]. The separation of forward and reverse zones (red dashed line) is considered with an angle of 45˚ and 25˚, but it is important to notice that the angle may be lower in some cases and it should be checked for each particular case. To better visualise the changes in impedance magnitude when comparing the combined fault with a SPTG fault at the same location, a circle of radius equal to the maximum impedance of the SPTG fault is also presented in the figure.

The RX diagrams for a fault at 10km from the LAG substation are similar, but with the distance relay installed at LAG seeing the lower impedances.

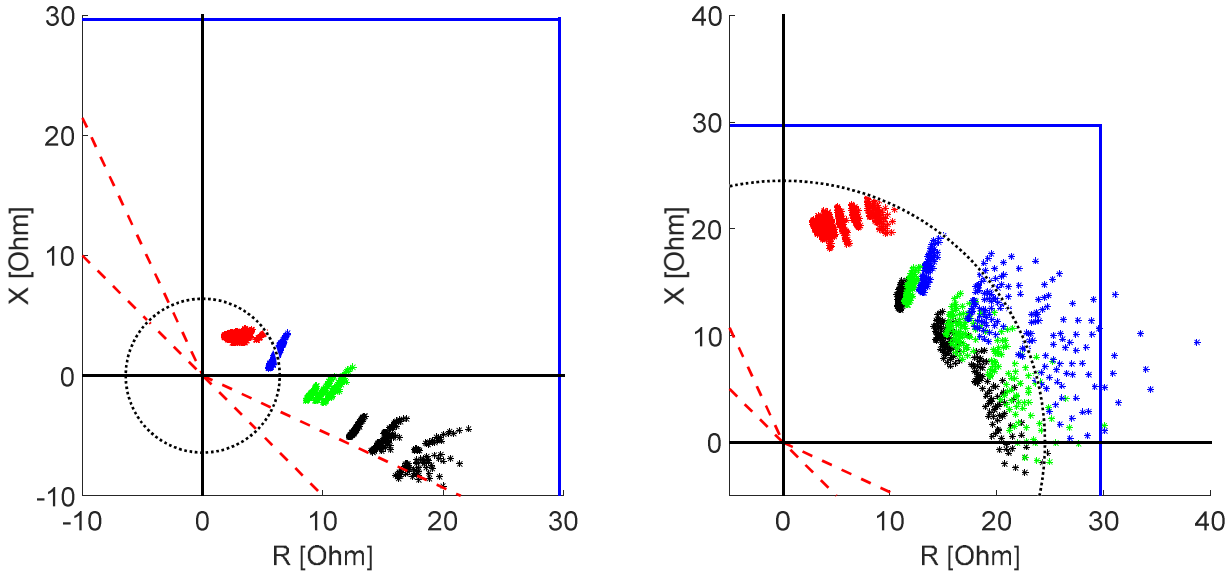

Figure 4 – Fault loop impedance at MAL (left) and LAG (right) for a SPTG fault (red stars) and a combined fault (remaining colours) at 10km from MAL, with the higher voltage level leading. Blue lines: Z_1 extended zone for autoreclosure for R/X=1. Circular black dots: Largest impedance of the SPTG fault

The results are in accordance with the theory presented previously. A combined fault is more resistive than a SPTG fault and the short-circuit power has a larger influence in the former. The simulation results show that the resistive component of the fault loop impedance is always smaller than the limit if one considers R/X=2 and almost always if one considers R/X=1; the cases outside of the protection zone are for the relay further away from the fault and correspond to a combination of rather high short-circuit power (6000MVA)

in MAL with very weak short-circuit powers (500MVA) in several other nodes, including the other end of the higher voltage line (LAG), which is not very realistic.

If the distance relay is close to the fault (left in Figure 4) the impedance increases substantially for combined faults when having the SPTG faults as reference, if the relay is distant from the fault (right in Figure 4), the increasing is smaller. This is explained by the fact that the short-circuit impedances have a higher influence for faults closer to the busbar.

The simulations also show that the fault loop impedance becomes capacitive for weak networks and it is seen in the reverse direction if an angle of 25˚ is used to separate the forward from the reverse zones. This situation is commented in the next section.

Figure 5 shows the RX diagram for a fault at approximately the middle of 400kV line, which in the combined fault case is for the line KNA-HAT that is not connected to MAL or LAG (see Figure 1). The results are in accordance to the expected and agree with the ones from Figure 4.

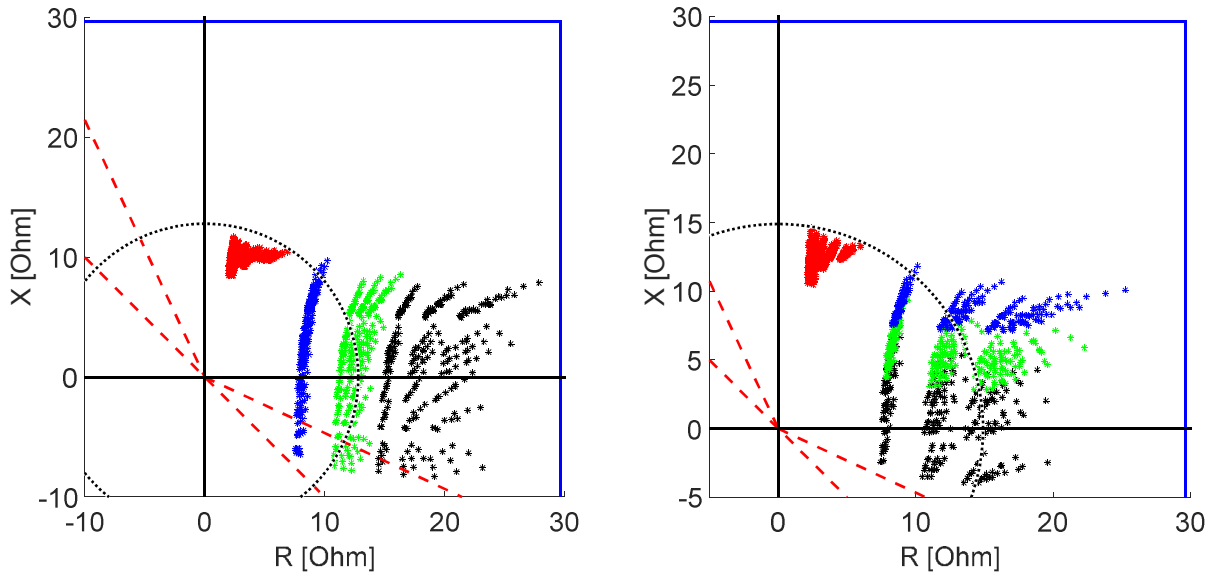

Figure 5 – Fault loop impedance at MAL (left) and LAG (right) for a SPTG fault (red stars) and a combined fault (remaining colours) at 44km from MAL and 34km from LAG, with the higher voltage level leading. Blue lines: Z_1 extended zone for autoreclosure for R/X=1. Circular black dots: Largest impedance of the SPTG fault

The simulations are repeated for a fault between phase A from the higher voltage level and phase C from the lower voltage level, which should result in a fault loop impedance with negative resistance for the

higher voltage level. Figure 6 shows the RX diagrams for a short-circuit in the reference system at 10km from substation MAL.

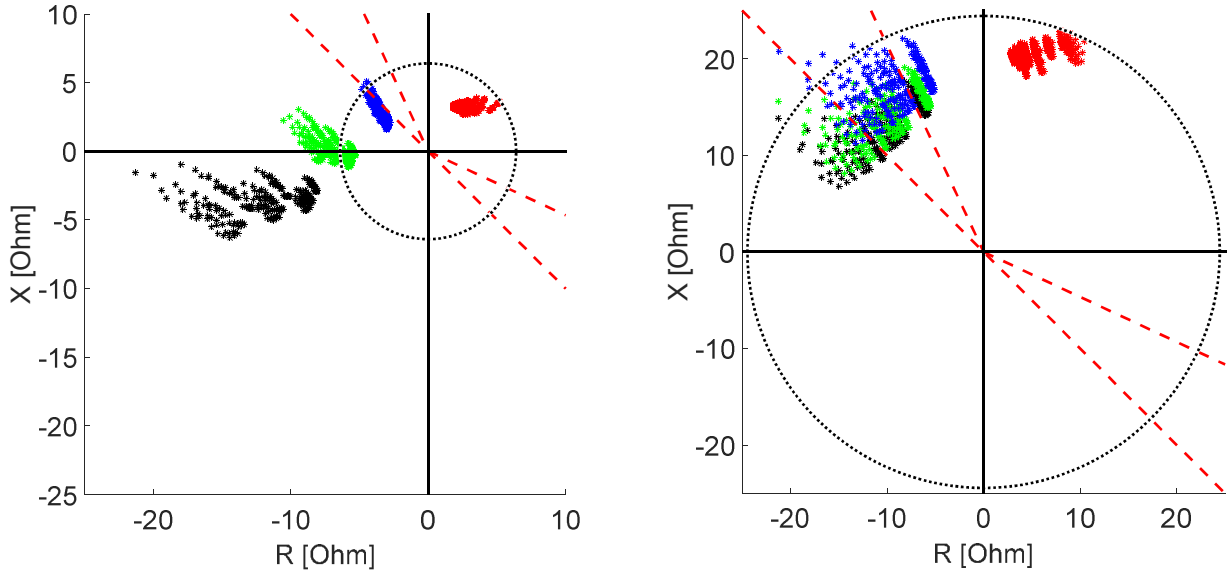

Figure 6 - Fault loop impedance at MAL (left) and LAG (right) for a SPTG fault (red stars) and a combined fault (remaining colours) at 10km from MAL, with the higher voltage level lagging. Blue lines: Z_1 extended zone for autoreclosure for R/X=1. Circular black dots: Largest impedance of the SPTG fault

As expected the real part of the loop impedance is negative for a fault where the higher voltage level is lagging the lower voltage level. It can also be seen that in absolute values the network strength affects the real part of the loop impedance, alike the combined fault with the higher voltage level leading (Figure 4), but with lower absolute values, which can be explained via (7); in this case the value 2.1 subtracts to 0.78 resulting in an absolute value of 1.32, whereas for the leading case they add, resulting in an absolute value of 2.88. The relation between these values is not the same in the simulations, because of the simplifications in (7), but the principle is the same.

The imaginary part moves from inductive to capacitive (Figure 6-left) as the network becomes weaker alike previously, but it shows a slightly more inductive behaviour than for the case with the higher voltage level leading. This is expected and explained using (7), as for the combined fault where the higher voltage level lags the value 0.21 adds to the 7.8 instead of subtracting.

A potential issue when the higher voltage level lags the lower voltage level is the high number of cases where the fault will be in the reverse direction, especially for the distance relay closer to the fault (MAL), which means a larger delay time before tripping the line. However, in this case the line should be protected

by the distance relays installed at the lower voltage level. Figure 7 shows the RX diagrams of the fault loop impedances for the distance relays installed in the MAL and HAT 150kV feeder for the same fault of Figure 6. In this case the distance relays at the lower voltage level see the faults in the forward direction. However, the values are much closer to the zone limit than for the higher voltage level and surpassing them for some of the short-circuit power combinations. Before discussing this behaviour and given the proximity of the loop impedance to the limits of the extended Z_{1B} zone for some of the cases, the simulations are redone considering a distance of 1km to the busbar, instead of 10km.

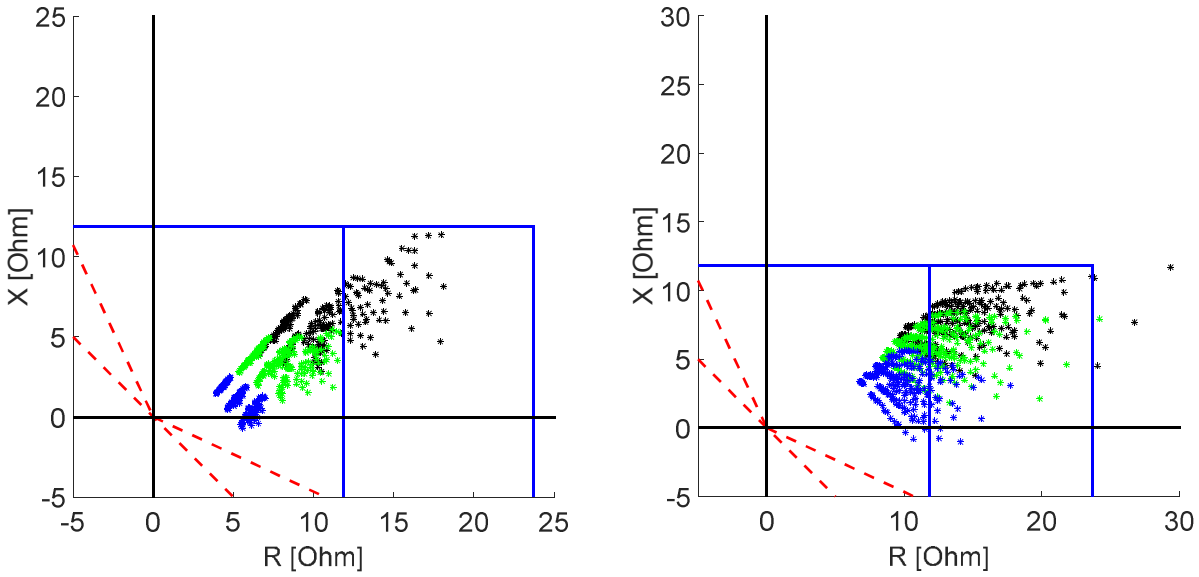

Figure 7 – Fault loop impedance at MAL-150kV (left) and HAT (right) for a combined fault at 10km from MAL, with the higher voltage level lagging. Blue lines: Z_1 extended zone for autoreclosure for R/X=1 and R/X=2

Figure 8 shows the results for the distance relays at the lower voltage if the higher voltage level lags the lower voltage level for a fault at 1km from MAL. The simulation shows several cases where the fault loop impedance is outside of the extended protection zone for the distance relay installed in the far end of the line, for both the real and imaginary parts. The approximation of the loop impedances to the limits of the extended zone and even their surpassing in some cases can be explained by using an equation analogous to (7), but for the distance relay installed in the lower voltage level, together with the shorter length of the lines. In this case, the equation is given by (8), with the x now representing the relation between the Thévenin equivalent of the lower voltage network and the loop total impedance.

$$Z_{R\_150} = a\left(\left(0.22 \mp 2.1 - x\right) + j\left(2.2 \pm 0.21 - 10x\right)\right) \quad (8)$$

Thus, the conclusions previously done for the higher voltage level regarding the influence of the short-circuit power continue to be valid for the lower voltage level, as the expressions are similar. A comparison of the equations and simulations even shows that the variations in the fault loop impedances due to the short-circuit power variations are slightly larger for the higher voltage level than for the lower voltage level. However, as the lower voltage line is shorter and the limits of the extended protection zone lower, the variations caused by changes in the short-circuit power lead to the loop impedance ending outside of the extended protection zone, as seen in Figure 8.

Figure 9 confirms this explanation by showing the fault loop impedance for the same fault, but with the higher voltage leading. In this case the distance relays from the higher voltage level see the fault inside of the extended protection zone with R/X=1 for practically all cases, with the exceptions being for the same reason of Figure 4. Thus, if the lines of the two voltage levels were of similar total impedance, the problem would be minimised when the distance relays of the lower voltage level are expected to clear the fault. This could happen if the two lines were in parallel along the entire way, but it is not unusual to have the lower voltage level connected to busbars in-between the busbars of the higher voltage level.

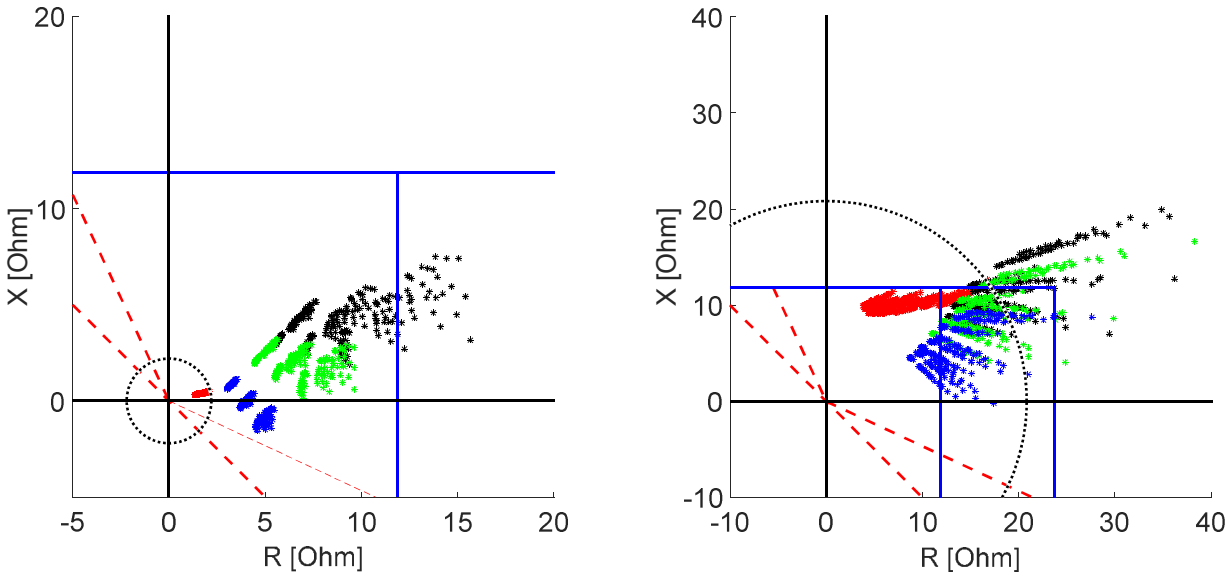

Figure 8 - Fault loop impedance at MAL-150kV (left) and HAT (right) for a combined fault at 1km from MAL, with the higher voltage level lagging. Blue lines: Z_1 extended zone for autoreclosure for R/X=1 and R/X=2. Circular black dots: Largest impedance of the SPTG fault

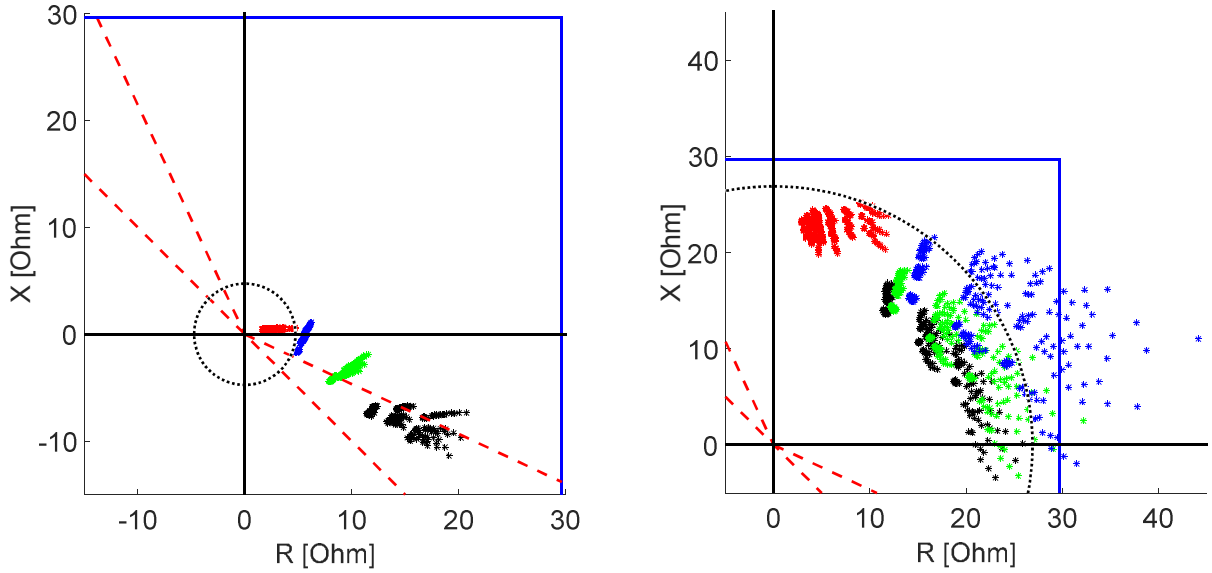

Figure 9 – Fault loop impedance at MAL (left) and LAG (right) for a SPTG fault (red stars) and a combined fault (remaining colours) at 1km from MAL, with the higher voltage level leading. Blue lines: Z_1 extended zone for autoreclosure for R/X=1. Circular black dots: Largest impedance of the SPTG fault

4. Discussion

This paper analysed combined faults between multiple circuit lines with different voltage levels and presents a protection philosophy for such lines, based on distance protection relays without pilot schemes. A thoroughly theoretical analysis supported by detailed simulations of a real multiple circuit line was done and the results show that just some changes in the settings used for SPTG faults setting, together with a preventive measuring when connecting the lines to the substation, are sufficient to assure the protection of the lines against combined faults for the majority of the cases.

Previous papers [1],[2] showed both via simulation and fault records that some distance relays see these faults in the reverse direction, which raised issues regarding potential delays in the clearing of such faults that could endanger a proper protection of the system. It was demonstrated in Part I that if the higher voltage level leads the lower voltage level, the fault current flows in the forward direction for the former, whereas the latter sees the fault current flowing in the reverse direction; the opposite happens if the higher voltage level lags the lower voltage level. This conclusion was based on an analytical model developed using symmetrical components for combined faults and verified via simulations for different systems and short-circuit powers.

The next step was the comparison of the fault current for combined faults and equivalent SPTG faults. Equations were developed in Part I using typical relations between symmetrical impedances and it was demonstrated that the current magnitude of a combined fault is typically slightly larger than of a SPTG fault at the same location at the higher voltage level; the exception being a system with a high short-circuit impedance in the higher voltage level and low short-circuit impedance in the lower voltage level, but only for a relation of short-circuit powers that is not expected in real systems.

If overcurrent relays are used as backup protection the comparison of the currents magnitudes demonstrated that they will be able to protect the lines for combined faults. However, the main case of interest is distance relays, without overcurrent relay backup, which requires the analysis of RX diagrams.

The combined faults are expected to happen between lines with a 120˚ phase difference. As a result, a distance relay sees combined faults with a higher resistance, when compared with SPTG faults, which are mostly inductive. The short-circuit powers of the different nodes have a substantial impact on the impedance seen by the distance relays for a combined fault, as the fault current flows through the Thévenin impedances. The fault loop impedance in absolute value seen by the relays in strong networks for combined faults is approximately equal to the one of a SPTG fault or even smaller, but it increases as the network becomes weaker. The phase variation for a SPTG fault at the same location depends on the voltage magnitude of the two voltage level in the tower: as an example, it is approximately 15˚ for a combined fault involving 400kV and 150kV and strong networks, but it varies with the short-circuit power. If the higher voltage level is leading, the distance relays from this voltage level see the loop impedance inside of the Z_{1B} zone, with the real part of the loop impedance getting closer to zone's threshold as the short-circuit power decreases. The distance relays installed at the lower voltage levels see the fault in the reverse direction, but the disconnection of the distance relays at the higher voltage level is sufficient to interrupt the fault loop. The simulations showed that the distance relay installed at the far end may see the loop impedance outside of the extended protection zone, because of too large resistance, when considering a R/X relation of 1 to the distance relay and using the reactance of the line as reference. Therefore, it is suggested to increase the R/X relation used for SPTG faults when using the distance relays for protecting multiple-circuit transmission lines. The distance relay installed at the closest end may also see in some cases the loop impedance outside of the extended protection zone, because the fault loop impedance may become capacitive. In order to assure a proper protection in these cases, it is advised to increase the angle separating the forward from the reverse zones.

It is important to refer that these extra precautions should not be necessary for the majority of the systems. The ending of the fault loop impedance outside of the protection zones happens for very low short-circuit

powers, not likely to be present in areas where one is expected to install multiple-circuit transmission lines; moreover, for these problems to occur it is required a combination of high short-circuit power in some busbars with low in others, which is also not expected to happen.

If the lower voltage level leads the higher voltage level, the distance relays installed at the busbars of the former are expected to clear the fault, as they should see the fault loop impedance in the forward zone, whereas the distance relays installed at the higher voltage level see it in the reverse zone. However, the risk of the fault loop impedance ending outside of the extended protection zone is higher in this case, because the length of the lines at lower voltage levels is often shorter than of the lines at higher voltage levels, resulting in lower thresholds for the extended protection zone. If the lines are of similar length the problem is minimised, but as the short-circuit impedance of the higher voltage level is expected to have a larger value, the variation in the fault loop impedance seen by the distance relays due to the variations in the short-circuit power is still expected to to be larger at the lower voltage level.

Based on the theory and demonstrations previously done it is suggested that the best way to protect multiple-circuit transmission lines with different voltages is to have a preventive attitude when connecting the phases and to assure that any prospective combined faults can only occur with the higher voltage level leading the lower voltage level (e.g., see Figure 2-right). The unbalancing of the lines is still minimised and the distance relays at the higher voltage level assure the clearing of the fault by seeing it as a SPTG fault, with a higher level of certainty.

Only temporary faults were considered for setting the protections zones. However, given the nature of the phenomenon and the type of analysis performed the conclusions can be extended for permanent fault, but doing the corrections that are also made for SPTG faults, because of the reduction of the protection zone from Z_{1B} to Z_1, which protects only 85%-90% of the line.

The dead time was not analysed in this paper and it is assumed that it would be sufficient to clear the fault. Given the coupling between voltage levels, even when disconnecting all three phases in one of the voltage levels, it is advised to set the dead time at least equal to the one that would be used for single-phase autoreclosure, even if doing three-phase autoreclosure.

An issue of interest to study in future work that is outside of the scope of this paper are the presence of overvoltages in multiple-circuit lines associated to fault clearing of combined faults, since the couplings and current flow during a fault are different from the typical scenarios.

Other topics of interest would be to compare the loop impedance RX diagram accounting for time, i.e., the impedance locus, and cascaded events. These are also left for future work.

5. Conclusion

This paper analysed faults between different voltage levels in multiple-circuit transmission lines with shared tower. It was demonstrated that the protection settings used in distance relays to protect the line against single-phase-to-ground faults also protect the line in the event of a combined fault, for typical short-circuit powers. The main differences between these two types of fault is the more resistive characteristic of the combined faults as compared with SPTG faults and the larger influence of the network's short-circuit power in their fault loop impedance. Consequently, it can be advised to increase the R/X relation used to set the extended protection zone Z_{1B} when having multiple circuit lines with different voltage levels, if the short-circuit power is low.

This conclusion is valid for combined faults where the faulted phase of the higher voltage level leads the one from the lower voltage level and it is suggested to layout the phases in a way that composite faults can only occur in this way. If the lower voltage levels leads the higher voltage level the line is still expected to be protected by the distance relays from the lower voltage level when using the settings of SPTG faults, but a R/X relation has to be increased and this may not be sufficient, as the imaginary part of the fault loop impedance can be too high, meaning that there is a higher risk of the distance relay not operating immediately. This happens for cases where the line of the lower voltage level is shorter than of the higher voltage level, being the problem minimised if the lines of the two voltage levels are of the same length.

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7. References

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