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Enhanced current and voltage regulators for stand-alone applications

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***Abstract*— State feedback decoupling permits to achieve a better dynamic response for Voltage Source in stand-alone applications. The design of current and voltage regulators is performed in the discrete-time domain since it provides better accuracy and allows direct pole placement. As the attainable bandwidth of the current loop is mainly limited by computational and PWM delays, a lead compensator structure is proposed to overcome this limitation. The design of the voltage regulator is based on the Nyquist criterion, verifying to guarantee a high sensitivity peak. Discrete-time domain implementation issues of an anti-wind up scheme are discussed as well. Laboratory tests in compliance with the standard for UPS systems (IEC 62040-3) are performed to validate the theoretical analysis.**

Keywords—voltage control; current control; power quality; uninterruptible power systems

I. INTRODUCTION

The spread diffusion of energy sources, interfaced by means of power converters requires demanding dynamics performance of voltage and current regulators. With reference to hierarchical control in microgrids [1], the performance of the overall control structure can be significantly lowered whenever the innermost loops do not guarantee high dynamic performance. The primary control of Voltage Source Inverters (VSIs) for stand-alone applications usually consists of loops in cascade, the innermost one being the inductor or capacitor current regulator.

The current loop is responsible for fast dynamics and should be designed for a bandwidth as wider as possible. Unfortunately, the main limitation in a fully-digital implementation is represented by computational and PWM delays. The outer voltage loop is responsible to track the desired reference with slower dynamics than the current regulator. Among the selection of the controlled states, the inductor current and capacitor voltage are usually preferred. However, the coupling between the two states variables significantly lowers the dynamics and tracking capability of the regulators.

In this context, an active control action to decouple the controlled states can be implemented. As a consequence, the damping and reference tracking capability are significantly improved. Ideally, system dynamics is not affected by the disturbance, represented by the output current in stand-alone applications. However, in real implementations not compensated system delays in the decoupling path forbid to completely decouple the states, thus reducing the effectiveness of the active control action.

The design of the regulators can be performed starting from the continuous-time domain by deriving Laplace-domain models, which provide a general perception of system dynamics [2]. Subsequently, some discretization method is employed for digital implementation.

However, the mapping from the *s*-domain to the *z*-domain can introduce some mismatch in the poles location [3], specifically for discretization of high-frequency harmonic compensators. On the other hand, the direct design of digital compensators in the discrete-time domain provides more accuracy. In fact, the use of Z-transformation allows to treat the latch effect and time lag precisely [4], without requiring the use of approximated rational transfer functions for modelling system delays [5].

Other advantages can be recognized such as: i) design for direct pole-assignment [6]; ii) improved dynamic performance and robustness of the regulators [7], especially if the current regulator is designed to achieve wide bandwidth [8]. According to the previous discussion, direct design in the discrete-time domain can be considered useful.

As recently proved in [9], the state feedback decoupling action can be improved by leading the capacitor voltage on the decoupling path. However, the analysis is performed in the continuous-time domain and the possibility to widen the current loop bandwidth using a lead compensator on the forward path is not investigated.

This paper is organized as follows. In Section II the analyzed system is introduced paying attention to its corresponding block diagram representation. In Section III the current regulator is designed in the discrete-time domain, together with the lead compensator, to achieve a wider bandwidth. In Section IV the voltage regulator tuning is performed by means of Nyquist criterion. The design of an anti-wind up scheme is also proposed. Finally, in Section V experimental results from a lab-test are shown to support the theoretical analysis.

II. SYSTEM DESCRIPTION

In a stand-alone configuration, the VSI is usually operated in voltage control mode to provide the desired output voltage. Moreover, a second-order LC filter is employed to smooth the inductor current and output voltage.

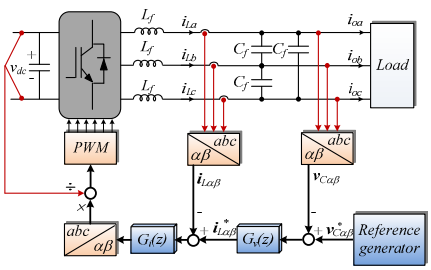


Fig. 1. Block diagram of a three phase VSI with voltage and current loops.

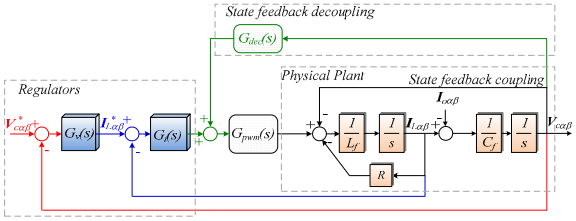


Fig. 2. Block diagram representation the closed-loop system in the continuos-time domain.

With reference to Fig. 1, the inner current loop has to track the commands provided by an outer voltage loop. At the same time, rejection of any disturbance within its bandwidth must be guaranteed [10]. The block diagram representation of the closed-loop system in the continuous-time domain is shown in Fig. 2, where $\boldsymbol{V}^*_{C\alpha\beta}$ and $\boldsymbol{I}^*_{L\alpha\beta}$ are the voltage and current reference vectors and $\boldsymbol{I}_{o\alpha\beta}$ is the output current vector, which represents a disturbance to the system. The current and voltage regulators transfer functions (TF) in the continuous-time domain are represented by $G_i(s)$ and $G_v(s)$. A first order Padé approximation of the type $G_{PWM}(s) \cong [1-(T_d/2)s]/[1+(T_d/2)s]$ is used to model computational and PWM delays, where $T_d = 1.5/f_s$, being f_s the switching frequency. $G_{dec}(s)$ is the TF associated to the decoupling of the controlled states.

Similarly, the closed-loop diagram in the discrete-time domain is shown in Fig. 3. Compared to Fig. 2, system delays can be exactly modelled by one sample delay due to the implemented regular sampled symmetrical PWM strategy [11] and the latch interface from the digital compensators to the physical plant.

III. Current Regulator Design

The design of the controllers is based on serial tuning. To provide a general perception of the effects of voltage decoupling, the analysis is firstly performed in the continuous-time domain with the system parameters shown in Table I.

TABLE I. System Parameters

Parameter	Value
Switching frequency	$f_s = 10\ kHz$
Filter inductor	$L_f = 1.8\ mH$
Filter capacitance	$C_f = 27\ \mu F$
Inductor ESR	$R_f = 0.1\ \Omega$
Resistive linear load	$R_l = 68\ \Omega$
Nonlinear load	$C_{NL} = 235\ \mu F$ $R_{NL} = 155\ \Omega$ $L_{NL} = 0.084\ mH$

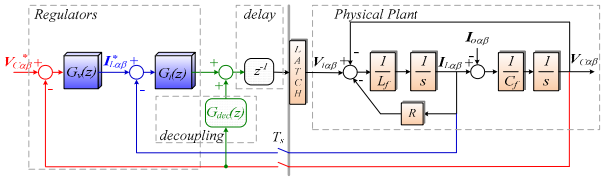


Fig. 3. Block diagram representation of the closed-loop system in the discrete-time domain.

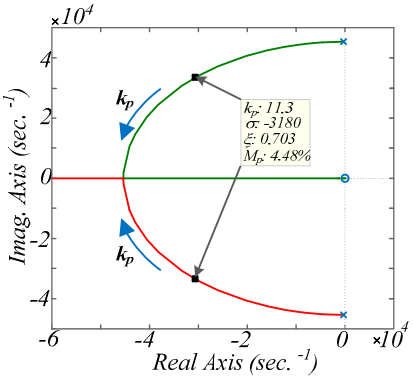


Fig. 4. Root locus for the inner current loop with P regulator and without voltage decoupling, neglecting system delays: x - open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI} = 11.32}$; o - zeros.

A. Continuous-time domain modelling

The proportional gain k_{pI} is set to achieve the desired current loop bandwidth (f_{bw}). By neglecting the delays of the system, the regulator gain can be evaluated by

$$k_{pI} = 2\pi f_{bw} L_f. \tag{1}$$

For the overall delay $T_d = 1.5T_s = 150\ \mu s$ and a bandwidth of 1 kHz, this gain is approximately $k_{pI} = 11.32$. With reference to the root locus in Fig. 4, it can be noticed that as the gain is increased, i.e. the bandwidth is widen, higher damping is achieved. It should be noted this behaviour is in contrast with the results where computational and PWM delays are included in the analysis.

On the other hand, as computational and PWM delays are considered in the analysis, the regulator gain for the same bandwidth is $k_{pI} = 5.61$ (see Fig. 5).

It can be seen that, if the controlled states are coupled, low damping with high overshoot is expected. This trend is not dependent on the gain value. Moreover, as expected, the increment of the gain effectively lowers the system damping. If the states are ideally decoupled (see Fig. 6), the order of the system is lowered to a second order degree and higher damping is achieved with less overshoot for the same bandwidth.

B. Discrete-time domain modelling

With reference to Fig. 3, the input voltage represents the latched input to the physical system. A P controller and a RL load modelled in the discrete-time domain are considered [8], as shown in Fig. 7. This block diagram in the stationary reference frame can be used for analysis since the ideal

decoupling of the controlled states determines no load dependence.

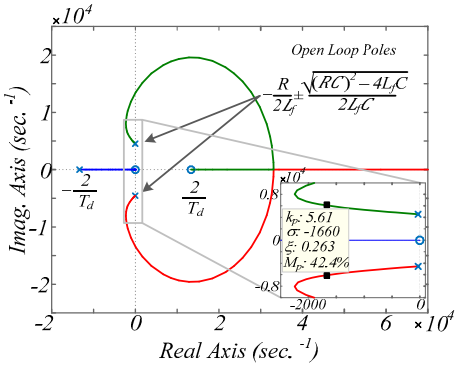


Fig. 5. Root locus for the inner current loop with P regulator and without voltage decoupling, including system delays: x - open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI} = 5.61}$; o - zeros.

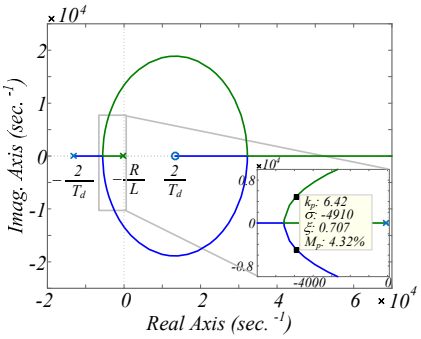


Fig. 6. Root locus for the inner current loop with P regulator and ideal voltage decoupling: x – open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI} = 6.42}$; o – zeros.

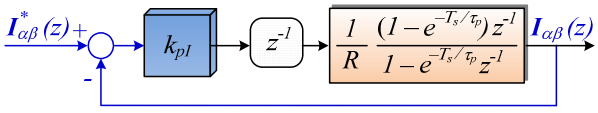


Fig. 7. Simplified block diagram of the current loop closed-loop system in the discrete-time domain.

The closed-loop TF of the inner current loop system in Fig. 7 is

$$\frac{\boldsymbol{I}_{\alpha\beta}(z)}{\boldsymbol{I}_{\alpha\beta}{}^{*}(z)} = \frac{k_{pI}b}{z^2 - az + k_{pI}b} \tag{2}$$

Where $b = (1 - e^{-\frac{T_S}{\tau_p}})/R; a = e^{-\frac{T_S}{\tau_p}}$.

The corresponding root locus is shown in Fig. 8.

Because of the delay, there is a limitation in the gain to achieve a well-damped system. Since there are two poles and only one variable (k_{pI}) that can change their locations, direct pole placement is not allowed. The designed gain to achieve a damping of $\xi = 0.662$ is $k_{pI} = 6.42$, as reported in Table II. To widen the bandwidth while still preserving a well-damped closed-loop system, a lead compensator structure as shown in Fig. 9 is designed [12].

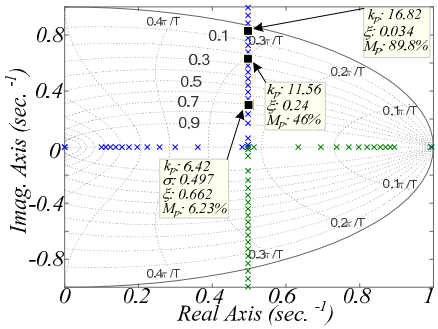


Fig. 8. Root locus of RL load including the lag introduced by PWM update.

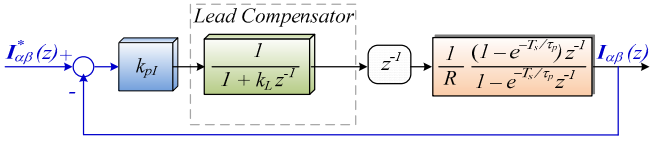


Fig. 9. Model of RL load including the lag introduced by PWM update, with the model of the lead compensator $G_L = 1/(1 + k_L z^{-1})$.

The closed-loop TF becomes

$$\frac{\boldsymbol{I}_{\alpha\beta}(z)}{\boldsymbol{I}_{\alpha\beta}{}^{*}(z)} = \frac{k_{pI}b}{(z + k_L)(z - a) + k_{pI}b}. \tag{3}$$

The poles of this TF must satisfy the relationship

$$z^2 - (p_1 + p_2)z + p_1p_2 = z^2 + (k_L - a)z - k_La + k_{pI}b. \tag{4}$$

being p_1, p_2 the desired pole locations, defined as

$$p_{1,2} = e^{-\xi\omega_n T_s}[\cos(\omega_d T_s) \pm jsin(\omega_d T_s)],$$

$$\omega_d = \omega_n\sqrt{1 - \xi^2}.$$

Solving the system leads to

$$\begin{cases} k_L = a - (p_1 + p_2) \\ k_{pI} = (p_1p_2 + k_La)/b \end{cases} \tag{5}$$

Given $\omega_n = 2\pi 3000\ rad/s$ and $\xi = 0.707$, the poles are located at $p_{1,2} = 0.0632 \pm j0.254$. The controller and lead compensator gains are also presented in Table II. The corresponding root locus with the lead compensator $k_L = 0.868$ is reported in Fig. 10. The poles location is more on the left compared to Fig. 8, which means the system is faster. Therefore, the proposed technique provides a wider bandwidth for almost the same damping factor.

TABLE II. CURRENT REGULATOR PARAMETERS

Parameter	Value
Proportional gain without lead	$k_{pI} = 6.42$
Proportional and lead gains @$\boldsymbol{\omega_n = 2\pi 3000}$ rad/s	$\begin{cases} k_{pI} = 16.82 \\ k_L = 0.868 \end{cases}$

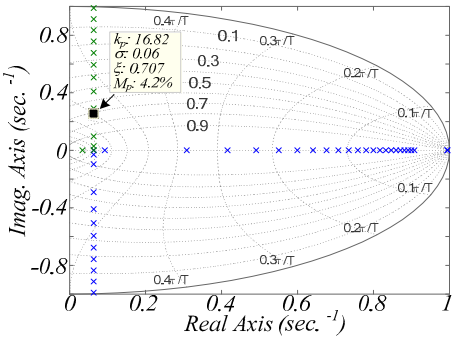


Fig. 10. Root locus of RL load including the lag introduced by PWM update, with the lead compensator: $k_L = 0.868$.

IV. Voltage Regulator Design

The voltage control loop employs PR controllers with lead compensators. The proportional gain k_{pV} is designed to achieve a bandwidth of around 300 Hz for the voltage regulator. It must be pointed out that such a wide bandwidth can be set because the current regulator bandwidth is spread via the lead compensator on the forward path. The design criterion is based on [9], such that the trajectories of the open loop system on the Nyquist diagram, with the PR regulators at fundamental, 5th and 7th harmonics, guarantee a sensitivity peak $1/\eta$ lower than a threshold value. The voltage regulator parameters are shown in Table III.

TABLE III. Voltage Regulator Parameters

Parameter		Value	
Proportional gain		$k_{pV} = 0.06$	
Integral gains and lead angles	@50Hz	$k_{iV,1} = 40$	$\varphi_1 = 3.3°$
	@250Hz	$k_{iV,5} = 15$	$\varphi_5 = 37°$
	@350Hz	$k_{iV,7} = 15$	$\varphi_7 = 44°$

The Nyquist diagram with the harmonic compensators at fundamental, 5th and 7th harmonics is shown in Fig. 11. The sensitivity peak is lower than 0.4, i.e. $\eta > 0.4$, thus fulfilling the design requirements. To avoid saturation of the resonant term in the voltage regulator an anti-wind up scheme is implemented, as the one shown in Fig. 12 [13]. No anti-wind up scheme is needed for the current loop since a P controller is used as regulator.

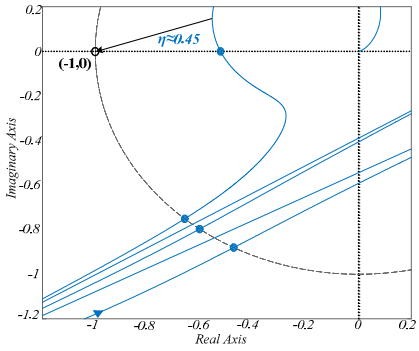


Fig. 11. Nyquist diagram of the system in Fig. 3.

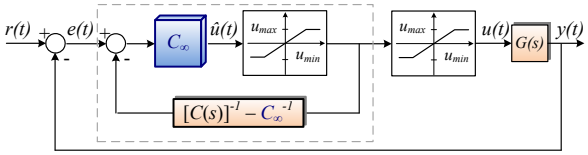


Fig. 12. Anti-wind up scheme based on [13].

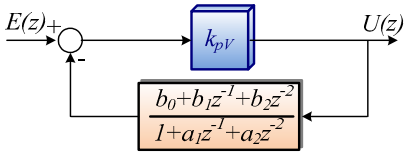


Fig. 13. Anti-wind up implementation in the discrete-time domain during normal operation.

According to [13], the controller $C(s)$ should be biproper and minimum phase. If these conditions are satisfied, the controller can be divided into a direct term (C_∞) and a strictly proper TF $\bar{C}(s)$ as

$$C(s) = C_\infty + \bar{C}(s) \tag{6}$$

For the case of an ideal PR controller it leads to

$$C_\infty = k_{pV}; \qquad \bar{C}(s) = k_{iV}\frac{s}{s^2 + \omega_o^2} \tag{7}$$

$$C(s) = k_{pV} + k_{iV}\frac{s}{s^2 + \omega_o^2} \tag{8}$$

During normal operation, i.e. $u_{min} < \hat{u}(t) < u_{max}$, the closed-loop TF, represented within the dotted line in Fig. 12, is equal to $C(s)$. During saturation the input to the controller states is bounded. As the anti-wind up scheme is implemented in the discrete-time domain, some interesting issues arise. In general, the discrete-time implementation of the feedback path in normal operation (without the saturation block) takes the form in Fig. 13. If $b_0 \neq 0$, an algebraic loop arises. This is directly related to the discretization method used for $\bar{C}(s)$. A possibility to avoid the algebraic loop can be the use of discretization methods like Zero-Order Hold (ZOH), Forward Euler (FE) or Zero-Pole Matching (ZPM), which assure $b_0 = 0$. However, the performance of the voltage controller is degraded if FE is used [14] since zero steady-state error is not achieved. This can be seen in Fig. 14, where the frequency response of the controller discretized with these methods is plotted. The gain at resonant frequency is no more infinite if FE is used as discretization method.

V. Experimental Results

With reference to the system of Fig. 1, lab-tests are performed to validate the theoretical analysis. To this extent, a medium power setup has been built using a Danfoss 2.2 kVA inverter developed for the automotive sector, controlled by dSpace DS1006 platform. Additional information regarding the LC filter and the reference loads used are reported in Table I. All the tests have been performed decoupling the controlled states.

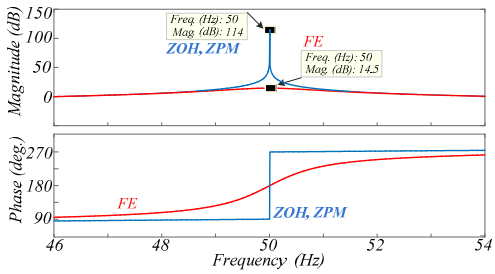
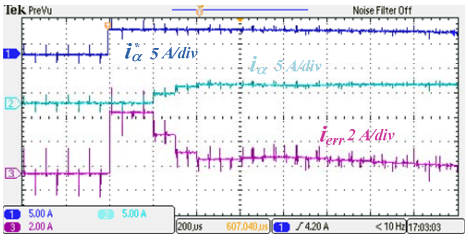


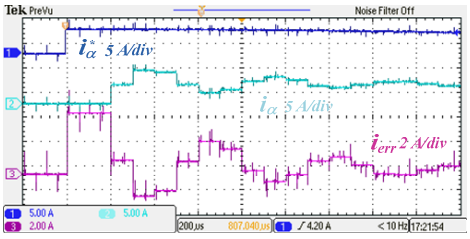
Fig. 14. Frequency response of the resonant controller using ZOH, ZPM and FE.

To effectively compare system dynamics a proportional controller with/without lead compensator is used, and a step change of the inductor current is imposed. Without lead compensator (see Fig. 7), the current response is not well-damped as k_{pI} is increased [see Fig. 15 (a)]. This result also shows that due to additional losses the experimental setup has more damping than expected. With reference to Fig. 15 (b) the step response is even less damped and with more oscillations as $k_{pI} = 11.56$. It is clear that the bandwidth is limited and this is mainly due to system delays.

If the control structure with a lead compensator is implemented (Fig. 9), the bandwidth can be increased respect to the test with a P controller only, for the same k_{pI} value, still achieving a well-damped response. The step response for $\omega_n = 6000\pi\ rad/s$, corresponding to $k_{pI} = 16.82$ according to the theoretical analysis, is less oscillatory, as can be seen in Fig. 16 (a).



(a)



(b)

Fig. 15. Step response – P controller: (a) $k_{pI} = 6.42$, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis); (b) $k_{pI} = 16.82$, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis).

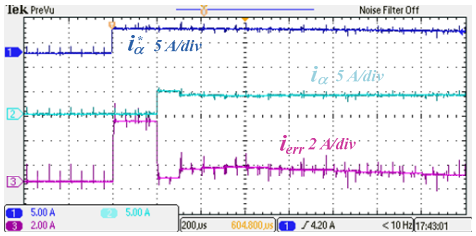
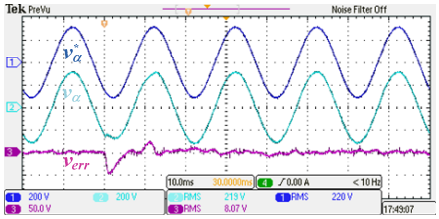


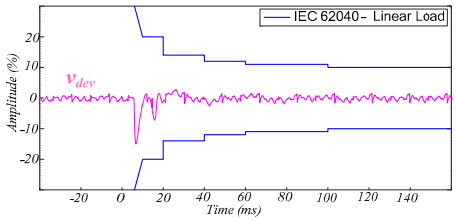
Fig. 16. Step response – P controller with lead compensator: $k_{pI} = 16.82$, $k_L = 0.868$, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis).

Fig. 17 and Fig. 18 show the control performances including both the voltage and current loops. Voltage decoupling is performed, a P controller is used as current regulator along with the lead compensator and the anti-wind up scheme proposed in the previous section is applied to the voltage regulator.

Fig. 17 (a) shows a full step change from open circuit to rated resistive linear load. The output voltage during transient is compared to the envelope of the voltage deviation v_{dev} according to IEC 62040-3 normative for UPS systems [see Fig. 17 (b)]. The capacitor voltage reaches steady-state in less than half a cycle after the load step change, verifying by a large extent the requirements imposed by the standard.



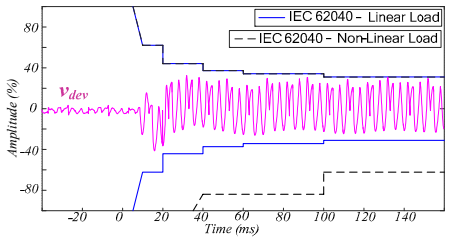
(a)



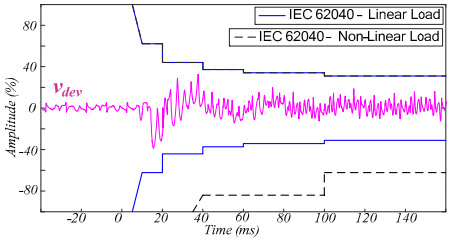
(b)

Fig. 17. Linear step load changing (0 – 100%): (a) reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (b) Dynamic characteristics according to IEC 62040-3 standard for linear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$).

A diode bridge rectifier with LC output filter supplying a resistive load is used as nonlinear load. Its parameters are reported in Table I. A full step change of the nonlinear load is performed with the harmonic compensator (HC) at fundamental only [see Fig. 18 (a)]. Subsequently, the voltage dynamics and steady-state performance are also verified with additional HC tuned at 5th and 7th harmonics [see Fig. 18 (b)]. The results show good agreement with the limits imposed by IEC 62040-3 (Uninterruptible power systems (UPS) - Part 3: Method of specifying the performance and test requirements), even for linear loads.



(a)



(b)

Fig. 18. Step response of the reference voltage: (a) without anti-windup scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (b) with anti-wind up scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis).

VI. Conclusions

An active control action based on the decoupling of the controlled states has demonstrated to provide better dynamics of power converters for stand-alone applications. The analysis proposed investigates other design and implementation features related to islanding application. Firstly, to enhance the current regulator dynamics, a lead compensator structure in the forward path is implemented. Its feasibility to widen the bandwidth, still preserving a well-damped system, has been demonstrated. This improvement in the current regulator permits to widen the bandwidth of the voltage loop. As the bandwidth of the voltage loop is widen, an anti-wind up scheme is even more needed. The proposed design in the discrete-time domain avoids algebraic loops, which could arise depending on the discretization method.

Experimental tests based on step response and step load change have been performed to verify the compliance with the standard IEC 62040-3 for UPS systems.

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