Supplementary Information

Graphene field-effect transistor array with integrated electrolytic gates scaled to 200 mm

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1. Experimental

1.1. Graphene synthesis and characterization

Single-layer graphene (SLG) was grown by chemical vapor deposition in a load-locked quartz tube 3-zone furnace (FirstNano EasyTube® 3000) onto 99.999% purity copper (Alfa Aesar) foils (25 μm thickness and ca. 25 × 25 mm in size). A gaseous mixture of methane/hydrogen at a gas flow rate ratio of (300 sccm of H2)/(50 sccm of CH4) was used for growth. The deposition was done as follows: after transferring the copper substrate into the reactor chamber, initial heating of the catalyst takes place at 1020 ºC for 20 minutes in a H2 atmosphere, for cleaning, increasing the grain size, and surface smoothing of the copper. Flow of the growth-precursor gas, methane, follows, keeping the hydrogen flow, for 30 minutes. Growth temperature is fixed at 1020 ºC and the pressure at 0.5 Torr. Both parameters have independent closed-looped control systems. The graphene grows on both sides of the copper foil.

For graphene transfer, a temporary poly(methyl methacrylate) (PMMA) substrate was used. PMMA was spin coated onto the top side of the graphene/Cu/graphene sample and copper was further dissolved by dipping the PMMA/graphene/Cu into a 0.5 M FeCl3 solution for 2 h. PMMA/graphene was cleaned in 2% HCl solution to remove metal precipitates and further washed in deionized water five times. PMMA/graphene films

were stored in ultrapure water before transferring to the pre-patterned silicon/silicon dioxide (Si/SiO2) wafer substrate. After transfer, the sample is dried with a N2 flow that also flattens the PMMA/graphene film followed by annealing for 7 hours at 180 °C to complete the drying process. The PMMA is then removed using warm acetone.

Graphene quality, i.e. the homogeneity of the obtained graphene film after transfer is first investigated by optical images. Confocal Raman spectroscopy was used to confirm the presence of SLG.

1.2. Fabrication of the graphene electrolyte-gated field-effect transistors (EGFET)

A 200 mm Si (100) wafer (B-doped, 8 – 30 Ω cm, LG Siltron) with 200 nm of thermal SiO2 was cleaned by ultrasonication in acetone for 5 min, rinsed sequentially in isopropanol and deionized (DI) water (≥ 18 MΩ.cm), and then dried in a nitrogen (N2) flow. The wafer was sputter-coated with chromium (Cr, 3 nm), used as adhesive layer, and gold (Au, 30 nm). Using optical lithography and ion milling, the wafer was patterned with 280 dies of ca. 10 mm in size, comprising of source and drain contacts each with a semicircular form 75 µm in diameter (channel width, W) separated by a gap (channel length, L) of 6.25, 12.5, and 25 µm, and contacts pads to connect to external measurement equipment.

An insulating layer of aluminum oxide (Al2O3, 320 nm) was patterned by lift-off on top of the contact lines, leaving uncovered the semi-circular area (corresponding to source and drain electrodes), prepared to receive the graphene. A planar ring-shaped gate of internal diameter 200 µm (figure 1c) separated ~50 µm from source and drain contacts was integrated in the transistor array. A thin layer of Al2O3 (10 nm) was deposited on top of the integrated-gate to protect it during the further microfabrication process.

The floating PMMA/graphene films were then transferred onto different areas of the pre-patterned wafer, until the desired degree of graphene coverage was obtained.

PMMA/graphene was patterned using optical lithography and oxygen plasma etching, keeping the integrated gates protected by Al2O3, which was later removed using diluted photoresist developer AZ400K 1:4 as etching agent.

After all lithographic steps, the wafer was cut into equal rectangular chips by dicing (dicing saw DISCO DAD 3350), each containing six graphene EGFETs. Each set of graphene EGFETs was washed in acetone and ethyl-acetate and dried with N2 flow, previously to the measurements.

1.3. Graphene EGFET electrical characterization

Graphene EGFETs were electrically characterized in phosphate buffered saline (PBS, Sigma-Aldrich P4417) solutions used as electrolytes. PBS has a total salt concentration of 161.5 mM. Measurements were performed in a computer-automated system using a Keithley 2400 source-meter and a Keithley 4687 picoammeter with an integrated voltage source. Transfer (output) transistor curves were obtained by fixing VSD and sweeping VG, and vice versa, while measuring ISD. Measurements were taken in air and the electrolyte was placed on the transistor channel by dropping of 5-20 µL from a micropipette. Some EGFETs were also electrically characterized in NaCl solutions with different ionic strengths (1.5, 15 and 150 mM) for testing. For comparison, a conventional Au wire was used as a gate electrode in selected devices. All experiments were carried out at a controlled temperature of 21-22 °C.

2. Raman analysis, imaging and interpretation

Raman analysis was performed in a Confocal Raman system Witec Alpha 300R using the software WITec Project Plus for data acquisition, and WITec Project FOUR+, for computing data. The Raman spectrum of graphene is characterized by the presence of two main modes, namely the G mode at ≈ 1580 cm^{-1} (first order in plane vibrational mode) and the 2D mode at ≈ 2690 cm^{-1}, which is a second-order overtone of a different in plane

vibration (of the D mode at ≈1350 cm^{-1} which corresponds to an inter-valley phonon and defect scattering). The presence of the otherwise forbidden D mode is an indication of defects in the graphene.

Raman image in Figure 3 in the main text was obtained using a Nd-Yag 532 nm line at a laser power of 1.5 mW a 100× objective with a 0.9 numerical aperture and an integration time of 1s, a XY scan was performed in a scan range of 110 μm × 90 μm, with a resolution of 110 pixels per line and 90 lines. A Raman spectrum was acquired and stored for each of the 9900 pixels. After background subtraction and cosmic ray removal, a cluster analysis was done. The cluster analysis consists in the identification of similarities in the Raman spectra of the analyzed area. In order to speed up the analysis and increase the relevance of the results, we used a filter that restricts calculations to selected spectral ranges that are used to identify graphene single and multilayers (D, G and 2D peaks were chosen). The software compares all stored Raman spectra and bins them according to their similarity. Each cluster is then represented by a Raman average spectrum calculated over all the spectra belonging to that cluster (Figure 3c). The clustering is finished when creating more sub-clusters does not change the average spectrum of the sub-cluster when compared to the parent cluster average spectrum. The three average spectra form a basis which is used to build the Raman image shown in Figure 3b. The (artificially) colored image follows from the expansion of all the spectra stored in the pixels in linear components over the three basis spectra. Each pixel color results from adding the colors of the basis spectra in an amount equal to the respective coefficients in the linear expansion of the spectrum stored in that pixel.

3. The effect of the asymmetry in contact area in the electrolytic gate capacitance

The EGFET gate capacitance is a series combination of two electrical double-layer capacitances plus the graphene quantum capacitance, C_q. The two EDLs form at the Au

gate contact/electrolyte interface and at the electrolyte/graphene interface, respectively. The first of these EDLs extends over an area A_1 equal to the gate contact area, which is the sum of the areas of the two ring-shaped lobes (see Figure S1). This area is equal to 3.32 mm^2. The second EDL forms over the channel area, A_2, which is equal to 9.4×10^{-4} mm^2, in case of a code 10 transistor (7.5×10^{-4} and 1.9×10^{-3} mm^2 for code 5 and code 20 devices, respectively). The three capacitors in series form a voltage divider. Although these capacitances are not directly measurable we can nevertheless make reasonable assumptions in order to estimate their order of magnitude. A reasonable value for C_q at a value of V_G arbitrarily taken from the data in Figure 2 (main text) or 5, e.g. V_G = 0.75 V, is 2 μF/cm^2, and the Debye length, λ_D, of the EDLs in PBS, is λ_D = 0.78 nm. With these assumptions we calculate the equivalent series capacitor, C_{eq}, of the three capacitors:

$$C_{eq} = \frac{A_1 \times C_{EDL1} \times A_2 \times C_{EDL2} \times C_{gr}}{A_1 A_2 \times C_{EDL1} C_{EDL2} + A_2 C_{EDL2} C_{gr} + A_1 C_{EDL1} C_{gr}} \quad \text{(S1)}$$

where,

$$C_{EDL1,EDL2} = \frac{\varepsilon \varepsilon_0}{\lambda_D} \text{ and } C_{gr} = C_q \times W \times L \quad \text{(S2)}$$

In equations (S2), ε is the dielectric constant of water, ε = 80 for C_{EDL1}, and, taking into account the hydrophobic gap that forms at the graphene/solution interface, we assumed arbitrarily[3] ε = 1, for water at the graphene interface, and used this number to calculate C_{EDL2}. W and L are channel width and length, respectively. Using equation (S1) and (S2) and the capacitive voltage divider, we compare the voltage drop at the graphene quantum capacitance for devices with different channel areas. The results confirm that, for a given gate voltage (V_G = 0.75 V, in this example) the voltage drop is larger for code 5 channel devices (V_q = 0.2714721 V), followed, in decreasing order, by code 10 (V_q = 0.2714718 V), and code 20 EGFETs (V_q = 0.2714712 V). The charge concentration per unit channel area is proportional to V_q, therefore GFETs with shorter channel will have their minimum conductivity point shifted towards lower voltages. The differences are minimal, of the

order of some μV in this example. This is not enough to explain the much larger shifts in V_G observed in Figures 2 and 5 in main text.

4. A portable Graphene EGFET

As a demonstration of graphene EGFETs portability and ease of use in sensing platforms we designed and fabricated a printed circuit board (PCB) to support the devices, which also provided easy, durable, and precise electrical connections to the sourcing and measuring equipment. The silicon chip containing the graphene EGFET was inserted in a Samtec MB1-120 connector, which is adequate for 0.7 mm silicon substrates. With the current design, up to three devices can be measured on each chip. A 3-pole switch selects which of the transistor circuits is addressed. Five banana connectors are provided at the PCB side opposite to the chip connection, to plug in the measuring equipment. Connections for source, drain, gate, ground, and an auxiliary port are provided.

Supplementary Figures

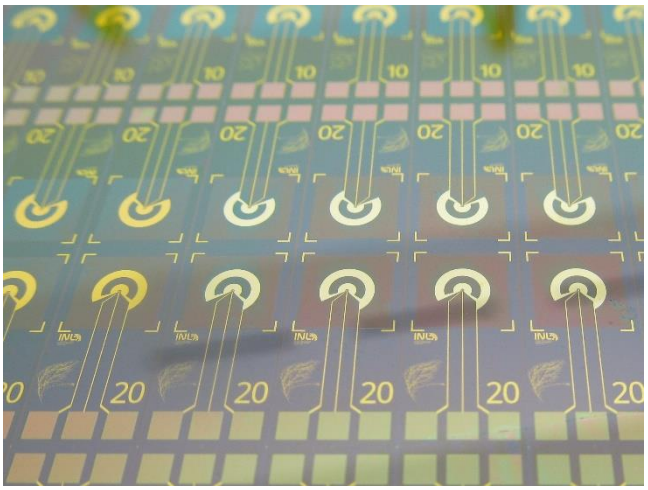

Figure S1. Partial view of the graphene transistor array, in an area where devices with channel length 25 μm (labelled 20), and 12.5 μm (labelled 10) are visible.

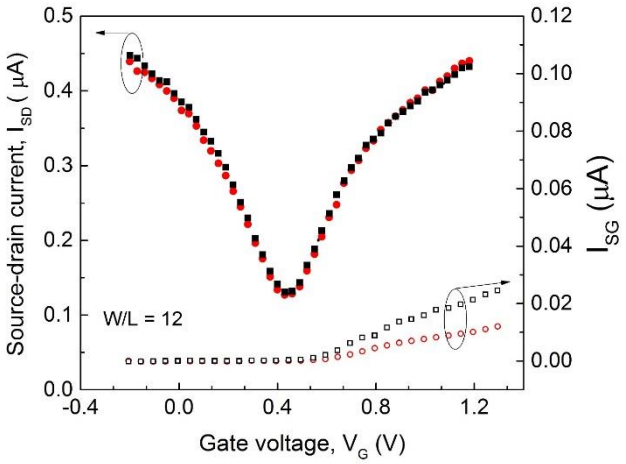

Figure S2. Transfer curves of a graphene EGFET gated via the integrated-gate (solid red dots) and via a conventional Au wire (solid black squares). Gate-source leakage current measured using the integrated-gate (open red dots) and the wire gate (empty black squares). Measurements performed in PBS at 25 °C.

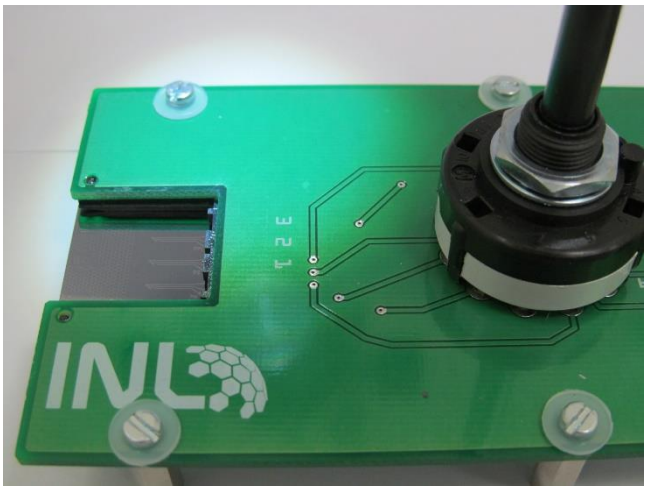

Figure S3. Printed circuit board designed for (a) easy plug-in of the graphene sensor, at one end, and (b) provide easy and rugged connection to electrical measuring equipment, at the other end. A 3-pole switch selects which of three different sensor circuits is addressed. The silicon chip is 25 × 22 mm^2 in size.