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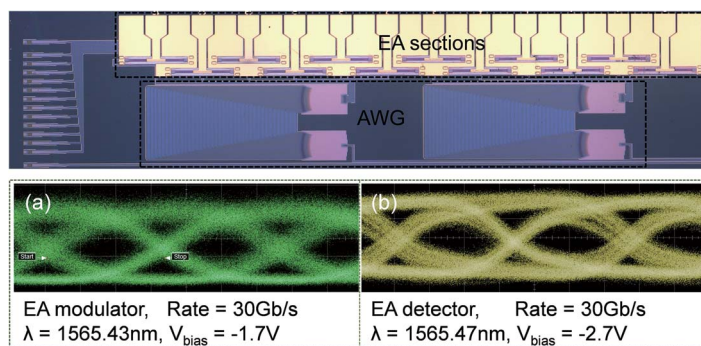
Wavelength-Multiplexed Duplex Transceiver Based on III-V/Si Hybrid Integration for Off-Chip and On-Chip Optical Interconnects

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EA modulator,   Rate = 30Gb/s
$\lambda = 1565.43$ nm, $V_{bias} = -1.7$V

EA detector,   Rate = 30Gb/s
$\lambda = 1565.47$ nm, $V_{bias} = -2.7$V

Wavelength-Multiplexed Duplex Transceiver Based on III-V/Si Hybrid Integration for Off-Chip and On-Chip Optical Interconnects

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Abstract: A six-channel wavelength-division-multiplexed optical transceiver with a compact footprint of 1.5×0.65 mm^2 for off-chip and on-chip interconnects is demonstrated on a single silicon-on-insulator chip. An arrayed waveguide grating is used as the (de)multiplexer, and III-V electroabsorption sections fabricated by hybrid integration technology are used as both modulators and detectors, which also enable duplex links. The 30-Gb/s capacity for each of the six wavelength channels for the off-chip transceiver is demonstrated. For the on-chip interconnect, an electrical-to-electrical 3-dB bandwidth of 13 GHz and a data rate of 30 Gb/s per wavelength are achieved.

Index Terms: Optical interconnects, waveguide devices, electro-optical systems.

1. Introduction

With the emergence of big data and super-computing, optical interconnects, first used in long-distance communication, have been considered as a promising technology for short-range applications, such as rack-to-rack, card-to-card, and even on-chip interconnects, in order to fulfill the ever increasing demand for low cost, high energy-efficieny, and high-bandwidth communication technology. Further increasing the data rate of a single channel poses many challenges to electrical signals and drivers [1]. On the other hand, optical interconnects provide a solution to cope with bandwidth and energy-consumption problems, which are hard to

overcome in electrical interconnects [2]. Monolithic integration based on III-V compound semi-conductor materials has already shown its potential for building photonic integrated circuits with various functionalities, including waveguides, filters, lasers, modulators, and detectors and has been adopted in fiber-based long-range communication systems [3], [4]. However, the expensive fabrication and material cost hinders further expansion of this type of monolithic integration to larger volumes [5], [6].

Silicon photonics, on the other hand, has its advantages for building low-cost and very large-scale photonic circuits due to the high refractive-index contrast of a silicon waveguide, the low optical loss in the communication wavelength range, and, most importantly, the compatibility with Complementary Metal–Oxide Semiconductor (CMOS) fabrication technology [7]–[9]. Many research groups and manufacturers have introduced a vast number of multi-functional, high-speed, and energy efficient devices, as well as demonstrator systems, for on-/off-chip intercon-nects based on the silicon photonics platform [10]–[13]. Although superior for passive circuits, silicon is not an ideal material for active functions, as compared to III-V ones. Based on the free carrier dispersion effect, a silicon modulator can work at a data rate of > 50 Gb/s, compromising either the device footprint and power consumption [14], [15] or the operational wavelength range [16]. Photo-detection on silicon also relies on the integration of other materials, such as germa-nium. Although germanium is often used also for electronic applications, its absorption drops quickly for wavelengths over 1600 nm [17], [18]. Germanium based EA-modulators thus far have not been shown to operate for wavelengths longer than 1580 nm [18], and efficient electri-cally pumped germanium lasers integrated on silicon have yet to be been shown [19]. Combing the best of both materials using hybrid integration through wafer bonding of III-V compound semiconductors onto silicon has recently led to the demonstrations of various active devices integrated on silicon [20]–[22]. The performance of these devices (such as lasers, modula-tors, and detectors) are already comparable to those based on the monolithic III-V approach [22]–[24]. Circuits such as multi-channel transmitters/receivers in different silicon chips con-nected by fibers have been demonstrated with an aggregate data rate over 100 Gb/s [25]–[27].

In this paper, we demonstrate a single silicon-on-insulator (SOI) chip which integrates a wave-length division multiplexed (WDM) optical transceiver module for off-chip and on-chip inter-connects using hybrid integration technology. The modulation and detection all rely on the electro-absorption (EA) effect of a IIIV-based quantum well (QW) epi-layer, which is integrated on a 6-channel arrayed waveguide grating (AWG) (de)multiplexer of a 1.6-nm channel spacing. Since the modulators and the detectors share the same EA structure, a duplex link can be achieved in the proposed transceiver [28], [29], which is not possible using normal all-silicon modulators or germanium detectors. An external laser was used for the measurement. 30 Gb/s capacity for each of the 6 wavelength channels with a low modulator driving voltage and a large extinction ratio for off-chip transmitter, as well as the same capacity with a high sensitivity for off-chip receiver, was obtained. For the on-chip interconnect, a 3-dB electrical-to-electrical band-width of 13 GHz and a data rate of 30 Gb/s per wavelength was measured.

2. Transceiver Design and Key Components

The presented transceiver consists of one SOI AWG (de)multiplexer and an array of hybrid inte-grated III-V EA sections, as shown in Fig. 1(a). When used as a transmitter [see Fig. 1(b)], the EA sections act as modulators, and external laser light is injected to the chip through grating couplers. As mentioned above, the same structure shown in Fig. 1(a) can also be used as a WDM receiver [see Fig. 1(c)] since the EA sections can also act as photo-detectors. This means that the transmitting and receiving functionalities of the structure can be switched over in the optical layer. Thus, thanks to the dual-functional EA sections, the proposed transceiver can work in a half-duplex manner. Furthermore, as bidirectional optical signals at different wave-lengths can transmit on the bus waveguide/fiber at the same time, the functions of different EA sections within one transceiver can be configured differently either as modulators or detectors. Such a link, in this case, operates in a full-duplex manner.
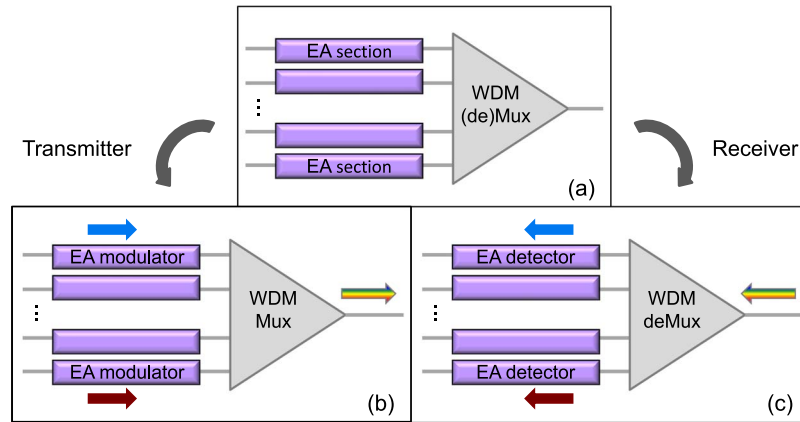
Fig. 1. (a) Present six-channel WDM optical transceiver architecture, which can be used as (b) transmitter or (c) receiver.
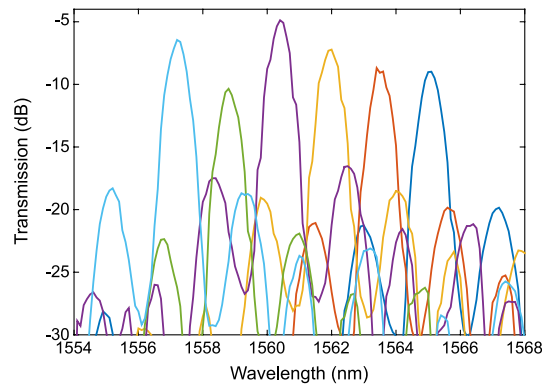

Fig. 2. Passive performance of the present transceiver chip showing the optical responses of the AWG integrated with the EA sections at different wavelength channels. The EA sections are biased at 0 V.

The AWG is designed with six wavelength channels and 1.6 nm channel spacing and was fabricated on an SOI wafer with 220 nm-thick top silicon layer through an ePIXfab multiple wafer run [30], together with all silicon routing waveguides and grating couplers. The loss of each grating coupler on the chip is ~7 dB. The transmission spectra for transverse electric polarized light from a single AWG integrated with the EA sections are shown in Fig. 2. Six dB–10 dB insertion losses and 10 dB–15 dB crosstalks were measured for the present (de)multiplexer, where the coupling losses between the fiber and the grating were normalized out. This loss comes partially from the AWG itself (2.5 dB–5 dB, due to imperfections in the fabrication), as well as the insertion losses for the EA sections (2 dB–7 dB) [26], which were fabricated using BCB adhesive bonding technology [31]. The 3-D structure of the EA section is sketched in Fig. 3. It includes a 100 μm long and 2 μm wide straight active segment and two 45 μm long bi-level adiabatic tapers for light coupling to and from the passive silicon waveguide [32]. To achieve a better coupling between silicon and III-V waveguides, a silicon rib waveguide structure constructed with a poly-silicon overlay of 120 nm thickness and 1.5 μm width under the III-V section is employed. The III-V layer stack contains InAlGaAs multiple-quantum-wells (MQWs) and two separate confinement heterostructure layers (SCHs) as described in Table 1. We refer to [26] for the detailed structure of the hybrid waveguide as well as the fabrication processes. A picture of the fabricated transceiver chip is shown in Fig. 4. The chip area occupied by one six-channel transceiver is about 1.5 $\times$ 0.65 mm^2, which is mostly taken by the AWGs and the metal contact pads.
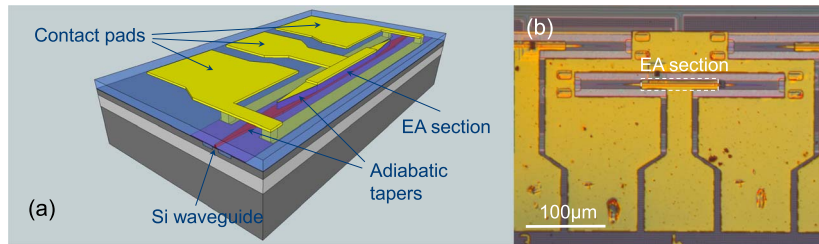
Fig. 3. (a) Three-dimensional sketch of the III-V/Si hybrid integrated EA section. (b) Top view of one fabricated EA section.

TABLE 1

Structure of III-V Epi-Layer

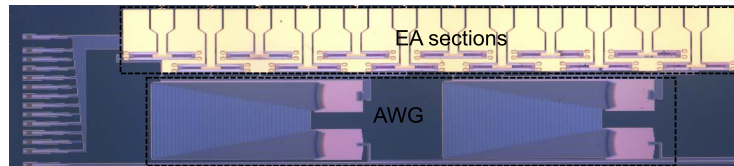| Layer	Composition	Thickness (nm)
P contact	p++-$In_{0.53}Ga_{0.47}As$	100
Cladding	p-InP	1500
SCH	$In_{0.52}Al_{0.16}Ga_{0.32}As$	150
MQW	$In_{0.47}Al_{0.2}Ga_{0.33}As$ (11×)	7
($\lambda_{PL} \sim 1.48 \mu m$)	$In_{0.59}Al_{0.08}Ga_{0.33}As$ (10×)	11
SCH	$In_{0.52}Al_{0.16}Ga_{0.32}As$	100
N contact	n-InP	150

Fig. 4. Fabricated chip where two-channel transceivers are present. The total size is 3×0.65 mm^2.

3. Performance for Off-Chip Interconnect

Fig. 5 shows the setups used for characterizing the transceiver. For the transmitter, the EA modulator sections are driven with non-return-to-zero (NRZ) pseudo random bit sequence (PRBS) codes of length 2^7-1 from a programmable pattern generator (PPG) (Anritsu, MU181020B). The peak-to-peak value (V_{pp}) of the RF driving signal applied on the device is adjusted by an RF amplifier (SHF, 807) with tunable gain and an attenuator after the PPG. A direct current (DC) bias is also applied through a bias tee. A high-speed probe (Picoprobe, 67A) is used for driving the device, which is sitting on a sample hold at a controlled temperature of 26 °C. An external tunable laser (TL) (Agilent, 81980A) is used as the light source. At the output of the bus waveguide, an Erbium-doped fiber amplifier (EDFA) is used to compensate for the losses from the chip, followed by a narrow band-pass optical filter to suppress the amplified spontaneous emission noise generated from the EDFA. The optical signal is then analyzed by a digital communication analyzer (DCA) equipped with an optical module (Agilent, 86116C). When used as a receiver, the external light is first modulated by a commercial LiNbO3 modulator (Fujitsu, FTM7938EZ), and the same light source and PPG are used as those in the off-chip transmitter measurement. The modulated light is coupled to the chip and demultiplexed to the corresponding wavelength channel. It is then detected by the reverse biased III-V EA section. An RF amplifier is also utilized to boost the photocurrent before sent to the DCA.

In [26], we have shown that, for modulation, the designed EA sections can provide a 3 dB bandwidth of 17 GHz. In this paper, we further measured the performance of such devices when used for detection. Fig. 6(a) shows the static response of one fabricated EA detector at
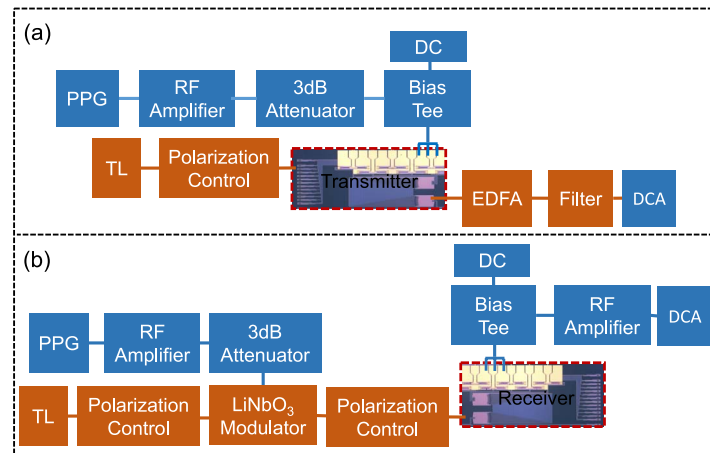
Fig. 5. Measurement setups for the off-chip (a) transmitter and (b) receiver.
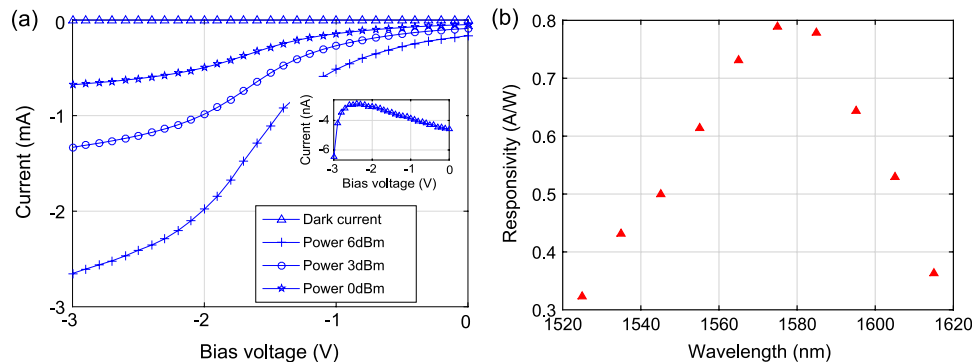

Fig. 6. (a) Static response of one EA detector section. Different curves are for different input light powers in the silicon waveguide. (Inset) Zoom-in view of the dark current. The operation wavelength is 1563.9 nm. (b) Responsivity of the EA detector section as a function of wavelength. The bias is −3 V.

the wavelength of 1563.9 nm. At 0 V bias, the absorption of the EA detector section is low. When the bias increases, the absorption also increases due to the red-shift of the bandgap wavelength of the IIIV QWs. At –3 V bias, the responsivity reaches 0.64 A/W, and the dark current is as low as 6 nA (see the inset). Fig. 6(b) shows the wavelength response of the EA detector at –3 V bias. The drop in the responsivity at the long wavelength side is related to the decrease of the material absorption beyond the QW band-gap. At shorter wavelengths, the QW is absorbing even at 0 V bias, and the input light is partially absorbed in the adiabatic taper coupler before reaching the 100-μm-long active section. Due to the bi-layer taper design adopted here, part of the coupler is unbiased [23], [26]. Thus, the generated carriers in this part cannot be swept out efficiently, which results in a decrease in the responsivity. Nevertheless, the detector response reached a peak value of 0.8 A/W and remains > 0.55 A/W in the working wavelength range of the AWGs (1550 nm–1570 nm), which is comparable to other types of detectors built on a silicon waveguide [17].

To evaluate the possibility of using a single device for both transmitter and receiver, we tested the dynamic behavior of a standalone EA section without the wavelength multiplexer. The respective eye patterns in terms of modulation and detection, taken at 30 Gb/s data rate, are shown in Fig. 7. The open eyes indicate that a duplex link can be built in the present transceiver. To show the full system performance of the present WDM transceiver, we further measured the large-signal responses of all wavelength channels in one transceiver. Eye patterns for
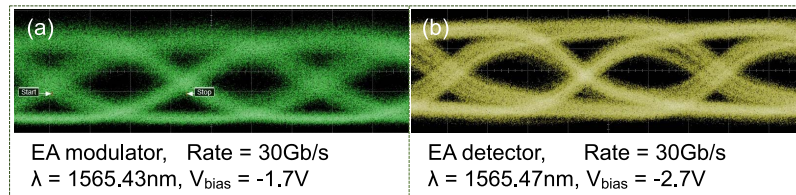
EA modulator,   Rate = 30Gb/s
λ = 1565.43nm, V_{bias} = -1.7V

EA detector,   Rate = 30Gb/s
λ = 1565.47nm, V_{bias} = -2.7V

Fig. 7. Thirty-Gb/s eye pattern for (a) modulation and (b) detection of a standalone EA device.

(a)

Channel 1
λ = 1557.58nm
V_{bias} = -2.0V
ER = 6.4dB
SNR = 4.7

Channel 2
λ = 1559.18nm
V_{bias} = -1.4V
ER = 8.1dB
SNR = 5.3

Channel 3
λ = 1560.68nm
V_{bias} = -1.6V
ER = 7.7dB
SNR = 6.1

Channel 4
λ = 1562.28nm
V_{bias} = -1.7V
ER = 10.8dB
SNR = 5.7

Channel 5
λ = 1563.84nm
V_{bias} = -1.7V
ER = 6.6dB
SNR = 5.1

Channel 6
λ = 1565.41nm
V_{bias} = -1.78V
ER = 12.7dB
SNR = 3.9

(b)

Channel 1
λ = 1557.6nm
V_{bias} = -2.8V

Channel 2
λ = 1559.1nm
V_{bias} = -3.3V

Channel 3
λ = 1560.7nm
V_{bias} = -3V

Channel 4
λ = 1562.3nm
V_{bias} = -3.3V

Channel 5
λ = 1563.9nm
V_{bias} = -3.1V

Channel 6
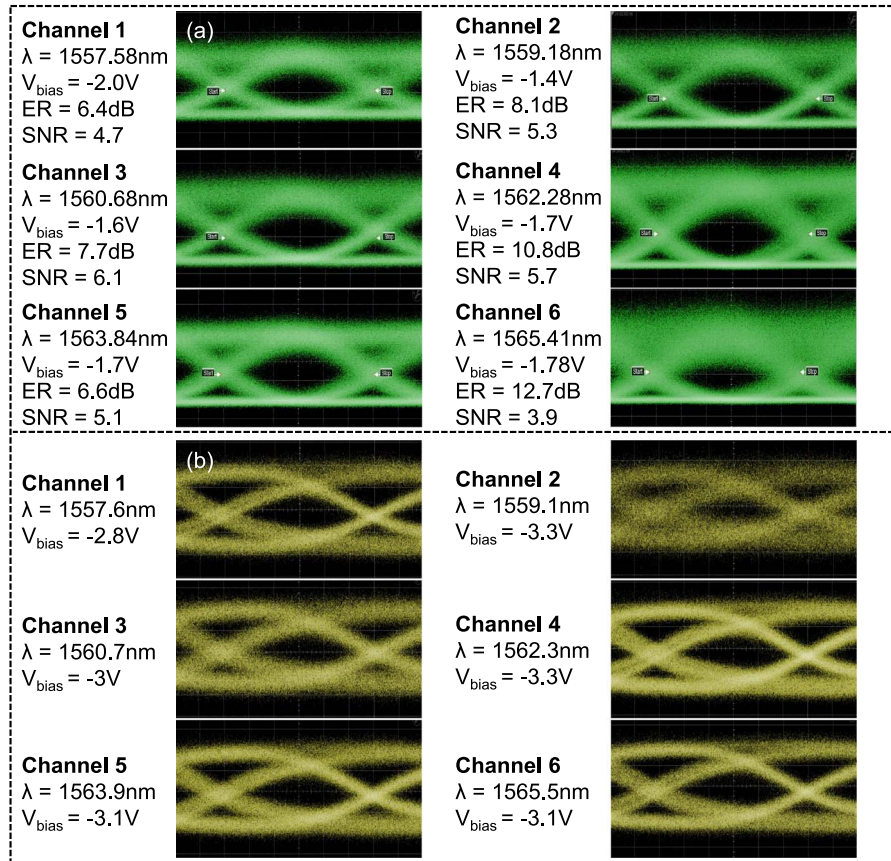λ = 1565.5nm
V_{bias} = -3.1V

Fig. 8. Measured eye diagrams at 30 Gb/s of the six different wavelength channels in the WDM transceiver for (a) transmitting and (b) receiving.

transmitting and receiving 30 Gb/s NRZ PRBS codes are shown in Fig. 8(a) and (b), respectively. Clear and open eyes can be observed for all six channels, which are ~1.6 nm spaced, although the timing jitter is somewhat large due to the poor performance of the coaxial cable connecting the device. When operating in transmitter mode, the EA sections were DC-biased at −1.4 V to −2 V, and the (V_{pp}) of the RF signals applied to them were from 0.8 V to 1.1 V. The optical power coupled in the input silicon waveguides was ~6 dBm. Under these conditions, dynamic extinction ratios (ERs) from 6.4 dB to 12.7 dB and signal-to-noise ratios (SNRs) from 3.9 to 6.1 were measured. The bit error rate for each modulator channel was measured and calculated with a real-time oscilloscope (Tektronix, DPO73304D) and is shown in Fig. 9. Due to the equipment limitation, bit error rate up to 10^{-6} and data rate up to 12.5 Gb/s is measurable. Nevertheless, no error floor is presented here. When operating as a receiver, the EA sections were biased at −2.8 V to −3.3 V, which is about twice the magnitude of the bias applied for
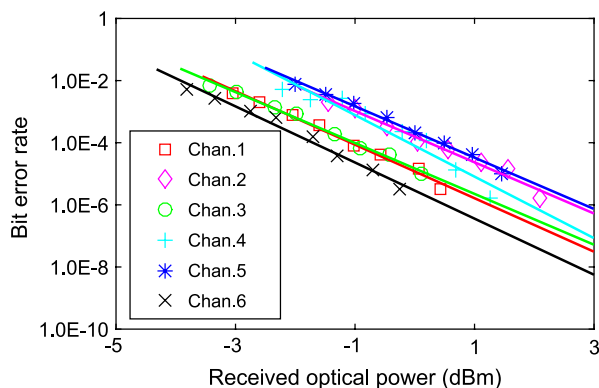
Fig. 9. Bit error rate for the transmitter at 12.5 Gb/s using the setup shown in Fig. 5(a) by replacing the DCA with a real-time oscilloscope.
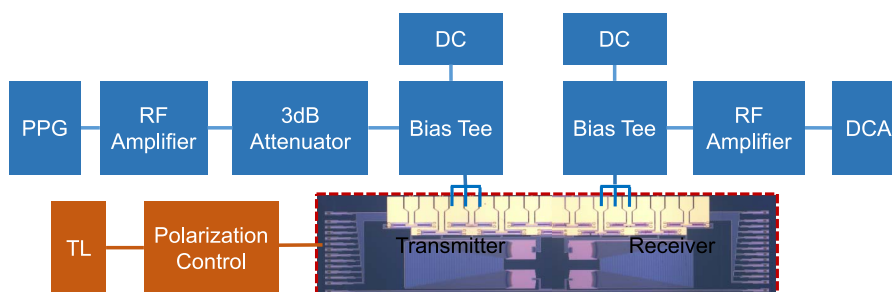

Fig. 10. Measurement setup for the on-chip interconnect characterization.

transmission discussed above, to ensure high responsivities for all channels. Therefore, a data rate of 30 Gb/s for each of the six wavelength channels can be obtained for the present transceiver when used for an off-chip duplex link. It is worthwhile mentioning that in the present chip only one EA section can be accessed and measured in the setup. When all channels are working simultaneously, a power penalty on each channel should be expected to reach the same performance. To thoroughly analyze the performance of the transceiver in this case, the electrodes and the positions of the access grating couplers have to be re-designed, which will be studied in next generation chips.

4. Performance for On-Chip Interconnect

An on-chip interconnect link is demonstrated by directly connecting the bus waveguides of two preset WDM transceivers. The characterization setup is sketched in Fig. 10. First, the static and dynamic electrical responses including crosstalks between different channels were characterized. Fig. 11(a) shows the static electrical-electrical response of a modulator-multiplexer-demultiplexer-detector link at a matching wavelength channel, as well as the behavior from the two adjacent modulator channels to the same detector (which gives crosstalks), as a function of the modulator biases (3 dBm input power in the input silicon waveguide). The detector response from the matching channel (e.g., channel 5-channel 5) varies from 19.2 μA to 85.8 μA at −3 V bias when the modulator bias is swept from 0 to −3 V. A static electrical-electrical response of 22 μA/V can be calculated for the full optical link in the presented on-chip interconnect configuration. This response can be improved, e.g., to 38 μA/V, by increasing the input optical power, e.g., to 6 dBm. Fig. 10(a) also shows that electrical crosstalks of 32.8 dB and 33.2 dB is measured for channels 4 and 6 of the transmitter to channel 5 of the receiver, respectively. The optical response of these channels measured from the corresponding grating couplers are also shown in Fig. 11(b). In this case, the EA sections at the transmitter and receiver are all biased
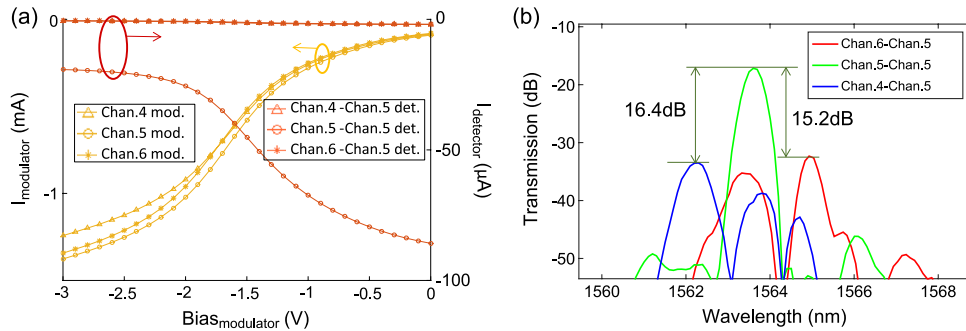
Fig. 11. (a) Static electrical-electrical response of channel 5-channel 5 (wavelength at 1563.8 nm), its two adjacent channels, i.e., channel 4-channel 5 (wavelength at 1562.3 nm) and channel 6-channel 5 (wavelength at 1565.5 nm). (b) Optical response of the three corresponding channels in the present on-chip interconnect link. Here, the EA sections at the transmitter and receiver sides are all biased at 0 V.
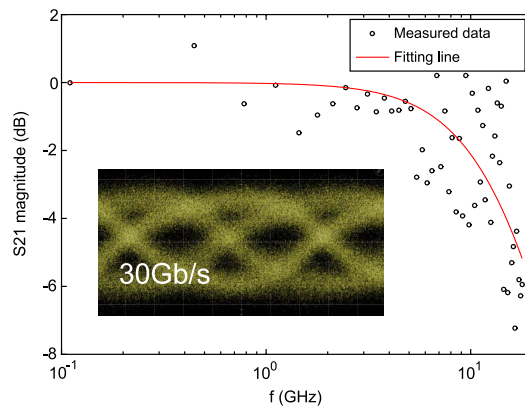

Fig. 12. Small-signal electrical-to-electrical response of the channel 5-channel 5 on-chip link (wavelength at 1563.8 nm). (Inset) Corresponding eye diagram at 30 Gb/s.

at 0 V, which minimizes the absorption of them at the measured wavelength range. Thus, the optical response mainly includes the insertion losses of two EA sections and the response of the two cascaded AWGs. The insertion loss for the matching channel is −17 dB, and the cross-talks of the adjacent channels are 15.2 dB and 16.4 dB, respectively, which corresponds to the electrical crosstalks of the corresponding channels, as shown in Fig. 11(a). It can then be con-cluded that the electrical crosstalks in the presented WDM transceiver mainly comes from the optical crosstalks from the cascaded AWGs. The performance of the AWG, as well as the central wavelength alignment, can be improved through a better quality control of the SOI pro-cess [33], [34]. The uniformity of the EA section can also be improved using a more robust dry-etching process for the III-V structures, instead of the wet etching employed currently [26].

Fig. 12 shows the small-signal electrical-to-electrical response of one modulator-multiplexer-demultiplexer-detector link with respect to channel 5 at a wavelength of 1563.8 nm measured through a vertical network analyzer (Agilent, N5247A) with −1.4 V bias on the modulator and −2.9 V bias on the detector. The influence of the measurement equipment, including the RF probes, is normalized out through a standard calibration chip. The measured result here is noisy due to the high loss of the link. Nevertheless, based on the fitting lines according to a theoretical circuit model, a 3 dB bandwidth of 13 GHz for this on-chip link can be obtained. The inset shows the eye pattern of the link driven by a 30 Gb/s NRZ PRBS code of 2^7-1 length, indicating that 30 Gb/s operation per wavelength channel is achievable for the presented on-chip WDM interconnect.

5. Conclusion

We have reported a WDM optical transceiver module for off-chip and on-chip interconnects in a single SOI chip realized through III-V/Si hybrid integration technology. A six-channel SOI AWG of 1.6 nm channel spacing has been used as the wavelength (de)multiplexer. Modulation and detection of the optical signals relies on the EA effect of III-V sections bonded on top of straight silicon waveguides. Thanks to the duplex functions of these EA sections, we can use the identical structure for modulator and detector. We have analyzed the static and dynamic response of the transceiver used in an off-chip optical interconnect. A data rate of 30 Gb/s for each of the 6 wavelength channels has been obtained for both transmitting and receiving functions. The electrical-to-electrical response and crosstalks of the transceiver used in an on-chip inter-connect link has also been studied. A 3-dB electrical bandwidth of 13 GHz has been obtained. 30 Gb/s data rate per wavelength channel has been achieved for this on-chip optical link. Benefits from the compact silicon AWG and hybrid integrated III-V modulators/detectors, the size of the present WDM transceiver can be reduced to 1.5×0.65 mm^2. By using travelling wave electrodes for the modulators and the detectors [35], the speed of the present transceiver can be further improved.

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