High Order VCO Based Delta Sigma Modulator

Amir Babaie Fishani

Promotor: prof. dr. ir. P. Rombouts
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Voorzitter: prof. dr. ir. R. Van de Walle
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Universiteit Gent
Faculteit Ingenieurswetenschappen en Architectuur
Vakgroep Elektronica en Informatiesystemen

Promoter:
Prof. dr. ir. Pieter Rombouts

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Universiteit Gent
Faculteit Ingenieurswetenschappen en Architectuur

Vakgroep Elektronica en Informatiesystemen
Technologiepark-Zwijnaarde 15 iGent, 9052 Gent, Belgie.

Tel: +32-9-264-3366
Fax: +32-9-264-3594

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Gent, December 2016
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Summary

This work aims at exploring new ways of realizing analog functions in time based blocks, instead of voltage based ones. The two functions that were of utmost importance to this work are integration and quantization. Using these two functions one can implement important analog blocks, such as analog filters and analog to digital converters.

The main incentive for time-domain signal processing is to benefit from the digital blocks that are becoming faster and more efficient in the newer CMOS technologies. Moreover, in the more advanced CMOS processes it has become more challenging to design these functions in the voltage domain. This is partly due to the fact the transistors can only deliver a smaller gain, the threshold voltage of the transistors is not dropping as rapidly as the supply voltage, and this loss of voltage headroom is causing dynamic-range loss.

This book investigates linear, low-voltage, low-area, solutions for the design of Continuous-Time Delta Sigma Modulators (CT-DSM) with high orders of quantization noise shaping. In this pursuit we have proposed the design of, and showcased the implementation of, high order VCO-Based ADC's, linear VCO's, and Asynchronous Delta Sigma Modulators (ADSM). All of the presented designs are digital friendly and make use of no traditional analog building blocks, like op-amps and highly linear transconductors. Being digital friendly means having the potential to benefit from technology scaling and being synthesizable using digital design flow.

On a system level, a new VCO-based CT-DSM structure is presented. In this system the combination of a VCO (Voltage Controlled Oscillator) and some digital blocks (referred to as up-down counter) is used as an integrator. The quantizer of the modulator is also VCO-based. Since a VCO can be implemented using an RO (Ring Oscillator), it can be very simple and digital friendly. In this manner a high order CT-DSM can be designed using only these blocks. Typical CT-DSM techniques, such as local feedback can

be incorporated in this novel structure. Many circuit level innovations and simplifications are presented to make the implementation of this modulator possible. The final circuit level solution is very simple to design and size. Therefore, it is expected to be easy to migrate from one technology node to another. The linearity of this modulator is limited by that of the first VCO on the signal path.

A thorough theoretical work is carried out in modeling an ADSM to predict its linearity performance. ADSM's are a family of PWM's (Pulse Width Modulator) that have many applications, like linearizing a VCO-based ADC. It is also proven this block can be implemented using only a Schmitt trigger and a passive loop filter, which is also simple to design and can benefit from technology scaling. Previous implementations of an ADSM or a PWM, presented in literature, required either an op-amp based or g_mC based integrator. The effect of delay in the loop of an ADSM is also studied and accurate equations to predict the linearity and oscillation frequencies of an ADSM with loop delay are extracted. As a proof of concept, a passive ADSM is implemented in 65nm CMOS technology. The design is operational under a 1 V supply and has more than 10 bit linearity over a 10 MHz bandwidth.

A circuit level solution is presented to design a voltage controlled ring oscillator with high linearity. The implemented prototype of this block was shown to be much more linear than previous works – in other works the non-linearity of the VCO is not mentioned, it is only stated that the VCO has severe non-linearity and should be compensated using different methods. This block can be used as the first VCO in a high order CT-DSM. This block determines the linearity of the overall modulator. A prototype is implemented in the 65 nm technology and the measured voltage to frequency conversion curve of the VCO for a rail-to-rail input shows a small 0.6 % deviation from an ideal line. Measurements on a pseudo-differential setup proved that the second harmonic distortion of the VCO can be heavily suppressed.

As a proof of concept, for the first time a 3rd order VCO-based CT-DSM is implemented in the low power version of a 65nm technology for a 10 MHz bandwidth. This prototype shows a measured performance of 71/66.2/62.5 dB DR/SNR/SNDR at a 10 MHz bandwidth while consuming 1.8 mW from a 1.0 V analog and 1.9 mW from a 1.2 V digital supply. With digital calibration, the nonlinearity could be pushed below the noise level, leading to an improved peak SNDR of 66 dB. The modulator covers a small

silicon area of only 0.01 mm^2.

As a second attempt to design a linear mostly digital low voltage high order VCO based CT-DSM, an ADSM is used before the first VCO to linearize it. A proof of concept is implemented in the low power version of a 65 nm technology for a 10 MHz bandwidth. This prototype shows a measured performance of 67.4/59/55.4 dB DR/SNR/SNDR at a 10 MHz bandwidth while consuming 2.3 mW from a 1.0 V analog and 2 mW from a 1.2 V digital supply. The modulator covers a silicon area of 0.018 mm^2.

List of the publications that have resulted from this work can be found here [1–7].

Samenvatting

Het doel van dit werk is het verkennen van nieuwe manieren om analoge functionaliteit te realiseren in het zogenaamde "tijdsdomein" in plaats van het gebruikelijke "spanningsdomein". Er zijn twee basisbewerkingen die de grondslag vormen van de rest van dit werk. Deze basisbewerkingen zijn enerzijds *integratie* en anderzijds *kwantisering*. Op basis van deze twee basisbewerkingen kan men belangrijke analoge bouwblokken realiseren, zoals analoge filters en analoog-naar-digitaal omzetters.

De belangrijkste stimulans om over te stappen naar "tijdsdomein"-signaalverwerking is om te proberen profijt te halen uit het feit dat de digitale blokken steeds sneller en efficiënter worden in de nieuwere CMOS-technologieën. Bovendien, in de diep-submicron CMOS-processen die vandaag bijna standaard zijn, wordt het steeds moeilijker om deze functies te realiseren in het "spanningsdomein". Dit is deels te wijten aan het feit dat de diep-submicron-transistoren slechts een lage versterking kunnen realiseren. Verder is er het probleem dat de voedingsspanning enorm veel verlaagd is, terwijl de drempelspanning van de transistoren niet evenredig mee verlaagd is. Het gevolg hiervan is dat er niet veel ruimte is om een acceptabele spanningszwaai te realiseren. Dit stelt uiteraard problemen als men een groot dynamisch bereik wil realiseren.

Deze tekst onderzoekt lineaire oplossingen voor het ontwerp van Delta Sigma Modulatoren op basis van filters die in continue tijd werken (Engels: Continuous Time Sigma Delta Modulator, afgekort CT-DSM). Hierbij is het de bedoeling dat deze circuits bij een lage voedingsspanning kunnen werken en dat ze een kleine chipoppervlakte innemen. Tijdens onze zoektocht hebben we verscheidene ontwerpsmethodes voorgesteld en die ook gedemonstreerd met praktische implementaties. In het bijzonder, hebben we Analoog-naar-Digitaal Omzetters op basis van VCO's voorgesteld die, in tegenstelling tot wat tot nu toe haalbaar was, een hoge orde van spectraal kneden realiseren. Verder hebben we een zeer lineaire VCO voorgesteld

en Asynschrone Delta Sigma Modulatoren (ASDM). Al de voorgestelde technieken en gerealiseerde ontwerpen leunen dicht aan bij digitale circuits (Engels: "digital friendly"): ze vereisen geen veeleisende traditionale analoge bouwblokken zoals operationele versterkers, of lineaire transconductantietrappen. Integendeel, alle voorgestelde circuits zouden in principe zelfs gedeeltelijk gesynthetiseerd kunnen worden met standaard digitale ontwerpssoftware.

Op systeemniveau, werd een nieuwe CT-DSM-structuur op basis van VCO's gepresenteerd. In dit systeem wordt de combinatie van een VCO en een aantal digitale blokken (die we kunnen beschouwen als een op-en-neerteller) gebruikt als een analoge integrator. Ook de kwantiseereenheid van de modulator is gebaseerd op een VCO. Aangezien een VCO kan worden uitgevoerd met behulp van een ringoscillator (RO), kan een dergelijk VCO heel eenvoudig zijn en zelfs bijna als een digitaal circuit beschouwd worden. Door meerdere van deze integratoren te combineren, kan een CT-DSM van hoge orde worden gemaakt. Typische verfijningen die in CT-DSM toegepast kunnen worden, zoals het gebruikt van lokale terugkoppeling, kunnen ook in deze nieuwe structuur worden opgenomen. Om de praktische realisatie van een prototype modulator mogelijk te maken, werden nog verscheidene innovaties en vereenvoudigingen op circuitniveau voorgesteld. De oplossing die we uiteindelijk op circuitniveau voorstellen, is zeer eenvoudig te ontwerpen en te dimensioneren. Daarom verwachten we dat dergelijke circuits gemakkelijk te migreren zullen zijn van de ene technologieknoop naar een andere. De voorgestelde structuur heeft echter één beperking: namelijk dat de lineariteit van de modulator wordt beperkt door die van de eerste VCO in het signaalpad.

In deze context, werd een grondige theoretische studie uitgevoerd om de niet-lineariteit van een ADSM te voorspellen. ADSM's zijn een familie van PWM's (Puls Breedte Modulatoren), die vele toepassingen hebben. De toepassing die ons interesseerde is het linearizeren van onze VCO-ADC. Bij onze studie, is aangetoond dat dit blok kan worden geïmplementeerd op basis van een Schmitt-trigger en verder een volledig passief lusfilter. Dit zijn weliswaar analoge circuits, maar ze zijn zo eenvoudig dat het ontwerp ervan geen enkel probleem stelt, zelfs in de geschaalde CMOS-technologie van vandaag. Eerdere implementaties van een ADSM of PWM, die in de literatuur werden beschreven, vereisten steeds een actieve integrator (met een operationele versterker of een lineaire transconductantietrap). Het effect van de vertraging in de lus van een ADSM werd ook bestudeerd en nauwkeurige

vergelijkingen om de lineariteit en de oscillatiefrequentie van een ADSM met lusvertraging te voorspellen werden voorgesteld. Als demonstrator, werd een passieve ADSM geïmplementeerd in 65 nm CMOS-technologie. Het ontwerp is operationeel bij een voedingsspanning van 1 volt en behaalt meer dan 10 bit lineariteit bij een bandbreedte van 10 MHz.

Daarnaast werd ook een oplossing op circuitniveau voorgesteld om een VCO met een hoge lineariteit te realiseren. De lineariteit van ons geïmplementeerd prototype van dit circuit bleek grootteordes beter te zijn dan de voorgaande "state-of-the-art". Dit circuit kan dan worden gebruikt als de eerste VCO in onze CT-DSM met spectrale kneding van hoge orde. We hadden al vermeld dat de eerste VCO in deze nieuwe architectuur de lineariteit van de totale modulator bepaalt. Ons prototype is geïmplementeerd in een 65 nm CMOS-technologie en de gemeten spanning naar frequentie omzettingscurve van de VCO, vertoont voor een volledige signaalzwaai van de onderste voedingslijn naar de bovenste voedingslijn slechts 0.6 % niet-lineariteit (afwijking van de ideale lijn). Daarenboven kan het circuit ook in een pseudo-differentiële opstelling gebruikt worden, waarbij de prestaties nog verder verbeterd werden doordat de tweede-orde vervorming van de VCO hierdoor sterk wordt onderdrukt.

Als proof-of-concept, hebben we de voorgestelde concepten dan gecombineerd in een CT-DSM op basis van VCO's. Dit is de eerste keer dat een circuit met 3de orde spectrale kneding van de kwantiseringsruis werd gedemonstreerd. Het ontwerp werd gedaan in de zogenaamde "low power" versie van een 65 nm-technologie. De signaalbandbreedte was 10 MHz. De gemeten prestaties van ons prototype zijn: een DR/SNR/SNDR van 71/66.2/62.5 dB bij een bandbreedte van 10 MHz en een verbruik van 1.8 mW aan de analoge voeding van 1.0 V en 1.9 mW aan de digitale voeding van 1.2V. Met digitale kalibratie kunnnen de fouten door nietlineariteit beneden het ruisniveau worden geduwd, waardoor een betere piek SNDR van 66dB behaald werd. De modulator neemt een zeer kleine chipoppervlakte in van slechts 0.01 mm^2.

Daarna hebben we een tweede poging gedaan om een lineaire bijnadigitale CT-DSM op basis van VCO's te ontwerpen. Weer werd een lage voedingsspanning en een hoge-orde van spectrale kneding van de kwantiseringsruis beoogd. Hierbij werd nu een ADSM gebruikt die voor de eerste VCO in het circuit werd geplaatst met als doel de ADC als geheel te lineariseren. Een proof-of-concept circuit van dit idee werd geïmplementeerd, opnieuw "low power" versie van een 65 nm-technologie. Hierbij werd ook

gemikt op een signaalbandbreedte van 10 MHz. De gemeten prestaties van dit prototype bij een bandbreedte van 10 MHz zijn: een DR/SNR/SNDR van 67.4/59/55.4 dB bij een verbruik van 2.3 mW aan de analoge 1.0 V voeding en 2 mW aan de digitale 1.2 V voeding. Deze modulator neemt een nog steeds een zeer kleine chipoppervlakte in van 0.018 mm^2 (zij het iets groter dan het eerste prototype).

Glossary of symbols and abbreviations

ADC	analog-to-digital converter
ADSM	asynchronous delta sigma modulator
BW	bandwidth
CT	continuous time
CT-DSM	continuous time delta sigma modulator
DAC	digital-to-analog converter
dB	decibel
dec	decade
DEM	dynamic element matching
DR	dynamic range
DSM	delta sigma modulator
DT	discrete time
DT-DSM	discrete time delta sigma modulator
DWA	data weighted averaging
FB	feedback
FF	feedforward
FS	full scale
gm	trans-conducting amplifier
LSB	least significant bit
MSB	most significant bit
NRZ	non-return-to-zero
NTF	noise transfer function
OSR	oversampling ratio
PWM	pulse width modulator
Q	quantization noise
PM	phase margin

RO	ring oscillator
RZ	return-to-zero
SCR	switched-capacitor-resistor
SDR	signal-to-distortion ratio
SNDR	signal-to-noise-and-distortion ratio
SNR	signal-to-noise ratio
SQNR	signal-to-quantization-noise ratio
STF	signal transfer function
THD	total harmonic distortion
VCO	voltage controlled oscillator
ZOH	zero-order hold

Chapter 1

Introduction

Traditionally, high-performance Analog-to-Digital converters (ADCs) have heavily relied on conventional analog building blocks such as operational amplifiers, transconductors and comparators [8–14].

Unfortunately, in today's ultra deep sub-micron CMOS technologies these building blocks become increasingly difficult to design because of limited voltage headroom due to the low supply voltage combined with reduced raw 'analog' performance of the elementary transistors (e.g. gain, matching, 1/f noise) [15]. Moreover these analog circuits have poor portability to other technology nodes and efficient testing is a specialty in itself [16].

For this reason, researchers have attempted to find more 'digital' solutions for these traditionally analog blocks. A promising approach here, are the VCO-based ADCs [17–26]. If the VCO-core is a ring-oscillator, this corresponds to a 'nearly digital' implementation. A Ring Oscillator consists a loop of inverters or buffers, with an input dependent propagation delay, which are easy to design in every given technology.

Such a VCO-ADC was shown to exhibit first-order quantization noise shaping and to have very similar behavior as a first-order $\Sigma\Delta$ modulator [20]. However, in the vast majority of the VCO-ADC designs that have been published, the VCO is still combined with sophisticated analog building blocks (i.e. opamps, transconductors, ...), e.g. [17–19]. The reason for this is to solve the two fundamental problems of VCO-ADC's. First, VCO-ADC's have poor linearity, and second, they have only first order noise shaping. In this book it is attempted to solve both deficiencies while avoiding sophisticated analog building blocks. A low supply voltage and low silicon area consumption have been the main targets through out this

exploration.

VCO-ADCs suffer from nonlinearity problems because the linearity of the voltage to frequency conversion of most VCOs is very poor. This problem can be tackled by combining the VCO-ADC with established analog techniques such as feedback. However, there are also digital-friendly solutions such as digital (self)-calibration [23–28]. And of course, the most simple solution would be to start from a VCO-ADC that has sufficient linearity, which is explored in this dissertation, where a very simple circuit for a linear ring-oscillator based VCO is proposed.

Another potential solution to solve the linearity issue is to convert the input voltage into a two-level signal where the information is stored in the duty cycle of the resulting square-wave using an Asynchronous Delta Sigma Modulator (ADSM) or a Pulse Width Modulator (PWM). This method is known as 'PWM pre-coding' [29–31]. Until now all reported implementations either required an op-amp, a highly linear ramp source, or a linear gm cell [30–32] ('gm' stands for a trans-conducting amplifier). In practice such high-performance analog circuits are difficult to implement at today's low supply voltages (of the order of 1 Volt) and hence are to be avoided. An alternative would be an ADSM with a passive RC loop filter [2, 3, 29]. However, it is not obvious how such a passive ADSM should be designed as to achieve simultaneously high bandwidth and good linearity. For this reason, until now, such a circuit has not yet been demonstrated in practice. In this work, we explain how such a passive ADSM linearization of a VCO can be designed to achieve good overall performance. The validity of the presented theory is confirmed by measurements on an implemented prototype.

As mentioned earlier, the second reason why most VCO-ADCs are combined with analog techniques is that, to the authors' knowledge, all publications of 'implemented' mostly digital VCO-ADC prototypes only exhibit first-order quantization noise shaping [23–28]. In some implementations a VCO-ADC is used as a noise shaping quantizer, to operate as the last integrator in the chain of integrators in a Continuous-Time Delta Sigma Modulator (CT-DSM). In this manner, the preceding integrators would be implemented in the traditional analog manner, using op-amp or gm-C based structures. So, in these approaches the challenge of designing traditional analog blocks would still remain.

This manuscript also contributes on this border and presents the design of – and measurements on – a linear 'mostly digital' VCO-ADC with 3rd

order quantization noise shaping. The idea of a high order VCO-ADC is first introduced on a system level, then a circuit level solution is proposed that can achieve high orders of quantization noise shaping using only VCO-based integrators and other digital blocks.

1.1 Dissertation organization

This dissertation is organized as follows:

Chapter 2 will examine some of the previous works in the field of VCO based ADC design. The key target is to implement a CT-DSM using VCO based integrators and avoid using traditional op-amp based loop filters as much as possible. System level solutions to improve the linearity and increase the order of quantization noise shaping will be discussed.

Chapter 3 introduces the system level concepts that are at the basis of our high-order noise shaping VCO-ADC. In this chapter it is shown that the combination of a VCO and a digital block called "up-down counter" can be used as an integrator in the loop of a CT-DSM and can eventually lead to a high order CT-DSM with only VCO-based integrators. In the following chapters we will propose circuit level implementations for this modulator.

The linearity of a VCO-based CT-DSM is limited by that of its first VCO. In chapter 4 a linear voltage controlled ring oscillator structure is proposed. This circuit level solution is further verified through measurement results. Later on in chapter 6 this circuit will be used as the first VCO of a high order all-VCO CT-DSM.

In Chapter 5 PWM pre-coding technique for linearizing the first VCO is examined. An ADSM structure is chosen to create PWM pulse signals. A full study is done on the behavioral model of an ADSM to predict its linearity and carrier frequency. The effect of loop delay is also analyzed separately. Eventually, a circuit level implementation of an ADSM is proposed. The effectiveness of the proposed circuit in linearizing a VCO is then verified by examining the measurement results of a ADSM-VCO combination.

Chapter 6 showcases the first prototype of a 3rd order modulator of this type (VCO-based CT-DSM). This chip uses the linear VCO introduced in chapter 4. Many circuit level innovations are introduced to make this design possible. The resulting ADC is measured to have a competitive noise and linearity performance, while being operational under a low supply voltage.

The core of the chip occupies many times less silicon area than its conventional CT-DSM counterparts. The measurement results are compared with some of the more relevant prior works.

In chapter 7 a second implementation of a 3rd order VCO-based CT-DSM is presented. In order to have a linear ADC, this design uses the ADSM-VCO combination introduced in chapter 5. The resulting modulator is then compared to the design proposed in chapter 6. It is, afterwards, discussed why the chip with ADSM linearization technique is inferior to the chip in chapter 6 in almost every aspect.

Chapter 8 concludes the dissertation and discusses future directions for this research.

Chapter 2

Previous work on VCO-ADC

In this chapter first we will provide some basic background knowledge about Nyquist Rate and Over-Sampling Analog to Digital Converters. Then we will give the motivations for designing Discrete Time or Continuous Time Delta Sigma Modulators (CT-DSM). Afterwards we will examine some of the previous works in the field of VCO based ADC design.

The key target is to implement a CT-DSM using VCO based integrators and avoid using traditional op-amp based loop filters as much as possible. System level solutions to improve the linearity and increase the order of quantization noise shaping will be discussed. Continuous-Time integrators and a quantizer are the main ingredients for developing such a modulator. The idea is to replace these with their VCO based equivalents.

2.1 Basics of Analog to Digital Conversion

An analog to digital converter, which is fundamentally a mixed-signal block, converts a continuous-time (CT) analog voltage to a discrete-time discrete-amplitude digital stream, or in other words "digitizes" it. So this digitization is applied to the both aspects of the input signal, its amplitude and its time. Digitization in the time domain is commonly known as sampling, and digitization in the voltage domain is known as quantizing.

The performance of such a conversion is limited by its sampling speed and quantization accuracy. Sampling puts a limit on the signal bandwidth and quantization adds noise. In this section we will discuss the two major ADC families. In the first group the quantization noise has a white (flat) spectrum, like Nyquist-rate ADCs, and in the second family the quanti-

zation noise is "shaped" such that its effect is minimized in the frequency range that is of our interest, like Delta Sigma Modulators.

2.1.1 Nyquist rate ADC

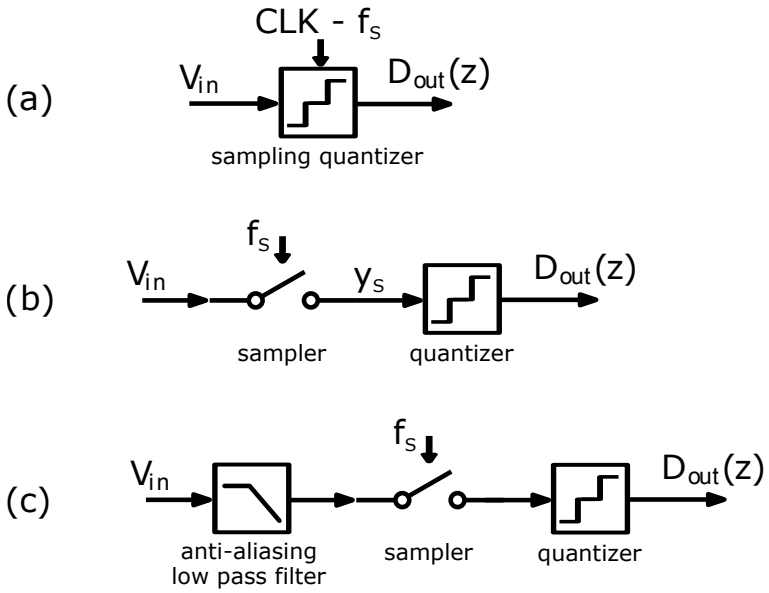


Figure 2.1: (a) A sampling quantizer as a Nyquist rate ADC,
(b) separating the sampling and quantizing functions, and
(c) adding anti-aliasing low pass filter.

A sampling quantizer, shown in Fig. 2.1(a), is the simplest implementation of an ADC. Here V_{in} is the continuous-time (CT) input voltage, CLK represent the clock signal with a frequency of f_s, and D_{out} is the digital output stream, which is both discrete-time (DT) and quantized in value.

The two functions of sampling and quantizing can be performed separately while one functionality follows the other. In this manner the system shown in Fig. 2.1(b) is strictly equivalent to the one in Fig. 2.1(a). The input voltage is sampled at the constant rate of f_s, resulting in the DT signal of Y_S. If the input bandwidth is limited and the sampling rate is high enough there will be no loss of information. The maximum bandwidth that the input signal can have to ensure a lossless transformation is $f_s/2$. In other words, the sampling frequency should be at least twice the input

bandwidth, $f_s = 2 * f_B$. This is commonly known as the Nyquist rate.

With a good approximation, the quantizer can be modeled as a linear gain, G, with an additive white noise with a variance of $G^2\sigma^2/12$, where σ is the quantization step in the input. In this manner, the Dynamic Range (DR) of the ADC can be calculated.

DR is defined as the ratio of the full-scale input power to the input power at which the signal-to-noise ratio (SNR) is one. SNR is defined as the ratio of the signal power to the noise power at the output. If the ADC doesn't introduce any distortion for larger signals the DR would normally be equal to the SNR for the full-scale input. For this ADC for an input sine wave $A_x \sin(\omega_{in} t)$ we have:

$$\frac{\text{signal power}}{\text{noise power}} = \frac{G^2 A_x^2/2}{G^2\sigma^2/12} \tag{2.1}$$

The accuracy of a quantizer is often reported in its number of bits, $nbit$, instead of its step size, σ. They can be interchanged like this:

$$\sigma = \frac{2 * A_x\{max\}}{2^{nbit} - 1} \tag{2.2}$$

So the dynamic range of this ADC will be:

$$DR = \frac{3}{2}(2^{nbit} - 1)^2 \tag{2.3}$$

The SNR that only includes the quantization noise is often referred to as signal-to-quantization-noise ratio (SQNR). These values are normally reported in dB scale. For this ADC we can have:

$$DR = SQNR_{max}[\text{dB}] = 6.02nbit + 1.76 \tag{2.4}$$

2.1.2 Over-sampling ADC

One of the known problems associated with sampling a CT signal (and converting it to a DT signal) is aliasing. For example, if an out of band blocker with an arbitrary frequency of $f_s + f_x$ is present in the signal V_{in} in Fig. 2.1(b), after sampling the aliasing effect will move this unwanted signal to the frequency of $f_s - f_x$. This aliased blocker could therefore fall into the band of interest and degrade the performance of the ADC. To avoid this an anti-aliasing low pass filter should precede the sampler, as shown in Fig. 2.1(c). Since we want to maximally benefit from the bandwidth

that the sampling quantizer (or the Nyquist rate ADC) can provide, the anti-aliasing filter should have a very sharp slope, which can be a serious design challenge.

This problem can be overcome by increasing the sampling frequency of the sampling quantizer to relax the design specifications on the slope of the anti-aliasing filter. Besides, since the quantization noise has a white spectrum a smaller portion of it will fall into the desired bandwidth. In other words, by increasing the sampling ratio by a factor two the quantization noise power in the baseband would be decreased by the same factor and the SNR will improve by the same factor, or 3 dB. The ratio of the new clock frequency over the Nyquist rate, $2 * fB$, is known as the Over Sampling Ratio, $OSR = f_s/(2 * f_B)$. So, the DR for an over-sampling ADC will be obtained as:

$$DR = SQNR_{max}[\text{dB}] = 6.02nbit + 1.76 + 10\log_{10} OSR \tag{2.5}$$

2.1.3 Discrete Time Delta Sigma Modulator

As mentioned earlier, the quantization noise doesn't come from the sampling function of the ADC but from its quantization function. So, in order to further benefit from the quantization noise reduction of over-sampling ADC one could pass the quantization noise through a high pass filter (a differentiator). This is known as quantization noise shaping. A common method for this is Delta Sigma modulation, shown in Fig. 2.2(a).

Here the loop filter is a discrete-time low pass filter, typically implemented using opamps and switch-cap structure. Let's assume a simple case where the loop filter is a first order integrator, $H(z) = \frac{z^{-1}}{1-z^{-1}}$. The quantizer can be modeled as a linear gain, G, and an additive quantization noise, $Q(z)$. For simplicity let's assume a gain of 1 both for the quantizer and the DAC. In this way the output, $D_{out}(z)$ is a function of two inputs, $V(z)$ which is the sampled version of the input, and $Q(z)$. Using superposition we can write:

$$D_{out}(z) = STF(z).V(z) + NTF(z).Q(z) \tag{2.6}$$

STF (signal transfer function) is the TF from the input to the output of the modulator and NTF (noise transfer function) is the TF from added quantization noise to the output. For the system shown in Fig. 2.2(a), assuming $H(z)$ is a first order integrator, we can simply calculate:

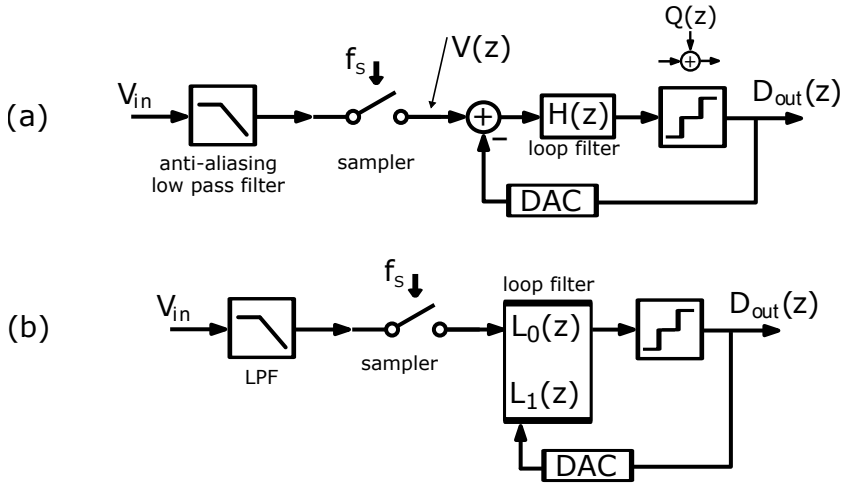


Figure 2.2: (a) System level structure of a typical DT-DSM, without additional feed-forward or local feedback paths, and
(b) a DT-DSM with a more general loop filter.

$$STF(z) = \frac{D_{out}(z)}{V(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \tag{2.7}$$

This means that the input signal appears unchanged at the output with a delay of one clock cycle. As for the NTF we have:

$$NTF(z) = \frac{D_{out}(z)}{Q(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \tag{2.8}$$

This shows that the quantization noise is shaped by a first order high pass transfer function. The DR of this system is:

$$DR = SQNR_{max}[\text{dB}] = 6.02nbit + 1.76 + 30\log_{10} OSR - 10\log_{10}\frac{\pi^2}{3} \tag{2.9}$$

Compared with eq. 2.5, we can see that here increasing the OSR can improve the DR three times faster.

A general structure of DT-DSM is shown in Fig. 2.2(b). Once again the output can be written as a linear function of its two inputs, like eq. 2.6. For this case we can calculate:

$$STF(z) = \frac{D_{out}(z)}{V(z)} = \frac{L_0(z)}{1 - L_1(z)} \tag{2.10}$$

and,

$$NTF(z) = \frac{D_{out}(z)}{Q(z)} = \frac{1}{1 - L_1(z)} \tag{2.11}$$

By properly designing $L_0(z)$ and $L_1(z)$ a higher order NTF can be realized while keeping STF just a few delays. A simple example of a high pass NTF of L order is:

$$NTF(z) = (1 - z^{-1})^L \tag{2.12}$$

For this case the DR will be:

$$DR = 6.02nbit + 1.76 + 10(2L + 1)\log_{10} OSR - 10\log_{10}\frac{\pi^{2L}}{2L + 1} \tag{2.13}$$

Thus, the DR improves with a rate of $2L+1$ as the OSR increases, which is a great improvement over simple oversampling. As a result, the number bits required to achieve a given DR is considerably less in a DT-DSM than in a Nyquist rate ADC.

2.1.4 Continuous Time Delta Sigma Modulator

$\Delta\Sigma$ ADCs, or DSMs, are divided into two different categories based on the location of the sampler. In a discrete-time DSM (DT-DSM), as shown in Fig. 2.2, the sampler is located at the input stage and switched cap filters are normally used to precess the discrete time signals. In a continuous time DSM (CT-DSM), as shown in Fig. 2.3, the sampling function happens just before the quantization, and the two functions can be merged to a single block.

The quantization noise shaping characteristic of a CT-DSM is very similar to that of a DT-DSM and its order is equal to the number of integrators in its loop filter. Fig. 2.3(b) shows a typical structure of a CT-DSM with an order of k without additional feed-forward or local feedback paths, [33].

It has been argued in the literature that a CT-DSM can operate at a higher clock frequency compared to a DT-DSM, because the latter is limited by the speed of the switches and charging time of the capacitors.

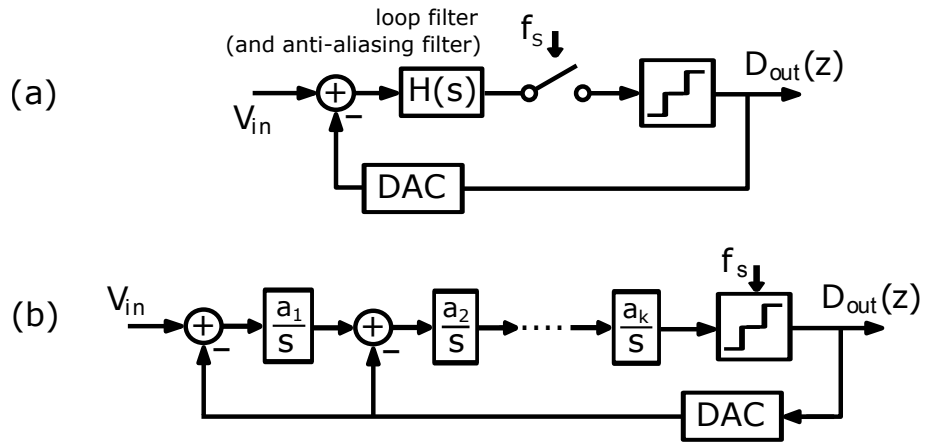


Figure 2.3: (a) System level structure of a typical CT-DSM, without additional feed-forward or local feedback paths, and
(b) a CT-DSM of the kth order.

More importantly, in a CT-DSM the sampler is located after the loop filter. As a result, this filter also operates as an anti-aliasing filter, which can save some power and chip area.

2.2 First order VCO-ADC

The combination of a VCO and a reset counter, shown in Fig. 2.4(a) is often used as either a stand-alone ADC with first order quantization noise shaping or as a noise shaping quantizer in the loop of a high order CT-DSM [20, 24, 25, 29, 30, 34–40].

The VCO converts the input voltage, V_{in}, to a square wave of which the frequency is proportional to the input voltage. Then the reset counter counts the number of rising edges of the square wave in every clock cycle. This way, it quantizes the phase which is the integral of the frequency. The reset function compensates this integration with an inherent differentiation. Apart from the quantization error, the resulting digital output signal D_{out} will be equal to:

$$D_{out} \approx \frac{f_{vco}}{f_s} = \frac{f_c + k_v V_{in}}{f_s} \tag{2.14}$$

where f_{VCO} stands for the VCO output frequency, f_c for the free run-

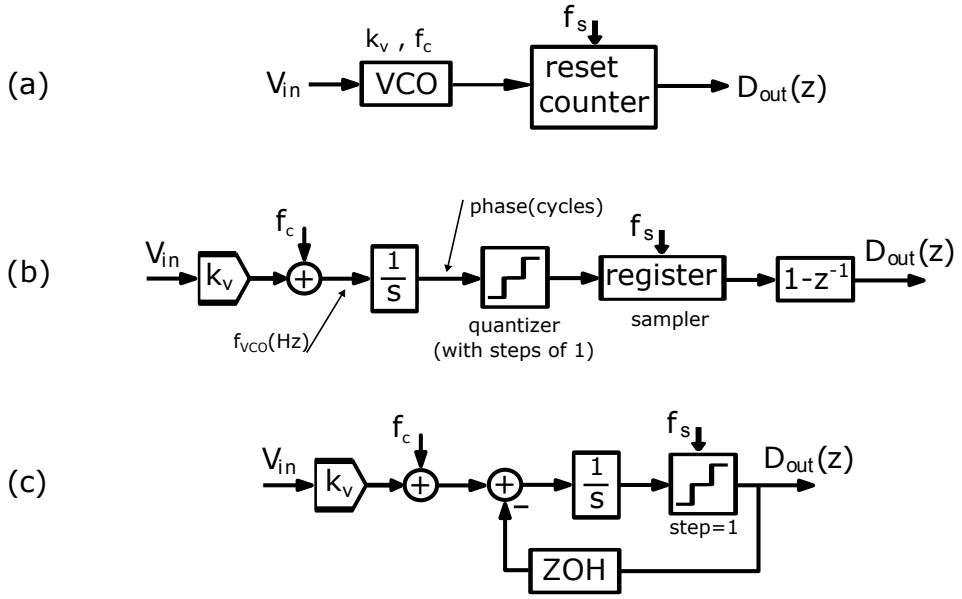


Figure 2.4: (a) an open-loop first order VCO based ADC, and (b) and (c) its equivalent model.

ning (zero input) frequency of the VCO, k_v for the gain of the VCO and f_s for the sampling frequency.

In a previous work [20] a thorough study of first order VCO-based ADC's has been done and different parameters of the modulator, such as SQNR or DR have been obtained as functions of the VCO and sampler parameters, such as the VCO's gain (k_v), OSR, input amplitude (A_x) number of phases (n_p), and sampling frequency (f_s).

$$SQNR = 6.02nq - 3.41 + 30\log_{10} OSR + 20\log_{10}(\mathrm{sinc}(\frac{1}{2OSR})) \quad (2.15)$$

where $nbit = \log_2(2A_x k_v n_p/f_s)$ is the resolution of the quantizer.

As expected, the SQNR of a VCO ADC is similar to that of first order DSM in terms of quantization noise shaping and dependency on OSR (referring to the term $30\log_{10} OSR$ in the equation above.)

An equivalent system is depicted in Fig. 2.4(b), [29]. In this model the quantization, sampling, and differentiation functions (which previously happened simultaneously in the reset counter) are separated. The conversion from frequency to phase domain is modeled as an integrator. The

quantizer represents the fact that we don't have full access to the output phase of the VCO, but only to its cycles. In other words, only a full cycle can be counted. After sampling, the output is differentiated in the digital domain.

Although this VCO-ADC is an open loop structure, in Chapter 3 it will be shown that it is strictly equivalent to a first order closed loop CT-DSM, similar to the one shown in Fig. 2.4.

What makes a VCO based integrator interesting is the fact that the output phase of the VCO is by definition the integrated frequency, and in that regard a VCO is an ideal integrator with an infinite gain at DC, a luxury that is impossible to obtain in a conventional op-amp based integrator.

2.2.1 Circuit level considerations

One of the main ideas behind a VCO-ADC, shown in Fig. 2.4, is to have a simple design that can ideally be synthesizable using digital flow design tools. Such a circuit would be relatively easy to migrate from one technology node to another. For this reason, it is of interest to look for circuit level solutions that are as "digital" as possible.

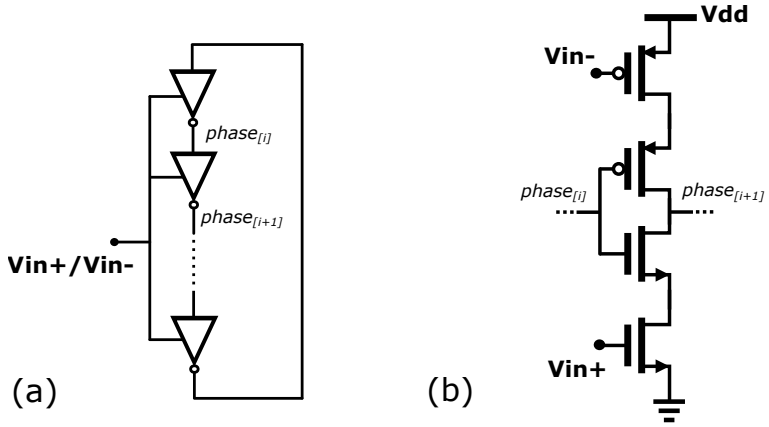


Figure 2.5: (a) a typical structure for a voltage controlled Ring Oscillator (b) a voltage controlled inverting delay stage, used in an RO.

Given this motivation, a Ring Oscillator (RO) is often used to manifest the VCO. An example of a typical RO is shown Fig. 2.5(a). An RO is an unstable loop of inverters, or delay stages. Such delay elements can be designed with a minimal number of transistors, which makes them a

suitable option for low voltage applications. Another benefit of an RO is the fact that it has multiple output phases that can be processed in parallel using digital blocks.

It is commonly known that RO's have a relatively linear current to frequency conversion curve, so the main challenge would be to develop a linear transconductance stage to convert the input voltage into current to drive the RO. Many implementations for such a block already exists, a simple solution for this is shown in Fig. 2.5(b) as an example [18]. As the figure shows, the input voltage $Vin+$, and its complementary counterpart $Vin-$ drive two trans-conducting transistors. This complementary structure, that uses a trans-conducting NMOS and PMOS at the same time, is chosen to minimize the even order harmonics that exists in the non-linear voltage to current conversion curve of a CMOS transistor.

In the VCO-ADC shown in Fig. 2.4(a) the RO is then followed by a reset counter, and since the different phases of the RO can be processed in parallel, each phase will be driving a separate, and rather simple, reset counter. The outputs of these counters will then be added in a digital adder that follows them.

Fig. 2.6(a) shows a typical implementation for a single-phase reset counter [18], where $VCO[i]$ is one of the output phases of the voltage controlled RO, and f_s is the sampling clock frequency. This particular circuit is triggered by both rising and falling edges of the VCO. The timing diagram of this reset counter is shown in Fig. 2.6(b).

An important parameter that the designer should take into account is the fact that the output phases of the RO are not rail-to-rail signals. Therefore, a level shifter can be used for the conversion. In some implementations, the first DFF in Fig. 2.6(a) is replaced with a SAFF (sense-amplifier-based flip-flop) to overcome this problem.

2.3 PWM pre-coding

One of the main issues of the system shown in Fig. 2.4(a) is the fact that the linearity of the overall ADC is limited by that of the VCO, which typically has a poor linearity performance in its voltage to frequency curve.

One of the system level solutions to overcome this issue is to put a Pulse-Width Modulator (PWM) before the VCO on the signal path, Fig. 2.7(a). The PWM will convert the input voltage to a two level signal, v_1 and v_2 , which will eventually drive the VCO, corresponding to only two instan-

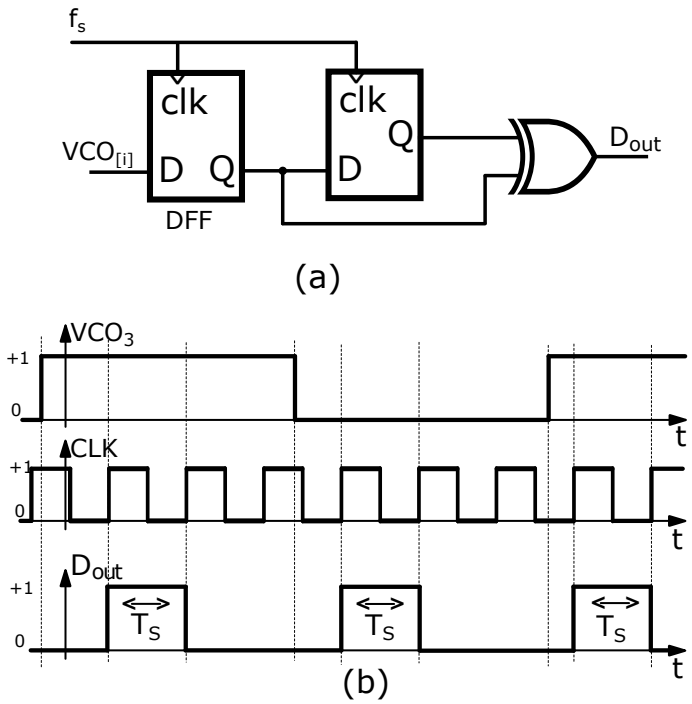


Figure 2.6: (a) a common implementation for a single phase reset-counter, (b) its timing diagram

taneous frequency values, Fig. 2.7(b). In this manner the non-linearity curve of the VCO wouldn't matter anymore, because that dotted line, connecting the two operating points, would be the new voltage to frequency curve, which is always inherently linear. This technique is known as PWM pre-coding [29–31, 41, 42].

The PWM has a gain of one for the baseband signal and is used in series on the signal path, that's why it will always directly contribute to the noise and power budget of the system.

The designer should also take the aliasing effects of the PWM into account. A PWM signal has high frequency spurs around its carrier, and its harmonics, that can alias into baseband. It is normally expected that the anti-aliasing characteristics of a CT-DSM can alleviate this problem, but it is possible that a first order VCO-ADC, which is equivalent with a first order CT-DSM, cannot suppress these spurious tones (spurs) enough for a given SNR requirement.

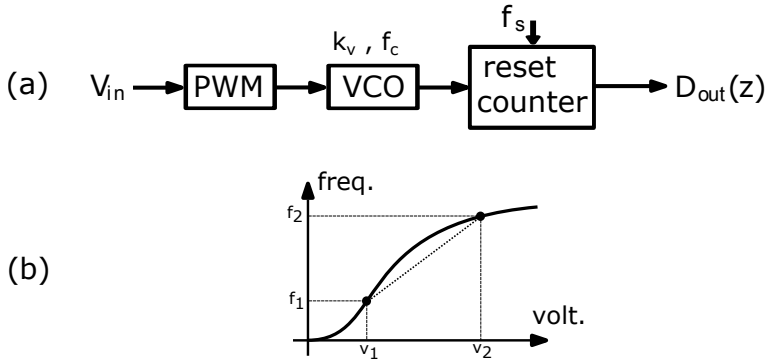


Figure 2.7: (a) the system level representation of the PWM pre-coding technique for VCO-ADC linearization.
(b) the effect of PWM pre-coding technique on the non-linearity curve of a VCO.

Also worth noticing is the fact that the VCO is, in this configuration, basically operating as mixer. The average frequency of the VCO and high frequency spurs of the PWM can mix, inter-modulate, and eventually get down converted into baseband. These effects will further be discussed in Chapters 5 and 7.

2.4 Coarse-fine structure

Another method to improve the linearity of a VCO-ADC is to reduce its input swing. By simply reducing the input voltage swing, applied directly to the VCO in Fig. 2.4(a), one can improve the linearity of the overall ADC. But it is obvious that this will be at the cost of SNR (Signal to Noise Ration) and DR (Dynamic Range) loss.

Coarse-fine structure, shown in Fig. 2.8, is a system level solution to reduce the swing of the VCO in a VCO-ADC. In this modulator the input voltage is first applied to a high speed coarse ADC with low accuracy, typically a flash ADC, annotated as ADC_f on the figure. The output of ADC_f is then subtracted from the input using a DAC (Digital to Analog Converter). The resulting quantization error signal is much smaller than V_{in} and as a result the non-linearity of the VCO would be much less significant.

The output of ADC_f will then be added as MSB (Most Significant Bits) to the digital output of the reset counter, representing the LSB (Least

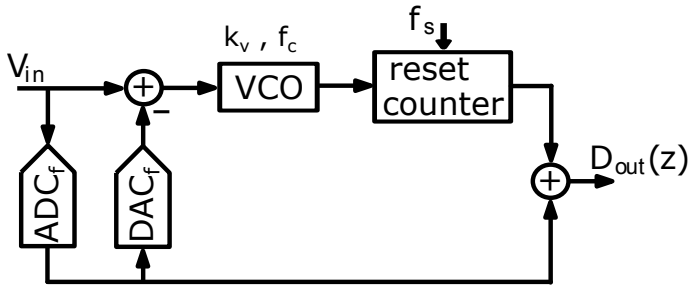


Figure 2.8: System level representation of a Coarse-fine VCO-ADC structure, also know as 0-1 MASH VCO-ADC or residue canceling VCO-ADC.

Significant Bits). The overall ADC has no loss of DR due to swing reduction and will have a first order quantization noise shaping.

One of the drawbacks of this structure is the fact that it heavily depends on the DAC gain accuracy. Any mismatch between the DAC and the feed-forward path will increase the swing on the VCO and will degrade the linearity performance of the ADC. One way to improve this problem is to use this ADC as a noise shaping quantizer in a closed-loop high-order CT-DSM. This way the remaining non-linearity of this ADC will be suppressed by the preceding integrators in the loop of the CT-DSM.

Another downside of this scheme is the fact that the power consumption of the overall ADC would typically be doubled, compared to a conventional VCO-ADC with similar DR (Dynamic Range).

Also worth mentioning is the lack of anti-aliasing filtering which inherently exists in a conventional VCO-ADC. In a coarse-fine structure the flash ADC would require an analog low-pass filtering before it to avoid aliasing problems.

This technique is often referred to in the literature as '0-1 MASH VCO-ADC' or residue canceling VCO-ADC, [22, 43–45].

2.5 Voltage-to-phase VCO-based ADC

As explained in the previous section, a VCO is a perfect frequency to phase integrator. In order to extract the phase information of the VCO, one could sample the phase, as it was the case in Fig. 2.4(a). In that approach the integration function of the VCO was compensated by differentiation in digital domain using a reset-counter. That method is often referred to as

'voltage-to-frequency VCO-based ADC' [46–48].

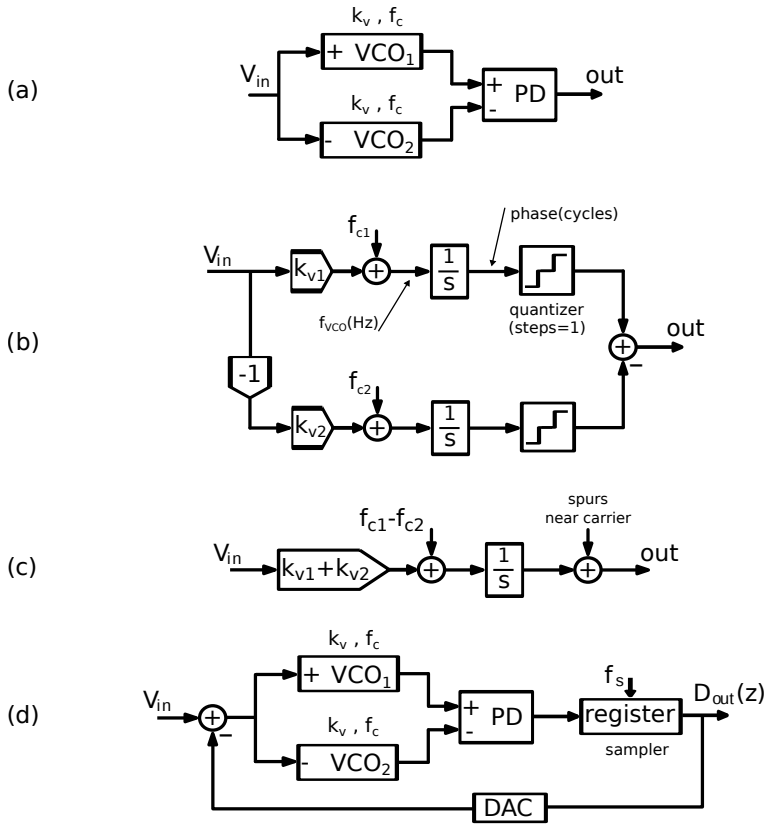


Figure 2.9: (a) a voltage-to-phase VCO based integrator,
(b),(c) its system level equivalents,
(d) a first order voltage-to-phase VCO based ADC.

Another method for extracting the phase information of a VCO is using the VCO-based integrator shown in Fig. 2.9(a). In this pseudo differential method, the input signal is applied to two complementary VCO's and the difference between their output phases is detected using a Phase Detector (PD). The output of the PD, which is a pseudo digital Continuous-Time signal, is the integrated version of the input, plus some high frequency spurs around the carrier of the VCO, f_c. As a result, this structure can be used as a CT integrator in any loop filter, including CT-DSM applications.

A system level model of this integrator is shown in Fig. 2.9(b). Two different values are assumed for the gain and carrier frequency of the two

VCO's in order to address the potential issue of mismatch. the quantization function represents the fact that the PD only responds to the rising edges of the VCO output, or in other words, the phase information of the VCO is only available at the end of a full cycle.

As Fig. 2.9(c) shows, the mismatch between the gain of the two VCO's is not important and the overall gain of the integrator equals their summation. The mismatch between the carrier frequency of the two VCO's, on the other hand, translates as a DC offset to the input and will also appear as a DC offset at the output after putting the integrator in a closed loop. The high frequency spurs due to the quantization in the PD is also modeled in this figure.

Using this integrator one can develop a first order voltage-to-phase VCO-based ADC, shown in Fig. 2.9(d). Bear in mind that the spurs modeled in Fig. 2.9(c) will not affect this first order CT-DSM, because in any DSM there is always a quantization function that completes the loop, and in this case the PD is performing the quantization function. As a result, the sampling quantizer that normally appears in a CT-DSM will reduce to a simple sampler, or register.

Similar to the previously discussed VCO-based integrator, it is also common to use ring oscillators to implement these VCO's, in which case, each output phase of $VCO1$ will be coupled to a corresponding output phase of $VCO2$, [49, 50].

In some implementations, instead of using two VCO's, the designers have chosen to have only one VCO, and compare its output phase with a reference frequency source. This reference source can even be the readily available clock of the system, or a fraction of it.

2.6 High order VCO-based ADC's

The VCO based ADC's discussed so far behave as a first order CT-DSM. In this section different methods to increase their order of quantization noise shaping is examined.

2.6.1 Using conventional loop-filter

It is well known that a low order CT-DSM can be used as the last stage of a high order CT-DSM to behave as a noise shaping quantizer. The same method has been used to incorporate a first order VCO-ADC into the loop

of a high order CT-DSM. In other words, the VCO-ADC will be preceded by a conventional Continuous-Time loop-filter such that together they can be modeled as the system in Fig. 2.3.

The VCO-ADC's that have been discussed so far only have a first order quantization noise shaping. In other words, once incorporated into the loop of the CT-DSM in Fig. 2.3, they will replace the last integrator and the sampling quantizer [17, 18, 46, 47, 51, 52].

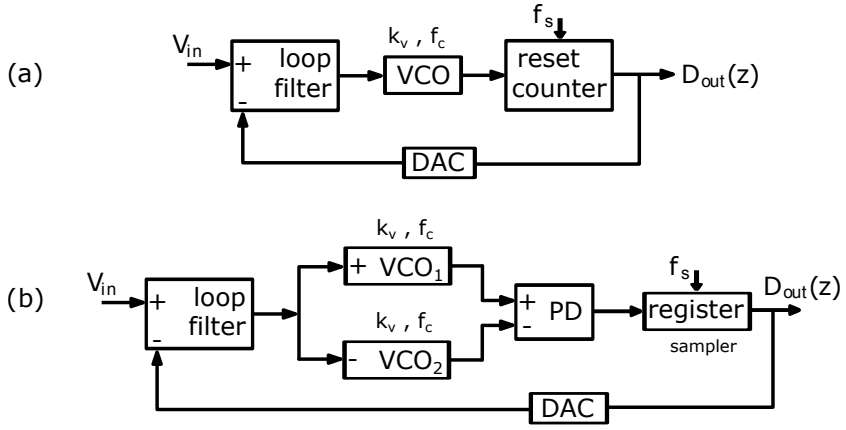


Figure 2.10: (a) using a voltage-to-frequency VCO-ADC as a noise shaping quantizer in the loop of a CT-DSM,
(b) using a voltage-to-phase VCO-ADC as a noise shaping quantizer in the loop of a CT-DSM.

Fig. 2.10(a), for example, shows the case where a 'voltage-to-frequency VCO ADC' is used to replace the last integrator and the quantizer of a high order CT-DSM [53]. As a second example, Fig. 2.10(b) shows a similar concept for a 'voltage-to-phase VCO ADC'.

Designing a proper quantizer for CT-DSM applications has become more challenging as channel length in the newer CMOS technologies shrinks. Unlike Nyquist rate ADC's, the quantizer of a CT-DSM should operate at a much higher clock frequency, depending on the OSR (Over Sampling Ratio) of the modulator. It is even more challenging to design a multi-bit quantizer. This is the main incentive behind using a VCO based quantizer. Such a quantizer can much easier operate at higher clock frequencies and provide a multi-bit output, mainly because a VCO-quantizer consists mostly of digital components and benefits from technologies with smaller transistors.

Nevertheless, the problem of designing the preceding integrators in the loop-filter still remains.

2.6.2 MASH VCO-ADC

A MASH VCO-ADC is an open loop structure that can potentially have high orders of quantization noise shaping using only VCO based integrators. In this method, the error signal of the first stage is extracted using only digital components, like edge triggered phase detectors, and then applied to a next VCO-ADC. This process can go on for multiple stages to have a higher order of quantization noise shaping [54–58].

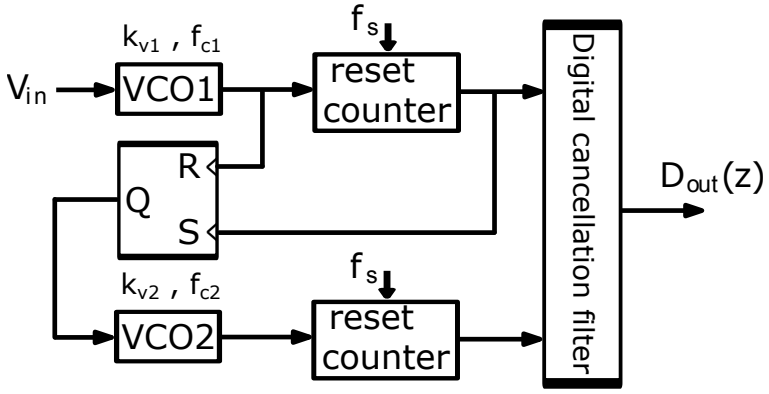


Figure 2.11: The system level structure of a second order 1-1 MASH VCO-ADC.

Fig. 2.11 shows the example of a second order MASH VCO-ADC. As the figure shows, the outputs of the two ADC's are not directly added, instead they need to be further processed and filtered in the digital domain before they are added.

To obtain the desired performance in the MASH structure, the analog filters need to be matched with the digital cancellation filters. Any mismatch between these two filters causes leakage of the quantization noise error of the first stage. In the VCO based implementation of a MASH structure the filters are first order integrators implemented by VCOs, the gains of which is proportional to the gain of the VCOs.

To the knowledge of the author, there are no successful implementations of this idea. This might be due to the fact that this is an open-loop structure and the imperfections of the phase detector, or in this case Set-Reset latch,

are not compensated in a control loop. Therefore, all the mismatches in the rise-time and fall-time of this element, and its delay, will leak into the next stage.

2.6.3 All-VCO CT-DSM

As it was mentioned earlier, the voltage-to-phase VCO based integrator in Fig. 2.9(a) can replace a conventional op-amp based integrator in the loop of a CT-DSM, and a voltage-to-frequency VCO based ADC can only be used as a noise shaping quantizer in a CT-DSM to replace its quantizer and last integrator. In the pursuit of designing a high order CT-DSM with only VCO-based integrators and quantizers, one can put the elements discussed earlier in this chapter together to accomplish that.

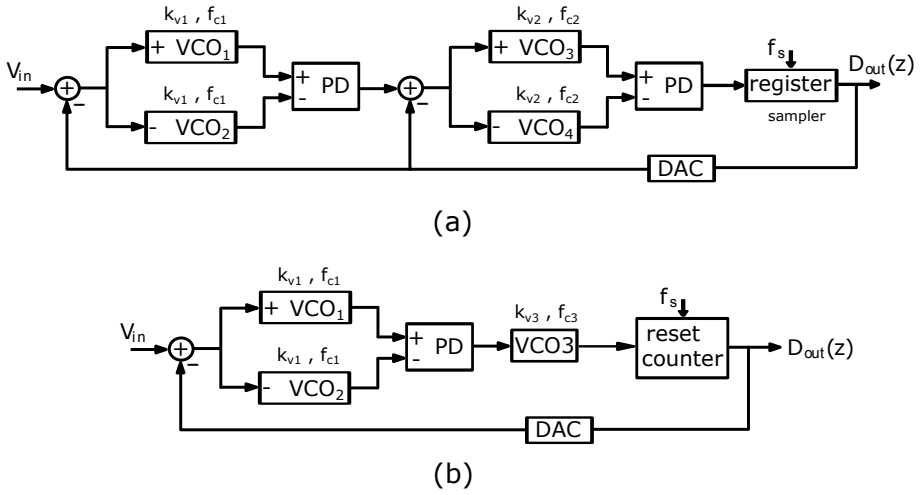


Figure 2.12: Two high order VCO based ADC's using voltage-to-phase and voltage-to-frequency integrators and quantizers.

For the case of a second order CT-DSM, for example, two VCO based modulators are shown in Fig. 2.12. In Fig. 2.12(a) both integrators of a second order CT-DSM are replaced with voltage-to-phase VCO-based integrator, [59].

In the second example, shown in Fig. 2.12(b), a voltage-to-phase VCO based integrator is used as the first integrator, and a voltage-to-frequency VCO based quantizer is used replace the second integrator and the quantizer [60].

Although these structures have been previously introduced in literature, there are no implemented proofs of concept for them available.

As mentioned earlier, voltage-to-frequency VCO based integrators can only be used as the last integrator in the integrator chain of a CT-DSM. In the following chapters we will introduce a novel system level solution that only uses voltage-to-frequency VCO based integrators. Two measured chips are also discussed as the first prototypes for such a high order VCO-based ADC.

Chapter 3

High order VCO-based CT-DSM

In this chapter a novel approach to use a voltage-controlled oscillator (VCO) as the first integrator of a high-order continuous-time delta-sigma modulator (CT-DSM) is presented. In the proposed architecture, the VCO is combined with a digital updown counter to implement the first integrator of the CT-DSM. Thus, the first integrator is digital-friendly and hence can maximally benefit from technological scaling.

Afterwards it will be shown that this VCO-based integrator can be used to replace all integrators in the loop of a CT-DSM, resulting in a new architectural concept for a mostly-digital all-VCO CT-DSM with a high order of quantization noise shaping.

3.1 Modeling a first order VCO-ADC

In order to model a first order VCO-ADC, and to prove that it is equivalent to a first order Delta Sigma Modulator, we will revisit the conventional Sampling quantizer and then use the results to model the VCO-ADC.

3.1.1 Splitting the Sampling Quantizer

A sampling quantizer, shown in Fig. 3.1(a), is one of the main building blocks of a Delta Sigma Modulator (DSM). This fundamentally mixed-signal block converts a continuous-time (CT) analog voltage to a digital stream, or in other words "digitizes" it. This digitization is applied to both

aspects of the input signal (V_{in}), its amplitude and its time. Digitization in the time domain is commonly known as sampling, and discretization in the voltage domain is known as quantizing. From a system level point of view, this block is similar to the famous Nyquist Rate ADC.

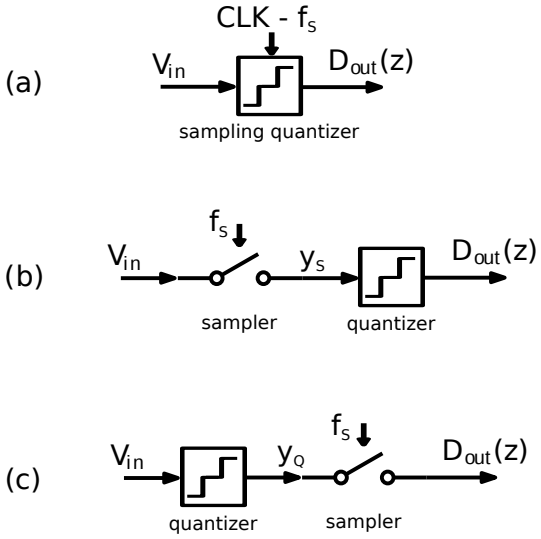


Figure 3.1: (a) a sampling quantizer,
(b),(c) and its equivalents.

The two functions of sampling and quantizing can be performed separately while one functionality follows the other. In this manner the three systems shown in Fig. 3.1(a-c) are strictly equivalent in the sense that their outputs, D_{out}, are bit by bit similar.

The signal y_S in Fig. 3.1(b) is the sampled version of the input (digitized in the time domain) and y_Q in Fig. 3.1(c) is the quantized version of the input (digitized in the voltage domain). At any given time the signal y_Q is an integer (i.e binary) and since it is not digitized in time the changes in its value are not synchronized with the clock signal. In other words, the "information" of this quantized waveform is not only stored in its values, but also in the location of the edges where the signal changes. In that sense this signal is very similar to the output of a Pulse Width Modulator (PWM) signal where the information is in the pulse width (or in the edges) of a two level signal. Signals of the same nature as y_Q are often referred to as 'multi-level PWM' signals or 'pseudo-digial' signals.

It is also worth mentioning that the sampler that follows the quantizer

in Fig. 3.1(c) is basically a clocked (edge-triggered) register, because its input has already a digitized (integer) value.

3.1.2 CT equivalence of a VCO ADC

The combination of a VCO and a reset counter, shown in Fig. 3.2 is often used as either an stand-alone ADC with first order quantization noise shaping or as a noise shaping quantizer in the loop of a high order CT-DSM.

The VCO converts the input voltage, V_{in}, to a square wave of which the frequency is proportional to the input voltage. Then the reset counter counts the number of rising edges of the square wave in every clock cycle. This way, it quantizes the phase which is the integral of the frequency. The reset function compensates this integration with an inherent differentiation. Apart from the quantization error, the resulting digital output signal D_{out} will be equal to:

$$D_{out} \approx \frac{f_{vco}}{f_s} = \frac{f_c + k_v V_{in}}{f_s} \tag{3.1}$$

where f_{VCO} stands for the VCO output frequency, f_c for the free running (zero input) frequency of the VCO, k_v for the gain of the VCO and f_s for the sampling frequency.

An equivalent system is depicted in Fig. 3.2(b), [29]. In this alternative structure the integration and differentiation functions (which previously happened simultaneously in the reset counter) are separated. After the VCO there is an up-counter which counts the rising edges of the output waveform of the VCO (the integration), and after sampling, the output is differentiated in the digital domain. Of course this implementation of a VCO-ADC is only conceptual, because in practice the output signal of the up-counter would go to infinity.

The functionality of a VCO as a voltage to frequency converter is shown in Fig. 3.2(c) using its parameters, k_v and f_c. The up-counter operates on the output phase of VCO, therefore, an integrator (with a gain of one) is put in place to show the conversion from frequency (Hz) to phase (cycles, or radians/2π). The output of the up-counter is the quantized phase with steps of one cycle. This functionality is addressed by putting the quantizer in Fig. 3.2(c).

In a next step, the differentiator in Fig. 3.2(c) can be replaced by a feedback loop with an integrator, which results in Fig. 3.2(d) and which is

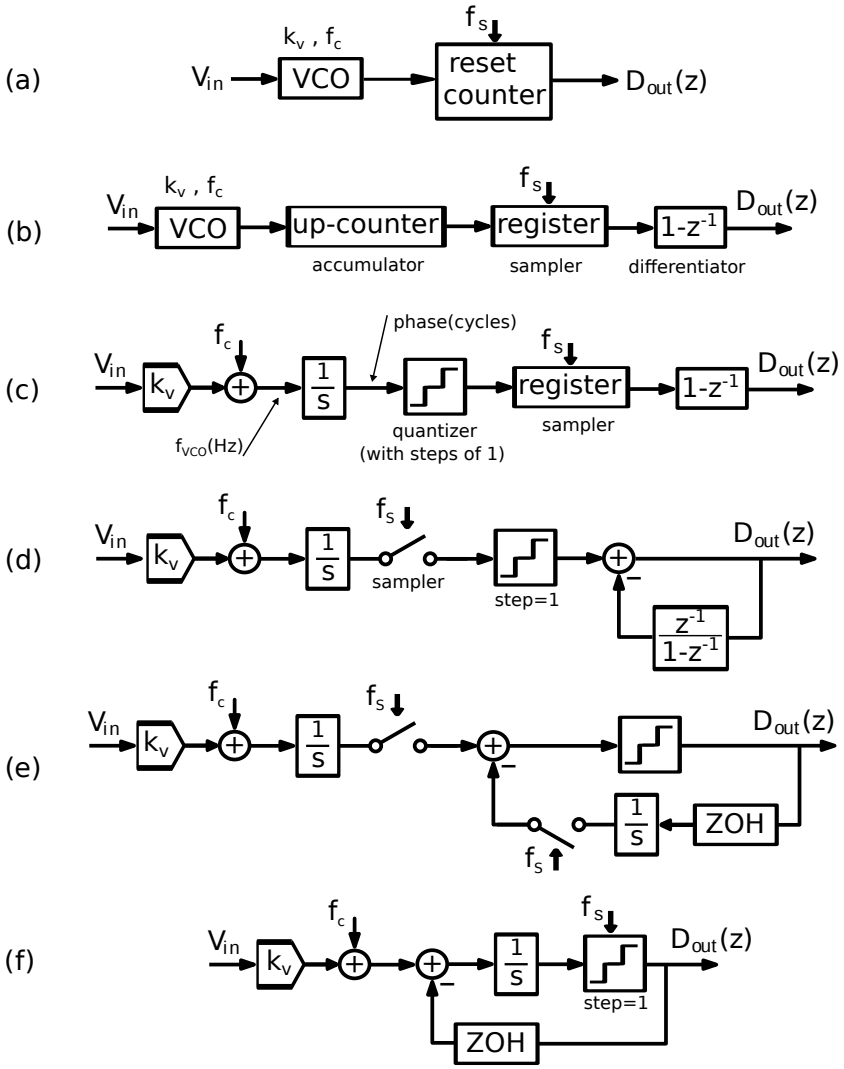


Figure 3.2: (a) a first order VCO ADC,
(b-f) and its system level equivalents.

still strictly equivalent to Fig. 3.2(c). The sampler and the quantizer are also interchanged, similar to Fig. 3.1.

Since the quantizer in Fig. 3.2(d) has a step of 1, it is transparent to digital signals (i.e has a gain of one for a digital signal). Therefore, the loop that is created in the digital domain can be extended to the input of the quantizer, see Fig. 3.2(e). It is also well known that the discrete time integrator $\frac{z^{-1}}{1-z^{-1}}$ is equivalent with the CT integrator $\frac{1}{s}$, preceded by a ZOH DAC and followed by a sampler (assuming a normalized sampling frequency of 1 Hz).

By combining the samplers and integrators in Fig. 3.2(e) we will arrive at the system Fig. 3.2(f) which is a conventional first order CT-DSM. This proves that a VCO-ADC is strictly equivalent to a first order CT-DSM.

The methodology presented in this section will be used later on in this chapter to use a VCO as the first integrator of a high order CT-DSM.

3.2 Using a VCO as the first Integrator

In most cases, in Continuous Time Delta Sigma Modulators (CT-DSMs) the first integrator is the bottle neck in terms of power consumption and noise. In deep-submicrometer processes, this block is becoming more and more difficult to implement in the voltage-domain due to the limited voltage headroom and gain of narrow channel transistors. For this reason, there is an increasing interest in VCO-based ADCs. One of the main issues with current VCO-ADCs with a VCO input stage is that they can only provide 1st order noise shaping. There have been a few attempts to increase the order by using multi-loop mash approaches [54, 55], but these techniques are very sensitive to analog imperfections [54].

A notable attempt to obtain a single-loop high-order VCO ADC which uses a VCO as the first integrator is [61]. However, this approach suffers from a high complexity and power consumption, and additionally it has high sensitivity to the center frequency of the VCO which makes this idea impractical.

In this section, we present a novel approach to use a VCO as the first integrator of a high order continuous time Delta Sigma Modulator. In the proposed architecture, the VCO is combined with a digital up-down counter to implement the first integrator of the continuous time Delta Sigma Modulator. The up-down counter in its simplest form can be implemented by adding a well established Phase Frequency Detector (PFD). This way,

the first integrator is digital friendly and hence can maximally benefit from technological scaling.

3.2.1 Introducing the Up-Down Counter

It was shown in the previous section that the VCO-ADC in Fig. 3.3(a) is equivalent to the model shown in Fig. 3.3(b), and that digital differentiator can be replaced by a feedback loop with an integrator, which results in Fig. 3.3(c).

The output of the digital integrator is a digital/integer number which is transparent to the sampling quantizer with the step of one. In other words, if a sampling quantizer has a step of one, it is like a gain of one for a digital input. Therefore, now that we have managed to create a loop in the digital domain, we can extend the loop and bring it to the analog domain using a zero order hold DAC, as in Fig. 3.3(d).

In order to have a balance in the terminology in the analog and digital domain, an integrator in the digital domain can be called and viewed as an "up-counter". Since the output of the two up-counters are being subtracted from each other, we can combine the two and call it an "up-down counter", as in Fig. 3.3(e).

This "up-down counter" functions as follows: at every rising edge of the VCO, its output is incremented by one. At every rising edge of the clock the counter output is decreased by the value D_{out} of the register (which will normally be multibit). By using a Return to Zero (RTZ) pulse, every rising edge of the clock also occurs in the feedback signal such that the up-down counter is now triggered by edges at both its inputs. We will come back to the implementation of such an asynchronous digital block later on.

We have already discussed that an up(-down) counter, from a system level point of view, behaves as an integrator; so we can clearly see that the system proposed in Fig. 3.3(e) is a first order Delta Sigma Modulator.

The output of this up-down counter doesn't go to infinity, in fact it's a limited pseudo digital integer number. However, since it can change at the rising edge of the VCO wave form, it is not synchronous with the sampling clock. In fact the information is partially stored in the position of the edges. This signal can be referred to as a "multi-level PWM" waveform. Note that the structure of Fig. 3.3(e) is still strictly equivalent to Fig. 3.3(a-d).

In the next subsection it will be shown that the combination of a VCO and an up-down counter can be used as the first integrator of a high order CT-DSM.

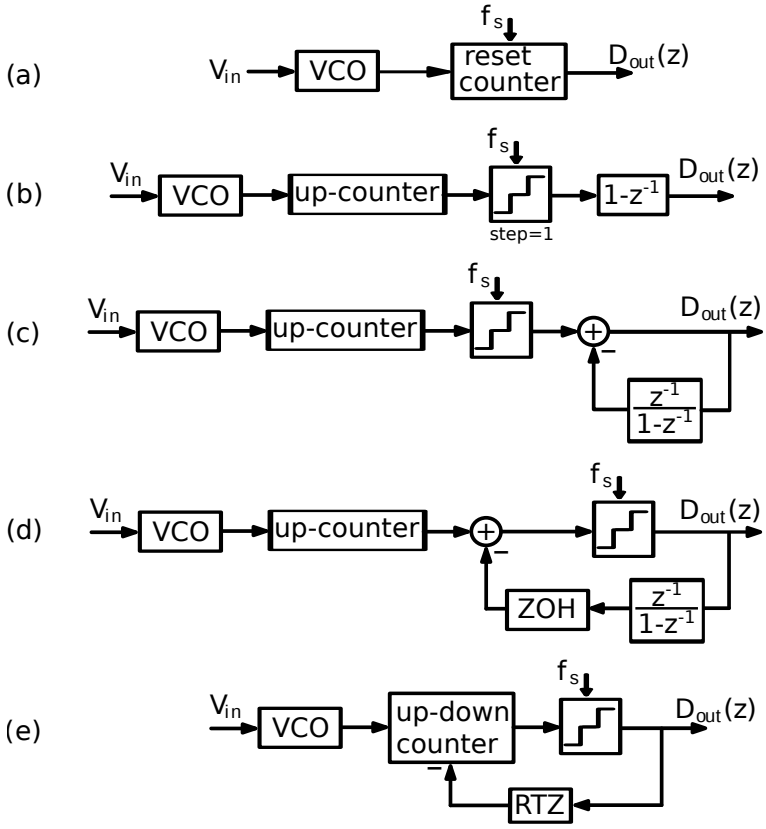


Figure 3.3: Metamorphosis of an open-loop first order VCO-ADC to a closed-loop one.
(a) the basic structure of a VCO-ADC
(b) An equivalent system with up-counter and digital differentiator
(c) replacing the differentiator with an integrator in the feedback
(d) extending the loop from digital to analog domain
(e) replacing the up-counter and the integrator with an up-down counter

3.2.2 Proposed Scheme

Now that we have managed to redraw the VCO-ADC as a feedback loop, as in Fig. 3.3(e), the next and final step is to increase its order by introducing additional integrators in the loop, as in Fig. 3.4(a). It is clear that the resulting structure can be of any order. Its first integrator is implemented by the combination of the VCO and the up-down counter, and hence is

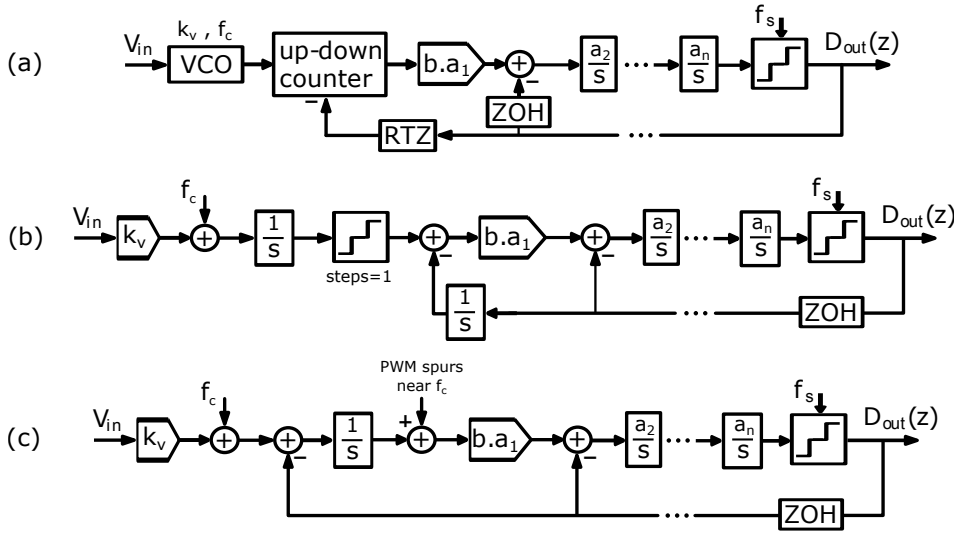


Figure 3.4: (a) The proposed system with a VCO as the first integrator, (b),(c) and its CT equivalents.

digital friendly and suitable for integration in today's deep sub-micrometer CMOS. The second and later integrators are still in the analog/voltage domain, but their implementation is very relaxed because their errors are reduced by the gain of preceding integrators. Moreover, particularly the second integrator has a pseudo digital input and can be realized using a set of charge-pump integrators (switched current sources and a capacitor) [1]. Local feedbacks to create notches in the Noise Transfer Function (NTF), as in conventional CT-DSMs, can also be integrated into this scheme.

The factor b in Fig. 3.4(a) is a "normalizing factor" which converts the output of the up-counter to the full scale of the system (i.e $\pm V_{ref}$). In practice this gain stage will be incorporated in the gain of the following integrator. The factor b is simply obtained by normalizing to the ratio of f_c/f_s:

$$b = \frac{f_s \cdot V_{ref}}{f_c} \tag{3.2}$$

In order to model the proposed structure, we can replace the up-down counter with integrators and a quantizer, as was shown in the previous subsection. This will result in the equivalent model in Fig. 3.4(b). The

output of this quantizer (which has steps of 1) is a multi-level PWM signal which consists of two main parts: the low frequency (baseband) components, which is the integrated input (with some additional gain and bias), and the high frequency components, which are mostly the undesired PWM spurs around the carrier frequency of the VCO, f_c.

After combining the two $\frac{1}{s}$ integrators, the high frequency spurs explained above can be separately modeled, as shown in Fig. 3.4(c). These high frequency spurs can alias to the baseband after the quantizing sampler has sampled their contribution in the last stage of the modulator. But one can expect the integrators before the sampler to alleviate this problem.

The additional branch representing the carrier frequency of the VCO, f_c, is added to the system as a DC offset and doesn't affect spectral integrity of the input signal.

Summarizing, the proposed structure is equivalent to a conventional CT-DSM with the same integration coefficients, a_i. The proposed system is simulated in the next section to provide a better understanding of the time domain behavior of the up-down counter. The output spectrum of the modulator is also compared to that of a conventional CT-DSM.

3.2.3 Simulation results

Some typical system level simulation results are shown in Figures 3.5 and 3.6. Here the modulator is a 3rd order single bit design with a Butterworth NTF and a $h_\infty = 1.6$ and a local feedback to create a notch in the NTF, (h_∞ is the stability factor, as defined by the Schreier toolbox). Fig. 3.5(a) shows the output spectrum for the conventional modulator for the case of a -14 dBfs input signal. The results for the corresponding new structure of Fig. 3.4(a) are shown in Fig. 3.5(b). It is clear that the output spectra for both cases are nearly identical.

A look at the internal waveforms of the two modulators, however, shows that they have a completely different time-domain behaviour.

Fig. 3.5(c) and (d) compare the output signals of the first integrators of the two ADCs. As it was previously explained, the output of an up-down counter is a multi-level PWM signal, which is in this case a 3-level signal, Fig. 3.5(d). Despite this obvious difference in the internal waveforms, the two modulators maintain almost identical spectral integrity.

The amplitude of the main tone (corresponding to the input signal) at the output of an integrator in a CT-DSM (be it conventional or VCO-based), which is normally the dominant contribution at these nodes, is

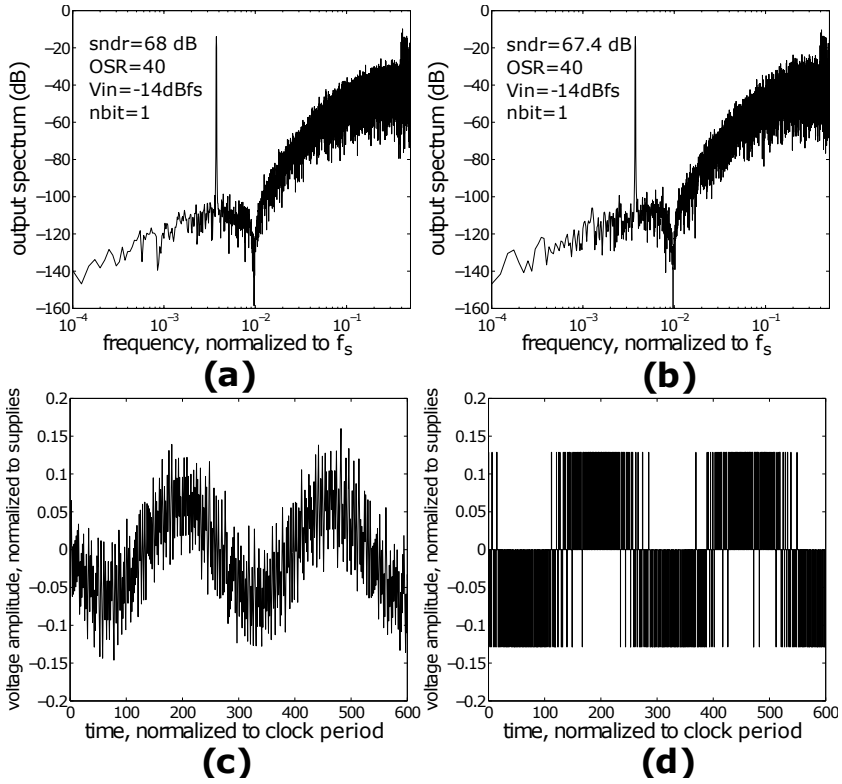


Figure 3.5: Simulation results of two 1-bit CT-DSMs with a -14 dBfs input tone.
(a) output spectrum of a conventional 3rd order modulator
(b) output spectrum of a VCO-based modulator with the same NTF
(c) output signal of the first integrator for the conventional modulator
(d) output signal of the first integrator for the VCO-based modulator

proportional to the amplitude of the input signal. Therefore, an increase in the input voltage will increase the signal level at these nodes too.

In the case of the proposed VCO-ADC, this higher swing would translate to a higher number of levels.

For Fig. 3.6, a higher input amplitude (-6 dB instead of -14 dB) is used. Again the overall output spectra are almost identical. As Fig. 3.6(c) shows, for the conventional CT-DSM, the voltage swing at the internal node has clearly increased. The equivalent node for the VCO-based CT-DSM, Fig. 3.5(d), also shows an increase in the signal swing, except here a higher

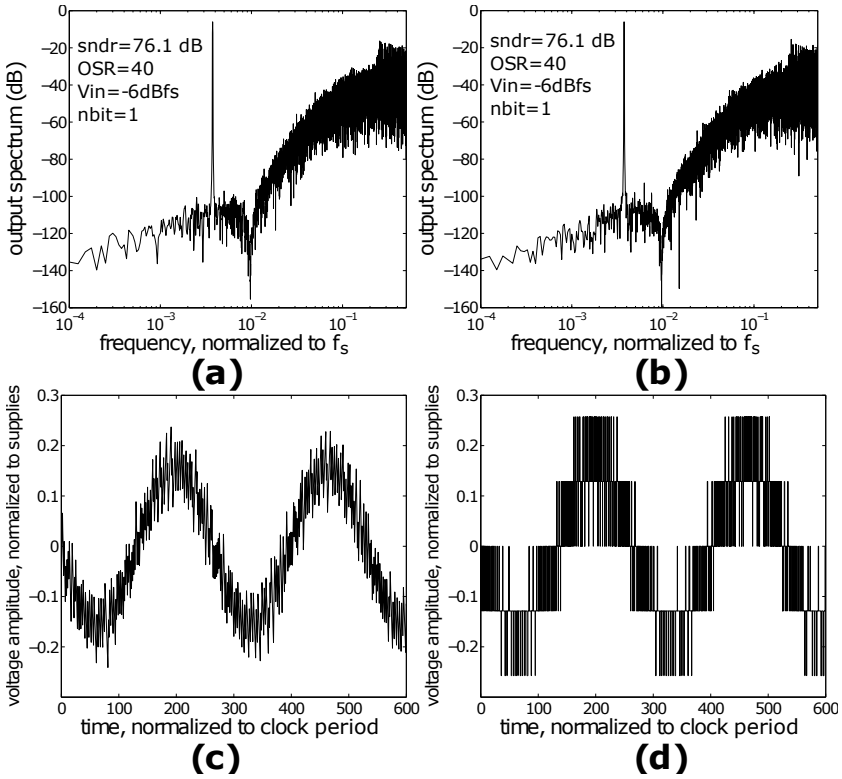


Figure 3.6: Simulation results of two 1-bit CT-DSMs with a -6 dBfs input tone.
(a) output spectrum of a conventional 3rd order modulator
(b) output spectrum of a VCO-based modulator with the same NTF
(c) output signal of the first integrator for the conventional modulator
(d) output signal of the first integrator for the VCO-based modulator

swing simply means that more levels are used in the PWM waveform.

3.2.4 Implementation considerations

The proposed structure has a VCO input stage and as such it is directly affected by VCO's nonlinearity. However, there are several ways to solve this problem, including PWM pre-coding [1, 29] and post calibration [62].

Another imperfection that can be associated with a VCO is inaccuracy in its carrier frequency f_c and its voltage to frequency conversion gain

k_{vco}, but these imperfections in the VCO don't impose any problem on the proposed scheme. Any error in f_c will be translated to a mere DC offset in the output and an error in the value of k_{vco} can be viewed as a gain error for the overall modulator.

The most important new block is the up-down counter which is triggered by edges at both its inputs. This way, this is basically an asynchronous circuit and in general its implementation can be challenging. However, its design can be greatly simplified by using a single bit quantizer (as was done in the simulations of Fig. 3.5 and 3.6). An additional important parameter is the signal swing at the output of the up-down counter. This swing can be controlled either by appropriately scaling the modulator coefficients or by restricting the modulator's input range. In the particular case that the output swing is only three-level (as in fig. 3.5(b)) the up-down counter collapses to the well known Phase-Frequency Detector (PFD) which is widely used in PLL's and for which efficient implementations are well known. If a higher swing is needed, some additional logic of similar complexity as a PFD is needed.

In the next section it will be shown that using a multi-phase VCO, instead of a single-phase one, will heavily simplify the design of the up-down counter and allow the designer to higher signal swings (i.e more levels) at the output of the up-down counter. It will also be shown that the combination of the VCO and the up-down counter can be used to replace all the integrators in the loop of a CT-DSM.

3.3 High order All-VCO CT-DSM

In this section the architectural concept of a mostly-digital VCO-ADC with high order quantization noise shaping is presented. The system is based on the combination of a VCO and a digital counter. This combination can function as a continuous time integrator to form a high-order Continuous Time Delta Sigma Modulator (CT-DSM). The counter consists only of digital building blocks and the VCOs can be implemented using Ring Oscillators, which are also digital friendly. No traditional analog blocks, like op-amps, OTAs or comparators, are needed.

3.3.1 VCO based continuous-time integrator

A core building block for an ADC with high order noise shaping is an integrator. In this context, the structure of Fig. 3.7(a) was studied in the

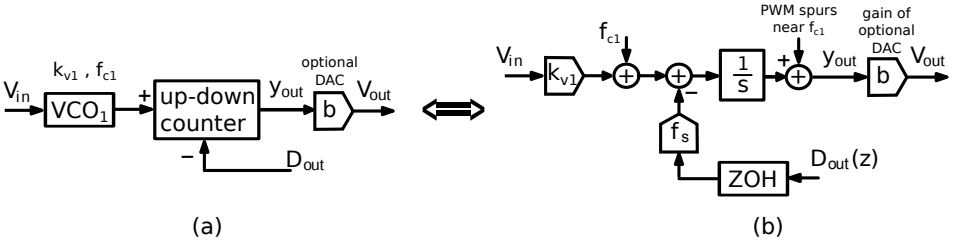


Figure 3.7: (a) A VCO based integrator
(b) and its equivalent continuous-time model.

previous section, see Fig. 3.4, which has a continuous time analog input V_{in} and a discrete time digital input. In a continuous time Delta Sigma Modulator (CT-DSM), the discrete time digital input will typically be driven by the overall ADC's output signal and is therefore called D_{out} here. The analog input voltage, V_{in}, is applied to a Voltage Controlled Oscillator VCO_1 with a gain K_{v1} and a carrier frequency f_{c1}. The VCO is followed by an "up-down counter", which is a continuous-time digital block. This up-down counter behaves differently on its positive (up) input (driven by the VCO) and negative (down) input (driven by the discrete time digital signal D_{out}). It functions as follows: at every rising edge of the VCO its output is incremented by one, and at every rising edge of the sampling clock the counter output is decreased by the value of the digital output at that time, D_{out} (which is a multi-bit integer).

The output y_{out} of the up-down counter is a (multi-bit integer) digital signal. However, it does not only change at the clock edges, in fact the information is encoded in the position of the edges: hence, it can be viewed as a multi-level PWM signal [5]. If a true analog output is needed, a Digital to Analog Converter (DAC) with a normalizing gain b can be added. We will see later on, that this component can usually be merged into successive building blocks or even omitted. As such in practice, this DAC does not add to the complexity of this solution.

From the equivalence set up in Fig. 3.4, it follows that this digital implementation of a VCO integrator can be modeled by the equivalent system shown in Fig. 3.7(b). This can be understood from the fact that the analog input signal is integrated and provided as a multi-level PWM at the output. Due to this, there are PWM-spurs at the output. Also, there is a fixed input referred contribution from the VCO carrier frequency. Clearly, the fact that there are high frequency modulation spurs, is a disadvantage.

Nevertheless, since we want to use this block in a CT-DSM, we can expect that this will not be a severe problem, because these high frequency spurs, normally will be rejected by the inherent anti-aliasing filtering of the CT-DSM [63]. However, in a final design this must be confirmed by system level simulations. It is obvious that the implementation of the integrator shown in Fig. 3.7(a) is much more digital friendly than conventional analog integrator designs based on op-amps, especially if the optional DAC block can be omitted. This integrator is a core ingredient of the high-order noise-shaping ADC in this chapter.

3.3.2 VCO based sampling quantizer

A second core building block in a noise shaping ADC is a sampling quantizer. For this, the conceptual structure of Fig. 3.8(a) has widely been used [53, 64, 65]. This structure performs the sampling, the quantization and in addition provides a first-order noise shaping of the quantization noise. This way, this structure can be used inside a $\Sigma\Delta$ loop and also as a stand-alone first order VCO-ADC.

An alternative implementation, that is closer to the implementation of Fig. 3.7, was obtained in the previous section, see Fig. 3.3(e). This structure, drawn again in Fig. 3.8(b), consists of an up-down counter (as the integrator of Fig. 3.7) and a sampling register, which samples at the sampling frequency f_s. The main advantage of this alternative implementation is that the input signal of the quantizer y_Q is now available. It will be shown below that this signal can be used to provide local feedback in an all-VCO CT-DSM.

By observing that sampling the multi-level PWM signal at the counter output, corresponds to a (time-domain) quantization of the integrator output, we can obtain the equivalent model of Fig. 3.8(c). Here the quantizer's quantization step is equal to the counter step, which is 1 in this diagram, where the instantaneous counter output is an integer.

This block diagram illustrates the equivalence between a VCO quantizer and a first-order $\Sigma\Delta$ modulator, which was also established in several prior works (e.g. [20]).

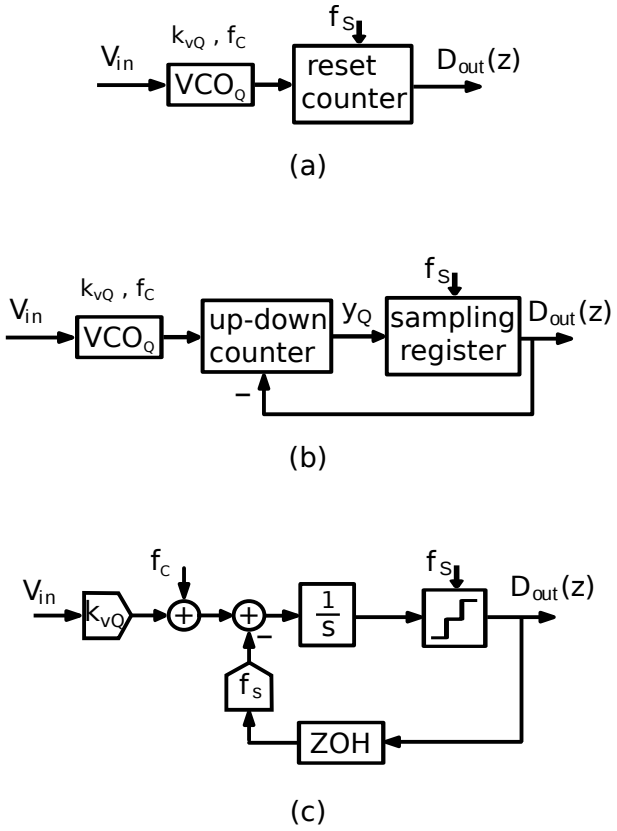


Figure 3.8: (a) A First-order noise shaping quantizer consisting of a VCO and a reset-counter,
(b) an alternative implementation with the same behavior
(c) and an equivalent continuous time model.

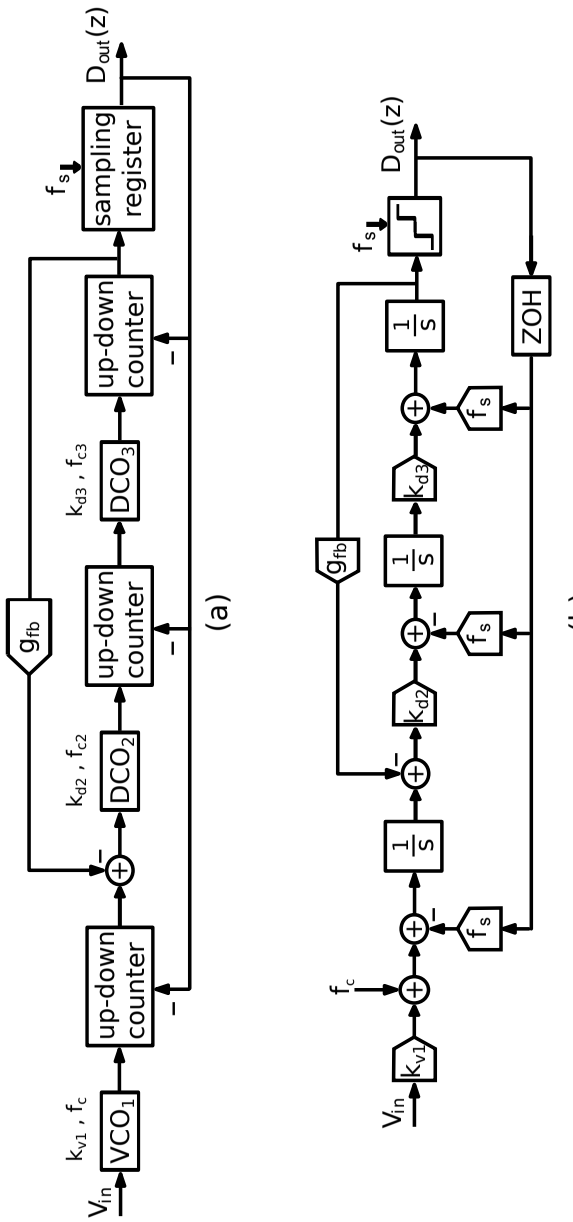


Figure 3.9: (a) Proposed architecture of a 3rd-order all-VCO CT-DSM (b) and its equivalent CT-DSM.

3.3.3 General All-VCO CT-DSM architecture

Based on our VCO based integrator and quantizer, we can now develop a VCO-ADC with noise shaping of arbitrary order. As an example of the proposed scheme, a third order all-VCO CT-DSM is shown in Fig. 3.9(a). As the figure shows, the (continuous time) digital output signals of the up-down counters directly drive the succeeding block without the optional DAC of Fig. 3.7. Due to this, the second and third controlled oscillator, do not have a voltage mode input and hence are not 'voltage' controlled oscillators. Instead they have an (integer) digital input, and hence are Digitally Controlled Oscillators (DCOs). Therefore, the gains of these two DCOs, k_{d1} and k_{d2} have the dimension *Hz per digit* (or simply Hz). We will show in chapter 6, that in our design the implementation of these DCOs is not more complex than the implementation of a conventional voltage input VCO. The optional coefficient g_{fb} is a small (dimensionless) number, and can be added to optimize the position of the NTF zeros [63].

By using the equivalence, set up in Fig. 3.7 and Fig. 3.8, an equivalent CT-DSM of the proposed system can be obtained, which is shown in Fig. 3.9(b). The carrier frequency of the first VCO appears on the equivalent system in Fig. 3.9(b) as a DC bias added to the input branch.

The carrier frequencies of DCO_2 and DCO_3 do not contribute to the output signal of the modulator, because, when referred to the input, they become zero. Therefore, the adding branches that should represent them, are not shown in Fig. 3.9(b). In order not to overload the figure, the extra branches corresponding to the PWM spurs, similar to the one in Fig. 3.7(b), are not shown either in Fig. 3.9(b). This is partially justified by the assumption that the modulator should provide sufficient anti-aliasing filtering to suppress them. However, this assumption must be confirmed by system level simulations.

In the following chapters we will propose circuit level implementations for this modulator. The first VCO is the most challenging component to design. In Chapter 4 a linear VCO design is introduced. In Chapter 5 PWM pre-coding technique for linearizing the first VCO is examined. Chapter 6 showcases the first prototype of a 3rd order modulator of this type. Chapter 7 is another prototype of the same modulator family, but instead of a linear VCO it utilizes the PWM pre-coding technique.

Chapter 4

Linear voltage controlled ring oscillator

In this chapter a very simple Ring-Oscillator VCO structure for use in VCO-ADC applications is presented. It has a greatly improved linearity compared to previously published VCO's. Measurement results of a 1 Volt, 65 nm CMOS prototype confirm the effectiveness of the proposed approach. This oscillator can be used as the first VCO in the system proposed in Fig. 3.9. As mentioned in Chapter 3, the first VCO is the most challenging one to design, because it has the most contribution in the noise and non-linearity performance of the overall modulator.

4.1 Ring oscillator input circuit

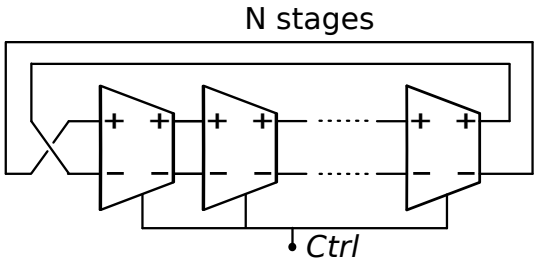


Figure 4.1: Ring oscillator with N differential delay elements.

Our starting point is the well known ring oscillator (RO), shown in Fig. 4.1. It consists of N differential delay elements placed in a ring. For

the delay element, the circuit of Fig. 4.2 was used [47]. It consists of 2 main inverters and 2 small auxiliary inverters. The task of the auxiliary inverters is to align the edges of both main inverters, such that both main inverters will switch at (almost) the same time stamp (one will have a rising edge and the other a falling edge). The circuit can be tuned through its control terminal (Ctrl).

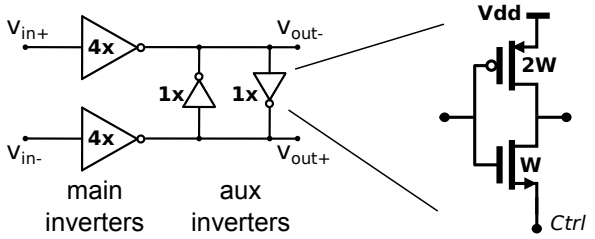


Figure 4.2: Delay cell used in the ring oscillator.

For this circuit, we investigated the overall linearity. Surprisingly, the available literature guidelines are completely contradictory. Some authors claim that the oscillation frequency f_{RO} is proportional to the voltage $V_{RO} = V_{dd} - V_{Ctrl}$ over the inverters in the ring [66, eq.14]. This leads to the conclusion that direct voltage mode control is the optimal choice. Other authors claim that the oscillation frequency is proportional to the current driven into the control terminal [67, fig.4] [47, fig.4]. This suggests that direct current mode control is best. And finally some other authors claim that the oscillation frequency is proportional to the ratio of the two [66, eq.10] [67, eq.2], which does not directly lead to a simple drive strategy.

Upon investigation, it turns out that all these claims are approximately valid in a certain operation range of the RO. But the actual curves exhibit (depending on how large the tuning range is) nonlinearities of several percents. The current control performs best, but, since in most cases the input signal is available as a voltage rather than a current, this control strategy imposes the need of an additional voltage to current conversion. This voltage to current conversion adds to the power budget and introduces additional nonlinearity.

In this work we propose the simple novel mixed input structure shown in Fig. 4.3. The structure can be considered as a go-between of the current mode control and the voltage mode control. This structure has several attractive features. First, the input circuit is much simpler than transcon-

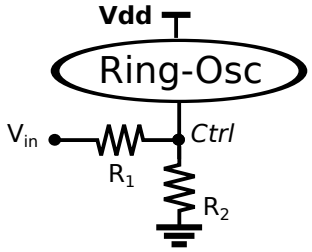


Figure 4.3: Ring oscillator with resistive input stage

ductor based circuits that are widely used. Due to this, it has significantly better noise performance and power efficiency than transconductor based circuits. Second, the linearity of this resistive input circuit is better than the linearity of an RO with an ideal current control. To understand this, the (simulated) frequency tuning curve with ideal current control is shown in Fig. 4.4(a). It is clear that the curve exhibits a negative curvature. In the proposed circuit the ring current I_{RO} will be:

$$I_{RO} = -\frac{V_{in}}{R_1} + V_{Ctrl}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{4.1}$$

The term $-\frac{V_{in}}{R_1}$ is linear in the tuning voltage, but the term proportional to V_{Ctrl} is nonlinear. A simulation of the relation between V_{in} and V_{Ctrl} for the case of a supply voltage $V_{dd} = 1\ V$ is shown in Fig. 4.4(b). It is clear that this curve exhibits the opposite curvature of the current mode tuning curve of Fig. 4.4(a). By appropriately sizing the resistors R_1 and R_2, both nonlinear effects will cancel out.

In sizing the resistors there are 2 degrees of freedom: the value of R_1 and the value of R_2. The ratio R_1/R_2 should be chosen such that both nonlinear contribution cancel. In the family of circuits that we examined (where the supply voltage was 1 Volt) the optimum was very close to the case of matched resistors: $R_1 = R_2 = R$. Then, there only remains 1 degree of freedom: i.e. the value of R. This value should be sized to satisfy the desired input referred noise of the VCO.

4.2 Oscillator core design

The final step in the VCO design is the sizing of the inverters of the delay cells and the choice of the number of elements in the loop. In the case where

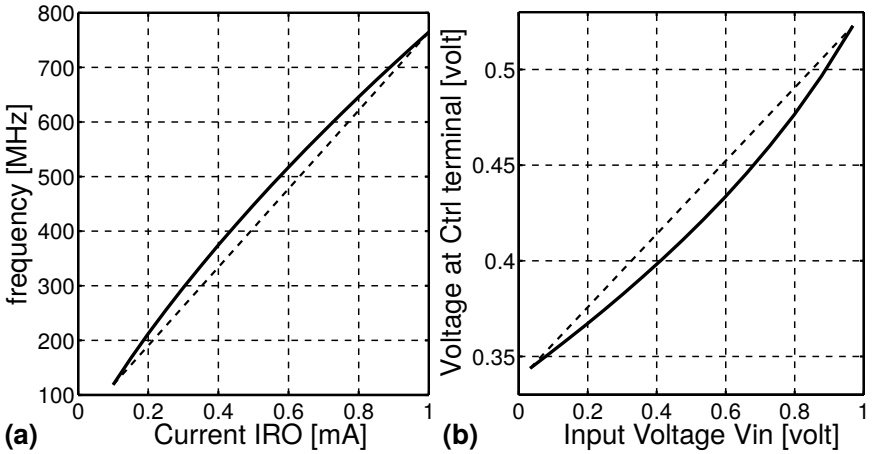


Figure 4.4: (a) Tuning curve with current control exhibiting a negative curvature,
(b) and Control voltage V_{ctrl} vs the input voltage curve exhibiting a positive curvature.

the ring is current controlled (as is roughly the case here), the propagation delay of each cell will be more or less inversely proportional to the current and directly to the total capacitive load C_{tot} that each delay cell drives. This capacitive load will consist in part of wiring capacitance C_{wire}, in part of C_{inv}, the input capacitance of the next inverter loading it and also of C_{load} the load formed by VCO phase readout circuits. This way, we can see that the oscillation frequency will behave according to:

$$f \propto (C_{tot} \cdot N)^{-1} \quad , \quad C_{tot} = C_{inv} + C_{wire} + C_{load} \tag{4.2}$$

In prior work, it has been shown that it is beneficial to design the delay stages so as to achieve a minimal delay [20]. This allows to have simultaneously a relatively high oscillation frequency and at the same time a high number of stages, which leads to improved quantisation noise and bandwidth performance of the ADC. The conclusion is that the inverters should be sized as small as possible (minimizing C_{inv}). However, in a low-voltage context (as we have today), there is an additionally important constraint: i.e. the voltage over the ring should remain sufficiently small (definitely sufficiently smaller than the supply voltage). The smaller the inverters are sized, the larger the voltage over the ring will be. The conclusion is that the inverters should be sized with the minimal size that still keeps the voltage

over the ring acceptable (less than the supply voltage) and that the number of stages N should be chosen to obtain the desired oscillation frequency.

4.3 Measurement Results

As a proof of concept, a test circuit of the proposed RO was manufactured in the low power flavor of a 65 nm CMOS technology (on a die with other test circuitry). The circuit was designed for a 1 V power supply and an oscillation frequency centered around 300 MHz. The resistors in the input network were $R_1 = R_2 = 770\ ohm$, which were arbitrarily sized in this test circuit, which focuses on linearity and not on noise. The resulting number of stages in the design was $N = 18$ stages.

The measurements reported here are for a 1 Volt supply but the circuit remained operational for supply voltages as low as 0.8 Volt. The measured voltage to frequency conversion curve of the VCO for a rail-to-rail input voltage sweep is shown in Fig. 4.5(a). Clearly, the curve is visually linear. The deviation of this curve from a best fit line (i.e. the nonlinearity error) is shown in Fig. 4.5(b). The worst case nonlinearity over the entire tuning range from 100 to 500 MHz is ±2.2 MHz, corresponding to 0.6% of the full scale.

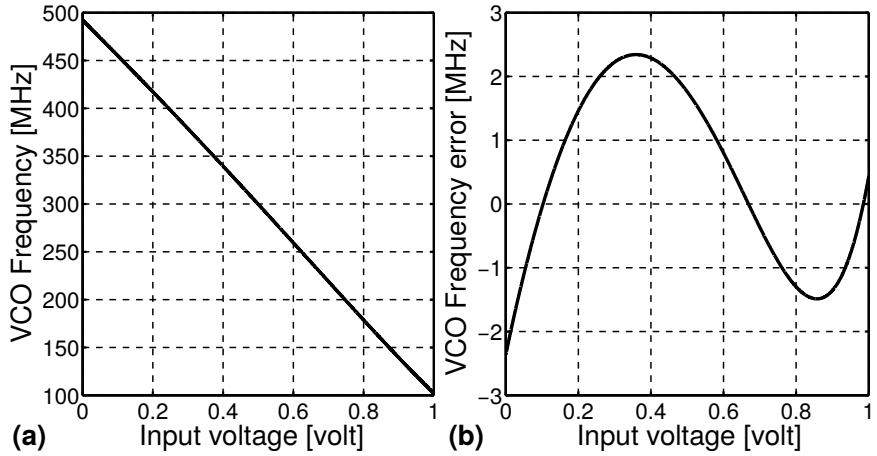


Figure 4.5: (a) the voltage to frequency conversion curve of the proposed VCO
(b) and the nonlinearity of its frequency error.

In another set of measurements, two VCO (each on a different die com-

ing from the same wafer) were configured as a pseudo dfferential ADC. For this, they are driven by a differential input signal with a midscale common mode voltage (of 500 mV). In our test circuit only one of the phases of the VCO was accessible (instead of the 18 phases as would be in an actual VCO ADC). Now, for each VCO, this output phase was captured by a 10 GS/s sampling oscilloscope and converted into a bitstream, and differentiated in the digital domain. Then the results for both VCOs were subtracted form each other. This way we obtain a configuration that is similar to an actual (pseudo-differential) first order noise shaping VCO-ADC (only with reduced performance because we are only using 1 out of the 18 phases) [20].

The corresponding output spectrum for the case of a 100 KHz, 400 mV_{pp} differential input sine wave is shown in Fig. 4.6. Note that this is -14 dB below the absolute maximum signal level which whould be 2 V_{pp}. The third harmonic is clearly visible at -74 dBc. The second harmonic distortion is also visible at -85 dBc but is so small that it almost does not affect the overall THD. This is due to the pseudo differential configuration. In the case where only 1 of the two VCO's was used (corresponding to a single-ended configuration), the second harmonic was -51 dBc, indicating that over 30 dB rejection of even order harmonics is easily achieved (even in this non-optimal configuration, where both VCO's are on a different die).

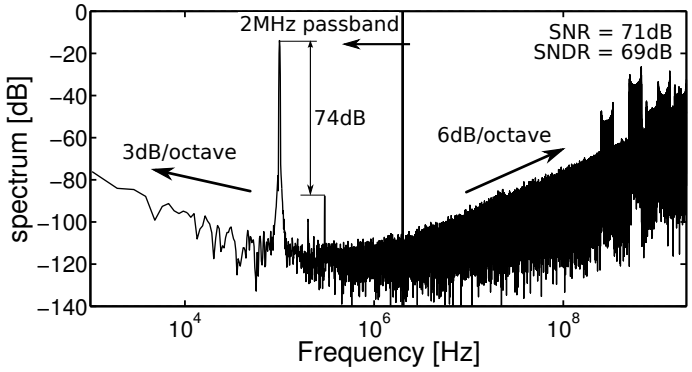


Figure 4.6: Output spectrum of the pseudo differential VCO ADC experiment.

The high frequency noise roll off of 6 dB/octave corresponds to the expected first order noise shaping. In this configuration, this noise contribution dominates above a few MHz, but as explained above this is due to the fact that only 1 of the 18 VCO phases is used here. Then there is

a white noise floor (related to the thermal noise of the resistors). At low frequencies there is also some 1/f noise. For this case, the SNR and SNDR over a bandwidth of 2 MHz were equal to 71 dB and 69 dB respectively.

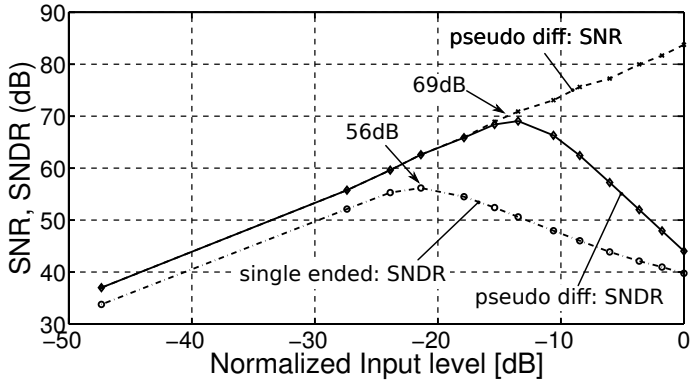


Figure 4.7: SNR and SNDR vs. the normalized rail to rail input level (of 2Vpp differentially).

Similar experiments were performed for varying input levels. The corresponding results for the SNR and SNDR in a 2 MHz bandwidth are shown in Fig. 4.7. It is clear that for large input signal levels the performance is limited by distortion, leading to a peak SNDR of 69 dB at 400 mVpp (the case shown in Fig. 4.6). The result for the case where only 1 VCO is read out (in a single ended configuration), is shown as well). Here, at high signal levels the distortion is dominated by the second harmonic, leading to a peak SNDR of 56 dB (much worse than the pseudo differential case).

The power consumption of a single VCO was 0.65 mw. This power consumption is almost entirely determined by the choice of the resistors R_1 and R_2 (which were 770 ohm in this case). As explained above, the power can easily be reduced by using larger resistors, but this is at the expense of a higher white noise level. The area for a single VCO is 60 $\mu m \times 25$ μm.

Although the linearity of the proposed VCO circuit is good enough for many applications, in the next chapter we will examine the potential of PWM pre-coding technique to even further improve linearity of the VCO.

Chapter 5

Theory and design of a passive ADSM

VCO based Analog to Digital conversion allows easy implementation of noise shaping A/D conversion [5,6,20,29–31]. However, in a straightforward implementation of such a VCO ADC, the overall linearity will be limited by the linearity of the VCO, which typically will not be good enough. A potential solution is to convert the input voltage into a two-level signal where the information is stored in the duty cycle of the resulting square-wave using an Asynchronous Delta Sigma Modulator (ADSM) or a Pulse Width Modulator (PWM). This method is known as 'PWM pre-coding' [29–31].

The PWM and ADSM that have been previously presented in the literature make use of typical analog building blocks, such as highly linear transconductance gain stages or op-amps. As it was discussed before, the main scope of this book is to avoid these traditional blocks, because they are specially very challenging to design in the most recent CMOS technologies with smaller transistor channel lengths and lower supply voltages.

As an alternative we propose the use of an ADSM with a passive loop filter and it will be shown that such a modulator, if properly designed, can provide sufficient linearity for almost any application.

The previous theoretical work to predict the linearity of passive and active ADSM was presented in [68], but it had some errors. Therefore, in the first section of this chapter we will revisit the theory and come up with a more accurate estimation.

In the second section, the effect of loop delay in an ADSM will be

analyzed. It will be shown that the loop delay, which is normally due to the Schmitt trigger doesn't necessarily ruin the performance of the ADSM, as long as it is properly modeled, taken into account, and compensated by lowering the threshold voltage of the Schmitt trigger.

Finally, an implemented prototype is measured and discussed in the last section of this chapter. The presented proof of concept is an ADSM with a passive loop filter with an input bandwidth of 10 MHz. This circuit is easy to implement and is operational under low supply voltages, 1 V.

5.1 Analyzing ADSMs without delay

This section investigates the commonly used Asynchronous Delta Sigma Modulator which consists of a schmitt-trigger and a continuous time loop filter. A detailed analysis is presented to accurately predict the distortion of such modulators. The extracted expressions are compared with simulation results and they illustrate an excellent match. The results are also compared with a previous work by Roza [68] and they show a drastic improvement in accuracy.

There has been related prior work on the distortion of PWMs, e.g. [68–71]. However, [69] and [70] concern PWM structures that deviate from the class that is studied in this manuscript. The PWMs studied in [69] are ADSMs that have a continuous time loop filter but instead of a schmitt-trigger they have a comparator in the loop. In such ADSMs, the order of the loop filter needs to be greater than two to have a stable oscillation. In the family of ADSMs that we are studying here, it is required that the hysteresis of the schmitt trigger is non-zero. The resulting ADSMs can already work with a passive 1st order loop filter.

On the other hand, [71] and [68] do focus on the same class of ADSMs as our manuscript. However, [71] concerns a simulation based aproach instead of an analytical one. The only work that presents analytical expressions to predict the 3rd order harmonic distortion of an ADSM is by Roza [68]. This work gives a good insight to the understanding and analysis of an ADSM, but the final equation for the distortion does not have a good match with simulation results. Therefore we will present a more accurate analysis below to find an expression for the distortion and carrier frequency of an ADSM, then we will compare the proposed theory with simulation results and with Roza's results [68] as well.

Fig. 5.1 shows a typical spectrum for the output of an ADSM with a

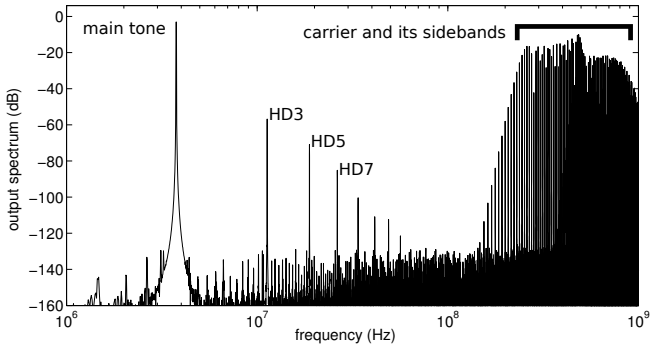


Figure 5.1: A typical spectrum for the output of an ADSM.

single tone input signal. As Fig. 5.1 shows, the output of this modulator consists of baseband distortion components (the harmonics of the input tone: HD3, HD5, ...) and higher frequency spurs corresponding to the carrier frequency and its sidebands [68]. As it will be proven later, and as Fig. 5.1 confirms, ADSM has an odd nature, therefore, its output only contains odd order harmonics of its input signal. The proposed theory accurately estimates these harmonics with explicit expressions for the 3rd and the 5th harmonic.

If the carrier frequency is high enough, depending on the application of the ADSM (i.e. ADC or PA), the high frequency spurs can be filtered later in the digital or analog domain. Nevertheless, as we will see later, the carrier frequency of an ADSM is important in determining the distortion of the modulator. Moreover, it puts a limit on the bandwidth and power consumption. Therefore, estimation of the carrier frequency is also included in this work.

In this section, first, an accurate theory is presented for a general input signal. Second, the theory is simplified, and third, it is applied to a special case where the input signal of the ADSM is sinusoidal. The harmonic distortion components and the carrier frequency for that case will then be derived. Then the simulation results are compared with both the presented and prior theory.

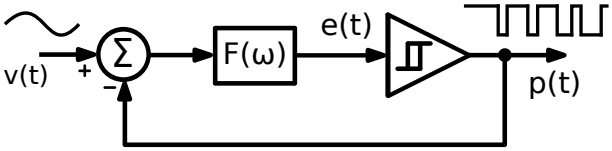


Figure 5.2: A general representation of an ADSM.

5.1.1 Proposed Theory

General Theory

Fig. 5.2 shows the general diagram of an ADSM. Here, $v(t)$ is an arbitrary input signal and is assumed to be limited to a full scale of ± 1. $e(t)$ is the filtered error signal at the input of the schmitt-trigger. $p(t)$ is the output square wave with a pulse width of α and instantaneous period T, which toggles between $+1$ and -1. As it will be shown later in this section, in this type of modulation, not only the duty cycle of the output square wave, $\frac{\alpha}{T}$, but also its carrier frequency are dependent on the input signal. The carrier frequency of an ADSM for a zero input is referred to as ω_c and $\omega_1 = \frac{2\pi}{T}$ is the (instantaneous) carrier frequency which is a function of the input signal, v. According to Fig. 5.2 we can write the signal flow at e(t):

$$e(t) = \left((v - p) \otimes f\right)(t) \tag{5.1}$$

where $f(t)$ is the time domain impulse response of the filter, $F(\omega)$, and $\otimes$ is the convolution.

In what follows, we will do the analysis based on the so-called *quasi-static approximation*. This means that we are going to build the theory assuming that the input signal $v(t)$ is a constant. This will allow us to obtain exact analytical results. Later on, we will apply these analytical results as an approximation for the case of a slowly varying input signal $v(t)$. Since the input bandwidth is much lower than ω_1, this approximation turns out to be very accurate.

In this case the overall output signal $p(t)$ can be considered to be a stable square wave with a fixed angular frequency ω_1 and a fixed duty cycle α. If we choose the origin of the time axis as shown in Fig. 5.3, this can be described by the Fourier series:

$$p(t) = \left(\frac{2\alpha}{T} - 1\right) + 4 \times \mathrm{Re}\left\{\sum_{n=1}^{\infty} \frac{\sin\left(n\omega_1 \frac{\alpha}{2}\right)}{n\pi} e^{jn\omega_1 t}\right\} \tag{5.2}$$

The term $(\frac{2\alpha}{T} - 1)$ term in $p(t)$ will be referred to as u. If the input signal $v(t)$ is constant (as we are assuming for the moment), this term u is constant as well. Later on we will consider the case where $v(t)$ is varying very slowly and then $u(t)$ will also vary slowly over time. Hence, we will refer to $u(t)$ as the baseband component of $p(t)$. It includes the desired signal and its harmonic distortion components.

From the definition of the duty cycle α we immediately obtain:

$$u = \left(\frac{2\alpha}{T} - 1\right) \qquad \text{or,} \qquad \omega_1 \alpha = \pi(u+1) \tag{5.3}$$

By combining this with (5.2) and (5.1), the signal $e(t)$ can be written as:

$$e(t) = \left((v-u) \otimes f\right)(t) - 4\sum_{n=1}^{\infty}\left(\frac{\sin\left(n\omega_1\frac{\alpha}{2}\right)}{n\pi}\right) \times \tag{5.4}$$
$$\left[\mathrm{Re}\left\{F(n\omega_1)\right\}\cos(n\omega_1 t) - \mathrm{Im}\left\{F(n\omega_1)\right\}\sin(n\omega_1 t)\right]$$

Here, the term $\left((v-u) \otimes f\right)(t)$ corresponds to the low-frequency component of $e(t)$, and will be denoted as e_{lf}. In the case where the input signal is constant, e_{lf} is a constant as well.

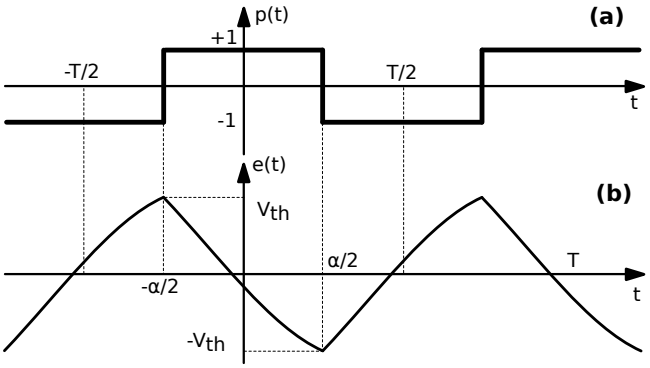


Figure 5.3: Typical waveforms for the ADSM in Fig. 5.2.

Fig. 5.3 shows typical waveforms of an ADSM. As the figure shows, the schmitt-trigger toggles when $e(t)$ reaches its positive or negative thresholds, V_{th} or $-V_{th}$. So if we evaluate $e(t)$ for $t = \frac{-\alpha}{2}$, we obtain:

$$V_{th} = e_{lf} - 4\sum_{n=1}^{\infty}\left(\frac{\sin\left(n\omega_1\frac{\alpha}{2}\right)}{n\pi}\right) \times \tag{5.5}$$
$$\left[\mathrm{Re}\left\{F(n\omega_1)\right\}\cos(n\omega_1\frac{\alpha}{2}) + \mathrm{Im}\left\{F(n\omega_1)\right\}\sin(n\omega_1\frac{\alpha}{2})\right]$$

and for $t = \frac{\alpha}{2}$ we will have:

$$-V_{th} = e_{lf} - 4\sum_{n=1}^{\infty}\left(\frac{\sin\left(n\omega_1\frac{\alpha}{2}\right)}{n\pi}\right)\times \tag{5.6}$$
$$\left[\mathrm{Re}\left\{F(n\omega_1)\right\}\cos(n\omega_1\frac{\alpha}{2}) - \mathrm{Im}\left\{F(n\omega_1)\right\}\sin(n\omega_1\frac{\alpha}{2})\right]$$

If we assume that e_{lf} is constant, the subtraction of (5.5) and (5.6) will result in:

$$\sum_{n=1}^{\infty}\frac{1}{n}\sin^2(n\omega_1\frac{\alpha}{2})\mathrm{Im}\left\{F(n\omega_1)\right\} = -\frac{\pi}{4}V_{th} \tag{5.7}$$

and the addition will give:

$$e_{lf} = \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{\mathrm{Re}\left\{F(n\omega_1)\right\}}{n}\sin\left(n\omega_1\alpha\right) \tag{5.8}$$

Solving (5.7) will give an expression for the oscillation frequency, ω_1, as a function of u. Afterwards, solving (5.8) will then give the baseband component of the output signal, u, as a function of the input signal, v.

In order to solve the series in (5.7) and (5.8), we should have an understanding about the loop filter. In most of the conventional filters that are generally used in ADSMs (like the ones used in the next section as examples or in [68], for example $1/(1+s\tau)$) for $\omega \geqslant \omega_1$ we have:

$$\mathrm{Re}\{F(\omega)\} \approx \frac{1}{(\tau_r\cdot\omega)^2} \tag{5.9}$$

and,

$$\mathrm{Im}\{F(\omega)\} \approx \frac{1}{\tau_i\cdot\omega} \tag{5.10}$$

where τ_r and τ_i are filter dependent constants. We will see that these assumptions are valid if the poles and zeros of the filter are much lower than ω_1. In this manner, the filter will have about 90° phase shift around the carrier frequency. The additional 90° phase shift required in the loop for the oscillation to take place, will be provided by the hysteresis of the schmitt-trigger.

Based on the assumption in (5.10), the series in (5.7) can be simplified using [72, p. 92, Eq. 4], which results in:

$$\omega_1 = \omega_c(1-u^2) \quad \text{with,} \quad \omega_c = \frac{\pi}{2\tau_i\cdot V_{th}} \tag{5.11}$$

In order to solve (5.8), we will first simplify it by substituting $\omega_1\alpha = \pi(u+1)$, according to (5.3). Then, considering the assumption of (5.9), the series in (5.8) can be evaluated using [72, p. 87, Eq. 4]:

$$\sum_{n=1}^{\infty} \frac{\mathrm{Re}\{F(n\omega_1)\}}{n} \sin(n\omega_1\alpha) = \frac{-\pi^3}{12} \frac{(u-u^3)}{(\tau_r \cdot \omega_1)^2} \tag{5.12}$$

Since ω_1 is also a function of u, in the right side of (5.12) we can substitute $\omega_1 = \omega_c(1-u^2)$ from (5.11). Now by inserting (5.12) in (5.8) we will have:

$$e_{lf} = \frac{2}{\pi}\left(\frac{-\pi^3}{12}\right) \frac{(u-u^3)}{(\tau_r \cdot \omega_c(1-u^2))^2} \tag{5.13}$$

and taking (5.9) into account, for ω_c, will give:

$$e_{lf} = -\frac{\pi^2}{6}\mathrm{Re}\{F(\omega_c)\}\frac{u}{1-u^2} \tag{5.14}$$

Untill now, we assumed that the signals $v(t)$, $u(t)$ and $e_{lf}(t)$ were constant. Now we will use the *quasi-static* approximation and assume that the results are also valid for the case where this signals are slowly varying. This leads to:

$$\left((u-v)\otimes f\right)(t) = \frac{\pi^2}{6}\mathrm{Re}\{F(\omega_c)\}\frac{u(t)}{1-u^2(t)} \tag{5.15}$$

Eq. (5.15) gives a very accurate relationship between the input signal, v, and the baseband output signal, u. Hence, in principle, all non-linearity effects of the modulator could be derived from this equation using numerical methods. After obtaining u from this equation, the instantaneous carrier frequency can also be accurately calculated using (5.11).

Eq. (5.15) also allows to make an important observation: if the real part of the loop filter transfer is zero, the modulation process does not generate in-band harmonic distortions. This occurs when the loop filter is an integrator. This was also already observed in [68] and hence in terms of modulation distortion, an integrating loop filter is the optimal choice.

Approximate Theory

In what follows we will further elaborate the results of (5.11) and (5.15) for the case where the input signal $v(t)$ is slowly varying. As a result the base-band component of the output signal $u(t)$ and the instantaneous oscillation angular frequency $\omega_1(t)$, will also vary slowly over time. However, not to overload the notation, in the following sections we will drop the explicit time dependence (t) for these signals.

Eq. (5.15) gives u as an accurate yet implicit function of v. Usually, we prefer to have an explicit analytical expression so that we don't need numerical methods to solve it. For this, we use Perturbation theory: first we make a rough and 1st order estimation of the output signal, u, then we use that estimation to simplify the equation, solve it again, and find a more accurate answer for u.

By observing that the term on the right hand of (5.15) is much smaller than the ones on the left hand, we obtain in a first approximation that $u \approx v$. Now, we can use this approximation to estimate the contribution of the right hand of (5.15) and we obtain the following improved approximation:

$$(u - v) \otimes f \approx \frac{\pi^2}{6} \mathrm{Re}\{F(\omega_c)\} \frac{v}{1 - v^2} \tag{5.16}$$

Eq. (5.11) also gives a very accurate expression for ω_1. But, since we prefer to have ω_1 as a function of the input signal v, rather than the output signal u, we can again use the approximation $u \approx v$, which gives the following simplified expression:

$$\omega_1 \approx \frac{\pi(1 - v^2)}{2\tau_i \cdot V_{th}} \tag{5.17}$$

Sinusoidal input signal

Now we will apply the approximate theory to the case where the input signal is a single tone, $v = A\sin(\mu t)$, to obtain the harmonic distortion components of the modulator. By assuming $v = A\sin(\mu t)$, the right side of (5.16) can be expanded using its Fourier series. Then we will have:

$$(u - v) \otimes f = \frac{\pi^2}{6} \mathrm{Re}\{F(\omega_c)\} \sum_{n=1}^{\infty} \mathrm{K}_n(A) \sin(n\mu t) \tag{5.18}$$

where $\mathrm{K}_n(A)$ comes from this Fourier integral:

$$\mathrm{K}_n(A) = \frac{\mu}{\pi} \int_{\frac{-\pi}{\mu}}^{\frac{\pi}{\mu}} \frac{A\sin(\mu t) \cdot \sin(n\mu t)}{1 - (A\sin(\mu t))^2} dt \tag{5.19}$$

It can be shown that the integral in $\mathrm{K}_n(A)$ is zero for even values of n. Therefore, according to (5.18), the Fourier expansion of u should also include only the odd harmonics of the input frequency, μ. So the Fourier expansion of u will be:

$$u = \sum_n a_n \cdot \sin(n\mu t - \theta_n), \quad n = 1, 3, 5, ... \tag{5.20}$$

By substituting (5.20) in (5.18), we obtain the phase θ_n and the amplitude a_n for each harmonic by matching the corresponding $\sin(n\mu t)$ terms from both sides of the equation. For the main tone, $n = 1$, since the terms on the right hand of (5.18) are much smaller than the main tones on the left, we can simply deduce that $a_1 \approx A$. For the harmonics we obtain:

$$\theta_n = \angle[F(n\mu)], \quad a_n \cdot |F(n\mu)| = \frac{\pi^2}{6} \mathrm{Re}\{F(\omega_c)\} \mathrm{K}_n(A) \tag{5.21}$$

and from that we can finally obtain the ratio of the magnitude of the nth harmonic over the main tone:

$$d_n = \frac{a_n}{a_1} \approx \frac{a_n}{A} = \frac{\pi^2}{6} \frac{\mathrm{K}_n(A)}{A} \frac{\mathrm{Re}\{F(\omega_c)\}}{|F(n\mu)|} \tag{5.22}$$

Eq. (5.19) for the K_n factors can also be calculated. E.g. for the 3rd and 5th harmonic this leads to (for $A \leq 1$):

$$\mathrm{K}_3(A) = \frac{2A^2 - 8}{-A^3} + \frac{6A^2 - 8}{A^3\sqrt{1 - A^2}} \tag{5.23}$$

$$\mathrm{K}_5(A) = \frac{2A^4 - 24A^2 + 32}{-A^5} + \frac{10A^4 - 40A^2 + 32}{A^5\sqrt{1 - A^2}} \tag{5.24}$$

By substituting (5.23) in (5.22), we obtain the 3rd order harmonic distortion of an ADSM:

$$d_3 = \frac{\pi^2}{6} \left(\frac{2A^2 - 8}{-A^4} + \frac{6A^2 - 8}{A^4\sqrt{1 - A^2}} \right) \frac{\mathrm{Re}\{F(\omega_c)\}}{|F(3\mu)|} \tag{5.25}$$

The average carrier frequency of the modulator, $\overline{\omega_1}$, can be accurately calculated by averaging (5.11). But it is easier to use the estimation in (5.17). For a sinusoidal input, $v = A\sin(\mu t)$, the average carrier frequency will be:

$$\overline{\omega_1} = \frac{\pi(1 - 0.5A^2)}{2\tau_i \cdot V_{th}} \tag{5.26}$$

Except for the accurate value of ω_1 in (5.11), the other approximations for ω_c, ω_1, and $\overline{\omega_1}$ in (5.11), (5.17), and (5.26) have been previously reported [68, 71, 73–75].

5.1.2 Simulation Results

To verify the proposed theory, the ADSM in Fig. 5.2 was simulated in Simulink for two cases, once with a 1st order passive loop filter and then with a 3rd order active one. The simulation results for the 3rd order harmonic distortion were also compared with a previous theory by Roza [68] which gave:

$$d_3[Roza] = \frac{\pi^2 A^2}{6} \frac{\mathrm{Re}\{F(\overline{\omega_1})\}}{F(\mu)} \tag{5.27}$$

Here, $d_3[Roza]$ comes from the series expansion of the output, $u \approx v + d_3 v^3$. This result is frequently misinterpreted as if $d_3[Roza]$ corresponds to the 3rd harmonic distortion component, this is incorrect because the cube of a sine wave equals:

$$\sin^3 x = \frac{1}{4}(3\sin x - \sin 3x) \tag{5.28}$$

This way, the correct 3rd harmonic distortion predicted by [68] equals $d_3[Roza]/4$, corresponding to a difference of 12 dB.

First order passive loop filter

As a first example, an ADSM with a 1st order passive loop filter, $F(s) = \frac{1}{1+s\tau}$, was evaluated. By mapping this to (5.9) and (5.10) we obtain $|\tau_i| = |\tau_r| = \tau$. We have chosen $\tau = 5\ ns$. To have a usable ADSM the threshold voltage V_{th} should be sufficiently small (otherwise the oscillation wouldn't begin), therefore it was set to $V_{th} = 0.1$ which corresponds to a (zero-input) self oscillation frequency, $f_c = \frac{\omega_c}{2\pi} = 500\ MHz$, according to (5.11). Different simulation setups were employed to examine different aspects of the theory.

In the first set of simulations, a DC signal has been applied to the input of the modulator. Both the DC level of the output and its carrier frequency have been evaluated. The output DC level has been compared both with the accurate theory of (5.15) and the approximate theory of (5.16). Take in mind that for DC signals we have $F(0) = 1$, and $\mathrm{Re}\{F(\omega_c)\}$ can be obtained by combining (5.9) and (5.11), so (5.15) will collapse to:

$$v = u - \frac{2V_{th}^2}{3}\left(\frac{u}{1-u^2}\right) \tag{5.29}$$

and by doing the same to (5.16) we will have:

$$u \approx v + \frac{2V_{th}^2}{3}\left(\frac{v}{1-v^2}\right) \tag{5.30}$$

As Fig. 5.4 (a) shows, there is a perfect match between the accurate theory in (5.29) and the simulation results. The curve corresponding to the approximate theory, (5.30), also has a good match and only a little deviation for higher input DC values. The same conclusion applies to Fig. 5.4 (b) where the carrier frequency has been compared with the accurate theory of (5.11) and the approximate theory of (5.17).

In the next set of simulations, a sinusoidal input with an amplitude of $A = 0.7$ is applied to the aforementioned modulator and the 3rd harmonic of the output is evaluated for a range of input frequencies. According to (5.26), with this input amplitude, an average carrier frequency of $\overline{\omega_1} \approx 377\ MHz$ is expected. Fig. 5.5 shows the corresponding simulation results. The plot also shows the proposed theory [Eq. (5.25)]. For comparison with [68], two curves have been added. The first corresponds to the incorrect interpretation of Roza's theory [i.e. use (5.27) for the 3rd harmonic distortion] and the other adds $-12\ dB$ to it to compensate for the $\frac{-1}{4}$ factor according to (5.28) and hence corresponds to a correct interpretation of Roza's theory. As this set of simulations confirms, the proposed theory predicts the distortion of an ADSM much more accurately than [68].

Fig. 5.6 illustrates the dependency of the (average) carrier frequency and the 3rd order harmonic distortion on the input amplitude, A, according to simulation and according to (5.26) and (5.25) for the case of an arbitrary input frequency of $\mu = 12.5\ MHz$ over a range of input amplitudes. Again the plot confirms a good match between the simulation and the theory.

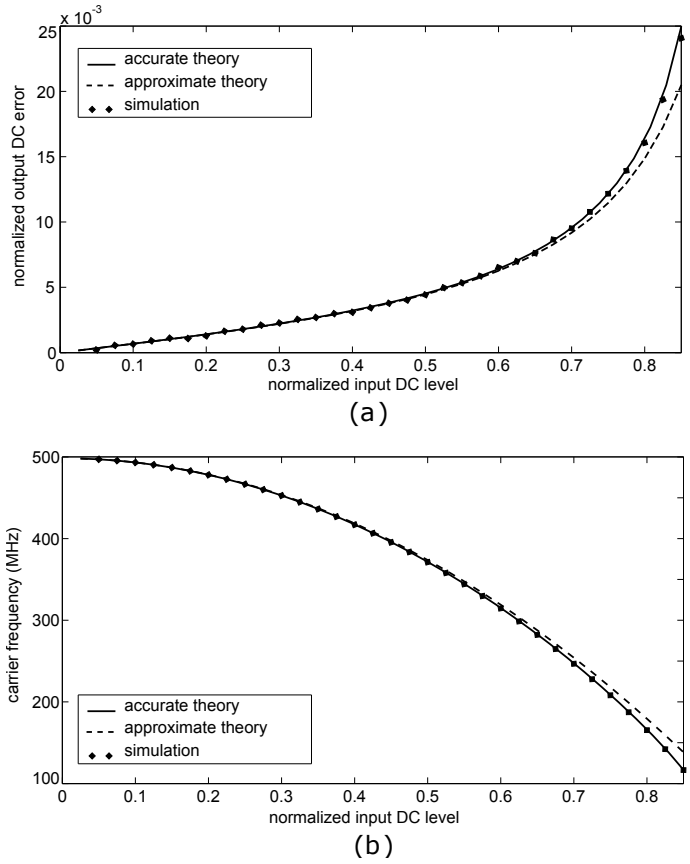


Figure 5.4: Comparison between simulation results and theory for a 1st order ADSM with a DC input:
a) the difference between the DC level of output and input signals,
b) and the carrier frequency.

Active loop filters

Many widely used active filters satisfy the conditions in (5.9) and (5.10), including the following family: $F(s) = \frac{\prod_{j=1}^{n-1}(1+s\tau_j)}{(s\tau_0)^n}$. In the second example, we will investigate the 3rd order case of $n = 3$, where we used the following ADSM parameters $\tau_0 = \tau_1 = \tau_2 = 5\ ns$ and $V_{th} = 0.1$. By mapping the given transfer function to (5.9) and (5.10) we will have $|\tau_i| = 5\ ns$ and $|\tau_r| = \frac{5\ ns}{\sqrt{2}}$. According to (5.11), these values correspond to a self oscillation frequency of $f_c = 500\ MHz$.

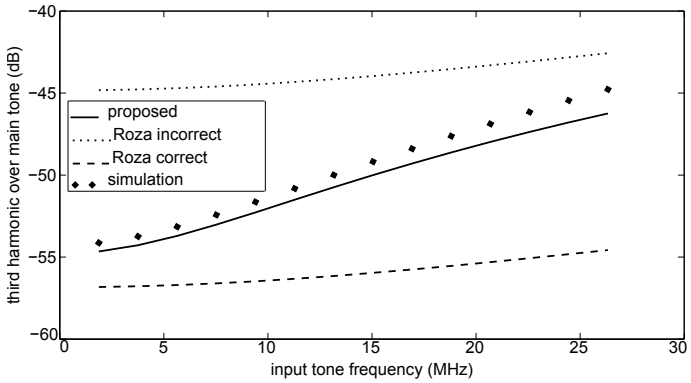


Figure 5.5: Comparison between simulation results and theory for an ADSM with a 1st order passive filter.

In the first set of simulations, the 3rd order harmonic distortion of the modulator has been compared with the proposed theory in (5.25) and [68]. The input has been given an arbitrary amplitude of $A = 0.7$ and the result has been drawn over a range of input frequencies. As in previous example, two curves have been drawn corresponding to the correct and incorrect interpretations of Roza's theory. As Fig. 5.7 shows, the proposed equation matches the simulation results almost perfectly and [68] (the curve tagged as "Roza correct") has an average error of more than 20 dB.

In the last set of simulations, for an arbitrary input frequency of $\mu = 12.5\ MHz$, the average carrier frequency and the 3rd order harmonic distortion were evaluated for varying input amplitudes and the results were compared with the proposed theory according to (5.26) and (5.25). Fig. 5.8 shows the corresponding results. Once again there is a good match between the simulation and theory.

5.1.3 Conclusion

In this section we have derived Eq. (5.25) to predict the 3rd harmonic distortion of an ADSM. The analytical results matched very well with simulations and showed considerable improvement over the prior art. The results of this work can be used in design and optimization of Schmitt trigger based ADSM's.

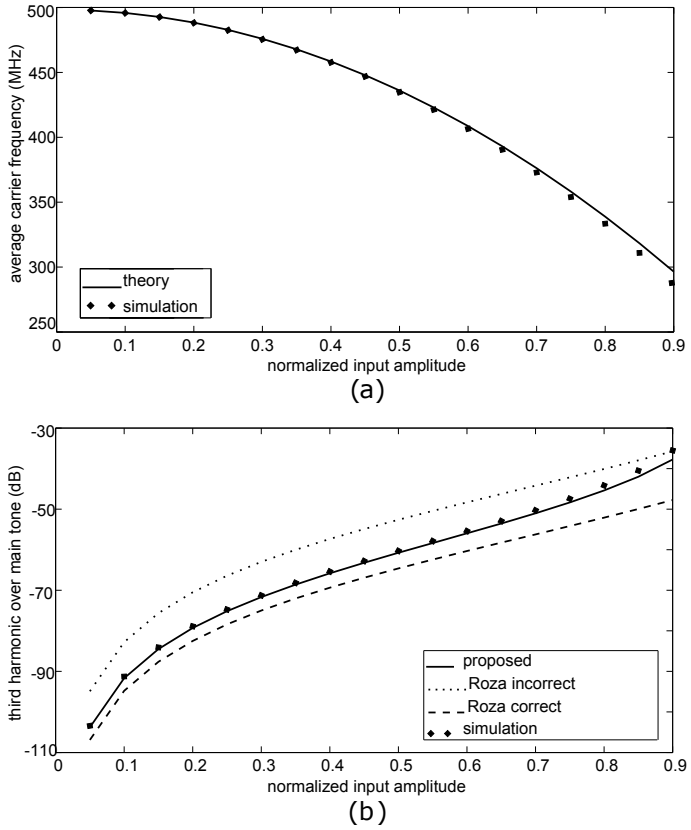


Figure 5.6: Average carrier frequency, $\overline{f_c}$, and the 3rd order distortion, d_3, of a 1st order ADSM as a function of its input amplitude A.

5.2 Analyzing ADSMs, with loop delay

In the previous section, exact expressions for the distortion in a commonly used family of Pulse Width Modulators (PWMs) known as Asynchronous Delta Sigma Modulators (ADSMs) were presented. Such an ADSM consists of a feedback loop with a schmitt-trigger (or a comparator), and a continuous time loop filter. However these previous results are not yet practically applicable because the effect of unavoidable loop delay (e.g. in the schmitt trigger) was not taken into account. Therefore we now present a more general theory that is also valid when there is a nonzero loop delay. A comparison of the resulting equations with computer simulations demonstrated a very good matching, confirming the validity of the theory.

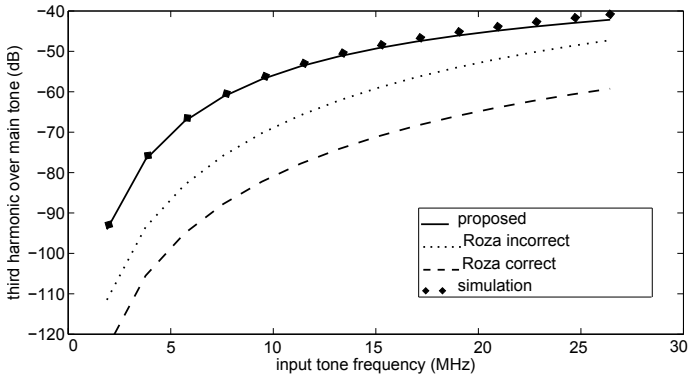


Figure 5.7: Comparison between simulation results and theory for the 3rd order harmonic distortion of a 3rd order ADSM over its input frequency.

This way, a designer can now easily understand the relationship between the loop filter dynamics and the linearity of an ADSM.

5.2.1 Previous theory and its limitations

According to [2] (i.e. the previous section), the third harmonic distortion of an ADSM, as in Fig.5.9 (a), with a loop-filter of F(ω) and an input voltage of $v = A\sin(\mu t)$ is (all voltages normalized to ± 1):

$$d_3 = \frac{\pi^2}{6}\left(\frac{2A^2-8}{-A^4} + \frac{6A^2-8}{A^4\sqrt{1-A^2}}\right)\frac{\mathrm{Re}\{F(\omega_c)\}}{|F(3\mu)|} \tag{5.31}$$

where ω_c is the self oscillation frequency of the PWM for $v = 0$ and d_3 is the amplitude of the third harmonic tone, $a_3\sin(3\mu t)$, over the amplitude of the main tone, $d_3 = \frac{a_3}{A}$.

This theory was obtained based on some assumptions. First, the highest order of s^i in the numerator of $F(s)$ should be exactly one degree less than the denominator to have a stable oscillation. Second, it assumes that all poles and zeros of the filter are at much lower frequency than ω_c, and finally, the filter should satisfy the following conditions for $\omega \geqslant \omega_c$:

$$\mathrm{Re}\{F(\omega)\} \approx \frac{1}{(\tau_r.\omega)^2} \quad \text{and,} \quad \mathrm{Im}\{F(\omega)\} \approx \frac{1}{\tau_i.\omega} \tag{5.32}$$

where τ_r and τ_i are filter dependent constants, the former could be real or imaginary and the latter could be positive or negative. Then, given a schmitt trigger threshold voltage of $\pm V_{th}$ we will have $\omega_c = \frac{\pi}{2\tau_i \cdot V_{th}}$.

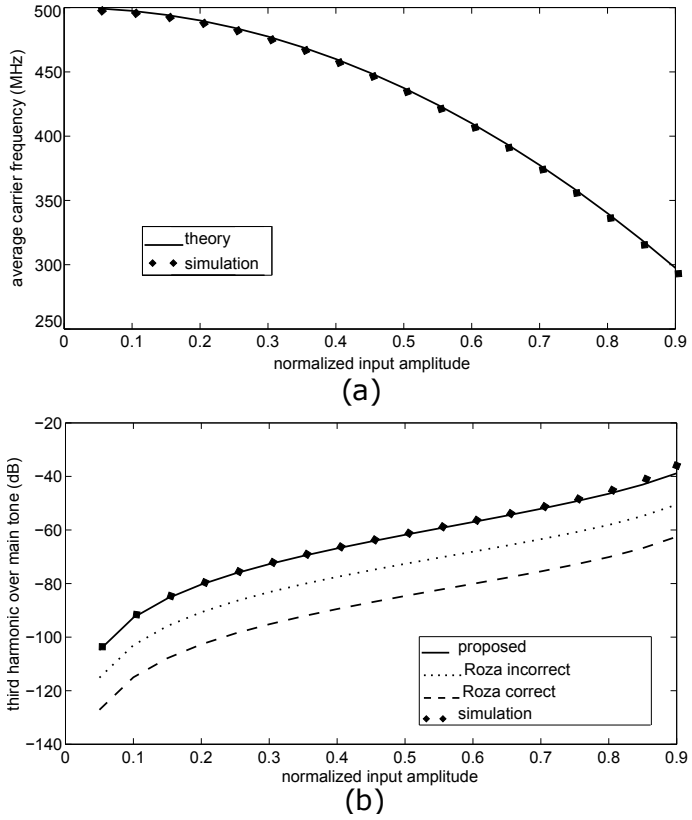


Figure 5.8: Average carrier frequency, $\overline{f_c}$, and 3rd order distortion, d_3, of a 3rd order ADSM vs. the input amplitude, A.

The theory in [2] only applies to a certain category of ADSMs where the schmitt trigger is ideal (has no delay). But in an actual circuit, the schmitt trigger always has a delay, modelled as T_D in Fig. 5.9 (b), and as the oscillation frequency of the PWM increases, the loop delay becomes more important in determining the oscillation frequency and the distortion.

In order to evaluate d_3 for the case with delay, the first solution that comes to mind is to merge the delay of the schmitt trigger in the loop-filter as a $e^{-T_D j\omega}$ factor and use (5.31) for calculating the third harmonic with the new loop-filter, $G(\omega) = F(\omega).e^{-T_D j\omega}$. But it can be easily shown that $\mathrm{Re}\{G(\omega)\}$ and $\mathrm{Im}\{G(\omega)\}$ will not satisfy the conditions in (5.32).

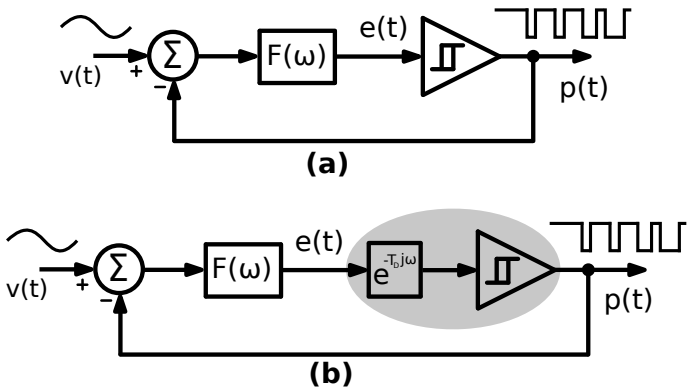


Figure 5.9: General representation of an ADSM,
(a) without extra delay in the loop,
(b) and with loop delay.

5.2.2 Proposed approach

Here we will revisit the equations in the previous section with similar assumptions while considering a delay of T_D for the schmitt trigger. Bare in mind that delay anywhere in the loop can be modelled this way without affecting the spectral qualities of the signals.

In Fig. 5.9 (b), $v(t)$ is a band limited input signal, $e(t)$ is the filtered error signal at the input of the schmitt-trigger, and $p(t)$ is the output square wave (± 1) with a pulse width of α and duration of T. As it will be shown later in this section, in this type of modulation, not only the duty cycle of the output square wave, $\frac{\alpha}{T}$, but also its carrier frequency are dependent on the input signal. The self oscillation frequency of this PWM for a zero input is called ω_c and $\omega_1 = \frac{2\pi}{T}$ is the (instantaneous) carrier frequency which is a function of the input signal, v. According to Fig. 5.9 (b) we can write the signal at e(t):

$$e(t) = ((v - p) \otimes f)(t) \tag{5.33}$$

where $f(t)$ is the time domain impulse response of the filter, $F(\omega)$, and $\otimes$ is the convolution.

Just as in section 5.1.1, we will use the quasi-static approximation and build the theory assuming that the input signal $v(t)$ is a constant. Then afterwards, we will adopt the results for the case of a slowly varying input signal $v(t)$. Then $p(t)$, which is a square wave, can again be described by

its Fourier series:

$$p(t) = \left(\frac{2\alpha}{T} - 1\right) + 4 \times \mathrm{Re}\left\{\sum_{n=1}^{\infty} \frac{\sin\left(n\omega_1 \frac{\alpha}{2}\right)}{n\pi} e^{jn\omega_1 t}\right\} \tag{5.34}$$

As before, the $\left(\frac{2\alpha}{T} - 1\right)$ term corresponds to the baseband component of $p(t)$ and will be referred to as u hereafter. For this, we can say: $u = \left(\frac{2\alpha}{T} - 1\right)$ or $\omega_1 \alpha = \pi(u + 1)$.
Similarly as before we can also consider the low-frequency component, e_{lf}, of the signal $e(t)$:

$$e_{lf} = \left((v - u) \otimes f\right)(t)$$

In the approximation that v is a constant, also u, e_{lf} and ω_1 will be constant.

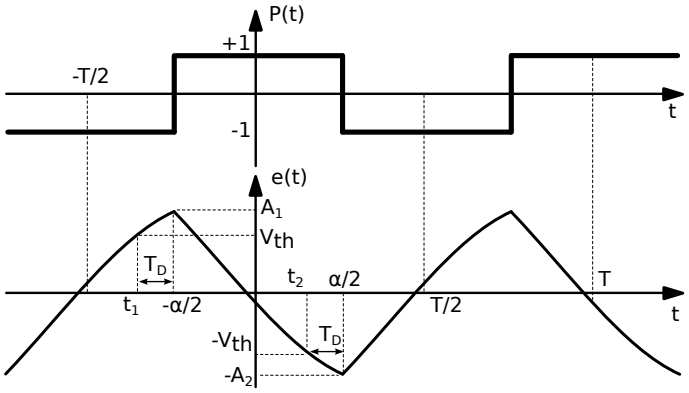


Figure 5.10: Typical waveforms of an schmitt trigger based ADSM with delay.

Fig. 5.10 shows typical waveforms of an ADSM. As the figure shows, the schmitt-trigger toggles with a delay of T_D after $e(t)$ reaches its positive or negative thresholds, V_{th} or $-V_{th}$. So if we use $t = \frac{\alpha}{2} - T_D$ and substitute (5.34) in (5.33), we obtain:

$$\begin{aligned} -V_{th} = e_{lf} - 4\sum_{n=1}^{\infty}\left(\frac{\sin\left(n\omega_1\frac{\alpha}{2}\right)}{n\pi}\right) \times \\ \left(\mathrm{Re}\left\{F(n\omega_1)\right\}\cos(n\omega_1(\frac{\alpha}{2} - T_D)) - \right. \\ \left. \mathrm{Im}\left\{F(n\omega_1)\right\}\sin(n\omega_1(\frac{\alpha}{2} - T_D))\right) \end{aligned} \tag{5.35}$$

and for $t = \frac{-\alpha}{2} - T_D$ we will have:

$$V_{th} = e_{lf} - 4\sum_{n=1}^{\infty}\left(\frac{\sin\left(n\omega_1\frac{\alpha}{2}\right)}{n\pi}\right)\times \tag{5.36}$$
$$\left(\mathrm{Re}\left\{F(n\omega_1)\right\}\cos(n\omega_1\frac{\alpha}{2} + n\omega_1 T_D) + \right.$$
$$\left.\mathrm{Im}\left\{F(n\omega_1)\right\}\sin(n\omega_1\frac{\alpha}{2} + n\omega_1 T_D)\right)$$

By adding the last two equations we will have:

$$0 = e_{lf} - 2\sum_{n=1}^{\infty}\frac{\sin(n\omega_1\alpha)}{n\pi}\times \tag{5.37}$$
$$(\mathrm{Im}\{F(n\omega_1)\}\sin n\omega_1 T_D + \mathrm{Re}\{F(n\omega_1)\}\cos n\omega_1 T_D)$$

and subtracting them will give:

$$\frac{-\pi V_{th}}{2} = \sum_{n=1}^{\infty}\frac{1-\cos(n\omega_1\alpha)}{n}\times \tag{5.38}$$
$$(\mathrm{Im}\{F(n\omega_1)\}\cos n\omega_1 T_D - \mathrm{Re}\{F(n\omega_1)\}\sin n\omega_1 T_D)$$

If the ADSM has a stable oscillation, then we can deduce from Fig.5.10 that $2T_D \leq \alpha + T_D \leq T = \frac{\omega_1}{2\pi}$ and from that we can say $0 \leq \omega_1\alpha \pm \omega_1 T_D \leq 2\pi$. The terms $\mathrm{Re}\{F(n\omega_1)\}$ and $\mathrm{Im}\{F(n\omega_1)\}$ are obtained from (5.32). This allows us to solve the series in (5.38) using [72]. Then (5.38) will result in:

$$\omega_1 = \omega_c\cdot(1-u^2) = \frac{\pi(\tau_i T_D - \tau_r^2)\cdot(1-u^2)}{2\tau_r^2\tau_i V_{th} + \tau_i T_D^2 - 2\tau_r^2 T_D} \tag{5.39}$$

This equation accurately gives the instantaneous and self oscillation frequencies, ω_1 and ω_c, as functions of the output base band signal, u, and the parameters of the modulator.

Same as above, we can calculate the series in (5.37) using (5.32), (5.39), [72], and the fact that $0 \leq \omega_1\alpha \pm \omega_1 T_D \leq 2\pi$. With that all, we can simplify (5.37) which will give:

$$-e_{lf} = \frac{\pi^2 u}{6(\tau_r\omega_c)^2(1-u^2)} - \frac{uT_D^2}{2\tau_r^2} + \frac{uT_D}{\tau_i} \tag{5.40}$$

Again, the result above was obtained for the case of a constant input signal $v(t)$. Just as before we will now apply it to the case of slowly varying

input signals. Then also u, e_{lf} and ω_1 will become time dependent. This leads to:

$$(u - v) \otimes f = \frac{\pi^2 u}{6(\tau_r \omega_c)^2(1 - u^2)} - \frac{uT_D^2}{2\tau_r^2} + \frac{uT_D}{\tau_i} \tag{5.41}$$

As before, the explicit time dependencies where dropped in order not to overload the notation. This equation gives an accurate relationship between the input signal, v, and the output baseband signal, u. In order to avoid the need to solve an implicit equation to obtain u as a function of v, we can simplify (5.41) using Perturbation Theory. So at first we make a rough first order estimation from (5.41). We can see that the terms on the right side of the equation are much smaller than the ones on the left, so we can say $u \approx v$. By applying this estimation to (5.41) we will obtain this simplified equation which gives u as an explicit function of v:

$$(u - v) \otimes f \approx \frac{\pi^2 v}{6(\tau_r \omega_c)^2(1 - v^2)} - \frac{vT_D^2}{2\tau_r^2} + \frac{vT_D}{\tau_i} \tag{5.42}$$

Now we will apply a sinusoidal input voltage, $v = A \sin \mu t$, to (5.42) to obtain the harmonic distortions of the ADSM. We can see that the right hand of this equation is an odd function of v, so we can expect u to only have odd harmonics of v. Therefore, we can replace u with its Fourier expansion:

$$u = \sum_n a_n \sin(n\mu t - \theta_n), \quad n = 1, 3, 5, ... \tag{5.43}$$

Since the terms on the right hand of (5.42) are much smaller than those on the left, for the main tone we can say $a_1 \approx A$. In the right hand of (5.42), only the first term can produce harmonic distortion. So if we write the Fourier expansion on both sides of (5.42) only for the harmonic tones ($n = 3, 5, ...$) we will have:

$$\sum_n a_n \sin(n\mu t - \theta_n) \otimes f \approx \frac{\pi^2}{6\tau_r^2 \omega_c^2} \sum_n \mathrm{K}_n(A) \sin(n\mu t) \tag{5.44}$$

where K_n comes from this Fourier integral:

$$\mathrm{K}_n(A) = \frac{\mu}{\pi} \int_{\frac{-\pi}{\mu}}^{\frac{\pi}{\mu}} \frac{A \sin(\mu t).\sin(n\mu t)}{1 - (A \sin(\mu t))^2} dt \tag{5.45}$$

and from (5.44) we can deduce for each harmonic that:

$$\theta_n = \angle[F(n\mu)], \qquad a_n \cdot |F(n\mu)| = \frac{\pi^2}{6\tau_r^2\omega_c^2}\mathrm{K}_n(A) \tag{5.46}$$

and by considering (5.32) for ω_c, we can find the ratio of the magnitude of the nth harmonic over the main tone:

$$d_n = \frac{a_n}{a_1} \approx \frac{a_n}{A} = \frac{\pi^2}{6}\frac{\mathrm{K}_n(A)}{A}\frac{\mathrm{Re}\{F(\omega_c)\}}{|F(n\mu)|} \tag{5.47}$$

The integral in (5.45) can be solved for any of the harmonics. For $n = 3, 5$, for example, it gives (for $A \leq 1$):

$$\mathrm{K}_3(A) = \frac{2A^2-8}{-A^3} + \frac{6A^2-8}{A^3\sqrt{1-A^2}} \tag{5.48}$$

$$\mathrm{K}_5(A) = \frac{2A^4-24A^2+32}{-A^5} + \frac{10A^4-40A^2+16}{A^5\sqrt{1-A^2}} \tag{5.49}$$

By substituting (5.48) in (5.47) we can find the 3rd harmonic distortion of an ADSM with loop delay:

$$d_3 = \frac{\pi^2}{6}\left(\frac{2A^2-8}{-A^4} + \frac{6A^2-8}{A^4\sqrt{1-A^2}}\right)\frac{\mathrm{Re}\{F(\omega_c)\}}{|F(3\mu)|} \tag{5.50}$$

and the term $\mathrm{Re}\{F(\omega_c)\}$ can be calculated using (5.39) and (5.32):

$$d_3 = \frac{1}{6}\left(\frac{2A^2-8}{-A^4} + \frac{6A^2-8}{A^4\sqrt{1-A^2}}\right)\frac{1}{|F(3\mu)|} \times \frac{(2\tau_r^2\tau_i V_{th} + \tau_i T_D^2 - 2\tau_r^2 T_D)^2}{\tau_r^2(\tau_i T_D - \tau_r^2)^2} \tag{5.51}$$

In ADSMs without loop delay (assuming that a high order aggressive loop filter is not chosen) the signal at the input of the schmitt trigger is limited to $\pm V_{th}$, e.g. Fig. 5.11(a). After introducing delay to the loop, a certain amplitude modulation effect occurs, Fig.5.11(b). The (above) envelope of this effect can be calculated by evaluating $e(t = \frac{-\alpha}{2})$, see Fig. (5.10). By replacing (5.34) in (5.33) and calculating the series we will have:

$$e(\frac{-\alpha}{2}) = uT_D(\frac{T_D}{2\tau_r^2} - \frac{1}{\tau_i}) - \frac{T_D}{\tau_i} + \frac{\tau_r^2 V_{th} - 0.5T_D^2}{\tau_r^2 - \tau_i T_D} \tag{5.52}$$

5.2.3 Implications and Results

ADSM equivalency

A surprising outcome is that (5.31) and (5.50) are the same and that implies that an ADSM with a schmitt trigger threshold voltage of V_{th} and loop delay of T_D is equivalent (regarding its distortion) with another ADSM that has an identical loop filter and identical oscillation frequency with a threshold voltage of $V_{th,eq}$ and zero delay where $V_{th,eq}$ can be calculated using (5.51) by solving $d_3(V_{th}, T_D) = d_3(V_{th,eq}, 0)$. This value of equivalent threshold happens to be equal to $e(\frac{-\alpha}{2})|_{u=0}$ in (5.52).

Amplitude modulation

In previous works, the amplitude modulation discussed before (5.52) was believed to be a source of distortion. In [74] a method was presented to cancel out this effect through an active feedback. The threshold voltage of the schmitt trigger was dynamically reduced to keep the envelope of the signal at the input of the schmitt trigger constant and equal with the desired threshold voltage. In this way, the modulator's waveform and behaviour will be similar to one without delay. This method is only applicable when the schmitt trigger is implemented using op-amp and resistors. However, as it has been shown in this work, the distortion in an ADSM with delay is the same as an equivalent one without delay and there is no need for extra circuitry to compensate it, it is enough to choose a schmitt trigger with a lower threshold voltage from the very beginning.

An ADSM with a comparator and loop delay

The theory presented in this work applies to ADSMs that use a schmitt trigger (with/without delay) as their non-linear element. But the theory is still valid for the case that the threshold voltage of the schmitt trigger is zero and the loop delay is non-zero. In other words, it is possible to use (5.51) to design an ADSM with a comparator and some delay blocks (like digital buffers) which may be designed easier in comparison with a schmitt trigger.

5.2.4 Simulation results

In this section, we will describe a few simulations to confirm the proposed theory. In all cases, for every ADSM with loop delay, an equivalent ADSM

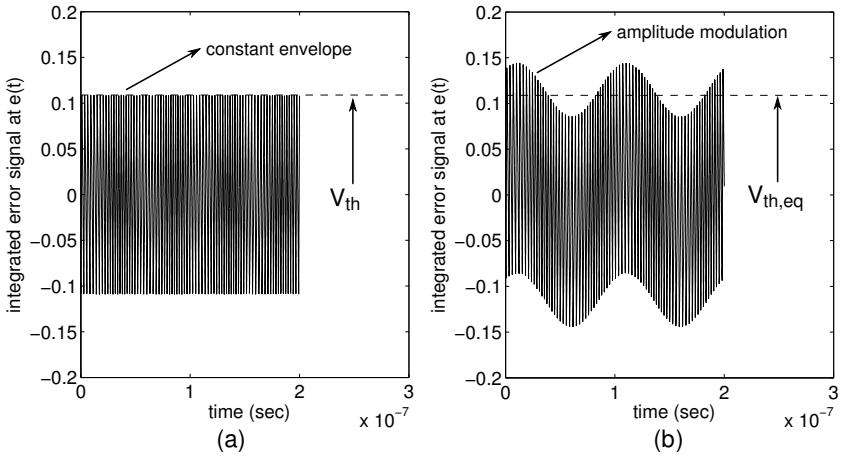


Figure 5.11: typical waveforms of two ADSMs,
a) without any delay in the loop,
b) and with loop delay.

without delay (with similar loop filter but higher threshold voltage according to section 5.2.3) has been simulated. Then the simulation results of these two ADSMs are compared with the proposed theory.

Output spectrum, first order loop filter

In the first set of simulations, we will take a look at the output spectrum of two equivalent ADSMs. The schematic of the two ADSMs is according to Fig. 5.9(a) and (b). They both have a first order passive loop filter, $F(s) = \frac{1}{1+\tau s}$, with $\tau = 5\ ns$. For the ADSM with delay, we have chosen $T_D = 150\ ps$ and $V_{th} = 0.1$. Therefore, according to section 5.2.3, the equivalent delay-less ADSM should have a threshold voltage of $V_{th,eq} = 0.1266$.

Fig. 5.12(a) and (b) show the output spectrum of these two ADSMs. According to [2] and (5.39) the average carrier frequency of an ADSM for a sinusoidal input voltage with an amplitude of A is $\overline{\omega_1} = \omega_c(1 - 0.5A^2)$. For these cases $A = 0.25$ was chosen, so $f_1 = 380.5\ MHz$ is expected and according to (5.51), the predicted third harmonic distortion is $d_3 = 74.9\ dB$. As the figure shows, there is good match between the two equivalent ADSMs and the proposed theory.

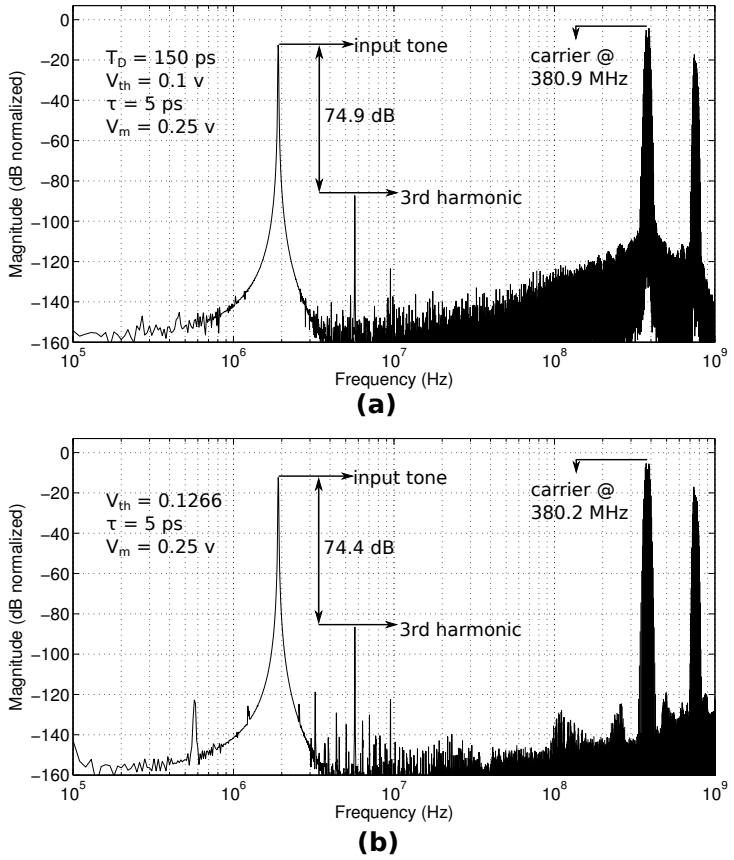


Figure 5.12: Output spectrum of two equivalent ADSMs with first order loop filter,
(a) with some delay in the loop,
(b) and without loop delay.

A second order ADSM with comparator and loop delay

In section 5.2.3 we argued that an ADSM that has a comparator as its non-linear element (instead of a schmitt trigger) and some delay in its loop can be equivalent with a delay-less ADSM with schmitt trigger.

In order to verify this argument, for this example we have chosen a second order loop filter, $F(s) = \frac{1+s\tau_1}{s\tau_2 \cdot s\tau_3}$, with $\tau_1 = \tau_2 = \tau_3 = 5\ ns$. The first modulator uses a comparator in its loop ($V_{th} = 0$) and has a delay of $T_D = 600\ ps$. According to section 5.2.3, this modulator should be

equivalent with another ADSM that uses a schmitt trigger with a threshold voltage of $V_{th,eq} = 0.1264$ and no delay, $T_D = 0$. According to (5.39) these values correspond to a self oscillation (zero input) carrier frequency of $f_c = 390\ MHz$

In Fig. 5.13(a) these two ADSMs have been compared with the theory in (5.51). A sinusoidal voltage with a frequency of $\mu = 9.75\ MHz$ has been applied to the input of both modulators and their third harmonic distortion d_3 has been evaluated over a range of input amplitudes. As the figure verifies, the two ADSMs are actually equivalent regarding their distortion and they both match well with the proposed theory in (5.51). A similar set of simulations have been carried out in Fig. 5.13(b) where the same ADSMs have been applied a sinusoidal signal as their input voltage. This time the amplitude of the input is constant, $A = 0.5$, and the frequency is swept. Once again a good match between the two modulators and theory can be seen.

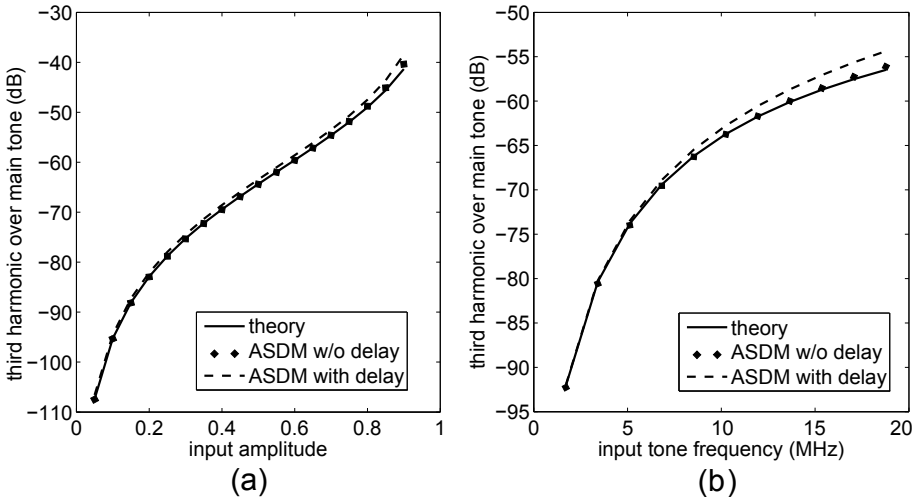


Figure 5.13: Comparing the distortion of two equivalent second order ADSMs with theory.

5.2.5 Conclusion

We have derived Eq. (5.51) to predict the 3rd harmonic distortion of an ADSM with loop delay. We have also argued that an ADSM with loop delay is equivalent with a similar ADSM that has no delay, but a higher

threshold voltage in its schmitt trigger. The simulation results matched very well with the analytical results and verified this equivalency.

From a designer's point of view, the main conclusion is that the distortion is essentially determined by the loop filter in combination with the self oscillation frequency. The delay in the loop affects the self oscillation frequency, but if the delay is known, this effect can be counter-acted by tuning the schmitt trigger's threshold voltage and choosing a lower V_{th}.

From another perspective, for a given loop filter, better linearity can be obtained by increasing the oscillation frequency, f_c, which can be realized by decreasing the delay or lowering the threshold voltage of the schmitt trigger (even as low as zero). The price of this approach is of course higher switching activity and power consumption.

In practice, all of the relevant requirements can be optimized using the explicit equations that have been presented in this chapter.

5.3 Implementation and measurement

In this section we present a very simple ADSM design for linearization of VCO ADC's. The circuit only consists of a passive feedback filter and a schmitt trigger. By proper sizing, the nonlinearity error can be reduced to well below 0.12 % for input signals that go almost rail-to-rail.

The design has been manufactured in the low power version of TSMC 65 nm technology and was measured at a 1 V power supply.

5.3.1 Passive ADSM

The structure of the passive ADSM, is shown in Fig. 5.14.a. The key element is that the linear loop filter $F(j\omega)$ should be passive. A potential implementation is shown in Fig. 5.14.b. Here, the linear loop filter $F(j\omega)$ equals $F(j\omega) = 1/[2(1 + j\omega\tau)]$ with $\tau = RC/2$.

The input signal V in the diagram of Fig. 5.14.a is symmetrical around 0 and is also normalized toward the full scale amplitude. Hence, the input signal V_{in} of the circuit of Fig. 5.14.b is related to the signal V in Fig. 5.14.a by the following relationship: $V = 2V_{in}/V_{dd} - 1$

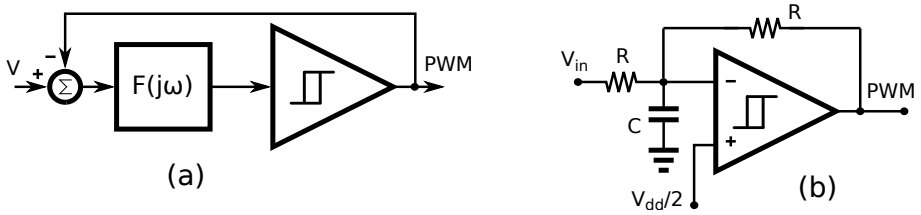


Figure 5.14: (a) block diagram of a Passive ADSM, (b) and its circuit.

By proper sizing of the Schmitt Trigger's delay and/or hysteresis width, the ADSM can be forced to oscillate at a desired oscillation frequency $f_P = \omega_P/(2\pi)$. This oscillation frequency should always be sufficiently higher than the relevant system bandwidth.

To obtain good performance both τ and ω_P should be carefully chosen. A first consideration is the nonlinear distortion, for which expressions were derived in the past sections of this chapter. A complication here, is that this distortion depends on the gain of the filter F and hence might vary over the signal band. However, the problem can be greatly simplified by

observing that the input referred noise of the Schmitt Trigger is also inversely proportional to the gain of the filter F. This means that the effect of comparator noise spectral components that are above the filter cut off frequency $(1/(2\pi\tau))$ will be significantly increased. Since this is not tolerable in the usefull signal band, this implies that the filter cut off frequency should not be smaller than the usefull signal bandwidth. When we take this into account, the filter F must have a flat gain over the signal band and the expressions of previous sections (in this chapter) are significantly simplified. In particular the expression for the signal band component PWM_{LF} of the PWM signal simplifies into:

$$PWM_{LF} \approx v - \frac{\pi^2}{6} \frac{v}{1-v^2} \frac{1}{1+(\tau\ \omega_P)^2} \tag{5.53}$$

For the case that the input signal is a sine, the expression for the distortion eq. 5.25 (dominated by the 3rd harmonic) becomes:

$$THD \approx -20 \log \left(\frac{\pi^2}{6A^4(1+(\tau\ \omega_P)^2)} \left(2A^2 - 8 - \frac{6A^2-8}{\sqrt{1-A^2}} \right) \right) \tag{5.54}$$

From this equation, it is clear that the ADSM performance is a strong function of the desired input range and of the ADSM oscillation frequency ω_P. Based on these considerations, we come to the following design flow. First, size the filter time constant τ such that it corresponds to the desired signal bandwidth. Second, decide the input signal range. And third, decide the desired self-oscillation frequency based on the nonlinearity by evaluating Eq. (5.54). In the circuit that we implemented, we aimed for a 10MHz bandwidth, and a usefull signal range of 750mV$_{pp}$ at a 1V supply voltage. Then we need an oscillation frequency of about 300 MHz to achieve a distortion performance of 65dB.

5.3.2 Circuit design

We implemented a differential version of the conceptual circuit of Fig. 5.14. If we assume that the circuit's delay is negligible, the Schmitt Trigger hysteresis width should be as low as 46 mV (differentially), to achieve an oscillation frequency of 300 MHz at a 1 V supply voltage and a filter bandwidth of 10 MHz. To obtain such a low hysteresis width in a controlled way, we added two pre-amplifier stages with a controlled gain to the actual Schmitt Trigger (as shown in Fig. 5.15.a). The pre amplifier schematic is

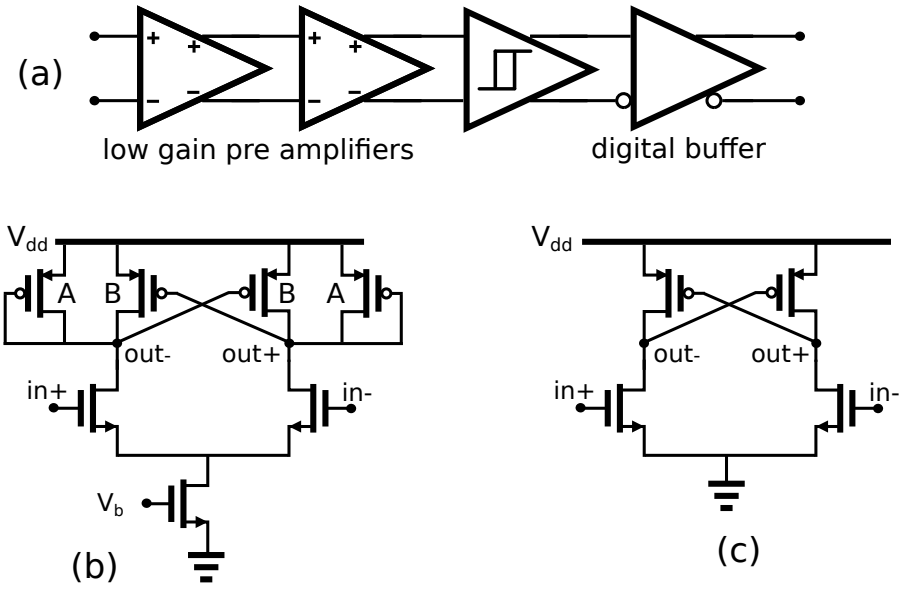


Figure 5.15: (a) Overall Schmitt Trigger structure,
(b) schematic of the Pre amplifier, which (apart from the sizing) is identical to the Schmitt Trigger's schematic,
(c) and the digital buffer circuit.

shown in Fig. 5.15.b. It consists of a simple NMOS differential pair with a combination of diode-connected and cross-coupled PMOS load transistors. Here, the weight A of the diode-connected PMOS is larger than the the weight B of the cross-coupled PMOS. The ratio A/B then sets the gain. The actual Schmitt trigger schematic is identical to Fig. 5.15.b, except that now the weight B of the cross-coupled PMOS is larger than the weight A of the diode-connected PMOS load transistors. In this case, the ratio A/B sets the hysteresis width. Finally a digital buffer (Fig. 5.15.c) is added to drive the resistors. All these stages consist of maximum three stacked transistors, and hence are suitable for low voltage designs.

After the first design iteration, it turned out that the circuit's delay (mostly due to the schmitt trigger) was not negligible and resulted in too low an oscillation frequency. It was also shown in previous section that loop delay will not ruin the performance of the ADSM, as long as it is (roughly) estimated, taken into account, and eventually compensated by choosing a hysteresis width of the schmitt trigger. In this case the actual circuit was

implemented with a lower hysteresis width of 20 mV and a delay of about 0.4 ns.

Two level ring VCO

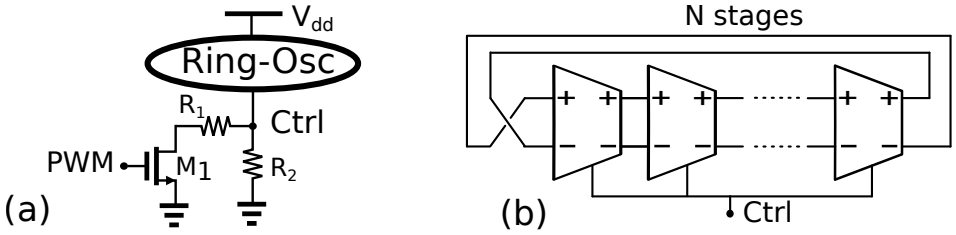


Figure 5.16: (a) input circuit of a Two-level Ring oscillator, (b) and the actual ring.

The VCO only has to operate at the two PWM levels. This is implemented by the circuit of Fig. 5.16a. The two-level PWM signal drives a switch, M_1 in series with a resistor, R_1. The two resistors, R_1 and R_2, allow to control the two frequencies at which the VCO will oscillate. For the actual ring, any form of current starved Ring Oscillator (see Fig. 5.16(b)) could be used. In this work we used a design with the same delay cell as in chapter 4. By turning the transistor M_1 off and on, the VCO oscillates at a low frequency, f_1 and a high frequency f_2 respectively. The average of the two, and their difference, determine the carrier frequency f_c and tuning range f_{tune} of the VCO. In theory, the best VCO ADC performance is achieved by setting the f_1 equal to zero [20]. However, it was found that this extreme gives additional switching noise [30]. Therefore in this work we set f_1 to approximately half f_2.

If the ADSM is implemented differentially, the two ADSM outputs can drive two pseudo differential VCOs. But unlike [6], the proposed technique is also effective in the single-ended configuration of Fig. 5.14.

5.3.3 Measurement Results

The proposed circuit was implemented for a 1 V supply in the low power (high threshold) flavour of a 65nm CMOS technology (on a die with other test circuitry). The ADSM was sized with a filter bandwith of 10 MHz and an oscillation frequency of 300 MHz. The VCO was a RO (Fig. 5.16) with 18 stages. In the input network, the resistor R_2 was sized 2 Kohm

and the series connection of R_1 and M_1 was sized for the same value. The corresponding 2 VCO frequencies are around 350 MHz and 175 MHz. The test chip was actually differential (i.e. a fully differential ADSM with 2 VCO's in a pseudo differential configuration). However, due to limitations on the test chip the output of only 1 of the VCOs was accessible. Moreover of this single VCO, only one of the 18 phases was accessible. Due to this, the measurement results are read out single-ended and are also reported as a single-ended measurement. For quantitative evaluation, the available VCO output signal was sampled with a 10 GS/s sampling oscilloscope, converted into a bitstream and differentiated digitally. This way, we obtain a configuration that is similar to an actual (single-ended) linearized VCO-ADC with first order noise shaping (only with reduced performance because we are only using 1 out of the 18 phases) [20]. With this set-up, the proposed ADSM is measured together with the VCO, and hence, both the linearity of the PWM can be determined, and the effectiveness of this linearisation method.

In a first experiment, the (static) voltage to frequency conversion curve of the ADSM-VCO was measured and is shown in Fig. 5.17(left) Bear in mind that in reality the VCO is switching between two frequencies (around 175 MHz and 350 MHz) and the plot actually shows the average frequency of the VCO (averaged over a long time). Clearly, the curve is visually linear. The deviation of this curve from a best fit line (the nonlinearity error) is shown in Fig. 5.17(right), where also the prediction of the nonlinearity according to Eq. (5.53) is shown. It is clear that the measured curve resembles the prediction. However, some even distortion is visible. This is attributed to unequal rise and fall times in the PWM signal, and would probably disappear in a fully differential setup. Still, over a near rail-to-rail signal range (50 mV-950 mV) the nonlinearity is well within ± 0.2 MHz, corresponding to 0.12 % of the full scale (of 175 MHz).

In another measurement, the circuit was driven with a 550 mV_{pp}, 100 kHz input sine wave. The corresponding output spectrum is shown in Fig. 5.18. This is about -5 dB below the absolute maximum signal level which whould be 1 V_{pp}. The dominant harmonic is the third at -63 dBc, which is adequate for several applications. The high frequency noise roll off of 6 dB/octave corresponds to the expected first order noise shaping. In this measurement, this noise contribution already dominates above a few MHz, but as explained above, this is due to the fact that only 1 of the 18 VCO phases is used here. Finally, there is a white noise floor (related to circuit's thermal

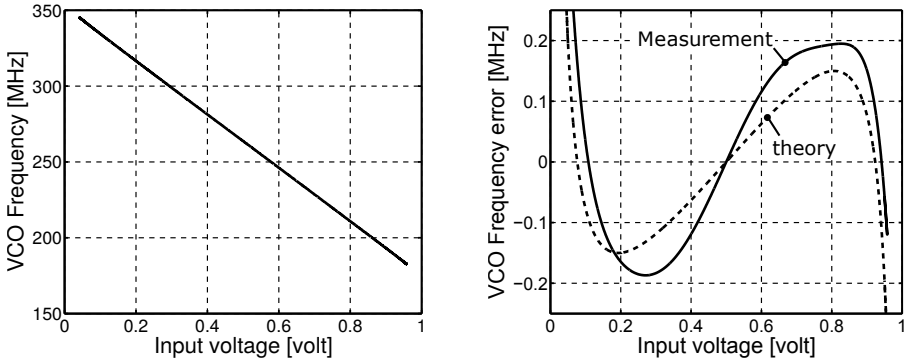


Figure 5.17: I/O and nonlinearity plots. (Theory from Eq. 5.53)

noise). For this case, the SNR and SNDR over a bandwidth of 2 MHz were equal to 69 dB and 61 dB respectively.

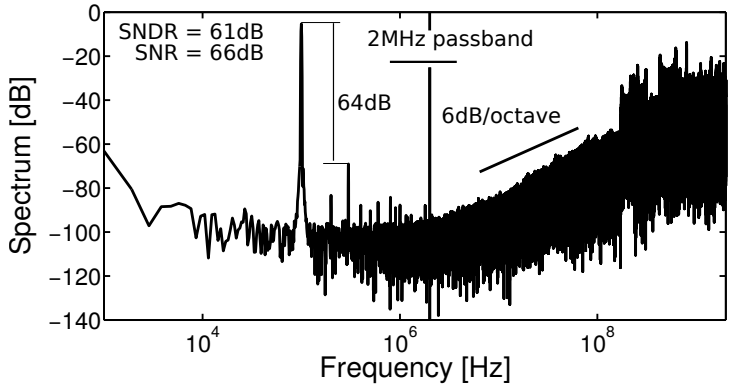


Figure 5.18: Output spectrum of the linearized VCO for a 550 mV_{pp} 100 kHz input signal.

The measurement of Fig. 5.18 was repeated for a range of input amplitudes and based on that a SNR-SNDR plot was drawn, for the case of a bandwidth of 2 MHz. The theoretical prediction of the SNDR based on the expression for the distortion of Eq. 5.54 is shown as well. It is clear that the circuit is only limited by the inherent ADSM distortion only at very high signal levels.

The entire (fully differential) ADSM consumes only 240 μW. The power consumption of 1 VCO channel is 500 μW. Hence, in a fully differential configuration the power overhead of the ADSM is modest. On the other

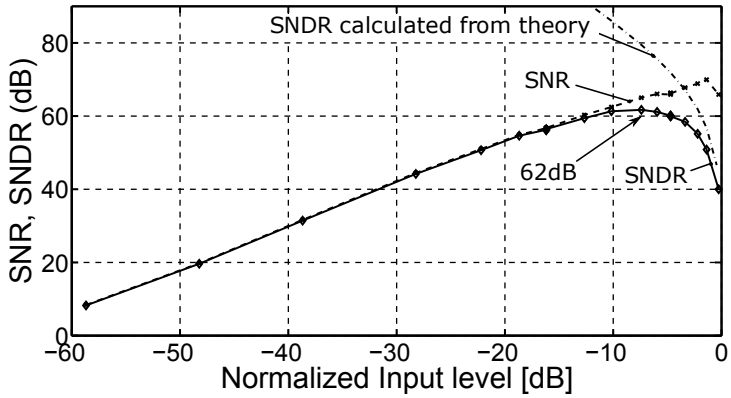


Figure 5.19: SNR and SNDR vs. the normalized rail to rail input level (of 1 Vpp). (Theory in Eq. 5.54)

hand there is a noise penalty (e.g. compared to [6], which comes from two sources: first the ADSM adds noise, and second the VCO full swing is reduced. The silicon area occupied by the PWM is 50 $\mu m \times 130$ μm and 60 $\mu m \times 25$ μm for a single VCO channel.

5.3.4 Conclusion

Presented was the design of a passive ADSM to linearize VCO ADC's. The key elements are a suitable selection of the filter time constant and the oscillation frequency. The approach is illustrated by a prototype design in 65 nm CMOS which demonstrates a nonlinearity error which is below 0.12 % for a near rail-to-rail input signal.

Chapter 6

Design and implementation of a mostly digital VCO-based CT-DSM with 3rd order noise shaping

In this chapter a circuit level implementation for the system presented in Fig. 3.9(a) is proposed. The proposed circuitry includes no traditional analog building blocks, like highly linear transconductance or op-amp. This novel scheme can potentially take advantage of technology scaling, is operational under low supply voltages, and requires a much smaller silicon area, compared to its conventional CT-DSM counterparts.

As a proof of concept, for the first time a 3rd order VCO-based CT-DSM is implemented in the low power version of a 65nm technology for a 10 MHz bandwidth. This prototype shows a measured performance of 71/66.2/62.5 dB DR/SNR/SNDR at a 10 MHz bandwidth while consuming 1.8 mW from a 1.0 V analog and 1.9 mW from a 1.2 V digital supply. With digital calibration, the nonlinearity could be pushed below the noise level, leading to an improved peak SNDR of 66 dB. The modulator covers a small silicon area of only $0.01; mm^2$.

6.1 Simplified Implementation

Many circuit level implementations can be developed for the noise shaping system presented in Fig. 3.9(a). In this section we will impose several restrictions which will enable a very efficient circuit implementation. In doing so, we sacrifice design freedom at the system level. In our implementation, one of the main parameters that we'll put a limit on is the gain and carrier frequency of the oscillators. As will become clear later on, lowering the VCO gain will limit the quantization noise shaping performance of the system, but as we will show, the resulting structure still has adequate performance.

6.1.1 Implementation for a Single phase VCO

As most VCO-ADCs, our design is based on a ring oscillator VCO, which provides multiple phase-shifted versions of its output. We will also use these multiple output phases, but for easier understanding, we will first explain our implementation for the case of a VCO with only 1 output phase.

To simplify the system, we first set the parameters f_{c2} and f_{c3} in Fig. 3.9(a) equal to zero. This will ensure that the output values of the first and second up-down counter (which drive DCO_2 and DCO_3) are always positive integers. Assuming that k_{d2} and k_{d3} are also positive, this can be understood by observing that the output frequency of the DCOs can only assume positive values. Moreover, by inspection of Fig. 3.9 we can conclude that the output of the modulator, D_{out} will be a digitized version of the first VCO's instantaneous frequency f_1 divided by f_s and hence cannot be negative. So, D_{out} and as a result also the output of the last up-down counter will also be non-negative.

To further simplify the system, we will assume, for the moment, that f_c is much smaller than f_s. This will ensure that D_{out} (the digitized value of f_1/f_s) can only have the instantaneous values of 0 and 1. Moreover, under this assumption, also the first counter can only take the instantaneous values of 0 or 1. This can be understood from the following reasoning: let us assume that the loop starts in a 'rest' state: i.e. the output $D_{out} = 0$ and also the counter values are 0. Now, every time VCO_1 generates a rising edge, the first up-down counter will go from 0 to 1. This creates a pulse in the loop, which will be processed and after some time create a '1' in D_{out}. This will reset the first up-down counter to '0'. Since we have assumed that $f_s \gg f_1$, the loop's processing time is much smaller than the pulse duration

of VCO_1. Hence, it is guaranteed that the counter will be reset before it could have been incremented from 1 to 2. Due to this, the first counter can only take the values 0 or 1. Under these constraints (i.e. $f_s \gg f_c$ and $f_{c2} = f_{c3} = 0$), the up-down counter can be implemented as shown in Fig. 6.1(a). The corresponding timing diagram in Fig. 6.1(b) shows how it is triggered to be set and reset by the rising edges of the VCO and D_{out}, respectively.

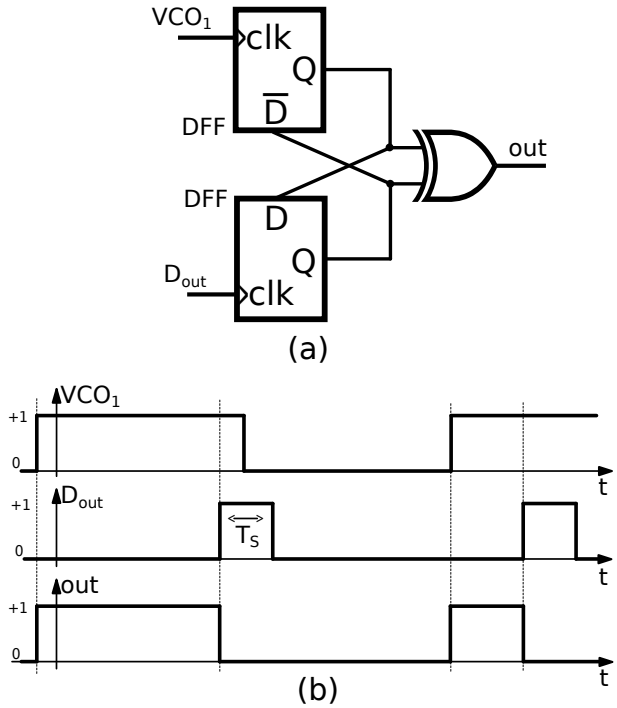


Figure 6.1: (a) The proposed implementation of a single phase up-down counter,
(b) and its timing diagram.

The loop of the modulator will dictate DCO_2 and DCO_3 to have the same average frequency as VCO_1. Hence, if the global loop filter is not too aggressive (and hence the quantization noise in the loop is limited), the other counters in the loop will also only take the values 0 and 1. Thanks to this, in our circuit, the second counter can use the same structure as the first. The implementation for the third (last) up-down counter [see Fig. 3.9(a)] is slightly different, because it is implemented together with

the sampling register. This circuit, shown in Fig. 6.2(a), consists of two parts: an up-down counter, and a DFF as the sampling register. The up-down counter is very similar to the one shown in Fig. 6.1(a) with the small difference that here one of the DFFs can be replaced by a D-Latch. The timing diagram of this block is shown in Fig. 6.2(b).

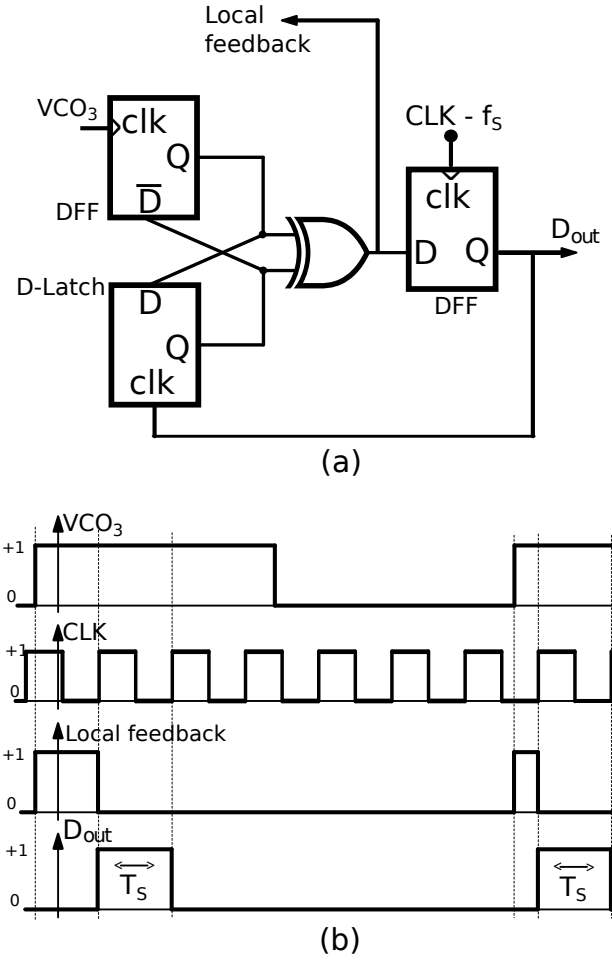


Figure 6.2: (a)The proposed implementation of a reset counter,
(b) and its timing diagram.

The circuit of Fig. 6.2(a) has the same functionality as the reset-counter, commonly used in VCO-ADCs [20], but, for our purposes, this structure has two advantages over prior reset-counters. First, it allows access to the last

integrator's output signal, which can be used to optimize the NTF's zeros by incorporating 'local feedback' in the modulators [63]. Second, unlike most prior implementations, this reset counter doesn't add loop-delay to the overall VCO-based CT-DSM.

6.1.2 Multi phase implementation

In a ring-oscillator VCO, there are multiple output phases, which can be exploited to increase the performance. This can also be done in the high order CT-DSM structure of Fig. 3.9(a) and effectively increases all VCO parameters by a factor n, where n stands for the number of VCO phases. Due to this, all the values of k_v, k_d and f_c in Fig. 3.9(a) should be replaced with $k_{vi,eff} = k_{vi} \cdot n_i$ and $f_{ci,eff} = f_{ci} \cdot n_i$. Here $k_{vi,eff}$, $k_{di,eff}$, and $f_{ci,eff}$ are the 'effective' values for the gain and carrier frequency and n_i is the number of phases of the corresponding VCO (or DCO). In theory, the VCO and the DCOs in Fig. 3.9(a) could have a different number of phases, but in our implementation, all the VCO/DCOs have the same number of output phases, n.

In this case, the single-phase implementation of the up-down counters shown in Fig. 6.1 and Fig. 6.2 can be extended toward a multi-phase implementation, by placing n single-phase blocks in parallel. The output is then provided in thermometer code at the n parallel outputs. The overall output signal D_{out} is a sampled version of the last counter output, and hence is also available in thermometer code to drive the 'down' inputs of the counter blocks. This is illustrated in Fig. 6.3. Here the blocks RO1, RO2 and RO3 correspond to ring oscillators with n output phases, which are discussed in more detail below. The first ring oscillator (RO1) is controlled through the resistive network $R_1 - R_2$ and operates as a VCO. The other ring oscillators (RO2 and R03) operate as DCOs and are controlled by arrays of n matched switched current sources. Each of these arrays is driven by n thermometer encoded digital signals.

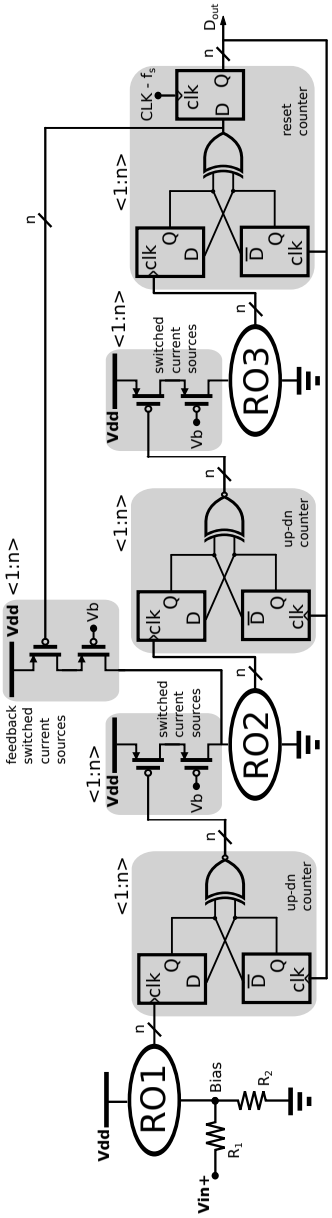


Figure 6.3: The proposed implementation of a high order VCO-ADC (with local feedback), where the digital signals are represented by n parallel thermometer encoded bits.

Consider e.g. the first up-down counter. The n 'up' inputs are driven by the n output phases of the first VCO, while the 'down' inputs are driven by the (thermometer encoded) representation of D_{out}. Under the constraints described above, again it can be understood that each of the n parallel single-phase blocks can only take the output values 0 or 1. This implies that every block that will be set to 1 by a rising edge on the corresponding VCO phase, will be reset to 0 shortly afterwards by a 1 on the corresponding D_{out} wire. As a result, the overall counter output is also available as n thermometer encoded parallel bits. Similar arguments can be made for the 2nd and the 3rd counter. Just as for the single phase structure, discussed above, it is the condition of $f_c \ll f_s$ that will ensure that, in a stable loop, neither the DFFs in the output sampler nor the single-phase up-down counters will ever saturate.

The small *feedback switched current sources* are optional and can be used to obtain optimized NTF zeros. The figure clearly illustrates the power of this 'digital' Continuous Time Sigma Delta Modulation ADC: i.e. there are no conventional analog blocks and all the internal signals are digital. It should be noted that, except the sampled overall output signal D_{out}, all the signals in the structure, are continuous time signals (i.e. they can have transitions at any moment and not only on clock edges).

6.1.3 Reduced degree of freedom in the system

In order to further simplify the design, all oscillators in the loop were sized to operate at the same oscillation frequency in the idle channel condition. For this, the current-sources driving RO2 and RO3, were sized such that for a mid-level input signal (i.e. $n/2$) the corresponding oscillation frequency was equal to the free running frequency of the first VCO (called simply f_c from now on). This implies that:

$$k_{d1} = k_{d2} = k_d = \frac{f_c}{n/2}$$

Taking into account that we are having an n phase design, this leads to the equivalent CT-DSM of Fig. 6.4, where the quantization step in the quantizer is 1. By inspection of the modulator of Fig. 6.4, it is clear that the parameter g_{fb} allows to set the NTF zero position. However, the NTF has 3 poles and there are only 2 design parameters (i.e. f_s and f_c) to set them. This means that we have lost the full control over the NTF. However,

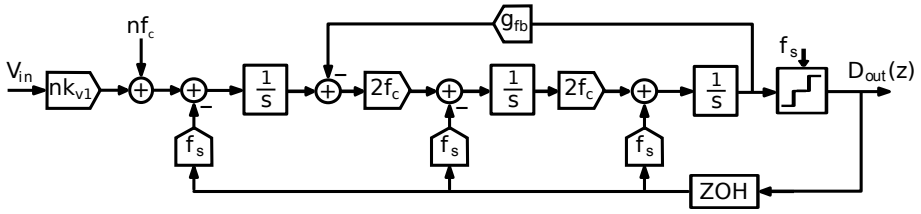


Figure 6.4: The equivalent CT-DSM of our implemented VCO-ADC with reduced degree of freedom.

we will see that the system still has enough design freedom to size the loop for adequate quantization noise shaping.

The number of VCO-phases n, sets the ratio of the quantization step to the modulator's full scale rang which corresponds to the effective number of quantizer levels $N_{lev} = 2n\frac{f_c}{f_s}$ [20]. This way, there is a trade-off with regard to this parameter: increasing n will improve the quantization noise performance, however this will also increase the complexity of the associated digital circuits. While this trade-off already existed as well in prior VCO ADCs, most previous 'digital' VCO ADCs did not allow to exploit this degree of freedom. The reason for this, is that the noise shaping in these prior designs was fixed to only first-order. This way, the only way to improve the quantization noise performance was to increase n (the number of VCO phases), and designers tended to go for the maximum feasible value of n. However, with our high-order quantization noise shaping structure, adequate quantization noise performance can also be achieved for a low value of n. In our design we have exploited this freedom by choosing a very small value of $n = 9$. As will be demonstrated later on, this leads to a circuit with a very small chip area.

Fig. 6.5 shows results of behavioral simulations of a dedicated sizing of our circuit. The result both for the actual implementation according to Fig. 6.3 as well as the equivalent continuous time system of Fig. 6.4, are shown. In the simulation, the local feedback coefficient g_{fb} was set to zero, f_s=1.6 GHz and f_c=250 MHz.We see that both systems indeed achieve 3rd order quantization noise shaping, and obtain nearly the same SQNR=80 dB for an OSR of 80. From this, we can conclude, that with this sizing, non of the counters in our modulator overloads. Also, we see that both systems match very well, which indicates that our assumption that the PWM spurs can be neglected is essentially fulfilled in this case.

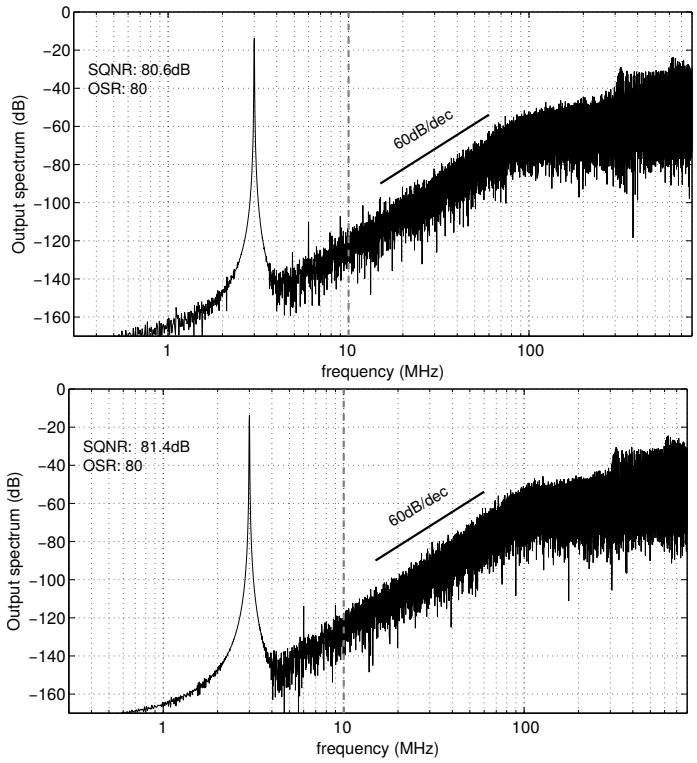


Figure 6.5: Output spectrum (160K pt FFT) of a behavioral simulation result for the case f_s=1.6 GHz,f_c=250 MHz and n=9:
(a) the actual structure of Fig. 6.3
(b) the equivalent continuous time model of Fig. 6.4

6.2 VCO and DCO's

As explained above, the VCO and DCOs are based on a ring oscillator core, which is shown in Fig. 6.6. It consists of n differential delay elements that are placed in a feedback loop. This oscillator core has 2 frequency control terminals ($Ctrl+$ and $Ctrl-$). It can be controlled from either or both these terminals. The differential delay element is shown in Fig. 6.7.

One of the main issues with the proposed system in Fig. 3.9 is the fact that the linearity of the system is limited by that of the first VCO. In the past, several solutions for this were proposed: calibration [23–28], PWM pre-coding [7] and input swing reduction by adding a coarse first stage [22]. All these techniques could be combined with the concepts described in this

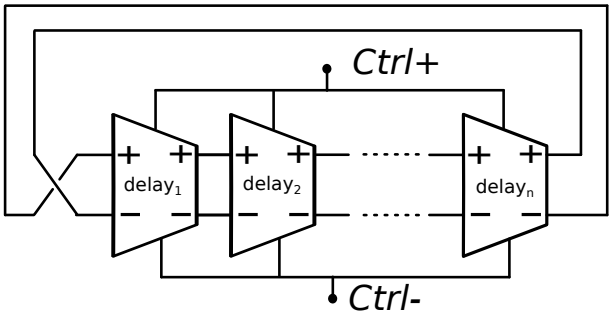


Figure 6.6: Ring Oscillator core

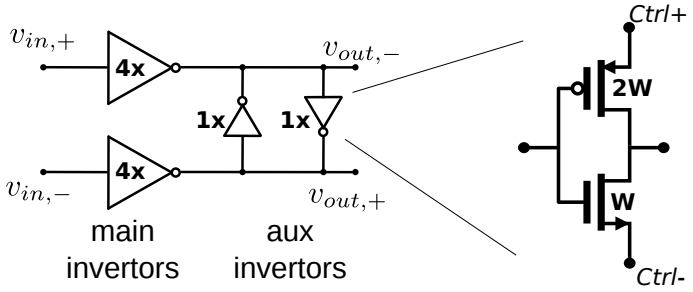


Figure 6.7: Differential delay element used in the Ring Oscillator core

work. However, in our proof-of-concept implementation, we have sticked to the very simple concept of [6] for the first VCO. Here the ring oscillator core is controlled through a resistive network consisting of R_1–R_2 at the $Ctrl-$ terminal (shown in Fig. 6.3). It was shown that this circuit can provide over 11-bit linearity for differential input signals up to 450 mVpp if it is used in a pseudo-differential configuration. For this reason, we have also used a pseudo-differential configuration and the final implementation of the overall ADC consists of two independent parallel channels processing the two differential inputs, V_{in+} and V_{in-}. The resistors R_1–R_2 were sized 770 ohm. The delay cells in the corresponding Ring Oscillator were sized as described in [6].

The DCOs (DCO_2 and DCO_3) are controlled by current control through their top control terminal $Ctrl+$ (see Fig. 6.3). The linearity of this control strategy is somewhat less good than that of the resistive input circuit, but the nonlinearity error is suppressed by the gain of the preceding integrator. The thermo-coded output of the previous stages directly drives an array of

nominally matched unit current sources. Since the voltage across a properly designed Ring Oscillator doesn't vary much [6], the current sources don't need to have a very high output impedance, and a simple structure without cascodes can be used (see Fig. 6.3). Note that any mismatch between the n switched current sources that drive the ROs, $RO1$ and $RO2$, is alleviated by the inherent data weighted averaging (DWA) in the system.

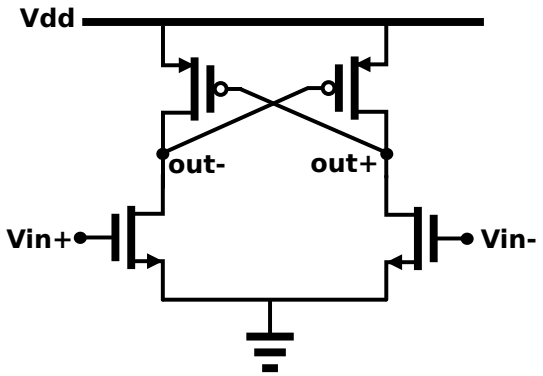


Figure 6.8: The level-shifter for RO2 and RO3.

Our ring oscillator implementation will be operated at a low voltage of 1 Volt. This introduces the problem that the delay elements in the ring (Fig. 6.7) have limited voltage headroom and their output swing is typically only around $V_{dd}/2$ (which is barely above the threshold voltage in our technology). This voltage swing is not enough to drive the following digital blocks. Therefore, a level shifter is needed. The variant corresponding to RO2 and RO3 is shown in Fig. 6.8 (the one for RO1 is flipped). Unfortunately, this block has a severe trade-off between its propagation delay and power consumption. In order to limit the power consumption, we had to allow a rather high propagation delay for the level-shifter, which in worst case can be as high as 700 ps.

It is well known that delay in a CT-DSM affects its stability. However, the coefficients in our design are not very aggressive, such that even this large delay does not make the loop unstable or degrade the SNR performance. However, it clearly alters the out-of-band shape of the NTF. This is illustrated in the simulation result of Fig. 6.9, which apart from the delay is equivalent to Fig. 6.5(a).

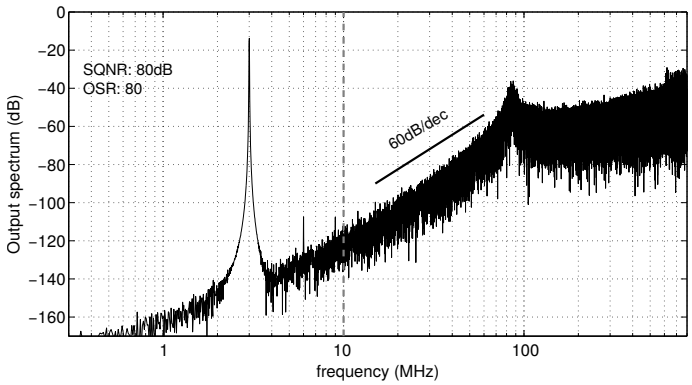


Figure 6.9: The output spectrum (160K pt FFT) of a behavioral simulation result for the case f_s=1.6 GHz,f_c=250 MHz and n=9, where a level shifter delay of 700 ps is inserted after each VCO.

6.3 Experimental Results

A pseudo-differential implementation consisting of 2 independent parallel channels of the circuit depicted in Fig. 6.3 was prototyped in the low power flavor of a 65 nm CMOS technology. The transistors in our circuits have a threshold voltage (V_{th}) around 400 mV.

In principle, the digital circuitry of our implementation (Fig. 6.3) could be designed through a standard digital flow. However, at the time of this design, we didn't have access to digital libraries for our target technology and hence the digital cells were designed by hand. In this proof-of-concept circuit, not much effort was done to optimize these cells in terms of power, nor area. Due to this, more than half of our prototype's power is consumed in these circuits (see below), but this could be significantly reduced by an improved design. The digital blocks were designed for a 1.2 V supply (which is the technology's recommended supply voltage). In a mixed-signal design, the analog supply is typically the bottle-neck and it is normally equal to, or higher than, the digital supply. But in our design the analog circuits (VCO, DCOs, level shifters, current sources, biasing, ...) were designed for a supply voltage of only 1 Volt, which is enabled by the fact that there are no traditional (high-performance) analog components at all.

A photograph of the fabricated die and the annotated layout is shown in Fig. 6.10. We can clearly distinguish the two channels and how the area is distributed over the different blocks. The resulting circuit measures

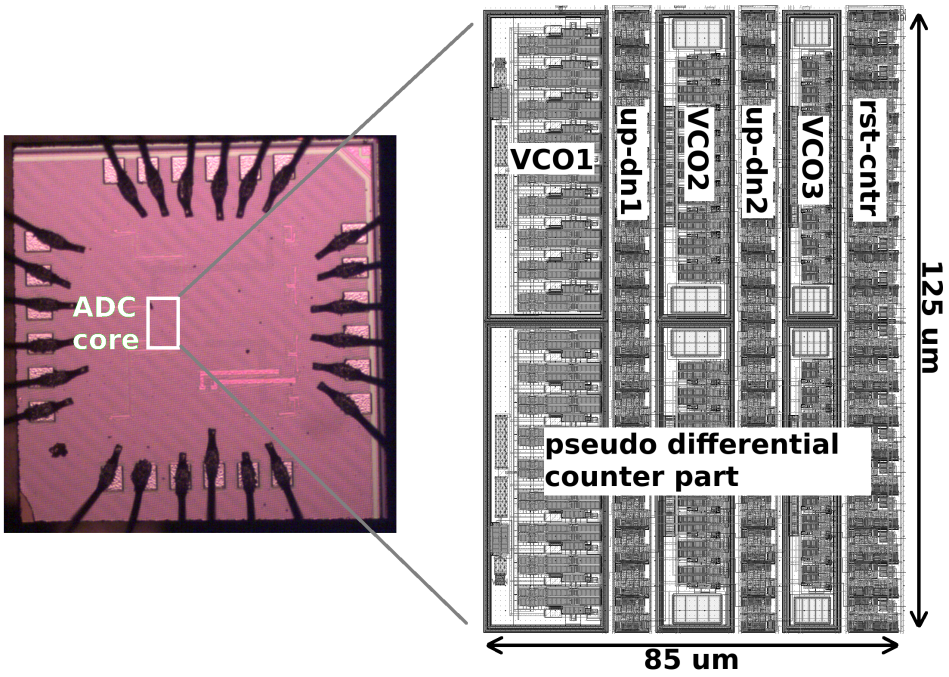


Figure 6.10: Chip microscope photograph with annotated layout.

$85 \times 125\ \mu\ \mathrm{m}^2 = 0.01\ \mathrm{mm}^2$. This surprisingly small silicon area, is thanks to the fact that the number of VCO phases was set as low as $n = 9$. This can be done in this architecture, where the performance is achieved through high-order noise-shaping and not by using a large number of VCO phases.

The presented prototype was designed such that it can operate under different sampling rates with different coefficients in the integrating VCO's. Therefore, the feedback path shown in Fig. 6.3 was omitted to simplify the reconfigurability of this ADC. As explained in section 6.1.3, in our system (with reduced degree of freedom) the modulator coefficients are set by the oscillator central frequency f_c and the sampling frequency f_s. The central frequency in the DCOs (DCO_2 and DCO_3) can be reconfigured by adjusting the bias current in the bias network. To reconfigure the first VCO, a tuning current can be injected into its control terminal ($Ctrl-$). In our prototype, the same effect can also be achieved by adjusting the biasing common mode voltage at the overall ADC input.

In a first batch of measurements, the circuit was configured for a carrier frequency f_c=250 MHz and a sampling frequency f_s=1.6 GHz. The

bandwidth was set to 10 MHz, corresponding to an OSR=80. In this mode, the analog power consumption was 1.8 mW. The digital power consumption (flipflops, latches and xor gates) was slightly higher, i.e. 1.9 mW, but it is expected that this could be cut significantly through an optimized re-design.

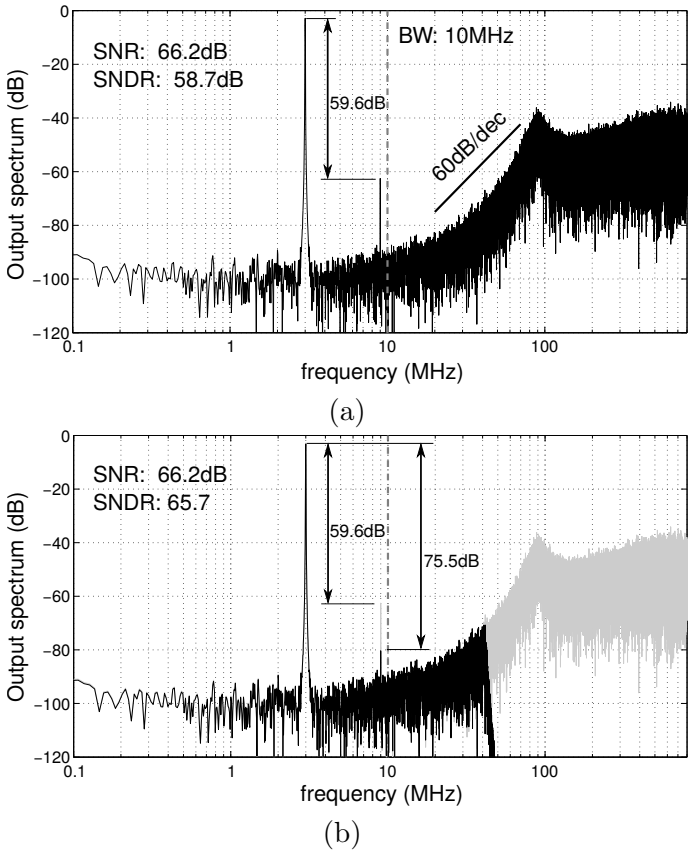


Figure 6.11: Measured output spectrum (160K pt FFT) for the case of $f_c = 250$ MHz and $f_s = 1.6$ GHz with a 3 MHz input tone with an amplitude of a 650mVpp differentially:
(a) normal (pseudo-differential) output,
(b) partially decimated (pseudo-differential) output with off-line digital calibration overlayed on the raw output.

An output spectrum for the case of a 3 MHz input tone with an amplitude of 650 mVpp differentially, is shown in Fig. 6.11(a). This amplitude is

deliberately chosen above the designed linear operating range of the VCO (which is 450 mVpp differentially), such that it creates large harmonics. The plot clearly exhibits the expected peaking in the noise transfer function which is due to the large delay of the VCO read-out circuits (see section 6.2). As expected for low frequencies, we can see a white noise floor. For this case, the SNR is 66 dB. Thanks to the pseudo-differential setup, where the outputs of both independent channels are subtracted from each other, there is no even order distortion, which confirms the effectiveness of this scheme and is consistent with the measurements of [6]. However, there is a large 3rd harmonic which limits the SNDR in this case to 59 dB. As explained above, this large third harmonic is due to the limited linearity of the first VCO in the system. To assess this, the static nonlinearity of the overall ADC was measured, by sweeping the input signal and averaging the ADC's output over a long time. The result is shown in Fig. 6.12.

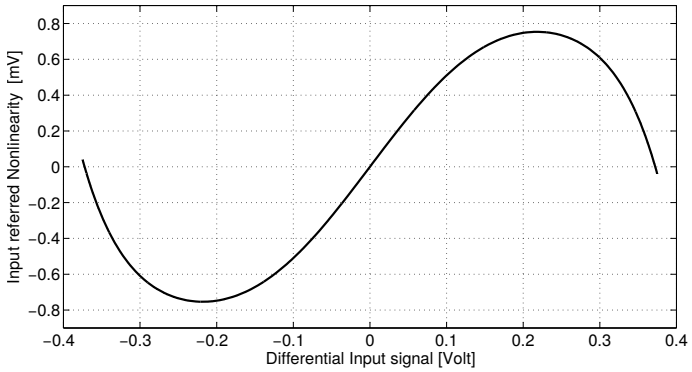


Figure 6.12: Static nonlinearity plot of the ADC for the case of of $f_c = 250$ MHz and $f_s = 1.6$ GHz in the pseudo differential configuration.

As mentioned above, our new high-order noise shaping technique can also be combined with digital calibration techniques, similar to e.g. [23–25]. Although not the focus of this work, a first assessment of the effectiveness of an off-line calibration technique such as the one of [23] was also performed based on the measured nonlinearity data of Fig. 6.12. The core idea of such an off-line calibration technique is shown in Fig. 6.13. It is based on the observation that the nonlinearity of the VCO occurs at the input of the system (shown as the nonlinear function $f(\cdot)$ in Fig. 6.13). If the nonlinearity is known, it can be inverted at the digital output of the converter (shown as the nonlinear function $f^{-1}(\cdot)$ in Fig. 6.13). This nonlinearity correction

can be implemented very efficiently by interpolating calibration data of a surprisingly small look-up-table [23]. In the conventional scheme, shown in Fig. 6.13(a), the nonlinearity correction is performed directly on the raw undecimated modulator digital output signal D_{out}. However, in this work, this conventional scheme, was found to increase the baseband noise level significantly. The reason for this, is that in our modulator, there is a large amount of shaped quantization noise, which after passing trough the nonlinearity correction block, is in part converted to white noise which in turn partially falls in the baseband. Therefore the modified setup of Fig. 6.13(b) was used, where first the bulk of the shaped quantization noise is removed in a first coarse decimation step. Then on this relatively clean signal, the nonlinearity correction is applied, and then passed for further decimation. This modified set-up with the nonlinearity correction at an intermediate decimation step, is preferred over performing the nonlinearity correction on the overall decimated output D_{dec}, to avoid that the baseband signals would be partially filtered (phase shifted or slightly attenuated) prior to the nonlinearity correction. This scheme was implemented in software (off-chip) and the result is shown in Fig. 6.11(b). As the figure shows, the distortion is now reduced to a level where it does not affect the SNDR anymore, leading to an SNDR which is virtually equal to the SNR.

Experiments as described above, were repeated for varying input amplitudes. The results are shown in Fig. 6.14. For the implemented chip (which does not have the calibration on board), the SNDR starts to drop above a differential input amplitude of 450mV_{pp}, which is consistent with the designed linear input range of the first VCO [6]. The corresponding peak SNDR equals 62.5 dB. The peak SNR is 66.2 dB and the dynamic range 71 dB. The SNDR for the case of the off-line (and off-chip) digital calibration is plotted as well and it is nearly identical to the SNR, indicating that digital calibration could work over the entire signal range. The corresponding peak SNDR for this case equals 65.7 dB.

To further asses the digital calibration scheme also a two-tone test was performed where the input signal is the sum of 2 sine waves with the same amplitude and input frequencies near the band edge (here: 8.855 MHz and 9.068 MHz). The result for the case of a signal level of 650mVpp differentially (identical to the case shown in Fig. 6.11) is shown in Fig. 6.15, both for the case without and with the digital calibration. Clearly, also in this case the calibration can significantly suppress the effect of the distortion.

As was explained above, the proposed implementation can work under

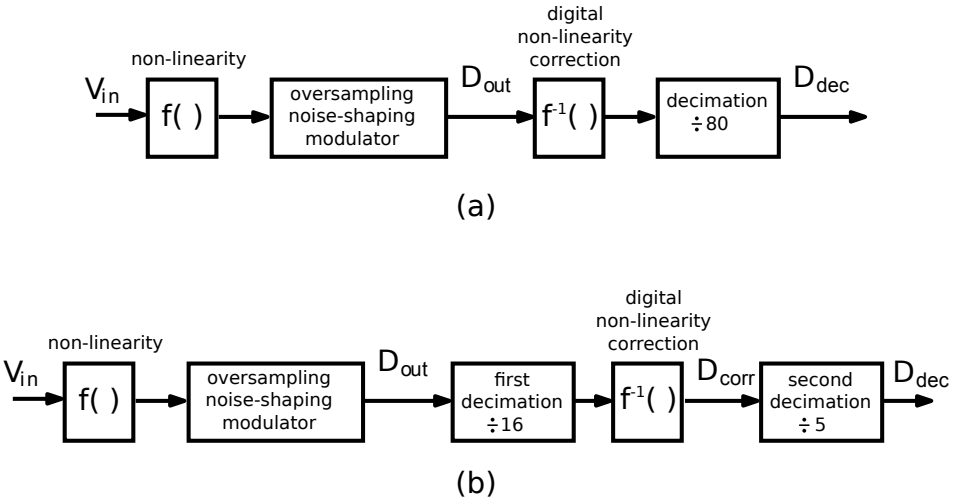


Figure 6.13: Block diagram of an oversampling converter with off-line digital calibration:
a) conventional setup discussed in this section,
b) and setup used in this work.

multiple sampling frequencies and can have multiple operation modes by adapting the VCO free running frequency values (and corresponding VCO gain values). To illustrate this, the same batch of experiments as described above was repeated for the case where the sampling frequency was set to $f_s = 1$ GHz and the VCO central frequency f_c to 133 MHz. It was found that at this lower operating frequency, the circuit was still functional also at reduced supply voltages: i.e. 0.8V analog and 1.1V digital. In this configuration, the accuracy performance (SNR, SNDR) was decreased but also the power consumption was more than halved. The results for both cases as well as a comparison with other related works about digital friendly ADCs are summarized in table 6.1. From the table we can see that our proof-of-concept circuit has a performance that is comparable to the state of the art, while it has a significantly reduced silicon area.

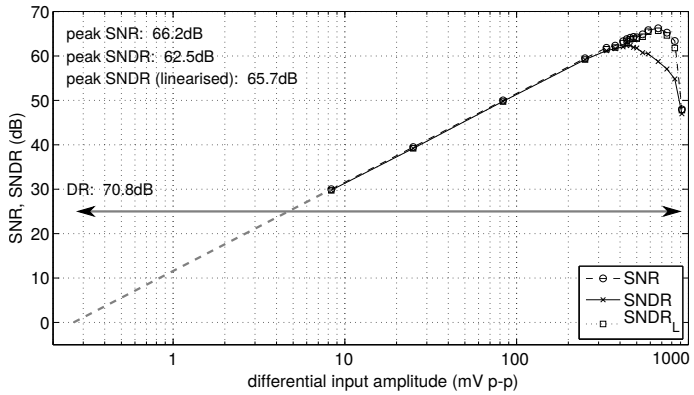
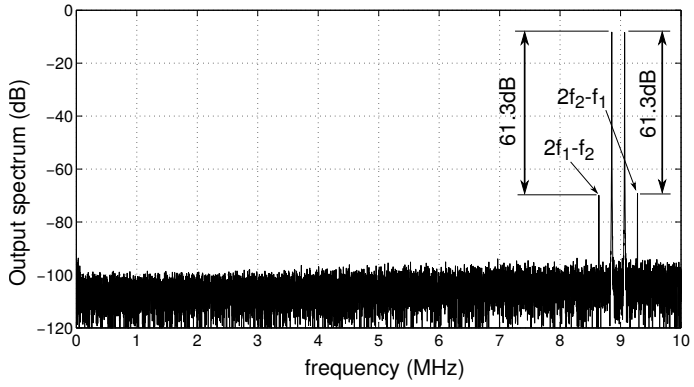
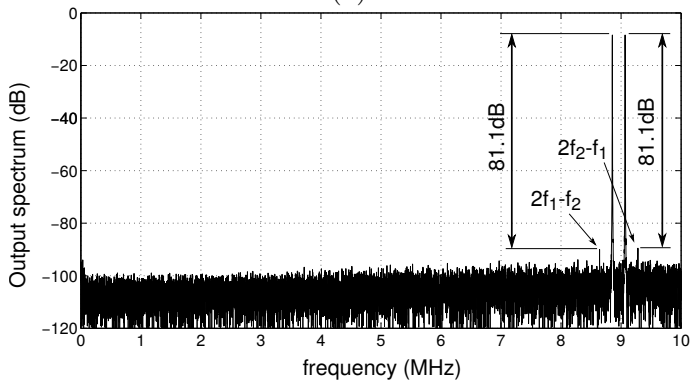


Figure 6.14: Dynamic range plot for the case of $f_c = 250$ MHz, $f_s = 1.6$ GHz and 10 MHz bandwidth.



(a)



(b)

Figure 6.15: Baseband FFT plot for the case of two-tone input signal of two tones near 9 MHz with the same peak-to-peak signal level as for the plot of Fig. 6.11 (650mVpp differentially): (a) normal (pseudo-differential) output, (b) (pseudo-differential) output with off-line digital calibration.

Table 6.1: Comparison with related work

	This work		[23]	[24]		[25]		[65]	[76]	[64]	[27]
Process	65 nm LP		65 nm	65 nm G+		65 nm LP		65 nm	90 nm	90 nm	65 nm
Area (mm^2)	**0.010**		0.020	0.075		0.070		0.150	0.170	0.120	0.026
Fs (MHz)	1600	1000	300	1600	2400	500	1152	250	480	300	205
Fc (MHz)	250	133	–	–	–	–	–	–	–	–	–
BW (MHz)	10	10	30	12.5	37.5	3.9	18	20	10	8.5	25.62
peak SNR (dB)	66.2	60.5	–	75	71	71.5	70	62	72.3	69.3	52.8
peak SNDR (dB)	62.5	55.1	–	74	70	71	67.3	60	70.3	67.2	50.3
peak $SNDR^*_L$	65.7	60	64								
DR (dB)	71	63	–	77	73	70	68	68	75	73	–
Supply (V), a/d	1/1.2	0.8/1.1	–	1	1.2	2.5/1.2	2.5/1.2	1.3/1.2	1.2	1.4/1.2	1.2
Power (mW), a+d	1.8+1.9	0.71+0.77	11.4	17.5	39	8	17	10.5	14.3	4.3	3.3
FOM^{**}_{SNDR} (dB)	157	153.5	–	162.5	160	158	157.5	153	158.5	160	149
$FOM_{SNDR,L}$	160	158.5	158								
FOM_{DR} (dB)	165.3	161.3	–	165.5	162.8	156.9	158.3	160.8	163.5	166	–

* $SNDR_L$ is the SNDR after decimation and calibration, which was done off-chip. Therefore its power is not included.

** FOM = (SNDR or DR) + $10\log(\mathrm{BW}/Power)$, [63]

6.4 Conclusion

We have demonstrated the first implementation of a mostly-digital VCO-ADC with 3rd order quantization noise shaping. For this, we have derived the structure of Fig. 3.9(a) and proposed the efficient implementation of Fig. 6.3. The resulting circuit occupies a surprisingly small area of only 0.01 mm^2. This is an inherent advantage of our approach, because it achieves its performance thanks to the high order noise shaping, and hence unlike most other designs does not require a high number of VCO phases with their associate read-out circuitry. Although our prototype was only a proof of concept where several potential optimization and tweaks were not implemented, it exhibits an adequate performance with a peak SNDR of 62 dB and a dynamic range of 71 dB over a 10 MHz bandwidth at a power consumption of 3.7 mW. One potential improvement, i.e. the use of digital calibration was already investigated and was shown to push the nonlinearity below the noise level, leading to an improved peak SNDR of 66 dB. Also, the digital circuits (e.g. the DFFs) were designed ad hoc in this proof-of-concept prototype and due to this, these circuits consume more than half of the overall power budget. By an optimized design, the associate power could be greatly reduced.

Chapter 7

Implementation of a 3rd order VCO-based CT-DSM with PWM pre-coding

As a second attempt to design a linear mostly digital low voltage high order VCO based CT-DSM, the idea of PWM pre-coding, elaborated in chapter 5, is combined with the system presented in chapter 3.

In order to investigate the effectiveness of the PWM pre-coding technique to linearize a VCO-ADC, it has been applied to a 3rd order VCO-ADC. The design and implementation of this modulator is discussed in this chapter.

A proof of concept is implemented in the low power version of a 65nm technology for a 10 MHz bandwidth. This prototype shows a measured performance of 67.4/59/55.4 dB DR/SNR/SNDR at a 10 MHz bandwidth while consuming 2.3 mW from a 1.0 V analog and 2 mW from a 1.2 V digital supply. The modulator covers a silicon area of 0.018 mm^2.

7.1 Implementation details

The system level representation of the proposed scheme is shown in Fig. 7.1. As the Figure shows, the core idea of this ADC structure is very similar to the one introduced in Fig. 3.9(a). The key difference is the PWM block that precedes the ADC. The final implementation, as the figure shows, is pseudo-differential.

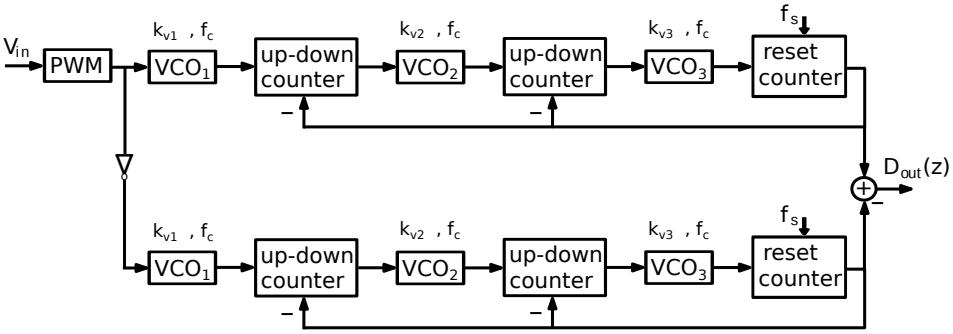


Figure 7.1: System level representation of the proposed pseudo differential 3rd order VCO-ADC with PWM pre-coding.

Notice that in this structure all VCO's have a pseudo-digital input signal. In that regard they can all be viewed as DCO's, which can potentially make their design even easier.

The circuit level implementation that we propose for this structure is a combination of the ADSM-VCO circuit discussed in section 5.3 and the VCO-ADC shown in Fig. 6.3, without the local feedback. The proposed circuit is shown in Fig. 7.2.

The fully differential ADSM, that generates the PWM signal, and the DCO's that follow it, DCO1, are designed and size as it was explained in Section 5.3. The design and sizing of the following blocks (like DCO2, DCO3, and the digital blcoks) is already explained in details in chapter 6.

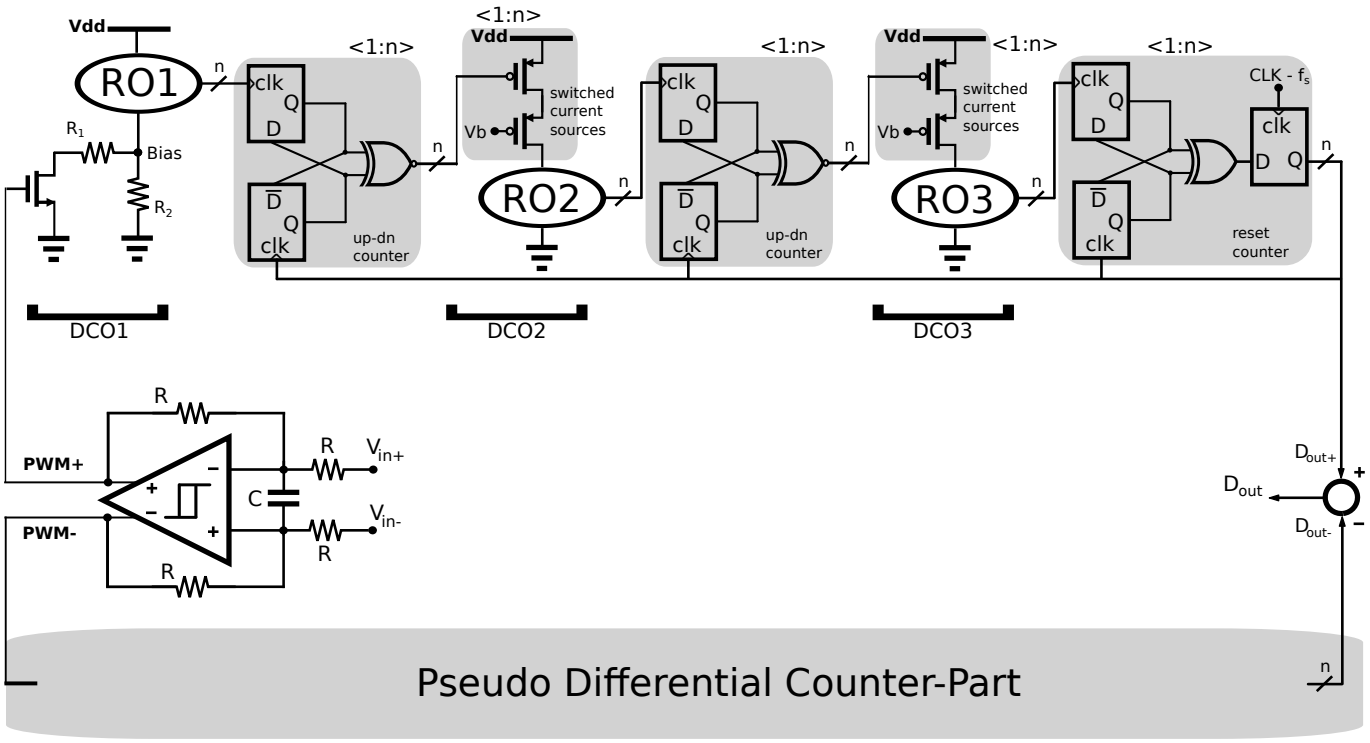


Figure 7.2: The circuit level implementation for the system proposed in Fig. 7.1.

7.2 Implementation and Measurement

A pseudo-differential implementation was prototyped in the low power flavor of a 65 nm CMOS technology. The transistors in our circuits have a threshold voltage (V_{th}) around 400 mV and the circuit was designed to work under a 1 V supply, while the nominal supply for this technology is 1.2 V.

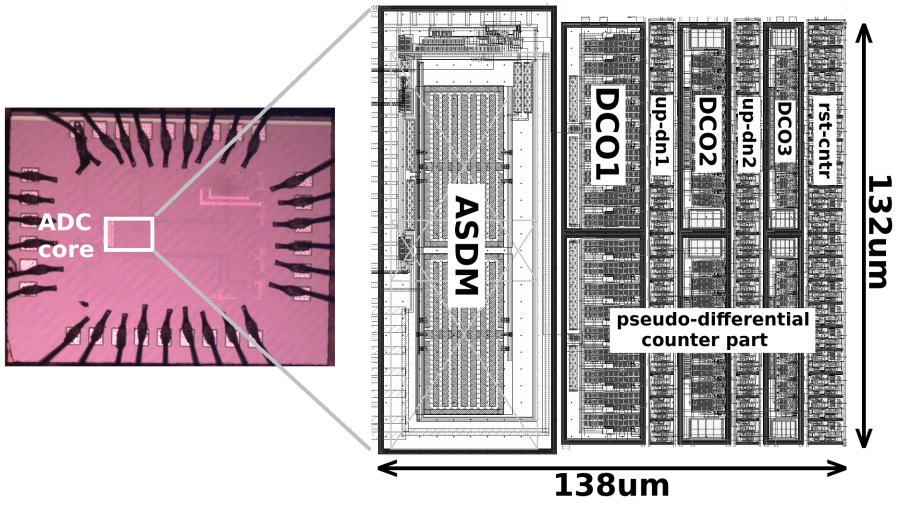
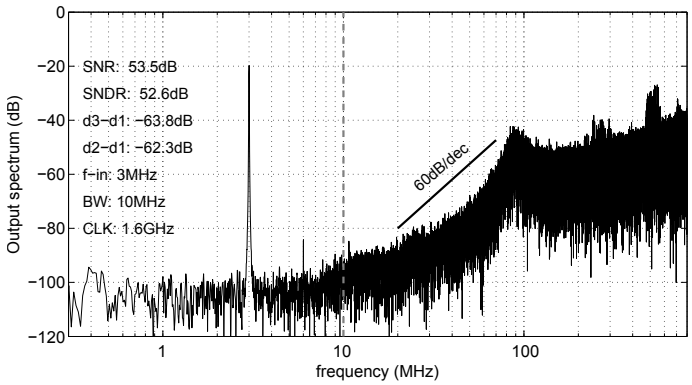


Figure 7.3: A photograph of the fabricated die.

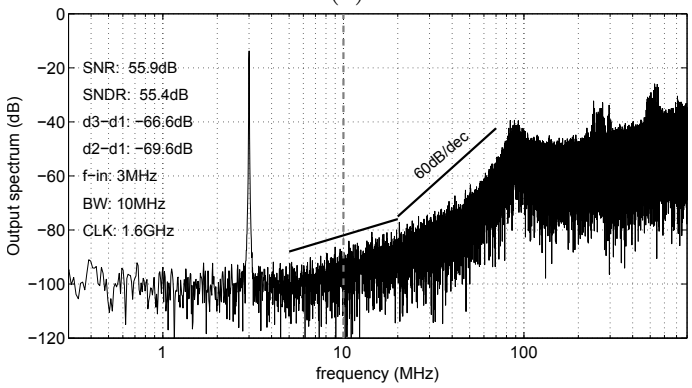
A photograph of the fabricated die and the annotated layout is shown in Fig. 7.3. We can clearly distinguish the two channels and how the area is distributed over the different blocks. The resulting circuit measures $132 \times 138\ \mu\text{m}^2 = 0.018\text{mm}^2$. This surprisingly small silicon area, is thanks to the fact that the number of VCO phases was set as low as $n = 9$.

The samplers in the reset counters were clocked at f_s=1.6 GHz. The bandwidth was set to 10 MHz, corresponding to an OSR of 80. The analog power consumption was 2.3 mW, including 0.3 mW for the ADSM, and 2 mW for the six DCO's. The digital power consumption (flipflops, latches and xor gates) was of the same order, i.e. 2 mW, but it is expected that this could be cut significantly through an optimized re-design.

All the oscillators have a carrier frequency of around 260 MHz. The whole system shows little sensitivity to the mismatch between the carrier frequency of the oscillators, even when increased up to 20%.



(a)



(b)

Figure 7.4: Measured output spectrum of the presented modulator with a sine wave input voltage, $V_{pp} = 400\ mv$,
(a) single-ended measurement,
(b) pseudo-differential measurement.

In the first batch of measurements a sine wave voltage source with an amplitude of 400 mv, peak to peak, and frequency of 3 MHz is applied to the input of the modulator. An output spectrum for this case is shown in Fig. 7.4.

The spectrum shown in Fig. 7.4(a) corresponds to the single-ended output of the modulator and the one in Fig. 7.4(b) is for the differential case where the two single-ended outputs are subtracted off-chip in a software.

As it was shown in chapter 5, an ADSM generates only odd order harmonics of the input tone. Nevertheless, even order harmonics can be ex-

pected too, due to the imbalanced response of the switching transistor in DCO1 to the rising and falling edges of PWM+ signal in Fig. 7.2. That's why a second harmonic is visible in Fig. 7.4(a). Fortunately, this even order harmonic is successfully suppressed by the pseudo-differential implementation, as shown in Fig. 7.4(b).

The peaking in the NTF that occurs around 90 MHz is due to delay in the level shifters that follow the oscillators, as it was explained in chapter 6.

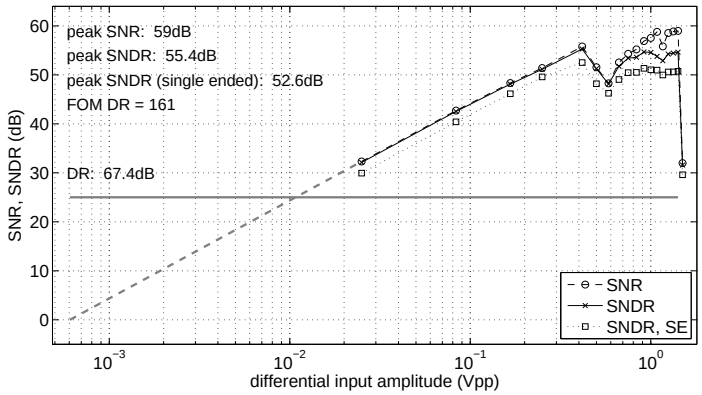


Figure 7.5: The SNR/SNDR curve of the measured ADC.

The same experiment is repeated for varying input amplitudes. The results are shown in Fig. 7.5. The peak SNR is 59 dB and the dynamic range 67.4 dB. The SNDR for the case of single-ended measurement is plotted as well.

7.3 Mismatch, aliasing, and inter-modulation

The SNR plot obtained from the measurements, seen in Fig. 7.5, reveals a signal dependent distortion that dominates the noise performance starting from the amplitude of 400 mv and is worst around 600 mv. The corresponding single-ended output spectrum for this amplitude is seen in Fig. 7.6. This plot clearly shows the in-band distortions responsible for the loss in SNR.

It is well known that in PWM pre-coding linearization method the high frequency spurs of the PWM carrier can alias into the desired baseband. On the other hand, it is expected from a third order CT-DSM to sufficiently suppress such spurs to below noise floor. A noise-less system level

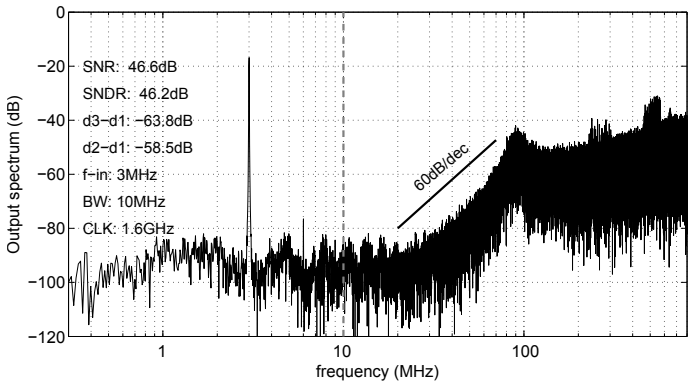


Figure 7.6: Measured output spectrum of the single-ended modulator with a sine wave input voltage, $V_{pp} = 600\ mV$.

simulation of the system in Fig. 7.1 verifies that, as expected, the PWM spurs do alias into baseband, but they are too small to degrade the SNR performance of the modulator. The output spectrum corresponding to this simulation is shown in Fig. 7.7.

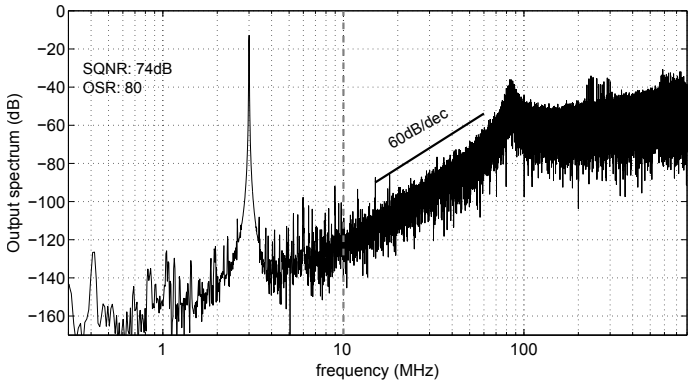


Figure 7.7: The output spectrum of a system level noise-less simulation of the modulator with a sine wave input voltage, $V_{pp} = 600\ mV$.

The source of the distortions in Fig. 7.6 is not aliasing, but it's a combination of mismatch and inter-modulation. To better understand this effect, take a look at the measured output spectrum of the single-ended modulator for a small input amplitude, shown in Fig. 7.8. As expected, the high frequency spurs due to the ADSM carrier are visible centering around

307 MHz. But there are also clear spurs around 258 Mhz, which is the average frequency of the oscillators.

On a system level these oscillator spurs wouldn't be visible, because it is the effective frequency of a ring oscillator that matters ($n \times f_{vco}$), not the average oscillation frequency of one phase of the ring oscillator. But in practice there is a mismatch between the readout circuits that follow each phase of the RO. This mismatch generates a pattern that repeats itself at the frequency of f_{vco}, so it can be referred to the input of the oscillator as some spurs around f_{vco}. The spurs due to DCO2 and DCO3 will be sufficiently suppressed by the loop, but the spurs generated by the first RO will directly appear at the output, as seen in Fig. 7.8 at 258 Mhz.

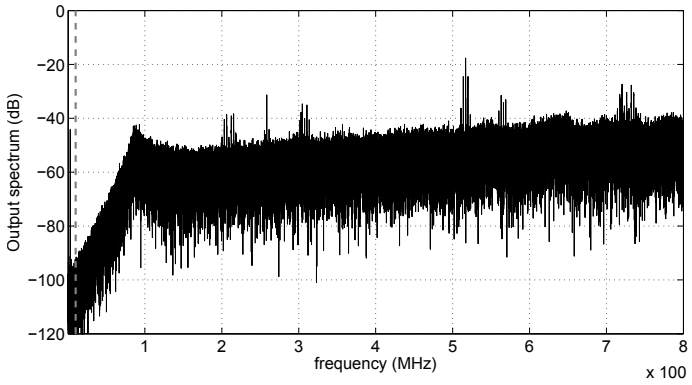


Figure 7.8: Measured output spectrum of the modulator on a linear scale for input sine wave with a small amplitude.

Furthermore, DCO1 operates as a mixer. In other words, the PWM spurs (307 MHz) and DCO1 spurs (258 MHz) and their harmonics, which are visible in Fig. 7.8, can inter-modulate. This mixing effect gives rise to the spurs visible at 209 MHz which is the mixing product of the second harmonic of the oscillator and the PWM spurs, ($2 \times 258 - 307 = 209$).

As the input amplitude rises, both the PWM spurs and DCO1 spurs become more widespread [71] and the chance of their inter-modulation products falling into baseband increases. After reaching that particular amplitude where the down converted spurs fall into the baseband, all the amplitudes higher than that will also suffer from the same distortion, as seen in Fig. 7.5.

7.4 Conclusion

We have demonstrated an implementation of a mostly-digital VCO-ADC with 3rd order quantization noise shaping and PWM linearization. The resulting circuit, implemented in the low power flavor of the 65nm technology, occupies a small area of only 0.018 mm^2. The analog circuitry was operational under a small supply voltage of 1v.

This proof of concept exhibits a peak SNDR of 55.4 dB and a dynamic range of 67.4 dB over a 10 MHz bandwidth at a power consumption of 4.3 mW.

The digital circuits (e.g. the DFFs) were designed ad hoc and due to this, they consume around half of the overall power budget and require a higher supply voltage than the analog blocks. In an optimized design, the associated power and supply voltage could be greatly reduced.

Table 7.1: Performance summary of the presented works in this book.

Presented in	Chapter 6	Chapter 7
Process	65 nm LP	
Area (mm^2)	0.010	0.018
Fs (MHz)	1600	1600
Fc (MHz)	250	258
BW (MHz)	10	10
peak SNR (dB)	66.2	59
peak SNDR (dB)	62.5	55.4
peak $SNDR^*_L$	65.7	–
DR (dB)	71	67.4
Supply (V), a/d	1/1.2	1/1.2
Power (mW), a+d	1.8+1.9	2.3+2
FOM^{**}_{SNDR} (dB)	157	149
$FOM_{SNDR,L}$	160	–
FOM_{DR} (dB)	165.3	161

* $SNDR_L$ is the SNDR after decimation and calibration, which was done off-chip. Therefore its power is not included.

** FOM = (SNDR or DR) + $10\log(BW/Power)$, [63]

for comparison with prior works, refer to Table 6.1

In order to better assess the effectiveness of the PWM pre-coding technique, the performance of the ADC presented in this chapter is compared

to the VCO-ADC discussed in chapter 6, see Table 7.1.

As the table shows, the work presented in this chapter is inferior to its PWM-less counterpart in almost every aspect. Following we will examine different parameters of the two designs (with Fs=1600 MHz) to better understand the root causes.

The first obvious difference between the two designs is area. As one could expect, PWM pre-coding requires some extra silicon area for the implementation of the ADSM. Moreover, in the design of the proposed VCO-ADC in chapter 6 no capacitors were used, and as a result the overall ADC required little chip area. But the design presented in this chapter requires big capacitors to be used in the loop of the ADSM.

The Dynamic Range (DR) of the ADSM-VCO-ADC is about 3.6 dB worse than the VCO-ADC in chapter 6. The same applies to the FOM of the system that is obtained based on DR. This is, as explained earlier in this chapter, an expected side effect of PWM pre-coding technique. The reason is that the PWM (or ADSM) stands in series on the signal path and adds to the power consumption and noise of the system, and eventually degrades its noise/power/DR/FOM performance.

The last, and probably the worst, disadvantage of PWM pre-coding linearization technique was the added noise and distortion due to aliasing and mixing. This phenomenon shows its effect in the huge loss of SNR and SNDR.

As it was elaborated in this chapter, the added noise due to aliasing is not severe enough to raise the noise floor of the modulator and the anti-aliasing behavior of the CT-DSM suppresses these spurs to a great extent. Nevertheless, on a system level design this effect should be taken into account as it could be more hurtful is some other designs with more strict noise performance requirements.

The added noise and spur due to mixing and inter-modulation between the carrier of the ADSM and that of the first DCO was proven to be the bottle-neck of this design and had the most contribution in the SNR/SNDR loss. This effect was partly due to the unavoidable mismatch between the output phases of the DCO. One way to avoid this problem is to better choose the carrier frequencies of the ADSM and the DCO, such that the products of their inter-modulation never falls into baseband.

Chapter 8

Conclusion

This work aimed at exploring new ways of realizing analog functions in time domain, instead of voltage domain. The two functions that were of utmost importance to this work are integration and quantization. Using these two functions one can implement important analog blocks, such as analog filters and analog to digital converters.

The main incentive for time-domain signal processing is to benefit from the digital blocks that are becoming faster and more efficient in the newer CMOS technologies. Moreover, in the more advanced CMOS processes it has become more challenging to design these functions in the voltage domain. This is partly due to the fact the transistors can deliver a smaller gain, the threshold voltage of the transistors is not dropping as rapidly as the supply voltage, and the loss of voltage headroom is causing dynamic-range loss.

This book investigated linear, low-voltage, low-area, solutions for the design of Continuous-Time Delta Sigma Modulators (CT-DSM) with high orders of quantization noise shaping. In this pursuit we have proposed the design of, and showcased the implementation of, high order VCO-Based ADC's, linear VCO's, and Asynchronous Delta Sigma Modulators (ADSM). All of the presented designs are digital friendly and make use of no traditional analog building blocks, like op-amps and highly linear transconductors. Digital friendly means, the potential to benefit from technology scaling and being synthesizable using digital design flow.

8.1 Contributions

- On a system level, a new VCO-based CT-DSM structure is presented. In this system the combination of a VCO (Voltage Controlled Oscillator) and some digital blocks (referred to as up-down counter) is used as an integrator. The quantizer of the modulator is also VCO-based. Since a VCO can be implemented using an RO (Ring Oscillator), it can be very simple and digital friendly. In this manner a high order CT-DSM can be designed using only these blocks. Typical CT-DSM techniques, such as local feedback can be incorporated in this novel structure.

- Many circuit level innovations and simplifications are presented to make the implementation of this modulator possible. The final circuit level solution is very simple to design and size. Therefore, it is expected to be easy to migrate from one technology node to another. The modulator has little sensitivity to mismatch between the VCO's. The DACs are also benefiting from the inherent DWA provided by this system.

- A thorough theoretical work is carried out in modeling an ADSM to predict its linearity performance. ADSM's are a family of PWM's (Pulse Width Modulator) that have many applications, like linearizing a VCO-based ADC. It is also proven this block can be implemented using only a Schmitt trigger and a passive loop filter, which is also simple to design and can benefit from technology scaling. Previous implementations of an ADSM or a PWM, presented in literature, required either an op-amp based or g_mC based integrator.

- The effect of delay in the loop of an ADSM is also studied and accurate equations to predict the linearity and oscillation frequencies of an ADSM with loop delay are extracted. It is proven that loop delay in an ADSM doesn't necessarily degrade the linearity performance of an ADSM and extra circuitry is not needed to counteract its effect. Instead the effect of the loop-delay can simply be compensated by lowering the threshold voltage of the Schmitt trigger.

- As a proof of concept, a passive ADSM is implemented in 65 nm CMOS technology. The design is operational under a 1v supply and has more than 10 bit linearity over a 10 MHz bandwidth.

- A low-voltage circuit level solution is presented to design a voltage controlled ring oscillator with high linearity. The implemented prototype of this block was shown to be much more linear than previous works. This block can be used as the VCO in a high order CT-DSM. This block determines the linearity of the overall modulator. A prototype is implemented in the 65nm technology and the measured voltage to frequency conversion curve of the VCO for a rail-to-rail input shows a small 0.6 % deviation from an ideal line. Measurements on a pseudo-differential setup proved that the second harmonic distortion of the VCO can be heavily suppressed.

- As a proof of concept, for the first time a 3rd order VCO-based CT-DSM is implemented in the low power version of a 65 nm technology for a 10 MHz bandwidth. This prototype shows a measured performance of 71/66.2/62.5 dB DR/SNR/SNDR at a 10 MHz bandwidth while consuming 1.8 mW from a 1.0 V analog and 1.9 mW from a 1.2 V digital supply. With digital calibration, the nonlinearity could be pushed below the noise level, leading to an improved peak SNDR of 66 dB. The modulator covers a small silicon area of only 0.01 mm^2.

- As a second attempt to design a linear mostly digital low voltage high order VCO based CT-DSM, an ADSM is used before the first VCO to linearize it. A proof of concept is implemented in the low power version of a 65 nm technology for a 10 MHz bandwidth. This prototype shows a measured performance of 67.4/59/55.4 dB DR/SNR/SNDR at a 10 MHz bandwidth while consuming 2.3 mW from a 1.0 V analog and 2 mW from a 1.2 V digital supply. The modulator covers a silicon area of 0.018 mm^2.

8.2 Future work

- The commonly available simulation tools cannot properly model the 1/f noise of switching transistors. Such transistors are the main ingredient of a ring oscillator and their noise performance directly affects the SNR of a VCO-based CT-DSM. Therefore, a study on this low frequency noise source seems to be necessary.

- In this work all the switching transistors in the ring oscillators had a minimum size channel length and the width was chosen such that they

provide sufficient parasitic capacitive load for their previous delay stage. Nevertheless, it is not obvious whether this is the optimum choice in terms of the noise performance of the switching transistors. A transistor with double the length and half the width can have the same capacitive load, and potentially a better, or worse, noise performance. Other secondary effects, such as threshold voltage of the transistor and voltage drop over the ring also needs to be investigated.

- The proposed VCO-based CT-DSM relied on a digital block called an "up-down counter". A simple circuit level for this block was presented. One of the main limitations of this solution was the fact the for larger inputs the output of the counter wouldn't just saturate, but overflows. This effect destabilizes the modulator for a few clock cycles. A simple solution would be to use PFD's (Phase Frequency Detectors) instead of PD's. This potential solution needs to be verified.

- The digital circuitry doesn't contribute to the noise performance of the modulator in the same way as analog blocks. In other words, scaling their power consumption doesn't directly affect the SNR. As a result, a low power design for these blocks can greatly improve the FOM of the system.

- The level shifters that followed the output phases of the ring oscillators where proven to be too slow and added too much loop delay in the overall CT-DSM. A better design of this block can decrease the loop delay, and eventually make the loop filter design more relaxed.

- The frequency of the ADSM carrier and that of the VCO in the second implementation were too close to each other and this caused a loss of SNR due to inter-modulation. In simulations this effect can only be detected when mismatch is taken into account. A study of the optimum choice for these carrier frequency could solve this problem.

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