Multi-level Optical Signal Generation Using a Segmented-Electrode InP IQ-MZM with Integrated CMOS Binary Drivers

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Abstract *We present a segmented-electrode InP IQ-MZM, capable of multi-level optical signal generation (5-bit per I/Q arm) by employing direct digital drive from integrated, low-power (1W) CMOS binary drivers. Programmable, multi-level operation is demonstrated experimentally on one MZM of the device.*

Introduction

Coherent technology has been firmly established as the backbone of modern telecom networks, in the form of 100G optical channels based on dual-polarization (DP) QPSK signaling. Faced with continuously rising demand for IP traffic, system designers are responding with a migration towards higher-order coding and modulation schemes, in order to increase the spectral efficiency of optical links; a seamless upgrade path enabled by coherent technology.

Moreover, the development of novel programmable devices capable of supporting a Software Defined Network (SDN) approach is seen as a necessity for realizing future flexible architectures. There is a clear advantage of employing photonic modules that can be directly operated and controlled by low-cost ASICs; eliminating the need for sophisticated and energy-consuming electronics such as DACs and linear drivers, leads to more manageable and efficient systems for network operators.

In this work we present a prototype optical transmitter based on an Indium Phosphide (InP) IQ Mach-Zehnder modulator that utilizes a segmented-electrode design (SEMZM). The SEMZM is driven by novel, low power CMOS electronics that consume only 1 W per I/Q arm.

This structure allows for the creation of multi-level optical signals with 5-bit resolution per I/Q arm without a DAC, using only binary signals as described in[1]. Each driver is controlled individually by CMOS logic functioning as an encoder which maps input binary words to the driver outputs; thus multiple optical levels can be produced. The transmitter is essentially a electro-optical digital-to-analog converter.

The device is demonstrated and evaluated with proof-of-concept experiments on a single SEMZM, showing potential for generation of multiple, higher-order modulation formats. It constitutes a promising approach towards addressing future network needs for high capacity and low power consumption. A low complexity control interface allows for programmable operation, making the device an attractive option for next generation, SDN-powered optical networks.

CMOS electronics and SEMZM

The driver IC was developed in a 40 nm CMOS LP (low-power) technology with a 3.3 mm × 1.65 mm footprint. It features a 10-
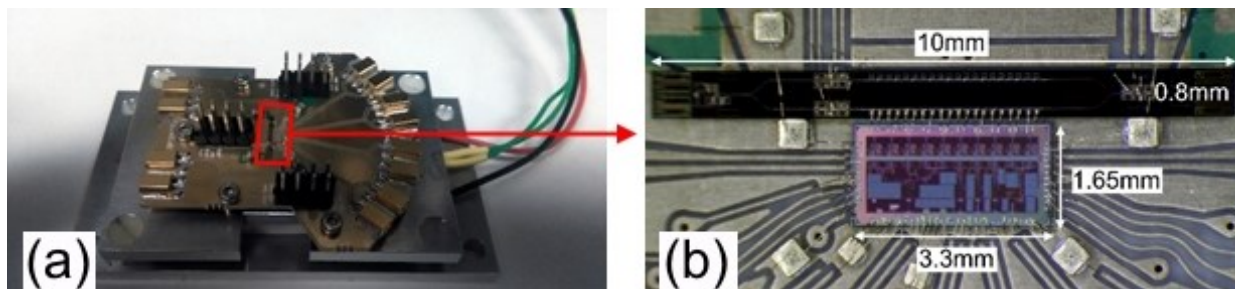

Fig. 1: (a) Test PCB assembly and (b) detail of bonded dies

channel differential output array with an output swing of 2.2 V_{pp}. This 10 channel configuration is a trade-off between a fully binary-weighted implementation and a thermometer coding[1]. Although the former minimizes the number of segments, the required driver loads range is significantly increased. On the other hand, in the case of thermometer coding, all segment lengths are equal, but the required number of channels increases exponentially with the desired resolution. As a consequence, the resulting power consumption rises drastically and integration becomes difficult. In the current design, various segment lengths are grouped to realize an effective binary weighted driving of the modulator. For this purpose, a 5×10 mapper circuit is included on chip, mapping the 5 input bits to the 10 output channels. The interaction length is made sufficiently long so as to be able to drive the modulator with the signal swing from an efficient tapered inverter chain, in a low-supply deep-submicron CMOS technology.

To match the optical signal propagation in the electronics, a timing architecture with tunable delays can be employed[2]. The designed delay control implementation has triple functionality and can be programmed through an SPI interface. First, there is an in-channel independent delay to compensate for process variations and load differences. Secondly, the inter-channel delay is controlled by a tunable transmission line to cope with accumulating delay differences resulting from a deviation in the optical signal velocity in the fabricated modulator. Finally, the direction of the propagation of the electrical signal can also be switched around, so that the driver chip can be used in multiple orientations. This is typically important in an assembly with an IQ-modulator, since it allows using an identical driver for both I and Q branches. The state-of-the-art segmented transmitter[3] is lacking this flexibility and as a result, two different versions of the driver IC are required for the IQ-solution. This would, of course, be troublesome for a cost-effective solution. Moreover, it lacks tunability to cover process variations which become more significant for higher bitrates.

The speed in this first version of the driver chip is limited to 15 GBaud due to a sub-optimal operation of the retiming cells which is resolved for the next tape-out, but the output stages are already showing their capability to drive the loads up to 28 GBaud. The total power consumption of the driver chip is around 1 W, with the output drivers contributing 10×40 mW (i.e. without taking into account the timing circuitry).

The fabricated IQ InP segmented modulator (IQ-SEMZM) footprint is 10 mm × 0.82 mm. It includes spot-size converters at the optical input and output, deeply-etched ridge waveguides, and multi-mode interferometers as splitters and couplers[4]. Each of the two SEMZMs has an active length, L_a = 2945 μm, divided in 10 segments of three different binary-weighted lengths. These segments match the driver IC outputs in both number and pitch. The fiber-to-fiber insertion loss is 10 dB at 1550 nm. The measured DC switching voltage V_π is equal to 1 V when a bias voltage of 7 V is applied, leading to a modulation efficiency of 0.29 V·dB. Since the IC driving voltage is well above $2 \cdot V_\pi$ full modulation depth is ensured.

Integration and assembly architecture
In the final assembly, two driver chips (I & Q) and the IQ-SEMZM will be mounted on opposite sides of a ceramic interposer. To enable early testing however, a 4-layer PCB was designed to host the IQ-modulator and a single CMOS driver (i.e. driving a single branch of the IQ structure). The distance between the two dies was minimized to keep parasitics low, and the driver outputs were directly wire bonded to the segments of a single SEMZM. The driver inputs, as well as the bias and SPI connections, were wire bonded to the board. The limited minimal trace width and spacing on a PCB allows connection of only 4 out of the 5 available input bits. Nonetheless, the operational concept and the designed architectures can be verified and optical amplitude/phase modulation can be evaluated.

Fig. 2: Experimental setup for the evaluation of the IC+IQ-SEMZM in back-to-back configuration.

Performance evaluation

The experimental setup shown in Fig. 2 was employed to evaluate the operation principle of the single SEMZM. The four input streams of the driver were provided by a Binary Pattern Generator (BPG) operating at 15 Gb/s, allowing the SEMZM to generate multi-level signals with 4-bit resolution. Biasing the modulator at the zero transmission point, combined amplitude and phase modulation was realized generating 4 and 8 point constellations in the form of 2-ASK-2-PSK (2 bits/symbol) and 4-ASK-2-PSK (3 bits/symbol). These formats were selected to show the potential for 16- and 64-QAM generation (assuming that the second MZM of the device would be driven in the same way).

The modulated signal output was then launched into a Variable Optical Attenuator (VOA) followed by an EDFA, in order to vary the optical signal-to-noise ratio (OSNR) and obtain back-to-back BER curves. The signal was received with a polarization-diversity coherent receiver and the resulting photocurrents were captured by a digital real time oscilloscope (33 GHz & 80 GSa/s) for further offline digital signal processing (DSP). In the DSP, the signal was resampled to 2 Sa/symbol and resynchronized with the Square Timing algorithm. The phase-entropy frequency offset estimation algorithm[5] was applied to compensate for the residual frequency difference between transmitter and local oscillator (LO) lasers, whereas the blind phase search algorithm was used to recover and track the phase of the signal. Prior to symbol detection, the signal was fed to a 31-tap symbol-spaced linear equalizer.

Fig. 3 depicts the measured BER of the two modulation formats as a function of OSNR (dotted lines). In order to roughly estimate the implementation penalties, the theoretical curves that would be obtained in an ideal AWGN channel are included in the plot (N.B.: the signal bandwidth was assumed to be twice the symbol rate). The 2-ASK-2-PSK signal exhibts negligible penalty (< 1 dB) for a BER equal to a hard-decision (HD)-FEC limit of $3.8 \cdot 10^{-3}$, whereas for the 8-level signal (4-ASK-2-PSK) the penalty is 1.95 dB. Fig. 3 shows the constellation points generated by the single SEMZM. In an IQ implementation (i.e. 2 SEMZM branches), two of these 4- and 8-level signals can be combined to generate 16- and 64-QAM formats.

Conclusions

A first optical transmitter prototype comprising of a segmented-electrode IQ-MZM driven by low power CMOS drivers has been demonstrated. Negligible implementation penalties for 2-ASK-2-

PSK and 4-ASK-2-PSK formats is achieved, showing potential for generating formats up to 64-QAM, using only binary driving signals.
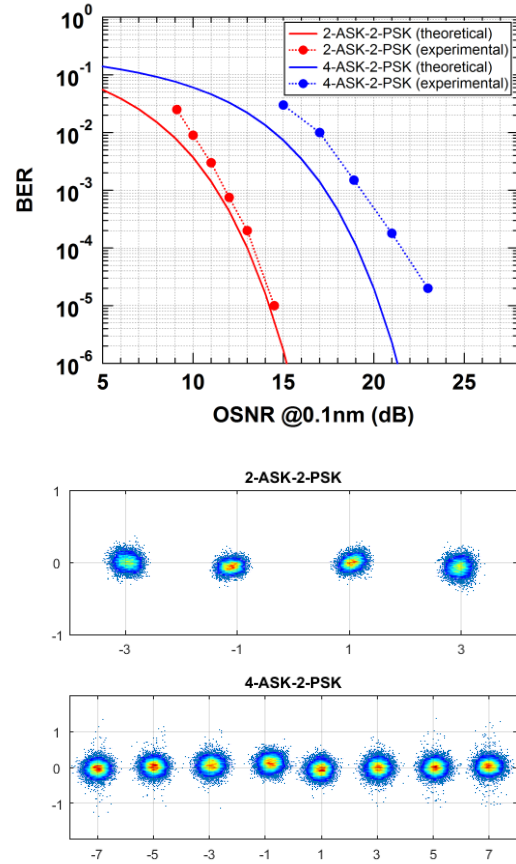
Fig. 3: (top) BER vs OSNR for the two modulation formats examined and a comparison with the theoretical curves for an AWGN channel. (bottom) Constellation diagrams obtained at the highest OSNR values

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