A 2x50 Gb/s PAM-4 driver IC integrated with a 1.5 µm VCSEL array

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Currently available optical datacenter transceivers exploit four lanes of 25 Gb/s to satisfy the 100 Gigabit Ethernet standard. Transitioning to PAM-4 modulation could extend the data rate while still using existing interfaces or optical devices. To evaluate the feasibility, we have designed a dual-channel PAM-4 driver IC in 130 nm SiGe BiCMOS, featuring a 4-tap symbol-spaced equalizer to drive a 1.5 µm VCSEL array. Both channels achieve a back-to-back BER below 1E-6 at 50 Gb/s. With 430 mW per channel, the presented VCSEL transmitter can be an efficient alternative to double the lane rate across single-mode fiber.

Introduction

Available 100 Gigabit Ethernet (GbE) optical transceivers such as QSFP28 or CFP4, utilize four lanes of 25 Gb/s with on-off keying (OOK) to achieve an aggregate data rate of 100 Gb/s. The integrated transmitter directly modulates either 850 nm vertical-cavity surface-emitting lasers (VCSELs) or power-hungry 1310 nm distributed-feedback (DFB) lasers depending on the required transmission distance. As the IEEE 802.3 task force is targeting 400 Gb/s across link lengths up to 2 km, single-mode lasers are favored over the multi-mode ones because of the transmission problems associated with modal dispersion. However, a significant amount of power can be saved by directly modulating long-wavelength single-mode VCSELs instead. In a short amount of time, these VCSELs have significantly improved in performance with small-signal bandwidths ranging up to 22 GHz and showing modulation rates up to 50 Gb/s by non-return-to-zero (NRZ) and without equalization [1]. By incorporating 2-tap feed-forward equalization (FFE) in an NRZ driver integrated circuit (IC), long-wavelength VCSELs were able to operate up to 56 Gb/s error-free [2].

An approach that is heavily considered for the next generation Ethernet standards is the use of 4-level pulse amplitude modulation (PAM-4) to double the data rate. This would effectively enable lane rates of 50 Gb/s while exploiting existing 25 Gb/s electrical interfaces. Recent experiments achieve data rates of 56 Gb/s by directly modulating long-wavelength VCSELs with pulse pattern generators (PPG) and applying offline equalization and forward error correction (FEC) at the receiver side [3]. However, to verify the real performance of PAM-4 VCSEL based links, experiments must be conducted that consist of dedicated ICs to generate the PAM-4 signal and directly modulate the laser. Recent VCSEL driver ICs verified in an optical link combine two NRZ data streams to generate a PAM-4 signal and either use a 2-tap FFE output stage to achieve 40 Gb/s at 1.5 µm [4] or use a high-bandwidth InP transistor technology for the driver to obtain 56 Gb/s at 850 nm [5].

In order to test the feasibility of 50 Gb/s multi-lane VCSEL links operating in the C-band, we developed a PAM-4 driver IC with a symbol-spaced 4-tap FFE output stage driving a dual-channel 1.5 µm VCSEL array. One channel was already tested up to 56 Gb/s [6], but for this paper we investigate the performance of both channels.

PAM-4 driver IC

The reported VCSEL driver is an improved and more versatile version of the 40 Gb/s PAM-4 driver [4]. The block diagram of the data path is shown in Figure 1. Two single-ended binary data streams MSB and LSB are synchronized with each other through retiming flip-flops before they are combined at the output stage. The tap coefficients A_0 to A_3 of the MSB path are twice as large as the LSB path creating the multi-level current. This current can be predistorted by changing the magnitude and the sign of the coefficients A_1 to A_3. The delay between consecutive FFE taps is derived from a cascade of flip-flops and corresponds to one symbol period. The effectiveness of the equalization is therefore independent of the data rate. Moreover, this topology consumes less power and area than a fractionally-spaced symbol delay implemented with delay cells [2]. Setup and hold time violations are resolved by preceding the FFE chain with an additional flip-flop and programmable delay cells. The reference clock is converted and amplified to a differential signal to drive the MSB and LSB flip-flops. The back termination resistor is changed from 50 Ω [4] to 160 Ω to increase the drive efficiency and dampen the peaking in the optoelectronic response. The driver can deliver a total average current of 29 mA into a 50 Ω equivalent load if the settings for the bias current (i_{bias}) and the FFE coefficients are maximized.

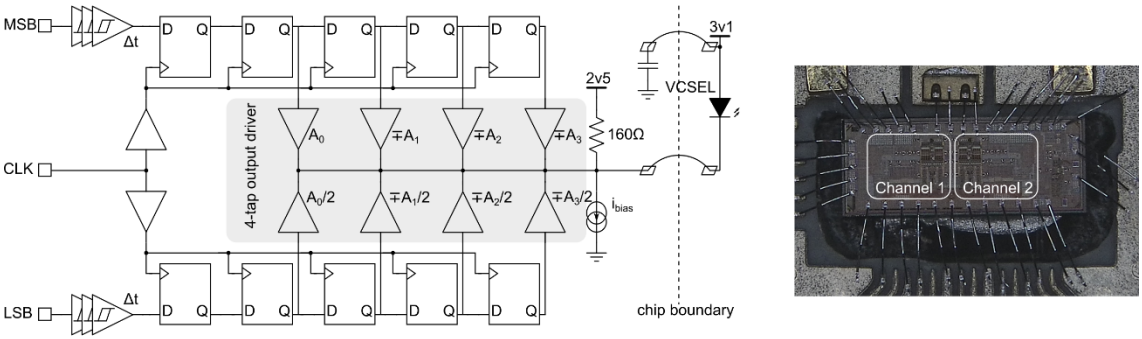

Figure 1: Block diagram and micrograph of the PAM-4 driver IC with integrated long-wavelength 2x1 VCSEL array.

Experiments

The driver IC is fabricated in a 130 nm SiGe BiCMOS process from ST Microelectronics and measures 1x2.8 mm^2. Interconnection to the printed circuit board and the VCSELs occurs through wire bonding and is depicted in the right part of Figure 1. The VCSEL was developed by the Technische Universität München and has a bandwidth of 22 GHz [1]. The tunnel junction diameter measures 4 µm and light is emitted at a wavelength of 1533 nm. The threshold current is only 0.9 mA while the rollover current is 9 mA. This corresponds to an optical power of 2.3 mW. The differential series resistance is characterized at 62 Ω.

MSB and LSB inputs are excited with an AC-coupled 300 mV 2^7-1 PRBS signal. Both streams are decorrelated from each other by introducing a cable delay difference of 1 ns and an inversion. The full-rate clock signal needs an output power of 2 dBm to bridge

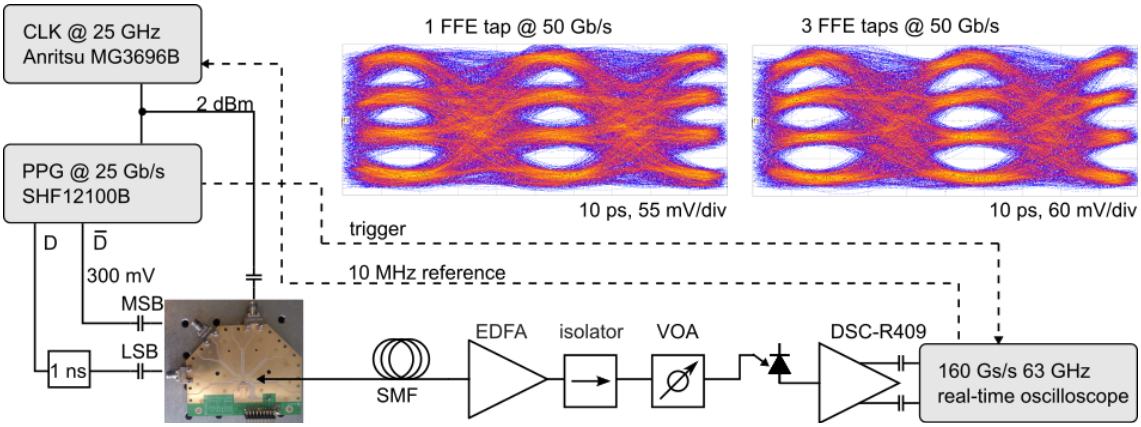

Figure 2: Optical measurement setup for testing channel 2 of the VCSEL driver at 50 Gb/s.

the losses introduced by the board traces. Despite alignment of the flat-cut fiber to the aperture of the VCSEL, coupling losses of 8 dB still exist which enforces us to insert an erbium-doped amplifier (EDFA) in the optical link, as seen in Figure 2. The receiver side is composed of a linear 32 GHz 500 V/W photodiode and transimpedance amplifier (DSC-R409) connected to the differential inputs of a 160 GS/s real-time oscilloscope. The clock generator is synchronized with the 10 MHz reference output from the oscilloscope to avoid time shifting of the recorded waveform. Offline processing of the received PAM-4 signal, with a record length of 2.8×10^7 bits, recovers the MSB and LSB stream and compares them to the reference PRBS to calculate the total bit-error ratio (BER). BER plots are generated by varying the received input power with a variable optical attenuator (VOA). To study the impact of the multi-tap FFE on the link performance, the number of taps is increased for each consecutive BER plot at 25 GBd. The average VCSEL current is fixed at 6.9 mA and tap coefficients are scaled to achieve identical steady-state modulation amplitude for all BER plots. FFE parameters are calculated offline by running a minimum mean square error algorithm on the received PAM-4 signal followed by a manual optimization. Each channel is measured separately to exclude crosstalk, thereby evaluating the maximum link performance.

Results and discussion

Predistorting the output current of the VCSEL driver with a 4-tap FFE significantly reduces the inter-symbol interference of the PAM-4 signal as can be noticed in the 25 GBd eye diagrams of channel 2 in Figure 2. This statement can also be derived from the BER plots at 25 GBd for both channels in Figure 3. Considering a RS(544,514) code with a pre-FEC BER limit of 5.2×10^{-4}, sensitivity is improved by 2.4 dB for channel 1 and 1.2 dB for channel 2. The discrepancy in sensitivity is assumed to be related to the accidental asymmetric wire bonding layout of the VCSEL array, observed in Figure 1. Nevertheless, at maximum input power, a 3-tap FFE is still able to achieve results well below FEC limit with a BER smaller than 10^{-6}. For channel 2, the transition from 1 to 2 taps lead to no difference as tap 2 was optimally set to zero. On the other hand, a marginal improvement can be observed for channel 1 when enabling the second tap. In both cases however, a 3-tap FFE results in the best trade-off between gain in sensitivity, driver complexity and power consumption. Consuming 430 mW per channel at 50 Gb/s, this results in an 8.7 pJ/bit efficiency, which is slightly better than the other SiGe BiCMOS PAM-4 driver [4] and more than twice as efficient as the 56 Gb/s NRZ driver

[2]. The comparison with the more efficient InP PAM-4 driver [5] is not really valid in this case since that driver synchronizes the MSB and LSB streams off-chip while we do it on-chip.

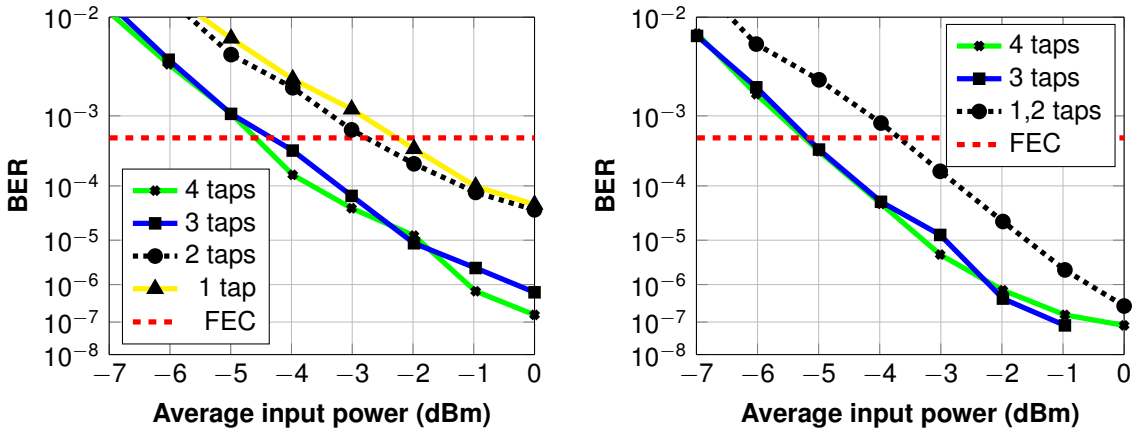

Figure 3: BER curves vs. number of FFE taps at 50 Gb/s PAM-4 for channel 1 (left) and channel 2 (right) of the VCSEL driver.

Conclusion

We have developed a SiGe BiCMOS PAM-4 driver IC that was implemented with a 4-tap symbol-spaced FFE output stage. Experiments at 50 Gb/s with a 22 GHz 1.5 µm 2x1 VCSEL array revealed that a 3-tap configuration is most efficient in reducing the BER in a back-to-back link for both channels. However, these results were obtained for each channel separately. To investigate the real performance in an array configuration, crosstalk should be taken into account by exciting both channels simultaneously.

Acknowledgments

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