Nieuwe ontwerpstrategieën en architecturen
voor Sigma-Delta-modulatoren in continue tijd

Novel Design Strategies and Architectures
for Continuous-Time Sigma-Delta Modulators

Bart De Vuyst

Promotor: prof. dr. ir. P. Rombouts
Proefschrift ingediend tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Elektronica en Informatiesystemen
Voorzitter: prof. dr. ir. R. Van de Walle
Faculteit Ingenieurswetenschappen en Architectuur
Academiejaar 2014 - 2015

UNIVERSITEIT
GENT

ISBN 978-90-8578-798-3
NUR 959
Wettelijk depot: D/2015/10.500/42

Universiteit Gent
Faculteit Ingenieurswetenschappen
Vakgroep Elektronica en Informatiesystemen

Promotor: Prof. dr. ir. Pieter Rombouts

Universiteit Gent
Faculteit Ingenieurswetenschappen

Vakgroep Elektronica en Informatiesystemen
Sint-Pietersnieuwstraat 41
B-9000 Gent, België

Tel.: +32-9-264.33.66
Fax.: +32-9-264.35.94

Examencomissie: Prof. dr. ir. Patrick De Baets - Voorzitter
Dr. ir. Guy Torfs - Secretaris
Prof. dr. ir. Luis Hernandez
Prof. dr. ir. Georges Gielen
Prof. dr. ir. Johan Bauwelinck
Prof. dr. ir. Jan Doutreloigne
Prof. dr. ir. Marc Moeneclaey

Dit werk kwam tot stand in het kader van een beurs van het FWO-Vlaanderen.

Proefschrift tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen: Elektrotechniek
Academiejaar 2014-2015

I did it my way.

- My Way, Frank Sinatra
lyrics by Paul Anka -

Acknowledgements
Dankwoord

"My way" was het zeker, al had ik 8 jaar geleden toen ik aan dit werk begon misschien wel een ander traject voor ogen. Een stuk ouder, en hopelijk wat wijzer, kijk ik toch terug met enige trots. Toegegeven, af en toe was het een mentale beproeving en leek een marathon er niets bij (zelfs niet die van Eindhoven), maar toch mag het eindresultaat er wezen. Een eindresultaat dat niet alleen ontstaan is door mijn inspanningen, maar ook door de hulp en steun van vele anderen.

Eerst en vooral dank ik mijn promotor prof. Rombouts. Pieter, reeds als thesisbegeleider heb je mijn interesse voor de analoge elektronica aangewakkerd. Je wijze raad en steun heb ik steeds geapprecieerd. In dit doctoraat geldt zeker de leuze "de aanhouder wint", al is het niet altijd duidelijk geweest wie nu die aanhouder was: jij of ik? Dank je om mij de kans te geven om het werk toch nog af te ronden, ondanks mijn plotse carrièrewending richting de industrie.

Daarnaast dank ik ook al mijn ex-collega's van de CAS groep. Ludo, de vele gesprekken die we samen hadden, werden steeds gesmaakt in wijlen de Overpoortresto. Johan, het was fijn dat je altijd klaarstond als klankbord voor wilde onderzoeksideeën. Stijn, Benoit, Pierre en Maarten, de andere doctoraatstudenten van mijn generatie.

Niet alleen professioneel, maar ook op persoonlijk vlak was ik steeds goed omringd. De schoonfamilie, of zoals zij zouden zeggen de *koede* kant, was altijd van de partij. Soms zelfs met dat tikkeltje teveel enthousiasme. Ook aan mijn familie, ik ben jullie erg dankbaar voor de nodige steun en toeverlaat. Dank je voor jullie familiale warmte en liefde al deze jaren.

Mama, bedankt om mij de kans te geven om te studeren wat ik wou. Een duw in de juiste richting was zeker jouw beslissing destijds voor de aankoop van onze allereerste computer. Dit waren voor ons gouden tijden, waarin we onze technische creativiteit konden botvieren! Dankjewel Peter en Pascal, dat ik deze tijden samen met jullie kon beleven.

Acknowledgements - Dankwoord

De quizgenoten van 4Hand verdienen ook hun plaats in dit dankwoord. Naast de welgekomen ontspanning van het quizzen zelf, dank ik jullie ook voor de hilarische momenten die we samen beleefd hebben, onder andere op onze jaarlijkse BBQ.

De *burgie*-vrienden wens ik te danken voor de vele leuke momenten tijdens onze studententijd, zoals de talrijke voetbalavonden op mijn kot. Maar ook na onze gemeenschappelijke Gent-tijd is het nog altijd fijn om jullie terug te zien.

In het bijzonder wil ik de bende van 6 danken, en hun weergaloze "WAGs". Het is nu tijd om een nieuw onderwerp te vinden om me te plagen. Ook al zijn we ondertussen allemaal wat verder uitgezwermd, toch ben ik ervan overtuigd dat we bij elkaar een vriendschap voor het leven gevonden hebben. Ik kijk alvast uit naar al onze toekomstige avonturen.

De belangrijkste persoon die ik in dit dankwoord wil vermelden is mijn *patner* (in crime). Domi, jij hebt mij steeds gesteund om deze queeste tot een goed einde te brengen. En ja, je hebt veel geduld moeten hebben. Gelukkig waren we zoals steeds goed uitgebalanceerd, ik doctorerend, jij dokter-lerend. Ik wil je ook oprecht feliciteren voor het winnen van de wedloop om het doc/kter-schap.

Ik ben ervan overtuigd dat we uit ons gemeenschappelijk traject veel geleerd hebben en dat het ons alleen maar sterker heeft gemaakt als koppel. Ik kijk dan ook uit naar onze fantastische toekomst samen.

Gent, mei 2015
Bart De Vuyst

Samenvatting

Wegens de technologische schaling in geavanceerde sub-micron processen, gebeurt steeds meer signaalverwerking in het digitale domein. Dit vereist analoog-naar-digitaal (A/D) omzetters die niet alleen zeer nauwkeurig moeten zijn, maar ook aan hoge snelheid moeten kunnen opereren. Door economische factoren, moeten deze omzetters bovendien geïntegreerd worden op dezelfde chip als de digitale verwerkingseenheid. $\Sigma\Delta$-modulatie is een conversiemethode om zeer nauwkeurige analoog-naar-digitaal omzetters (ADCs) te implementeren. De methode combineert het effect van overbemonstering met dat van ruiskneding, door het gebruik van een resonant lusfilter. Afhankelijk van de implementatie van het lusfilter, ontstaat ofwel een $\Sigma\Delta$-modulator in discrete-tijd (DT) of continue-tijd (CT).

$\Sigma\Delta$-modulatoren in discrete-tijd zijn ondertussen vrij matuur geworden, door hun implementatie met geschakelde condensator circuits. De laatste tijd, is er in de wetenschappelijke wereld een verhoogde interesse ontstaan voor $\Sigma\Delta$-modulatoren in continue-tijd. Een belangrijke reden hiervoor is net de technologieschaling. CT $\Sigma\Delta$-modulatoren zijn beter verenigbaar met kleinere technologieën, omdat hoog performante schakelaars niet langer noodzakelijk zijn voor hun implementatie. Bovendien treedt het effect van frequentie vouwing niet op, door het continue-tijdskarakter van de lus. Dit zorgt ervoor dat de signaalbandbreedte voor CT $\Sigma\Delta$-modulatoren kan worden uitgebreid tot in het brede MHz bereik.

Een belangrijk voordeel van de CT $\Sigma\Delta$-modulator, is het impliciete anti-frequentieverwarrings filter. Door de werking in continue-tijd, bevat de signaal transfer functie inherent onderdrukking op hoge frequenties. Alhoewel, in de meeste gevallen bevat deze functie ook een piek in de transitie van de signaalband naar hoge frequenties, die de modulator kan oversturen. Zeker voor ADCs gebruikt in communicatie standaarden is dit ongewenst gedrag. De transitieband piek is gecorreleerd aan de topologie van het lusfilter. Een lusfilter in terugkoppelingstopologie (Engels: feedback, FB) heeft algemeen gezien de laagste transitieband piek, een lusfilter in voorwaartse topologie (Engels: feedforward, FF) de hoogste.

Samenvatting

Tot nu toe, is er in de literatuur geen duidelijke ontwerpstrategie voor ΣΔ-modulatoren in continue-tijd naar voor geschoven. Ondanks het feit dat er een wiskundige equivalentie kan gedefinieerd worden tussen de ruis transfer functies (Engels: noise transfer function, NTF) van zowel CT als DT modulatoren, toch kunnen de ontwerpstrategieën voor DT modulatoren niet zonder meer aangewend worden. De lus van een ΣΔ-modulator in continue-tijd is meer onderhevig aan parasitaire effecten, die enkel van tweede orde zijn voor DT modulatoren. Een belangrijk effect is dat van bijkomende lusvertraging (Engels: excess loop delay, ELD) in het terugkoppelpad, wat ervoor zorgt dat de orde van de NTF zal stijgen. Op die manier ontstaat een beperking op het ontwerp, want het aantal ontwerpparameters is niet langer toereikend om elke mogelijke NTF te implementeren. Ook is er het effect van een parasitaire pool in de transfer functie van de integrator. In een *RC*-actieve implementatie van de integrator wordt deze parasitaire pool gevormd door de lusbandbreedte van de lokale terugkoppeling rond de operationele versterker. Bovendien zijn sommige van de parameters van het continue-tijd systeem model onderhevig aan variaties. Bijvoorbeeld zullen proces variaties hoofdzakelijk de nauwkeurigheid van de integrator coëfficiënten van het lusfilter beïnvloeden.

In dit werk worden 2 nieuwe ontwerpstrategieën voor CT ΣΔ-modulatoren geïntroduceerd. Beide richten ze zich op multibit kwantisatie, voor ΣΔ-modulatoren in continue-tijd met een lage overbemonsteringsfactor (Engels: oversampling ratio, OSR). In beide strategieën wordt een nominaal continue-tijd systeem gedefinieerd, dat meteen al sommige van de parasitaire effecten, eigen aan CT ΣΔ-modulatie, bevat. In de eerste strategie, wordt het Nyquist criterium aangewend om robuuste stabiliteit te kwantificeren. Deze robuustheid wordt slechts geoptimaliseerd voor de nominale modulator, zonder parameter variaties. De ontwerpstrategie resulteert in robuuste modulatoren, in het bijzonder voor modulatoren met beperkte controle.

In de meeste gevallen kunnen de parameter variaties vrij goed op voorhand afgelijnd worden. In een tweede ontwerpstrategie, introduceren we een nieuw robuustheidsgetal, het $\mathcal{S}$-getal, dat de variaties op sommige parameters mee in rekening brengt. Hierdoor zal de resulterende modulator een gegarandeerde performantie halen, ook wanneer de parameter variaties in het spel komen. Daarnaast laat het $\mathcal{S}$-getal ook toe de performantie criteria uit te breiden. Niet alleen stabiliteit is nu een mogelijk ontwerpcriterium, maar er worden ook voorbeelden gegeven die de jitter-gevoeligheid optimaliseren alsook de transitieband piek van de signaal transfer functie.

Voor ΣΔ-modulatoren met een zeer hoge verwerkingssnelheid, ontstaat er

een probleem bij het gebruik van multibit kwantisatie. Zowel de multibit terugkoppel digitaal-naar-analoog omzetter (DAC), als de kwantisatie-eenheid worden zeer uitdagend qua circuit implementatie. Tijdsencodering werpt zich op als een veelbelovende techniek om de grootste problemen van multibit kwantisatie te vermijden, terwijl toch multibit performantie behouden blijft. Hierbij wordt de multibit amplitude kwantisatie vervangen door een kwantisatie in de tijd. Hierdoor wordt deze techniek beschouwd als uitermate geschikt in de hedendaagse sub-micron technologieën die uitblinken in hun verbeterde tijdsresolutie. Een overzicht van tijdsencoderende technieken uit de literatuur wordt gegeveven: het gebruik van een VCO-gebaseerde kwantisatie-eenheid en het gebruik van een pulsbreedte modulatie (Engels: pulsewidth modulation, PWM) terugkoppel DAC.

Verder wordt er aandacht geschonken aan synchrone zelf-oscillerende CT $\Sigma\Delta$-modulatoren. Bij deze modulatoren wordt tijdsencodering gecombineerd in zowel de kwantisatie-eenheid als de terugkoppel DAC. Deze oplossing vereist slechts een 1-bit kwantisatie-eenheid of comparator evenals een 1-bit terugkoppel DAC, wat een belangrijke reductie vormt in de circuit complexiteit. Een opzettelijke zelf-oscillatie, op een gehele fractie van de klokfrequentie, wordt in de $\Sigma\Delta$ lus geïnstalleerd. De ingangsspanning moduleert de uitgangsoscillatie in pulsbreedte. Hierdoor hoeven de componenten in het lusfilter enkel signalen op de gereduceerde zelf-oscillatie frequentie verwerken. Een extra voordeel van een zelf-oscillerende $\Sigma\Delta$-modulator is zijn verbeterde jitter gevoeligheid. In tegenstelling tot bij een conventionele CT $\Sigma\Delta$-modulator, is het jittervermogen in de signaalband niet afhankelijk van de agressiviteit van het lusfilter. Daarentegen is er een vaste bijdrage doordat het uitgangssignaal in elke oscillatieperiode 2 keer omschakelt.

Een tweede orde prototype van een zelf-oscillerende CT $\Sigma\Delta$-modulator werd ontworpen. In dit ontwerp is een extra toevoeging de eindige impulsrespons (Engels: finite impulse response, FIR) terugkoppel DAC. Deze zorgt ervoor dat de jitter gevoeligheid verder verlaagd wordt en relaxeert ook de vereisten op de slewrate van de eerste operationele versterker in de lus. De prototype modulator toont een dynamisch bereik van 66 dB voor een 5 MHz bandbreedte. Door de lage circuitcomplexiteit, is de oppervlakte van de kern van de modulator slechts $0.025\,\mathrm{mm}^2$.

Summary

Due to technology scaling in deep sub-micron technologies, more and more signal processing is performed in the digital domain. This requires high-accuracy analog-to-digital (A/D) and digital-to-analog (D/A) converters with a higher conversion speed. Because of economic benefits, these converters should be integrated on the same chip as the digital processing core. $\Sigma\Delta$ modulation is a conversion scheme to implement high-accuracy analog-to-digital converters (ADCs). It combines the effects of oversampling and noise shaping by means of a resonant loop filter. Depending on the implementation of the loop filter, either a discrete-time (DT) or a continuous-time (CT) $\Sigma\Delta$ modulator results.

Discrete-time $\Sigma\Delta$ modulators have become very mature because of the implementation with switched capacitor circuits. In the last decade, a renewed interest for continuous-time $\Sigma\Delta$ modulators has appeared in the research field. An important driver for this is technology scaling. CT $\Sigma\Delta$ modulators are more compatible with smaller technology nodes, as high performance switches are no longer required. In addition, the lack of frequency folding due to the continuous-time nature of the loop, provides the possibility of extending the signal bandwidth into the wide MHz range.

An important advantage of a CT $\Sigma\Delta$ modulator is the implicit anti-aliasing filter. Due to the continuous-time operation, the signal transfer function (STF) inherently contains suppression for higher frequencies, before the sampling operation occurs in the quantizer. However, peaking can still occur in the transition from the signal band to higher frequencies. This could overload the modulator. Certainly for ADCs used in communication standards, this is undesired behaviour. The out-of-band peaking is correlated to the loop filter topology. A feedback topology generally has the lowest out-of-band peaking, the feedforward topology has the strongest.

So far, no clear design strategy for CT $\Sigma\Delta$ modulators has been reported in literature. Although a mathematical equivalence can be defined between the noise transfer functions (NTFs) of both CT and DT modulators, the well-known design strategies for DT modulators cannot be applied as such. The loop of the CT $\Sigma\Delta$ modulator is more sensitive to several parasitic effects,

which are only of second order for DT modulators. An important effect is that of excess loop delay (ELD) in the feedback path of the modulator, which will increase the order of the modulator's NTF. This leads to a constrained design, where the number of design parameters no longer suffices to implement any NTF possible. Also, parasitic poles in the integrator transfer functions occur in reality. In an *RC*-active implementation for the integrators, a parasitic pole appears due to the gain-bandwidth product (GBW) of the opamp feedback loop. On top of that, some of the continuous-time system-model parameters are usually prone to variations. For example, process variations will mainly influence the accuracy of the loopfilter integrator coefficients.

In this dissertation, two new design strategies for CT $\Sigma\Delta$ modulators are proposed. Both of them focus on multibit quantization, for CT $\Sigma\Delta$ modulators with a low oversampling ratio (OSR). In both of the design strategies, a nominal continuous-time system is defined, which already includes some of the parasitic effects specific to CT $\Sigma\Delta$ modulation. In a first design strategy we use the Nyquist criterion to install a stability robustness figure-of-merit. The robustness is only optimized for the nominal modulator, without any parameter variations. The design strategy provides robust modulator solutions, particularly for constrained designs.

In most cases, the parameter variations can be well defined a-priori. In a second design strategy, we introduce a new figure of merit, the $\mathcal{S}$-figure which does take into account the a-priori knowledge of the variation spread. As a result, a guaranteed performance of the modulator is obtained, even when subjected to variations. Next to this, the $\mathcal{S}$-figure is also interesting, because it allows to define more general performance requirements. Design examples are given to control not only stability robustness but also the modulator's jitter performance or the STF out-of-band peaking.

For very high-speed $\Sigma\Delta$ modulators, multibit quantization tends to become cumbersome in deep sub-micron technologies. Both the multibit feedback DAC and the quantizer become hard to realize. Time-encoding is employed as a promising technique to avoid the main issues from multibit quantization, while preserving multibit performance. Essentially, the multibit quantization is replaced by a quantization in time. As such, this solution is considered to be very well suited for today's ultra deep sub-micron technology, which should be able to provide ample time resolution. An overview of techniques already presented in literature is given, like VCO-based quantization or the use of a pulsewidth modulation (PWM) feedback DAC.

Further attention is given to synchronous self-oscillating CT $\Sigma\Delta$ modula-

tors. Here, time-encoding is combined in both the quantizer and the feedback DAC. This solution only requires a single-bit quantizer (comparator) and a single-bit feedback DAC, which is an important reduction in design complexity. A deliberate self-oscillation is installed in the $\Sigma\Delta$ loop, at a rational fraction of the clock frequency. The input will modulate the output oscillation in a PWM fashion. As a result, the loopfilter building blocks only have to process signals at the lower self-oscillation frequency. An extra benefit of a self-oscillating $\Sigma\Delta$ modulator is its jitter performance. In contrast to a conventional CT $\Sigma\Delta$ modulator, the in-band jitter does not rely on the loopfilter's aggressiveness, but instead it is fixed as the output signal merely toggles twice per self-oscillation period.

A second order self-oscillating CT $\Sigma\Delta$ modulator prototype was designed. An additional key element in this design, is the use of a feedback finite-impulse-response digital-to-analog converter (FIRDAC) which further reduces the jitter sensitivity and relaxes the slewing requirements of the first operational amplifier in the loop. The prototype modulator achieves a dynamic range (DR) of 66 dB for a 5 MHz bandwidth. Due to the low complexity of the circuit, the modulator core area is only $0.025\,\mathrm{mm}^2$.

Table of Contents

IV Closing Remarks

V Appendices

List of Figures

List of Tables

List of Abbreviations

A/D analog-to-digital.

AAF anti-aliasing filter.

ADC analog-to-digital converter.

CILFD complementary injection-locked frequency divider.

CMFB common-mode feedback.

CMOS complementary metal-oxide-semiconductor.

CT continuous-time.

D/A digital-to-analog.

DAC digital-to-analog converter.

DEM dynamic element matching.

DR dynamic range.

DT discrete-time.

DWA data-weighted averaging.

ELD excess loop delay.

ENOB effective number of bits.

FB feedback.

FF feedforward.

FIRDAC finite-impulse-response digital-to-analog converter.

FOM figure of merit.

GBW gain-bandwidth product.

GM gain margin.

IBQN in-band quantization noise.
IIT impulse-invariant-transformation.
ISI inter-symbol interference.

MASH multi-stage noise shaping.
MOS metal-oxide-semiconductor.
MSA maximum stable amplitude.

NRZ non-return-to-zero.
NTF noise transfer function.

OSR oversampling ratio.

PDK process design kit.
PM phase margin.
PWM pulsewidth modulation.

RZ return-to-zero.

SAR successive approximation.
SC switched capacitor.
SNDR signal-to-noise and distortion ratio.
SNR signal-to-noise ratio.
SOPA self-oscillating power amplifier.
SQNR signal-to-quantization-noise ratio.
STF signal transfer function.

VCO voltage-controlled oscillator.

ZOH zero-order-hold.

List of Publications

The content of this work has led to several research contributions in the field of CT $\Sigma\Delta$ modulators. Besides some stand-alone publications, the research can be roughly divided in two major parts:

Novel design strategies for CT $\Sigma\Delta$ modulators. In this part we focus on design strategies leading to robust CT $\Sigma\Delta$ modulators with multibit quantization. In [J1] a robust design strategy based on the Nyquist criterion is proposed. Further research has led to a more general robustness criterion, the $\mathcal{S}$-figure, described in [J2].

Novel architectures for CT $\Sigma\Delta$ modulators. In this part we focus on time-encoding as an emerging architectural direction for the design of CT $\Sigma\Delta$ modulators in deep sub-micron technologies. In [J3, C3] the design and measurement of a second-order self-oscillating $\Sigma\Delta$ modulator prototype has been reported.

Publications in International Journals

J1. **B. De Vuyst**, P. Rombouts, J. De Maeyer, and G. Gielen, "The Nyquist Criterion: A Useful Tool for the Robust Design of Continuous-Time $\Sigma\Delta$ Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 57, no. 6, pp. 416–420, 2010.

J2. **B. De Vuyst**, P. Rombouts, and G. Gielen, "A Rigorous Approach to the Robust Design of Continuous-Time $\Sigma\Delta$ modulators," *IEEE Trans. Circuits Syst.-I*, vol. 58, no. 12, pp. 2829–2837, 2011.

J3. **B. De Vuyst** and P. Rombouts, "A 5-MHz 11-Bit Self-Oscillating $\Sigma\Delta$ Modulator with a Delay-Based Phase Shifter in 0.025 mm^2," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1919–1927, 2011.

Publications in the Proceedings of International Conferences

C1. P. Peev, **B. De Vuyst**, P. Rombouts, and A. Hamoui, "An Anti-Aliasing Filter Inspired by Continuous-Time ΣΔ Modulation," *Proc. IEEE Int. Conf. Electronics, Circuits and Syst. (ICECS)*, pp. 854–857, 2008.

C2. B. Catteau, **B. De Vuyst**, P. Rombouts, and L. Weyten, "A 14-bit 250MS/s Digital to Analog Converter with Binary Weighted Redundant Signed Digit Coding," *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, pp. 3345–3348, 2010.

C3. **B. De Vuyst** and P. Rombouts, "A 5-MHz 11-bit Delay-Based Self-Oscillating ΣΔ modulator in 0.025 mm2," *Proc. IEEE Custom Integ. Circuits Conf. (CICC)*, pp. 1–4, 2010.

Part I

Introduction

Chapter 1

Research Scope and Goal

1.1 Research Scope

The continuous scaling of complementary metal-oxide-semiconductor (CMOS) deep sub-micron technologies has led to massive integration of high-complexity electronic systems. The scaling is mainly digital driven, as it allows to integrate more digital functionality on the chip for each new technology node, while it reduces the power consumption per gate at the same time. The area efficiency and flexibility of digital electronics is exploited to implement large parts of the signal processing in the digital domain. The fact that digital signal processing is inherently "noise-free", is a huge benefit. Furthermore, in contrast to analog design, digital design is highly automated. The signals which have to be processed are in most cases still analog of nature. This requires high-accuracy analog-to-digital (A/D) and digital-to-analog (D/A) converters, which interface with the digital core. Due to economic benefits, these converters should be integrated as much as possible on the same chip as the digital core.

In contrast to digital gates, high-accuracy analog circuits usually do not benefit from technology scaling. A first problem lies in the fact that the supply voltage decreases for more advanced technology nodes. For 90 nm, the core supply voltage has already become as low as 1.2 V. This limits the signal range for analog input signals and thus requires to push thermal noise-levels down for the same desired accuracy-level. Furthermore, it prevents the application of cascoding, which has been extensively used to implement high-gain amplifier stages. Finally, the conduction of metal-oxide-semiconductor

(MOS) switches decreases. The threshold voltage of the MOS devices does not scale proportional to the supply voltage. Low-ohmic MOS switches are required to implement switched capacitor (SC) circuits. A second problem which arises, is the intrinsic gain deterioration of the MOS transistor, mainly due to the reduction of the output impedance.

$\Sigma\Delta$ modulation is a data-conversion technique to implement high-accuracy analog-to-digital converters (ADCs). In contrast to other ADC topologies, the accuracy does not heavily rely on component matching. $\Sigma\Delta$ modulators trade off time resolution for amplitude accuracy by using oversampling and noise shaping. Discrete-time (DT) $\Sigma\Delta$ modulators have become very mature because of the implementation with SC circuits. They have dominated the $\Sigma\Delta$ modulator designs for many years. Recently, continuous-time (CT) $\Sigma\Delta$ modulators have attracted more attention because of their possibility of extending the ADC bandwidth into the wide MHz range. In contrast to their discrete-time counterparts, the loopfilter is now a continuous-time filter, which allows higher bandwidth processing. Also CT $\Sigma\Delta$ modulators are more compatible with the technological scaling trend, due to the absence of high performance switches. The higher bandwidth possibilities, combined with multibit quantization, have even led to the use of CT $\Sigma\Delta$ modulators for communication transceivers with MHz bandwidth and 10-12 bit resolution. In addition, the fact that $\Sigma\Delta$ modulation can be easily combined with bandpass A/D conversion has increased its popularity in analog front-ends for communication chips.

1.2 Goal and Outline

In this work we investigate the use of a continuous-time $\Sigma\Delta$ modulator as an analog-to-digital converter. We specifically focus on the modulator itself, being the analog core of the converter. The design of the digital decimation filter, to downsample the output data stream, is outside the scope of this work. The goal of the research is twofold. First of all, new design strategies for CT $\Sigma\Delta$ modulators have been developed. So far, no clear design strategy has been introduced in literature. Most of the designs published, do not give much insight in the design parameter selection. Some are still strongly mapped on the design strategies for DT $\Sigma\Delta$ modulators. Chapters 3 to 5 cover the research on robust design criteria which lead to these new design strategies. Secondly, new architectures for CT $\Sigma\Delta$ modulators using time-encoding are investigated in chapters 6 and 7. These architectures show

promising results in the light of co-integration of high-accuracy ADCs in advanced digital technologies.

Chapter 2 contains a basic introduction to the use of a $\Sigma\Delta$ modulator as the core of an ADC. A large part of this chapter focuses on continuous-time $\Sigma\Delta$ modulation.

Chapter 3 reveals some of the design considerations which are specific to the design of CT $\Sigma\Delta$ modulators. This chapter will set the boundary conditions which will be used in the next two chapters to define new robustness criteria for CT modulators.

In chapter 4 and 5, novel design strategies for CT $\Sigma\Delta$ modulators are developed. In chapter 4, robustness based on the Nyquist criterion is proposed. In chapter 5, the $\mathcal{S}$-figure is introduced, as a new robustness criterion based on the worst-case distance concept.

Chapter 6 introduces time-encoding as an emerging architectural direction for CT $\Sigma\Delta$ modulators in the context of continued scaling of deep submicron technologies.

Chapter 7 describes the design and measurement of a prototype self-oscillating $\Sigma\Delta$ modulator. While achieving state-of-the-art performance, this design specifically excels in low circuit complexity, small area and improved robustness to clock jitter.

Finally, chapter 8 concludes this dissertation and proposes directions for improvements and further research.

Chapter 2

$\Sigma\Delta$ Modulation

2.1 Introduction

This chapter explains the basics of $\Sigma\Delta$ modulation. The chapter starts off with the fundamentals of A/D conversion: sampling and quantization. Then the operation of the $\Sigma\Delta$ modulator as the core of an ADC is illustrated. In this part we mainly focus on the discrete-time $\Sigma\Delta$ modulator. In the last section the continuous-time $\Sigma\Delta$ modulator is covered. A mathematical framework for dealing with mixed DT/CT systems is introduced to allow a unified framework for both DT and CT $\Sigma\Delta$ modulators. Readers which are familiar with the subject can safely skip this chapter.

2.2 Analog-to-Digital Conversion

The $\Sigma\Delta$ modulator will be used as the core of an analog-to-digital converter in this work. In such an ADC two basic signal processing operations are performed on the analog input: sampling and quantization. The outcome is a waveform which can be digitally represented and processed by a digital processor (computer, micro-controller, ...).

2.2.1 Sampling

The sampling operation transforms the analog input signal $x(t)$ into a discrete-time signal:

$$x_d[n] = x(t)|_{t=nT_s}, \tag{2.1}$$

where $T_s = \frac{1}{f_s}$ is the uniform sampling period. To collect all of the signal information on the digital level, the sample frequency f_s must satisfy the Nyquist-Shannon theorem [1]. This implies that f_s should be at least twice as high as the bandwidth of $x(t)$, to prevent the occurrence of aliasing.

2.2.2 Quantization

Of course $x_d[n]$ still has continuously varying amplitude levels at each sample moment. To provide a digitally representable form, quantization of these values is performed. The accuracy of this quantization operation determines the accuracy of the ADC. Fig. 2.1 shows the input-output characteristic for a 3-bit quantizer. In that case 8 quantization levels are present to represent the input.

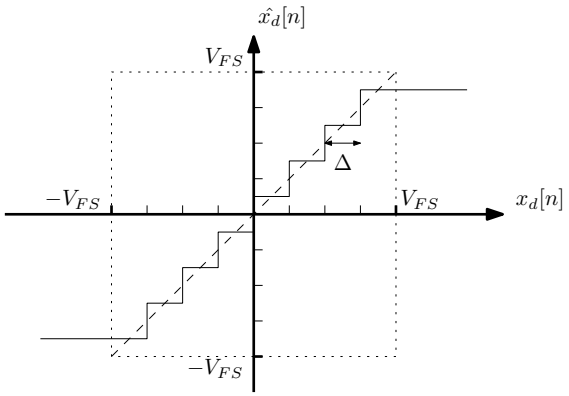

Figure 2.1: Input-output characteristic for a 3-bit quantizer.

The output of the quantizer $\hat{x_d}[n]$ can be expressed as the non-quantized input augmented with an error signal $q[n]$:

$$\hat{x_d}[n] = x_d[n] + q[n]. \tag{2.2}$$

If the input signal amplitude stays below the quantizer fullscale amplitude V_{FS}, then the error signal is bounded by:

$$-\frac{\Delta}{2} \leq q[n] \leq \frac{\Delta}{2}, \tag{2.3}$$

where Δ is the quantization step:

$$\Delta = \frac{2V_{FS}}{2^B}, \tag{2.4}$$

and B the number of quantizer bits.

The fact that quantization is a non-linear operation, makes it hard to analyze. However, if the input randomly varies between two samples with a value larger than or comparable to the quantization step Δ, the error signal $q[n]$ becomes practically uncorrelated from the input. $q[n]$ then contains uniformly distributed samples in the interval given by equation (2.3). Under these conditions, which were first reported in [2], the quantizer operation can be approximated by an additive white-noise source model, as displayed in fig. 2.2.

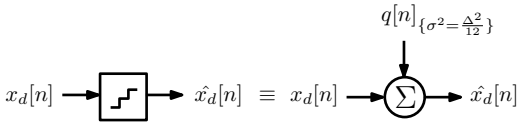

Figure 2.2: Additive white-noise source approximation for the quantizer operation.

The power of $q[n]$ can be calculated as the variance of its uniform distribution [3]:

$$P_q = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2 \mathrm{d}q = \frac{\Delta^2}{12}. \tag{2.5}$$

In the spectral domain, this power is uniformly spread over the whole Nyquist band.

The accuracy of the ADC can be expressed as the signal-to-quantization-noise ratio (SQNR) for a sine-wave input of fullscale amplitude:

$$\begin{aligned} \mathrm{SQNR}_{[\mathrm{fullscale,dB}]} &= 10\log_{10}\left(\frac{V_{FS}^2}{2}\frac{12}{\Delta^2}\right) && (2.6)\\ &= 1.76 + 6.02B. && (2.7) \end{aligned}$$

An interesting benchmark, the effective number of bits (ENOB), is derived from previous equation. It is used to determine the accuracy of real-life ADCs which, beside being limited by quantization noise, are also subjective to thermal noise and harmonic distortion. Therefore the SQNR from equation (2.7) is replaced here by the signal-to-noise and distortion ratio (SNDR):

$$\mathrm{ENOB} = \frac{\mathrm{SNDR}_{[\mathrm{fullscale,dB}]} - 1.76}{6.02}. \qquad (2.8)$$

2.3 ΣΔ Modulation

ΣΔ modulation combines the effect of oversampling and noise-shaping to implement high-resolution A/D converters. Fig. 2.3 shows the basic conversion scheme. It consists of an anti-aliasing filter (AAF), a sampler at rate f_s, the actual modulator (which includes the analog-to-digital interface) and a digital decimation filter.

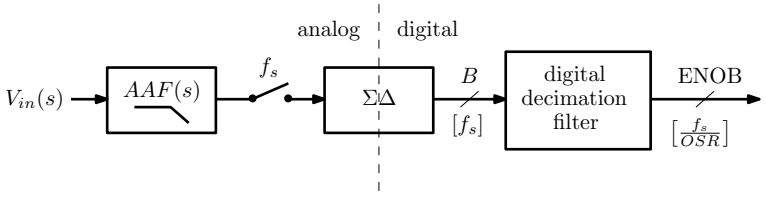

Figure 2.3: Basic A/D conversion scheme with a ΣΔ modulator.

2.3.1 Oversampling

Oversampling implies that the input signal after the AAF is sampled at a much higher rate than required by the Nyquist-Shannon theorem. The oversampling ratio (OSR) is defined as the ratio between the edge of the signal band f_b and the Nyquist frequency:

$$\mathrm{OSR} = \frac{f_s}{2f_b}. \tag{2.9}$$

This significantly relaxes the requirements for the AAF in fig. 2.3. The cutoff frequency does not have to be very accurate and the roll-off can be less steep than for a traditional AAF for a Nyquist-rate converter. The spectrum of an oversampled system is schematically shown in fig. 2.4 (a). Although the signal bandwidth is much smaller, the white quantization noise floor is still spread out over the whole Nyquist band.

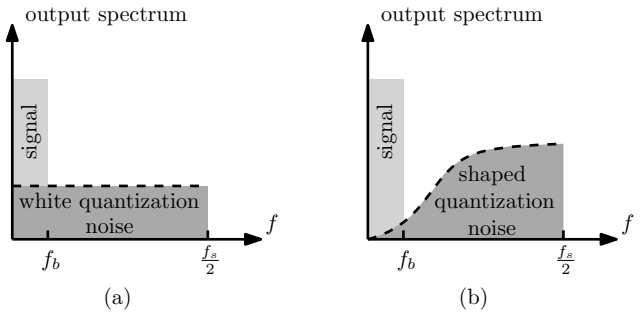

Figure 2.4: Output spectrum of (a) an oversampled system (white quantization noise floor) and (b) a ΣΔ modulator (shaped quantization noise).

Since we are only interested in a fraction of the Nyquist band, the digital decimation filter from fig. 2.3 will filter off the undesired high-frequency white noise content. The B-bit signal at sample rate f_s is transformed into a higher accuracy signal (ENOB $> B$) at lower sample rate $\frac{f_s}{\mathrm{OSR}} = 2f_b$. The SQNR for an oversampling converter increases by 3 dB (0.5 bit) with every doubling of the OSR:

$$\begin{aligned} \mathrm{SQNR}_{[\mathrm{fullscale,OSR,dB}]} &= 10\log\left(\frac{V_{FS}^2}{2}\frac{12}{\Delta^2}\mathrm{OSR}\right) && (2.10)\\ &= 1.76 + 6.02B + 10\log(\mathrm{OSR}). && (2.11) \end{aligned}$$

2.3.2 Noise-shaping

Noise-shaping is used to further increase the accuracy of the converter. The general block diagram of a ΣΔ modulator is shown in fig. 2.5. It consists of a loopfilter $H(z)$, a low-resolution quantizer (B bit) and a feedback digital-to-analog converter (DAC). As explained previously, the quantization error $Q(z)$ can be modeled by an additive white-noise source with power $\frac{\Delta^2}{12}$. This approximation is generally accepted for the case of multibit quantizers, which are examined in this dissertation. The loopfilter is formed by a cascade of integrator stages. The DAC closes the feedback loop. For the moment we will approximate the feedback DAC by an ideal unity operation (with conversion from the digital to the analog domain).

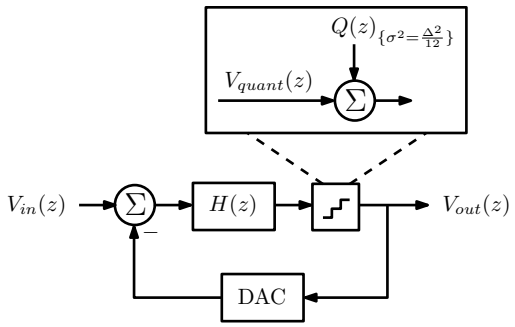

Figure 2.5: General block diagram of a ΣΔ modulator with indication of the linearized quantizer model.

Two important system transfer functions are defined. The noise transfer function (NTF) defines the transfer of the quantization noise input to the output, while the signal transfer function (STF) defines the transfer from the input signal to the output:

$$V_{out}(z) = \mathrm{STF}(z)V_{in}(z) + \mathrm{NTF}(z)Q(z) \quad (2.12)$$

$$= \frac{H(z)}{1+H(z)}V_{in}(z) + \frac{1}{1+H(z)}Q(z). \quad (2.13)$$

Since we are dealing with an oversampled system the input is very low-frequent compared to f_s. As the loopfilter has a very high gain for low frequencies (cascade of integrators), we assume the STF equals 1 within the signal band. The output can be approximated by:

$$V_{out}(z) \approx V_{in}(z) + \frac{1}{1+H(z)}Q(z). \quad (2.14)$$

Hence the output of the modulator is a digital signal (since V_{out} is the output of a quantizer), that represents the input signal with addition of a second term, the shaped noise spectrum. The situation is depicted schematically in fig. 2.4 (b). As a result of the high loopfilter gain for low frequencies, the white noise quantization spectrum $Q(z)$ is heavily suppressed within the signal band. The suppression decreases in function of frequency, due the roll-off of the loopfilter. For frequencies around the Nyquist frequency, the noise power can even be increased. Keep in mind that a digital decimation filter will be applied to the output data stream, and eventually only the noise power within the signal band is of importance. Compared to the plain oversampling situation from fig. 2.4 (a), the in-band accuracy is heavily increased due to the noise-shaping.

2.3.3 ΣΔ Modulator Performance

The reference NTF for an N-th order ΣΔ modulator is given by a N-th order differentiation:

$$\mathrm{NTF}_{\mathrm{reference}}(z) = (1-z^{-1})^N = \frac{(z-1)^N}{z^N}. \quad (2.15)$$

The shape of this NTF is illustrated in fig. 2.6 for orders 1 up to 4. The transfer function has an out-of-band gain of 2^N at $\frac{f_s}{2}$.

All the NTF zeros are located at DC ($z = 1$) and all the poles at the origin ($z = 0$). The in-band quantization noise (IBQN) can be calculated as:

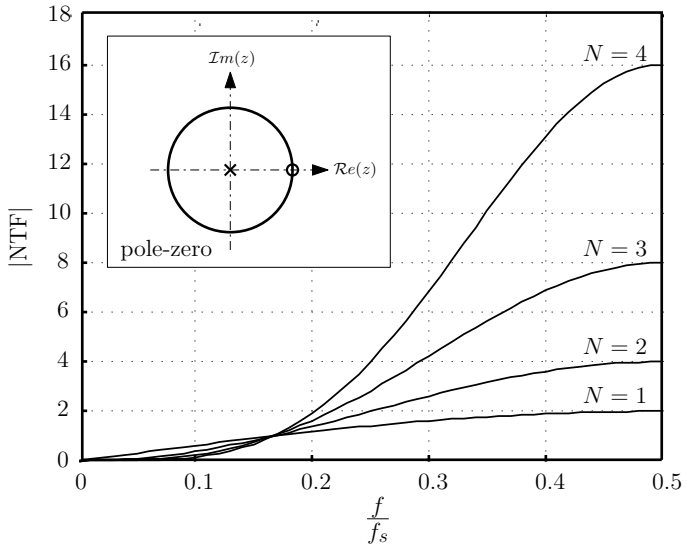

Figure 2.6: Reference NTF for different modulator orders with indication of the pole-zero positions in the complex $\mathcal{Z}$-plane.

$$\text{IBQN} = \int_0^{f_b} |\text{NTF}(e^{j2\pi f_s})|^2 \frac{\Delta^2}{12} \frac{2}{f_s} \mathrm{d}f \tag{2.16}$$

$$= \int_0^{f_b} \left[2\sin(\pi f T_s)\right]^{2N} \frac{\Delta^2}{12} \frac{2}{f_s} \mathrm{d}f. \tag{2.17}$$

As we consider an oversampled system, only the low-frequent part of the noise spectrum accounts to the system resolution, and thus:

$$\sin(\pi f T_s) \approx \pi f T_s. \tag{2.18}$$

This leads to an IBQN of:

$$\text{IBQN} = \frac{\pi^{2N}}{2N+1} \frac{1}{\text{OSR}^{2N+1}} \frac{\Delta^2}{12}. \tag{2.19}$$

Compared to the Nyquist rate converter with an in-band quantization noise of $\frac{\Delta^2}{12}$, the fullscale SQNR becomes:

$$\begin{aligned} \mathrm{SQNR}_{[\mathrm{fullscale},\Sigma\Delta,\mathrm{dB}]} &= 1.76 + 6.02B - 10\log\left(\frac{\pi^{2N}}{2N+1}\right) \\ &\quad +(2N+1)10\log(\mathrm{OSR}). \end{aligned} \tag{2.20}$$

This means that for an N-th order ΣΔ modulator the accuracy increases by $(N+0.5)$ bit with every doubling of the OSR. In fig. 2.7 the SQNR increase, compared to a Nyquist rate converter, is plotted in function of the oversampling ratio for different modulator orders. The modulator with order zero is a plain oversampling converter, with an increase of 3 dB when the OSR doubles as stated by equation (2.11). For a fixed OSR, the largest accuracy increase can be seen in the transition from a plain oversampling converter to a first order modulator. For higher orders, the increase progressively becomes smaller.

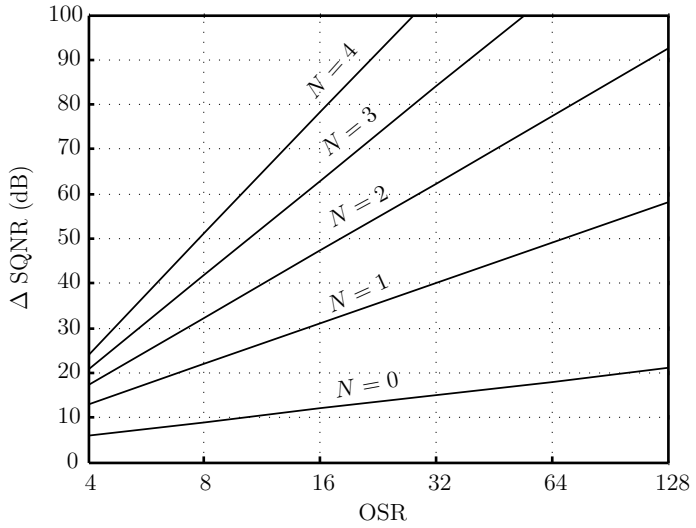

Figure 2.7: SQNR increase compared to a Nyquist-rate converter in function of the OSR for the reference ΣΔ modulator.

2.3.4 Modulator Stability

Due to the high out-of-band gain, the reference modulator from equation (2.15) can become unstable if $N \geq 3$. This occurs due to overloading of the quantizer, even if the modulator's input signal amplitude stays well below the fullscale quantizer level V_{FS}. The input to the quantizer can be written as (see fig. 2.5):

$$V_{quant}(z) = \mathrm{STF}(z)V_{in}(z) + [\mathrm{NTF}(z) - 1]Q(z). \tag{2.21}$$

The maximum stable amplitude (MSA) is defined as the largest input amplitude, which the modulator can still process without overloading. Based on equation (2.21), we propose following heuristic for calculating the MSA [4]:

$$\mathrm{MSA} \approx V_{FS} - \frac{3}{2}\sqrt{\int_0^{\frac{f_s}{2}} |\mathrm{NTF}(e^{j2\pi f_s}) - 1|^2 \frac{\Delta^2}{12}\frac{2}{f_s}\mathrm{d}f}. \tag{2.22}$$

Again, we made the approximation that the STF is close to unity within the signal band. The second term is proportional to the power of the contribution from the quantization noise.

Equation (2.22) is particularly valid for multibit modulators, where the quantization error is heavily decorrelated from the quantizer input signal. In early papers on ΣΔ modulation, other stability criteria are also proposed [5, 6]. They were mainly deployed for single bit modulators, for which the additive white noise approximation is less justified. Furthermore, these criteria were found to be too conservative or, even worse, in some cases could lead to unexpected instability [5]. However, all stability criteria are based on a mathematical norm (1-norm, 2-norm or ∞-norm) of either the NTF or its impulse response. They share the fact that modulators with a larger out-of-band gain are more prone to instability, just like in equation (2.22). In the previous section we described that the out-of-band gain for the reference N-th order differentiation NTF increases with the modulator order. For example, the reference third order modulator has an out-of-band gain of 8. As a consequence of equation (2.22), the modulator only remains stable up to less than half the fullscale level, when using a 3-bit quantizer. The fourth order reference modulator is even unstable for any input amplitude with a 3-bit quantizer.

Increasing the number of quantizer bits (smaller Δ), is one way to increase modulator stability. A more effective strategy however, is to place the NTF

poles in a different position than having them all placed at the origin. A popular NTF pole constellation was proposed in [5]. The NTF which arises, is a maximally flat NTF, with maximum out-of-band gain at $\frac{f_s}{2}$, denoted by the design parameter $\mathcal{H}_\infty$. Due to the resemblance with the pole constellation of a Butterworth filter, this type of NTF is also identified as a Butterworth NTF. In fig. 2.8 a third order Butterworth NTF is shown with $\mathcal{H}_\infty$ equal to 4 for an OSR of 16. The figure also displays the pole-zero constellation in the complex plane. $\mathcal{H}_\infty$ is the only design parameter to fully determine the NTF. The value for $\mathcal{H}_\infty$ can be used as a tradeoff: a lower value gives rise to poles which are closer to the zeros at DC, which results in a smaller out-of-band gain at the cost of a lower in-band noise suppression.

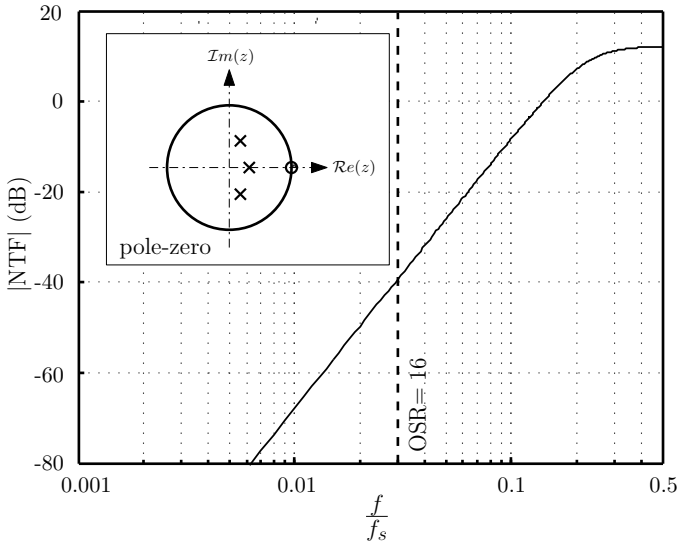

Figure 2.8: Third order NTF with poles in Butterworth position and $\mathcal{H}_\infty = 4$. Bode plot of the NTF with indication of the signal band edge (dashed) and pole-zero positions in the complex $\mathcal{Z}$-plane.

A different NTF design strategy is proposed in [6]. This methodology is called CLANS and is based on an optimization algorithm of the pole constellation, to achieve the maximum peak SQNR performance. In both cases, due to the altered pole constellation, the general NTF looks like:

$$\mathrm{NTF}(z) = \frac{(z-1)^N}{P_N(z)}, \tag{2.23}$$

with $P_N(z)$ an N-th order polynomial in z whose coefficients can define any pole constellation. The coefficient in z^N is thereby always equal to 1 for reasons of causality [3]. Both design strategies were incorporated in a free Matlab toolbox [7].

Formerly, we defined the accuracy based on the fullscale quantizer level. However, the modulator will never be able to process these high input amplitudes. As such, the peak SQNR (or SNDR) is a more justified accuracy measurement:

$$\mathrm{SQNR}_{[\mathrm{peak,dB}]} = 10\log\left(\frac{\mathrm{MSA}^2}{2\mathrm{IBQN}}\right). \tag{2.24}$$

Based on this definition, the example of fig. 2.8 with a 3-bit quantizer achieves a peak SQNR of 73.7 dB for a maximum stable amplitude of 2/3 of the fullscale quantizer level.

2.3.5 NTF Zero Spreading

To further increase the accuracy, the NTF zeros, which were previously located at DC, can be spread out over the signal band. In [5] optimal locations, relative to the signal band edge, for these zero positions are given for several modulator orders. This way an extra increase in noise suppression can be achieved. As the effect is localized in the signal band, the global modulator stability is not affected. In fig. 2.9 the previous example with $\mathcal{H}_\infty = 4$ is extended with zero spreading. The zeros are still on the unit circle. Since the order is odd, one of the zeros remains at DC, while the other two form a complex conjugate pair within the signal band. Actually, the NTF zeros originate from the poles of the loopfilter $H(z)$. In this case, the loopfilter is no longer a pure cascade of integrators, but instead it is a filter with low-frequency resonance peaks within the signal band. Since the NTFs in fig. 2.8 and 2.9 are plotted on a logarithmic scale, especially their values at f_b determine the in-band noise. Clearly the optimization of the zeros results in a lower NTF value at f_b. This is also quantitatively confirmed: the peak SQNR has increased to 81.7 dB for the same MSA.

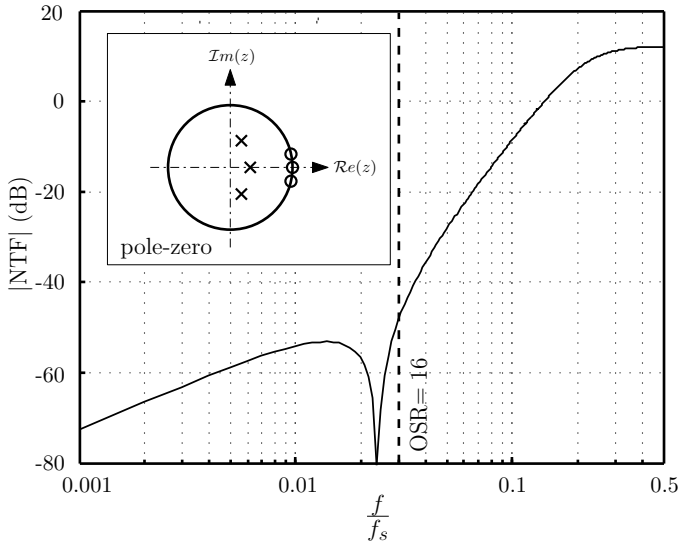

Figure 2.9: Third order NTF with poles in Butterworth position, optimized zeros and $\mathcal{H}_\infty = 4$. Bode plot of the NTF with indication of the signal band edge and pole-zero positions in the complex $\mathcal{Z}$-plane.

2.4 ΣΔ Modulation in Continuous Time

So far, we have described ΣΔ modulators with loopfilters in discrete time. In fig. 2.3 the input was sampled before entering the actual modulator. Due to the ease of implementation with switched capacitor circuits, these converters have dominated publications on ΣΔ modulators during the 90's and the beginning of the years 2000 [8–17].

In continuous-time ΣΔ modulation, the sampler is shifted inside the ΣΔ loop. Fig. 2.10 shows the block diagram for a CT ΣΔ modulator. $V_{in}(s)$ is now a continuous-time analog input and the loopfilter $H(s)$ is formed by a cascade of continuous-time integrators. The sampling operation is performed within the clocked quantizer. Again, the white-noise approximation can be made for the quantization. Due to the continuous-time integration, the shape of the feedback DAC pulse, indicated by its transfer function $H_{DAC}(s)$, is important and will influence the ΣΔ loop behaviour.

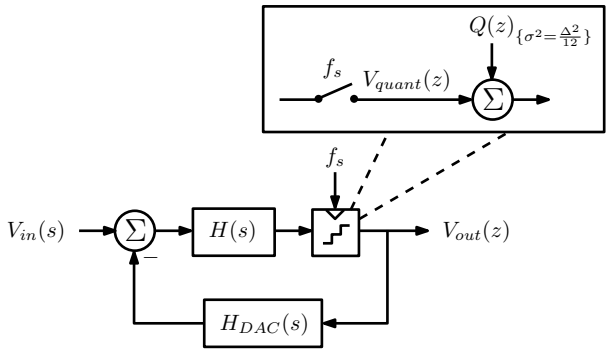

Figure 2.10: Block diagram of a CT ΣΔ modulator.

2.4.1 Sampling in Mixed DT/CT Systems

The difficulty in analyzing a CT ΣΔ modulator lies in the fact that the loop processes both discrete-time and continuous-time signals. For this reason, it would be interesting to have a unified mathematical framework, which we can apply to both CT and DT signals. More specifically, a link between the spectrum of a continuous-time signal and its sampled discrete-time counterpart, must be identified. For this purpose the $*$-operator is introduced [18]. It defines the sampled signal from equation (2.1) as an artificial CT signal:

$$x^*(t) = \sum_{n=0}^{\infty} x_d[n]\delta(t - nT_s), \tag{2.25}$$

where $\delta(t)$ is the continuous-time Dirac impulse. We identify the Laplace transform ($\mathcal{L}$) of this signal as:

$$\begin{aligned} X^*(s) &= \sum_{n=0}^{\infty} x_d[n]\mathcal{L}\{\delta(t - nT_s)\} && (2.26)\\ &= \sum_{n=0}^{\infty} x_d[n]e^{-snT_s} && (2.27)\\ &= X_d(e^{sT_s}). && (2.28) \end{aligned}$$

The Laplace transform of $x^*(t)$ thus equals the $\mathcal{Z}$-transform of the sampled signal $X_d(z)$, evaluated at $z = e^{sT_s}$.

A second relation can be derived by expressing $x^*(t)$ as a multiplication of $x(t)$ and the time-domain Dirac comb function:

$$\begin{aligned} x^*(t) &= x(t)\delta_T(t) && (2.29)\\ &= x(t)\sum_{n=-\infty}^{\infty}\delta(t-nT_s). && (2.30)\end{aligned}$$

The convolution in the Laplace domain results in the well-known fact that the spectrum of the sampled signal is a periodic expansion of the continuous-time spectrum, with a period equal to the sampling frequency.

$$X^*(s) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(s + jn2\pi f_s). \quad (2.31)$$

The spectral domain $*$-operator has two more interesting properties, which we will use further on:

$$\begin{aligned} [\alpha X(s) + \beta Y(s)]^* &= \alpha X^*(s) + \beta Y^*(s) && (2.32)\\ [X(s)Y^*(s)]^* &= X^*(s)Y^*(s). && (2.33)\end{aligned}$$

The first property states that the $*$-operator is a linear operator. The second property states that the sampled spectrum of a Laplace domain multiplication equals the product of the two sampled spectra, provided that one of the signals was already a sampled signal. This property can easily be proven but can also be intuitively understood, since one of the two spectra is already periodic.

2.4.2 Discrete-Time Modulator Equivalence

To further investigate the continuous-time modulator, the system diagram is rearranged as in fig. 2.11. The loopfilter $H(s)$ and sampler are shifted into the feedback path of the loop and towards the analog input. Similar to the DT modulator, we can identify the NTF and STF as the system's response to the quantization noise and input respectively, by applying linear superposition.

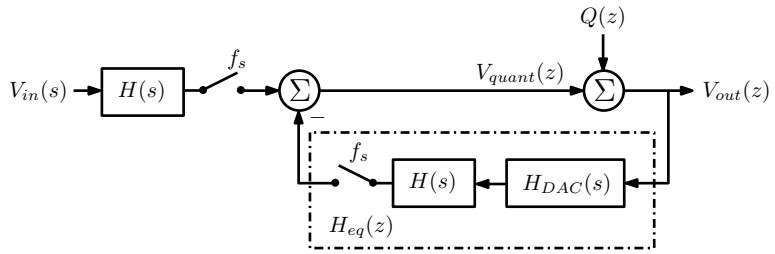

Figure 2.11: Rearranged CT ΣΔ modulator system diagram to identify the equivalent DT loopfilter.

Noise Transfer Function $[V_{in}(s) = 0]$

Based on the theory of sampled signals from the previous section and the introduction of the $*$-operator, the input to the quantizer can be written as:

$$V_{quant}(e^{sT_s}) = -[H(s)H_{DAC}(s)V_{out}(e^{sT_s})]^*, \tag{2.34}$$

when no input signal is applied. As the quantizer input and the output signal are discrete-time signals, we use equation (2.28) to link them to the CT Laplace domain variable s. From now on we will no longer explicitly indicate DT signals and their $\mathcal{Z}$-transform with a subscript annotation. It will be clear from the context whether the referred signal is a CT or a DT signal. Note the importance of the DAC pulse transfer function. As it implements the real transition between discrete-time and continuous-time, its waveform is important for the analysis of the modulator. A widely used feedback pulse is the non-return-to-zero (NRZ) pulse (sometimes also indicated as the zero-order-hold (ZOH) pulse), where the digital value is merely held during the whole clock period:

$$H_{DAC,NRZ}(s) = \frac{1 - e^{-sT_s}}{s}. \tag{2.35}$$

The output signal in (2.34) is already a sampled signal, hence equation (2.33) can be applied. This results in a direct connection between the $\mathcal{Z}$-transform of V_{out} and V_{quant}:

$$V_{quant}(z) = -\underbrace{[H(s)H_{DAC}(s)]^*}_{H_{eq}(z)} V_{out}(z). \tag{2.36}$$

The cascade of the DAC pulse, the analog loopfilter and the sampler can thus be seen as an equivalent discrete-time loopfilter $H_{eq}(z)$. This is indicated by the dashed rectangle in fig. 2.11.

A practical method to calculate the equivalent loopfilter $H_{eq}(z)$ is the impulse-invariant-transformation (IIT):

$$\begin{aligned} H_{eq}(z) &= \text{IIT}\{H(s)H_{DAC}(s)\} &(2.37)\\ &= \mathcal{Z}[\mathcal{L}^{-1}\{H(s)H_{DAC}(s)\}|_{t=nT_s}]. &(2.38)\end{aligned}$$

Mathematically, it is obtained by taking the inverse Laplace transformation ($\mathcal{L}^{-1}$) of $H(s)H_{DAC}(s)$, sampling the result and finally performing the $\mathcal{Z}$-transformation. It is a direct consequence of equation (2.28). On the other hand, using equation (2.31), the spectrum of $H_{eq}(z)$ also equals:

$$H_{eq}(e^{sT_s}) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} H(s + jn2\pi f_s)H_{DAC}(s + jn2\pi f_s). \tag{2.39}$$

This relation can be used to determine the DT loopfilter numerically. As the continuous-time loopfilter is a lowpass filter, the infinite sum can be approximated by only taking into account a limited number of terms. The continuous-time loopfilter can be simulated as the result of a Spice AC simulation. A third method to calculate the equivalent discrete-time loopfilter is by using the residue theorem [18, 19]:

$$H_{eq}(e^{sT_s}) = \sum_i \text{residues}\left[H(\phi)H_{DAC}(\phi)\frac{e^{sT_s}}{e^{sT_s} - e^{\phi T_s}}\right] \text{ at } \phi = s_i. \tag{2.40}$$

This theorem, which is a result of complex contour integration, is particularly interesting, as it allows a closed expression between the non-sampled spectrum $H(s)H_{DAC}(s)$ and the equivalent sampled spectrum $H_{eq}(e^{sT_s})$. The residues are evaluated at the poles s_i of the loopfilter $H(s)$. This is under the assumption that the DAC pulse has no poles, which is usually the case. It is the most practical method and can be implemented by a

partial fraction decomposition of the loopfilter [20] (e.g. the *c2d* function in Matlab).

Using all the above, a similar definition for the noise-transfer-function (NTF) as for the case of a DT ΣΔ modulator can be adopted:

$$NTF(z) = \frac{1}{1 + H_{eq}(z)}. \tag{2.41}$$

This well-known relation allows us to use a unified framework for both DT and CT ΣΔ modulators with respect to their noise shaping.

A straightforward design strategy for CT ΣΔ modulators, is to start off from the desired DT NTF, for example the NTF shown in fig. 2.9. This NTF has an equivalent DT loopfilter:

$$H_{eq}(z) = \frac{2.3446(z^2 - 1.142z + 0.4027)}{(z-1)(z^2 - 1.977z + 1)}. \tag{2.42}$$

Note that due to the NTF zero-spreading, the loopfilter poles are spread out over the signal band. For calculating the inverse IIT, we will use the NRZ feedback DAC pulse. Along the frequency axis the NRZ-pulse is evaluated as:

$$\begin{aligned} H_{DAC,NRZ}(f) &= e^{-j2\pi f \frac{T_s}{2}} \cdot \frac{sin(\pi f T_s)}{\pi f T_s} && (2.43) \\ &= e^{-j2\pi f \frac{T_s}{2}} \cdot sinc(\pi f T_s). && (2.44) \end{aligned}$$

Hence, it is a linear phase filter (with delay $\frac{T_s}{2}$) with notches at multiples of f_s due to the sinc interpolation. The resulting CT loopfilter equals:

$$H(s) = \frac{1.5482[(sT_s)^2 + 0.9063(sT_s) + 0.396]}{sT_s[(sT_s)^2 + 0.02313]}. \tag{2.45}$$

The poles on the unit circle are translated to CT poles on the imaginary axis. Note that the resulting loopfilter coefficients scale with the sample frequency. In the rest of this work, we will normalize the sample frequency to 1 for notational simplicity. In fig. 2.12, the frequency response of both the equivalent DT loopfilter and the cascade of the CT loopfilter with the NRZ

DAC pulse are displayed. The spectrum is not limited to $\frac{f_s}{2}$ to see the high-frequency roll-off of the continuous-time filter. Of course the DT spectrum is periodic with period f_s. Within the signal band (indicated by the dashed lines for an OSR of 16) the three resonance peaks of both filters coincide. Due to the sinc notches at multiples of f_s, practically no high-frequency information aliases back into the signal band in the transformation from continuous-time filter to discrete-time filter.

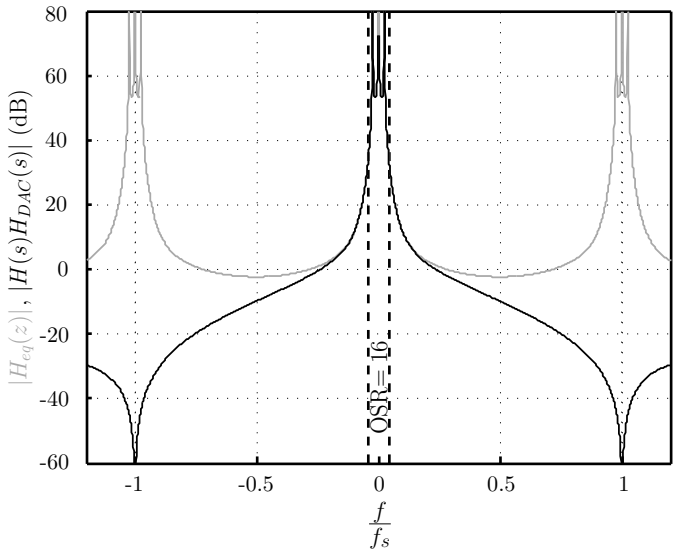

Figure 2.12: Spectrum of the equivalent DT loopfilter (gray) and the cascade of the analog loopfilter and the DAC pulse (black) for the third order NTF with poles in Butterworth position, optimized zeros and $\mathcal{H}_\infty = 4$.

Signal-Transfer-Function $[Q(z) = 0]$

The input signal is first filtered by $H(s)$ and then sampled before entering the noise-transfer-function loop (see fig. 2.11). If we use equation (2.33) in the reverse direction, the system response to the CT input can be written as:

$$V_{out}(z) = \big[H(s)V_{in}(s)\big]^* NTF(z) \tag{2.46}$$
$$= \big[\underbrace{H(s)NTF(e^s)}_{\mathrm{STF}(s)} V_{in}(s)\big]^*. \tag{2.47}$$

The response to the input is denoted by the signal-transfer-function (STF). This function is still defined in the CT domain. Its sampled (aliased) version is the eventual contribution in the modulator's DT output signal. For the example of equation (2.42), the STF is displayed in fig. 2.13.

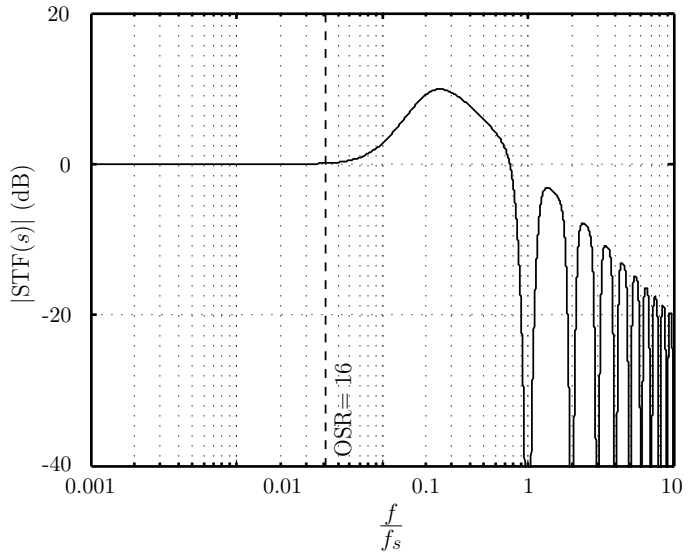

Figure 2.13: Signal transfer function for the CT ΣΔ modulator with third order NTF with poles in Butterworth position, optimized zeros and $\mathcal{H}_\infty = 4$.

In the signal band, the CT loopfilter and the DT NTF will compensate for each other, leading to an amplitude response close to one. For high frequencies, the input signal is lowpass filtered by the first-order roll-off of $H(s)$ before being sampled. This is known as the implicit anti-alias filter of the CT ΣΔ modulator and was first reported in [21]. At multiples of f_s, notches appear, due to the periodic spectral behaviour of the NTF. In contrast to

DT modulators, an explicit anti-alias filter in front of the modulator seems no longer necessary. However, fig. 2.13 also reveals that peaking outside the signal band can appear. In this transition zone, interferer signals can be amplified, which could cause overloading of the modulator. In most practical cases also a CT modulator will be preceded by an extra filter, indicated as the "overload prevention" filter. For low oversampling ratios, the peaking appears close to the signal band, which heavily increases the requirements for this filter.

2.4.3 Loopfilter Considerations

Feedback/Feedforward Topology

Similar to regular filter topologies, the loopfilter of a CT ΣΔ modulator can also be implemented in a feedback (FB) or feedforward (FF) topology. Both topologies can be used to implement any NTF.

In the FB topology (fig. 2.14), there is a feedback path to every integrator input. As a consequence, multiple feedback DACs have to be installed. The feedback paths generate the NTF poles necessary to stabilize the loop, according to equation (2.23). The philosophy is similar to stabilizing a regular continuous-time filter. At the crossover frequency (the 0 dB point in the Bode plot), the loopfilter should reduce to a first order system to attain sufficient phase margin. For the FB topology, the loopfilter can be written as:

$$H(s) = \frac{c_N}{s} + \frac{c_{N-1}c_N}{s^2} + \ldots + \frac{\prod_{i=1}^{N} c_i}{s^N}. \tag{2.48}$$

In practice the stability requirement almost automatically leads to coefficients where $c_{i+1} > c_i$. As the integrators have a large gain for frequencies within the signal band, nullator hypotheses can be applied to every summation node. The integrator output signal practically equals the input signal in this frequency range. Therefore the output signal of each integrator contains a strong contribution of the input. This means that the signal swing on the integrator outputs is quite large, which puts requirements on the linearity of the integrators on the circuit level [22].

For the FF topology, the reciprocal situation applies. The loopfilter now equals:

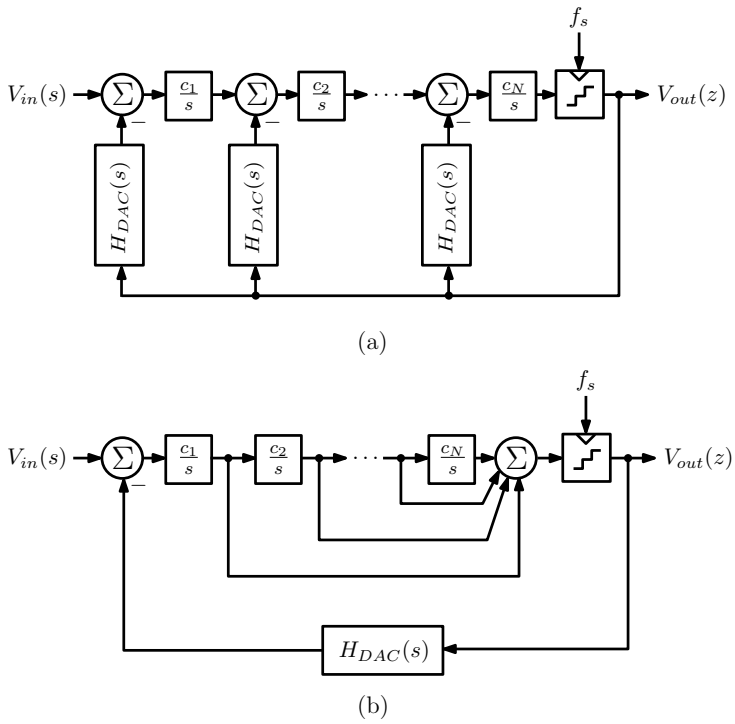

Figure 2.14: CT ΣΔ modulator with loopfilter in (a) feedback topology and (b) feedforward topology.

$$H(s) = \frac{c_1}{s} + \frac{c_1 c_2}{s^2} + \ldots + \frac{\prod_{i=1}^{N} c_i}{s^N}. \tag{2.49}$$

To stabilize the loopfilter, here generally the coefficients $c_{i+1} < c_i$. In the FF topology, the outputs of all integrators are added in front of the quantizer input. This means an extra summation circuit is necessary. In this topology, nullator hypotheses can only be applied to the first integrator. Consequently, the loopfilter only has to process quantization noise, and the integrator outputs do not contain a large input signal contribution. Hence, the linearity requirements can be relaxed compared to the FB topology.

Suppression of Error Signals

In both topologies, errors due to non-linearity and noise become gradually less important when propagating through the loopfilter. For example, an error contribution after the first integrator is differentiated towards the input. Therefore, the first integrator always has the highest power consumption, because its input referred noise almost fully determines the global system accuracy.

In the FF topology, the first integrator happens to coincide with the first-order path of the loopfilter (with the largest coefficient). This means that errors at the first stage output are more suppressed than in the corresponding FB topology (where the first integrator has the smallest coefficient). In the FB topology this leads to larger power consumption in the following stages. In general, it is assumed that the FF topology is easier to stabilize. Due to the larger power consumption in the first-order path, its loopfilter is less sensitive to high-frequency parasitics. An exploration of publications on CT ΣΔ modulation also indicates the popularity of the FF loopfilter topology [21, 23–27].

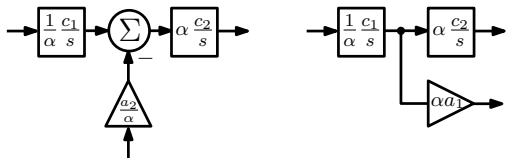

Figure 2.15: Illustration of integrator output scaling in (a) the feedback topology and (b) the feedforward topology.

In fig. 2.14 all coefficients were assigned to the integrators. In reality, these coefficients will be split up between an integrator coefficient and a feedback-/feedforward coefficient. This gives an extra degree of freedom to keep the integrator output signal swing within the desired range. The situation is depicted in fig. 2.15, where the FB/FF coefficients now also have weights a_i. For example in the FB topology, coefficients c_1 and a_2 can be lowered with the same factor α to reduce the first integrator output swing. To end up with the same NTF, the next integrator coefficient c_2 has to be increased with the same factor α. In the situation of a FF topology, a similar analysis

can be made except for the fact that the feedforward coefficient increases when lowering the first stage signal swing.

NTF Zero Spreading

The loopfilters displayed in fig. 2.14 do not include NTF zero spreading within the signal band. All the poles of the loopfilter are still located at DC ($s = 0$). To implement a low-frequency resonance in the loopfilter, a local negative feedback path around two integrators must be installed (see fig. 2.16). The transfer function of this resonator section is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{c_1 c_2}{s^2 + c_1 c_2 g}, \tag{2.50}$$

which is in the same form as for the zero-spreaded CT loopfilter of equation (2.45). The local feedback coefficient g is a small coefficient which shifts the resonance from DC to a very low frequency within the signal band.

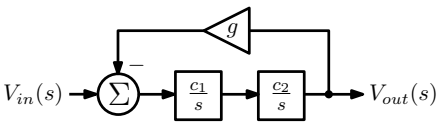

Figure 2.16: Implementation of NTF zero spreading by a local feedback path around 2 integrators.

Circuit Implementation

The two basic circuit implementations used for the continuous-time integrator are shown in fig. 2.17. The circuits are displayed differentially, as it is common practice to implement high accuracy ADCs in a differential way, increasing immunity to common-mode disturbances. In the active-RC implementation, the integrator is formed by a feedback loop around an operational amplifier. The feedback configuration with high loop gain results in good output linearity. The feedback DAC is usually implemented by a current-steering DAC towards the virtual ground node of the opamp. If loaded by the input resistors of the following stage, the opamp is implemented as a two-stage amplifier.

The other implementation option is the g_mC integrator. In this configuration the input voltage is converted into a current, through the transconductance of a transistor. In most practical implementations, the g_m is actually formed by the reciprocal of a resistor as in fig. 2.17 (b), due to a better controllability. The resulting output voltage appears due to integration of this current over the capacitor. Due to the simplicity of this open-loop circuit, power consumption is lower than the active-RC implementation. However, this has to be traded off to a decreased linearity. For completeness, we state that other topologies than the one displayed in fig. 2.17 (b) exist, which can have a better linearity. However, usually the increased linearity also has to be paid for by increased power consumption.

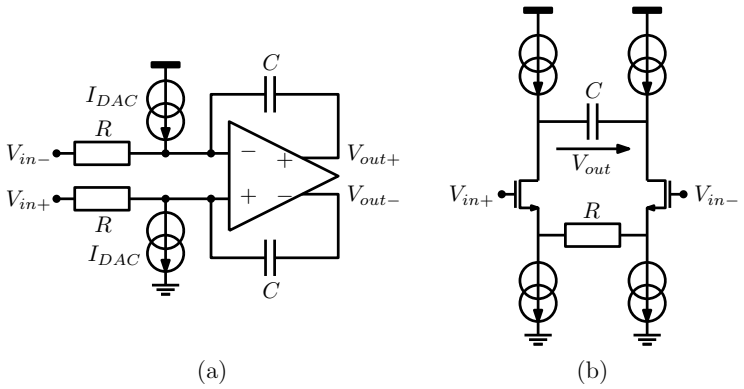

Figure 2.17: Circuit implementation of a continuous-time integrator with current-steering feedback DAC: (a) active-RC implementation and (b) g_mC implementation.

As the linearity is of utmost importance in the first stage, it will almost always be implemented as an active-RC integrator. The following stages can use a g_mC integrator to reduce power consumption.

2.4.4 Advantages Compared to DT Modulators

Lower Power Consumption

In a DT modulator, the integrator stages are built up with SC circuits, which require step-response settling at the output of each clock cycle. The gain-

bandwidth products (GBWs) of the operational amplifiers therefore have to be in the range of $3f_s$ or more to achieve accurate settling [16, 28]. In a CT ΣΔ modulator, no settling behaviour occurs as the filter operates in the continuous-time domain. GBWs of f_s, or lower, can suffice for the opamps in the integrators [21,29]. In addition, the feedback factor around the amplifier is practically equal to 1 for frequencies in the range of the GBW. In a SC circuit, the feedback factor is usually smaller than 1, depending on the implemented integrator coefficient. In general, the lower GBW specification leads to a smaller power consumption. Vice versa, higher accuracies can be achieved with CT ΣΔ modulation for the same power budget.

Sampling Inside the Loop

The location of the sampler in front of the quantizer (actually in most circuits the sampling operation is incorporated within the quantizer), relaxes its requirements. Errors due to the sampler are shaped in the same way as the quantization noise within the signal band. In a DT ΣΔ modulator, the input sampler has to achieve the full system accuracy. Furthermore, sampling inside the loop also gives rise to the implicit anti-aliasing filter of a CT ΣΔ modulator.

Input Impedance

For both the active-RC or the g_mC implementation, a constant load condition towards the ADC driver is present. In a DT modulator, the switched capacitor input stage generates peaked current pulses, drawn from the driver at the ADC sampling moments. This generally requires drivers with high slew-rate and excellent harmonic distortion specifications, which makes the design of this driver more complex.

No Switches

In a CT ΣΔ modulator, no real switches are present. As already stated, the sampling switch is usually combined with the quantizer in a latch-type structure, which does not require low-ohmic switches. It makes the CT modulator more compatible with deep sub-micron technologies than its DT counterpart. Since no aliasing appears inside the loopfilter, also the limited switching behaviour of the DAC feedback signals has less chance of corrupting the modulator output.

$\frac{kT}{C}$ Noise

For DT ΣΔ modulators, the inherent switched behaviour of the circuit introduces back-folding of noise at higher alias band which end up in the baseband spectrum. This results in the input referred noise power of a DT modulator, being proportional to $\frac{kT}{C}\frac{1}{\mathrm{OSR}}$ [12, 13, 30], where k is the Boltzmann constant, T the absolute temperature in Kelvin and C is the input capacitor of the first integrator stage.

CT ΣΔ modulators do not suffer from the noise back-folding mechanism. The only sampling operation occurs at the input of the quantizer, where the implicit anti-alias filter has already suppressed the main noise contributors. The input referred noise power ends up being merely proportional to $4kTRf_b$ [31]. In both cases, reducing the input noise complies with lowering the impedance (higher C for DT modulators, lower R for CT modulators), and hence, increasing the power consumption. The pure baseband operation of the CT modulator is generally perceived as an advantage compared to the DT modulator.

2.4.5 Disadvantages Compared to DT Modulators

Of course, CT ΣΔ modulation also shows disadvantages compared to DT ΣΔ modulation. This is the content of the next chapter.

Chapter 3

Design Considerations for Continuous-Time $\Sigma\Delta$ Modulators

3.1 Introduction

In this chapter, we will present an overview of the design challenges in CT $\Sigma\Delta$ modulators. More specifically, several parasitic effects are described, which can degrade the performance. Some of them were already present in DT modulators while others are specifically linked to continuous-time $\Sigma\Delta$ modulation. An overview of the most important effects is given, without claiming completeness.

In the design of CT $\Sigma\Delta$ modulators, a strong focus lies on extending the conversion bandwidth into the wide MHz range. Therefore, from this chapter on, we will consider modulators with a low OSR, combined with multibit quantization. Without loss of generality, we will use the third-order CT $\Sigma\Delta$ modulator architecture shown in fig. 3.1 to illustrate the main effects. The loopfilter is in a feedforward topology with zero spreading in the signal band. The loopfilter transfer function equals:

$$H(s) = \frac{a_1 c_1 s^2 + a_2 c_1 c_2 s + (a_1 g + a_3) c_1 c_2 c_3}{s(s^2 + c_2 c_3 g)}. \tag{3.1}$$

The NRZ pulse from equation (2.35) will be used for the feedback DAC, unless stated otherwise. It is important to notice that this architecture is

purely instructive and that the effects described here are equally present in a FB topology.

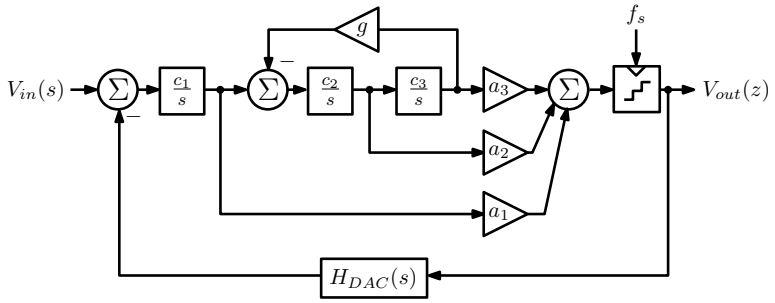

Figure 3.1: Third-order CT ΣΔ modulator architecture with the loopfilter in a feedforward topology.

3.2 Loopfilter Variations

3.2.1 Process Variations

From the previous chapter we know that the loopfilter integrators are implemented by opamp-RC circuits or, alternatively, by using g_mC integrators. Either way, the integration coefficients c_i are determined by a combination of a capacitor and a resistor (or the reciprocal of a transconductance). Since these two physical parameters originate from devices of a different type, large process variations are expected on the integrator coefficients:

$$c_{i,actual} = c_{i,nominal}(1 + \delta_{IC}). \tag{3.2}$$

Here δ_{IC} is a statistical parameter originating from a zero mean Gaussian distribution. Although the variations can be large between devices originating from different wafers (possibly processed at different times), the assumption is made that good correlation exists between devices on the same die. This explains why the variation parameter δ_{IC} has no index i and integrator coefficients within the same modulator will all shift in the same direction. Usually, process variations are handled as process corners in the process design kits (PDKs) of commercial foundries. These corners can

for example be defined as the 6σ values of a Gaussian distribution. As such, the statistical nature of these variations is treated as worst-case boundaries. The RC-variations can easily range up to $\pm$ 20 % or more in current deep sub-micron CMOS technologies.

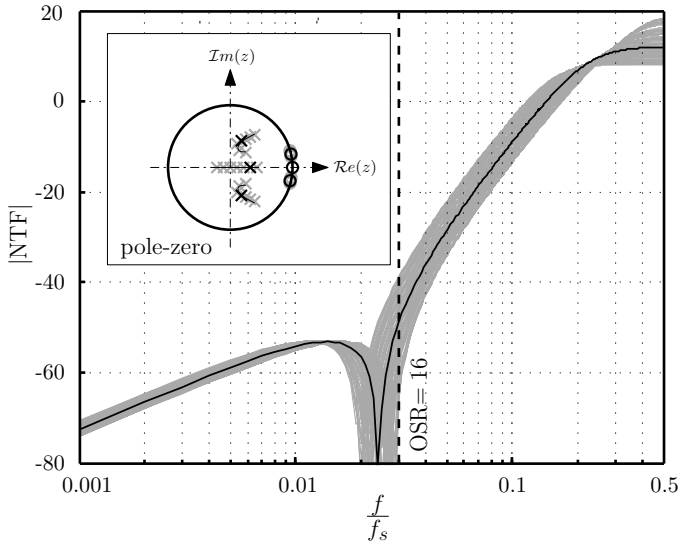

Figure 3.2: Third order NTF with poles in Butterworth position, optimized zeros and $\mathcal{H}_\infty = 4$. Effect on the NTF for $\pm$ 20 % integrator coefficient variations in the architecture of fig 3.1. ($a_1 = 1$, $a_2 = 1$, $a_3 = 1$, $c_1 = 1.5482$, $c_2 = 0.9063$, $c_3 = 0.4114$, $g = 0.0620$)

Fig. 3.2 shows the effect of 100 uniformly distributed integrator coefficient variations within $\pm$ 20 % on the NTF for a typical 3rd-order modulator design with loopfilter from equation (2.45). The nominal NTF is shown in black, while the gray band indicates the influence of the variations. The feedforward coefficients are taken 1 to implement the required loopfilter here. In reality the designer will apply the appropriate output scaling at each integrator stage, as described in the previous chapter. However, even with non-unity feedforward coefficients, it can be seen from equation (3.1) that integrator coefficient variations will have the same impact on the loopfilter. Although all modulators remain well below their stability boundary, the noise suppression within the signal band shows a large variation due to process variations. Using equation (2.22) to determine the maximum sta-

ble amplitude, the peak SQNR values vary between 75 dB and 82 dB for a 3-bit quantizer modulator with an OSR of 16. To ensure the effective ADC performance, this leads to quite conservative designs.

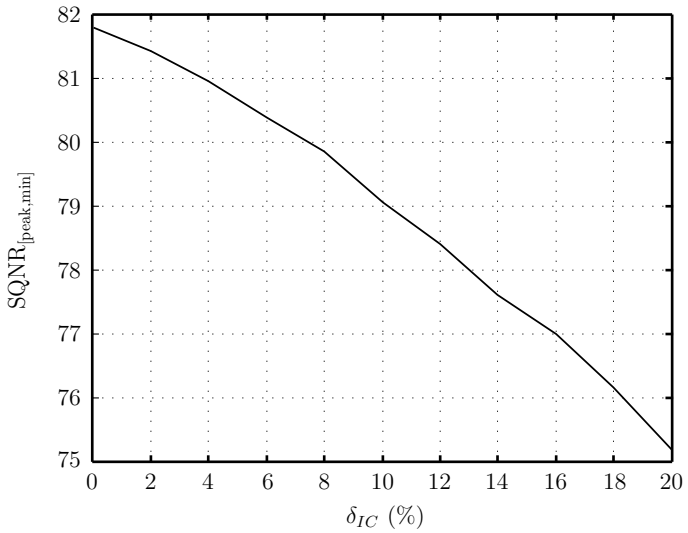

Figure 3.3: Minimum achievable $\mathrm{SQNR}_{\mathrm{peak}}$ for the third order NTF in function of the integrator coefficient variations.

To avoid large performance degradation, coefficient tuning is a well established solution to tackle this problem [24, 26, 32–34]. Fig. 3.3 shows the influence of the relative integrator coefficient variations on the minimum achievable $\mathrm{SQNR}_{\mathrm{peak}}$ for the previous example. A tune accuracy of 5-10 % usually suffices to limit the performance degradation to 2-3 dB in CT ΣΔ modulators [32, 34]. To tune the coefficients, an extra bit-selectable capacitor bank is present at each integrator. In most cases a 4-5 bit tuning range is sufficient. By only changing the capacitor value, the modulator's thermal noise performance and linearity are not affected. Two main tuning strategies can be found in literature. In one case a replica integrator circuit is present, which is used as RC-oscillator (or g_mC oscillator in the case of g_mC integrators). The oscillation period is proportional to the RC time constant and is determined by a digital counter [26, 32, 33]. Based on this measurement, the capacitors can be tuned for the required RC value. In another case the capacitor tuning bits are determined by analyzing the

digital output of the modulator. In [34], the statistical variance of the first-order difference of the modulator output is used as a tuning criterion. From the design phase, the expected value for this criterion is known and can be approximated by changing the capacitor tuning values.

The dependency on the absolute RC time constants distincts the CT $\Sigma\Delta$ modulator from the DT modulator (see equation (3.2)). In a DT modulator, the loopfilter is in the $\mathcal{Z}$-domain and its coefficients are only depending on capacitor ratios. As such, process variations are highly suppressed due to the good correlation between the capacitor values within the same modulator. As a consequence the DT modulator's frequency response scales with the applied clock frequency. Hence the modulator can be used in a broad frequency range operation (as long as the integrator stages still have a sufficient bandwidth overhead compared to f_s). The CT $\Sigma\Delta$ modulator is clearly only designed for 1 clock frequency.

3.2.2 Mismatch

Mismatch is a second source of variations which can influence the integrator coefficients. It represents the deviations between the coefficients within the same modulator, which was not taken into account by the process variations. However, since good correlation exists between devices on the same die, the mismatch influence is very small [31]. Furthermore, mismatch can be controlled by the designer [35–38]. In practice, the mismatch error on the integrator coefficients can easily be limited to 1 % or less [37]. As such, mismatch is not considered as a design consideration for CT $\Sigma\Delta$ modulators, as it will always be overruled by process variations.

Next to the integrator coefficients, the modulator architecture from fig. 3.1 also contains the feedforward coefficients a_i and the local feedback coefficient g. These coefficients are determined by a ratio of resistor or capacitor values in a typical implementation and hence they are only subjective to mismatch. In the same philosophy, their variation will also be overruled by the process variations of the integrator coefficients.

Only one component in a multibit $\Sigma\Delta$ modulator (both DT and CT) is highly susceptible to mismatch: the DAC. Since the DAC is in the global feedback path, its non-idealities will not be suppressed by the modulator loop gain. Therefore, in the signal band, the DAC should achieve the full ADC accuracy. Since the global ADC accuracy will be in the range of 11-16 bit, the matching between the DAC unit cells should be equally accurate. Matching above the 10-bit level is hard to achieve by only increasing

physical device area. Therefore, calibration of the DAC unit cells has been proven as a good practice in high resolution DAC design and can also be applied for ΣΔ modulators [26, 39, 40]. Next to this, dynamic correction of the DAC error can also relief the issue. In this case, the oversampling behaviour of the system is exploited. By selecting the DAC unit element cells with a certain algorithm, the DAC error can be shaped out of the low-frequency band-of-interest. These algorithms are identified as dynamic element matching (DEM) techniques, because they dynamically allocate the selection signals to the DAC unit cells [41, 42]. A popular algorithm is data-weighted averaging (DWA) [43, 44], where a rotating pointer tries to select all unit cells an equal number of times as fast as possible. This way, on average the matching error will disappear. In the spectral domain, the error is first-order noise shaped and its contribution within the signal band is suppressed this way.

In high-bandwidth ΣΔ modulators, due to higher clock frequencies, dynamic DAC errors start to have an impact on the accuracy. These are the errors linked to the non-ideal settling behaviour of the DAC pulse, which can be caused by charge injection, clock feedthrough or small time delay errors in the DAC. In [45], a clear analysis of the problem has been made. It was shown that DEM techniques which are optimized to enhance the static behaviour of the DAC (due to the matching error) can even worsen the dynamic DAC response. By doubling the number of unit cells in the DAC and by constraining the use of a specific cell to only one of two subsequent clock cycles, dynamic DAC errors can also be shaped using the standard DEM techniques.

3.3 Excess Loop Delay

In the system architecture of fig. 3.1 the quantizer determines the modulator output bits at the clock sample moment. At the same time, these bits are directly fed back by the DAC pulse to the input of the modulator. In reality, the quantizer cannot make an instantaneous decision and some delay will always be present. Furthermore, the feedback DAC will also exhibit delay in the production of its output waveform. For multibit quantization it also includes the delay of DEM techniques, necessary to improve the feedback DAC performance. These two time delay effects can be modeled by an extra analog delay element in the feedback path of the modulator. This is shown in fig. 3.4 were the dashed rectangle contains an analog element with delay τ. The effect is denoted as excess loop delay (ELD) and has been

described by several authors as being an extra cause of degradation of the loop performance [20, 46, 47].

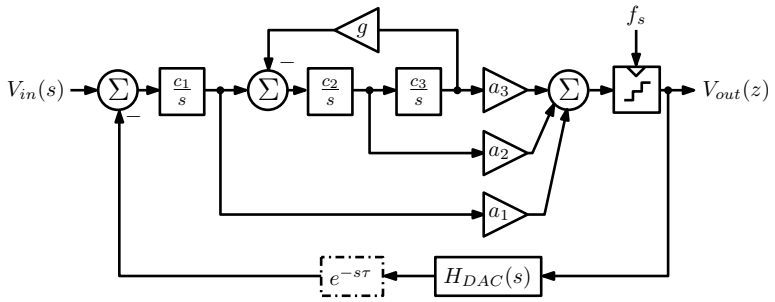

Figure 3.4: The modeling of ELD in a third-order CT ΣΔ modulator architecture.

Fig. 3.5 shows the effect of ELD on the third order maximally flat design with $\mathcal{H}_\infty = 4$. The delay is swept from 0 to a half clock cycle delay. The nominal NTF is shown in black, the grey bundle indicates the effect of increasing delay. For the nominal NTF, one can see that the pole-zero plot contains a pole-zero doublet at the origin. With non-zero delay, the pole of this doublet shifts away while the zero remains at the origin, and the effective order of the resulting NTF increases with 1. In the pole-zero inlet of fig. 3.5, the root locus curve of the poles can be seen. For small delays, two real poles are present, which move towards each other to become complex once the delay has crossed a certain threshold. In the mean time, the original complex poles are shifting towards the unit circle and for delays in the order of $0.17T_s$, the NTF becomes unstable. This can also be seen from the resonance, which is visible in the NTF plots. Since we are dealing with an oversampled system, it is clear that the influence of delays up to half a clock cycle is rather limited within the signal band. As such, ELD in mutibit CT ΣΔ modulators mainly affects the stability. This makes sense, because the delay can be seen as an extra phase shift, which does not change the amplitude behaviour of the loop. Remember that this will limit the maximum stable input amplitude. Although in-band noise has not increased, the peak SQNR will non the less decrease.

A simple explanation why the loopfilter order increases due to excess loop delay can be found in fig. 3.6. The delayed NRZ pulse can be written as the sum of two pulses, of which the second one is a short pulse of length

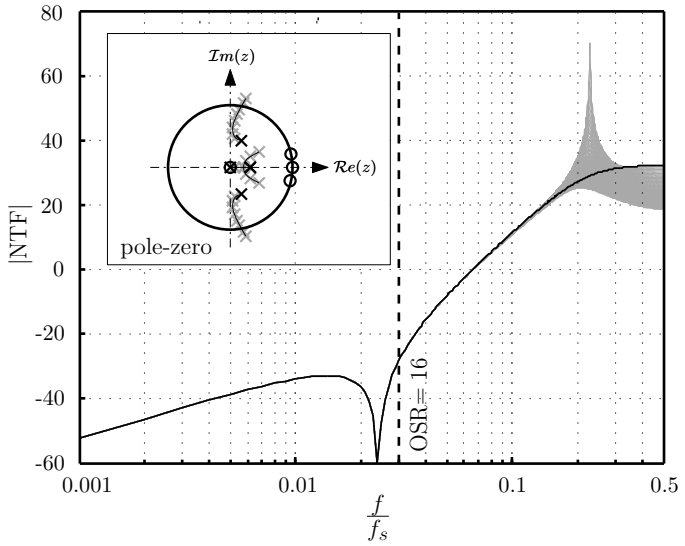

Figure 3.5: Third order NTF with poles in Butterworth position, optimized zeros and $\mathcal{H}_\infty = 4$. Effect of ELD between $[0, \frac{T_s}{2}]$ on the NTF with a NRZ feedback DAC.

τ that is delayed by 1 clock cycle. As such, the equivalent DT loopfilter can be found by taking the impulse-invariant-transformation of the sum of these two contributors:

$$\begin{aligned} H_{eq}(z) &= \text{IIT}\{H(s)H_{DAC,1}(s)e^{-s\tau}\} + \text{IIT}\{H(s)H_{DAC,2}(s)e^{-sT_s}\} \\ &= H_{eq,1}(z) + z^{-1}H_{eq,2}(z). \end{aligned} \tag{3.3}$$

Both equivalent DT filters $H_{eq,1}(z)$ and $H_{eq,2}(z)$ are still N-th order filters, but due the clock-cycle delay in the second term, the global DT loopfilter will become of order $N+1$. An extra pole in the origin appears for the equivalent DT loopfilter. This results in the NTF zero at the origin, illustrated in fig. 3.5.

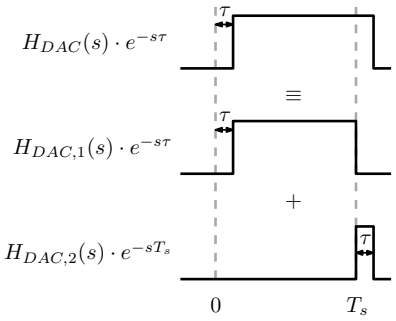

Figure 3.6: Illustration of the modulator's order increase due to ELD.

3.3.1 Synchronization Flip-flop and Coefficient Tuning

In reality, the loop delay is not fixed but depends on the quantizer input level. Typically, the quantizer delay will be larger for smaller input signals. Therefore the system behaviour will become signal dependent and spurious tones will appear in the output spectrum. A generally applied solution to make the loop delay fixed, is the introduction of a synchronization flip-flop in front of the feedback DAC [24, 33]. The clock signal for this flip-flop is usually a delayed version of the system clock by a half or a quarter of the clock period. This way only the delay of the feedback DAC contributes to the variable part of the loop delay, which should be made small by design.

Once the delay has been fixed by a synchronization flip-flop, the coefficients of the modulator can be adjusted to compensate for the delay [20]. The only problem is that the design lacks one degree of freedom to fully map the required NTF behaviour. We identify this as a constrained design. This is clear from equation 3.3, as the number of design coefficients remains N, the modulator order, but the filter order becomes $N + 1$. As such, the desired filter can only be approximated by this strategy.

3.3.2 Alternative Feedback Structures

So far, we have only considered the use of a NRZ feedback DAC. For this DAC type, the slightest delay already leads to a constrained design. Other

types of feedback DACs do not suffer from this disadvantage. In general, the rectangular feedback DAC pulse can be described by (fig. 3.7):

$$H_{DAC}(s) = \frac{e^{-\alpha s} - e^{-\beta s}}{s}, \tag{3.4}$$

which reduces to a NRZ pulse for $\alpha = 0$ and $\beta = T_s$. An alternative is the return-to-zero (RZ) DAC [20], where the feedback value is only held during the first half of the clock period ($\alpha = 0$ and $\beta = \frac{T_s}{2}$). For the RZ DAC, the delay can be as high as a half clock cycle, before the modulator order rises. As such, the system can still be fully controlled in the case of ELD. Since charge is only fed back during half of the clock cycle, the total current consumption for the RZ DAC doubles, compared to the NRZ DAC.

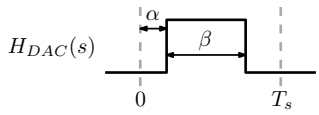

Figure 3.7: General rectangular feedback DAC pulse.

Another solution to fully control the modulator's NTF, is the use of a direct feedback to the input of the quantizer [46]. This is illustrated in fig. 3.8. In the next clock cycle, the previous output is also sampled by the quantizer input. When using a NRZ DAC, the new equivalent loopfilter can be written as:

$$H_{eq}(z) = \text{IIT}\{H(s)H_{DAC}(s)e^{-s\frac{T_s}{2}}\} + dz^{-1}. \tag{3.5}$$

The direct feedback path adds an extra degree of freedom and the global $N + 1$-th order loopfilter can be fully controlled. In [47], the coefficients for the new unconstrained modulator design (including the direct feedback coefficient) are calculated based on a Taylor series expansion of the delay factor $e^{-s\tau}$.

In a feedback topology, a drawback of the direct feedback path is that generally a dedicated extra adder circuit is necessary. In the example of fig. 3.8 an analog adder circuit was already present because of the feedforward topology. In [33], the direct feedback path is combined with the use of a combination of NRZ and RZ DAC pulses. The combination of these DAC pulses implements a digital differentiation of the output, and this way

the direct feedback path can be applied at the input of the last integrator, instead of at the input of the quantizer. The need for an extra adder can be avoided this way.

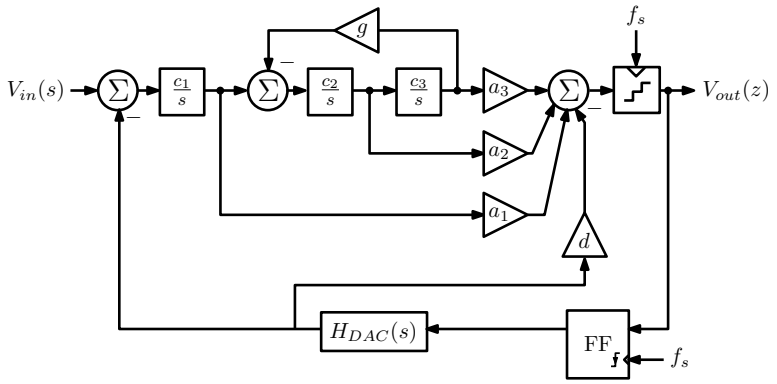

Figure 3.8: Third order FF topology with a synchronization flip-flop on the falling clock edge and a direct feedback path to the quantizer.

3.4 Clock Jitter

Clock jitter is the effect of uncertainty on the actual modulator clock edge. It originates from non-idealities in the clock generation circuit (e.g. thermal noise in a phase-locked loop). The resulting clock edges do not exactly appear at time instants $t = nT_s$, but instead there is an extra statistical uncertainty on their arrival: $t = nT_s + \Delta T_s(n)$. In most cases, this extra clock jitter term is modeled as white noise and follows a zero-mean Gaussian distribution with variance $\sigma^2_{\Delta T_s}$ [48, 49].

In a CT $\Sigma\Delta$ modulator, the clock impacts the system in two places. First the quantizer inherently contains a sampling operation. However, as already stated, the error made here is suppressed by the loop gain and its impact is considered to be negligible [49]. Second, the clock edge has impact on the DAC feedback pulse. The errors made in the DAC are not suppressed by the loop. As such, the impact of clock jitter is most dominant for the feedback DAC. The situation is depicted in fig. 3.9 for the NRZ pulse and the RZ pulse.

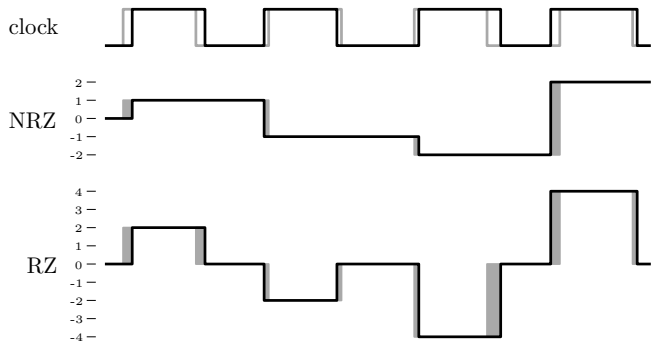

Figure 3.9: Impact of clock jitter on the DAC feedback pulse for a NRZ and a RZ DAC pulse.

The ideal clock edges are indicated in gray, the actual ones in black. We assume that the variation on both rising and falling edge compared to the ideal clock edge has the same variance $\sigma^2_{\Delta T_s}$. The errors made on the multi-bit feedback signals are indicated by the grey rectangles. For the NRZ pulse, the error $e_{jitt}(n)$ is proportional to the difference between subsequent modulator output codes:

$$e_{[\text{jitt,NRZ}]}(n) = \big[V_{out}(n) - V_{out}(n-1)\big]\frac{\Delta T_s(n)}{T_s}. \tag{3.6}$$

The in-band noise contribution due to jitter can be calculated as [49]:

$$\text{IBN}_{[\text{jitt,NRZ}]} = \frac{\sigma^2_{\Delta T_s}}{T_s^2}\frac{2}{OSR}\int_0^{\frac{f_s}{2}} |(1-e^{-j2\pi fT_s})\text{NTF}(e^{j2\pi fT_s})|^2\frac{\Delta^2}{12}\text{d}f. \tag{3.7}$$

For the RZ pulse, the error $e_{jitt}(n)$ is only proportional to the current modulator output code. Also, because the feedback pulse is reset in the second half of the clock cycle, an error occurs on both rising and falling edge:

$$e_{[\text{jitt,RZ}]}(n) = V_{out}(n)\frac{\Delta T_{s,rise}(n) - \Delta T_{s,fall}(n)}{T_s}. \tag{3.8}$$

Remember that the feedback signal levels in the RZ DAC are also double as high as in the NRZ pulse. On average, the same energy must be fed back and the RZ pulse only uses half of the clock period to do so. The in-band noise contribution due to jitter can be calculated as [18, 49]:

$$\mathrm{IBN}_{[\mathrm{jitt,RZ}]} = 8\frac{\sigma^2_{\Delta T_s}}{T_s^2}\frac{2}{OSR}\int_0^{\frac{f_s}{2}} |\mathrm{NTF}(e^{j2\pi f T_s})|^2 \frac{\Delta^2}{12}\mathrm{d}f. \tag{3.9}$$

Compared to the NRZ pulse an extra factor of 8 appears, of which a factor of 2 is associated to the jitter influence on both rising and falling edge and another factor of 4 originates from the double signal levels.

A third feedback pulse, which we did not mention so far, is the switched capacitor (SC) feedback pulse [18, 23, 50]. The switched capacitor pulse appears by connecting a charged capacitor to the first integrator input. This situation is similar to a DT ΣΔ modulator. The waveforms are depicted in fig. 3.10. The current pulse can be described by the following equation:

$$h_{DAC,SC}(t) = I_{SC}e^{-\frac{t}{\tau}}, \tag{3.10}$$

where τ is the settling time-constant of the charge transfer, correlated to the first integrator opamp GBW. To integrate the same charge as for the NRZ pulse in one clock period, the current factor can be calculated as:

$$I_{SC} = \frac{T_s}{\tau}\frac{1}{1-e^{-\frac{T_s}{\tau}}} \approx \frac{T_s}{\tau}. \tag{3.11}$$

The approximation is valid due to the requirement that the GBW needs to exceed the sample frequency by a factor 3 or more and hence $T_s \gg \tau$.

The in-band noise contribution due to jitter can now be calculated as [18, 23]:

$$\mathrm{IBN}_{[\mathrm{jitt,SC}]} = 2\left(\frac{T_s}{\tau}\frac{e^{-\frac{T_s}{\tau}}}{1-e^{-\frac{T_s}{\tau}}}\right)^2 \frac{\sigma^2_{\Delta T_s}}{T_s^2}\frac{2}{OSR}\int_0^{\frac{f_s}{2}} |\mathrm{NTF}(e^{j2\pi f T_s})|^2 \frac{\Delta^2}{12}\mathrm{d}f. \tag{3.12}$$

The first term scales the error contribution to a very small value compared to the rectangular pulses. This can be seen from fig. 3.10, as the errors

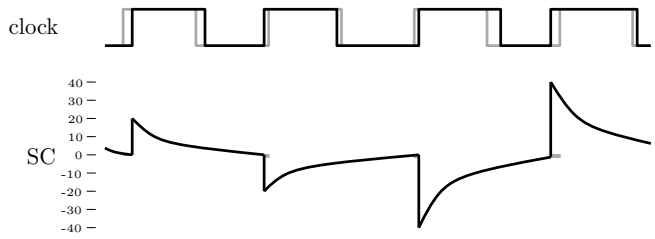

Figure 3.10: Impact of clock jitter on the DAC feedback pulse for a SC DAC pulse.

occur at the end of the clock period, when the largest portion of the charge has already been transferred.

To conclude, we can state that independent of the DAC pulse, the in-band jitter contribution is mainly determined by the NTF out-of-band behaviour. As such, it is closely related to the stability issue for ΣΔ modulators. Not only will more aggressive NTFs have a lower maximum stable amplitude, they will also be more subjective to clock jitter. On the other hand, the DAC pulse has a significant impact on the in-band jitter noise. For the rectangular feedback pulses originating from a current steering DAC, the RZ pulse is more subjective to clock jitter, because of the influence of both rising and falling edge and because of the higher signal levels compared to the NRZ pulse. These pulses are generally outperformed by an order of magnitude by the switched capacitor pulse. This explains why the issue of clock jitter is mainly allocated to CT ΣΔ modulators. Of course, there exists a large difference in current profile between the pulses. In a SC DAC, a peak current has to be delivered by the first stage. This will increase both the bandwidth and slew rate requirements for this stage (and thus the current consumption). For a RZ DAC pulse, the current always drops back to zero in the middle of the clock period. Although slew rate requirements are not as stringent as for the SC pulse, it still remains a point of attention. For the NRZ DAC pulse, slew rate requirements are most relaxed, since the current only jumps between the different output codes of the multibit modulator. In that case, inter-symbol interference (ISI) is a point of attention, as data dependent settling of the DAC can create harmonic distortion in the output signal [51].

3.5 STF Design

In chapter 2, the STF and its implicit anti-aliasing property were already briefly covered. In the STF frequency response, an important role is played by the continuous-time forward filter. This is the continuous filter from the modulator input to the input of the quantizer, when no feedback DAC signal is present. In fig. 2.10 this filter happened to coincide with the loop-filter, which exhibits a first order roll-off at high frequencies due to stability reasons. This would be the case for a FF modulator topology (see fig. 2.14). For a FB topology, the forward filter $G(s)$ can be written as:

$$G(s) = \frac{\prod_{i=1}^{N} c_i}{s^N}, \tag{3.13}$$

which exhibits an N-th order roll-off for high frequencies. More generally the STF is identified by following equation:

$$STF(s) = G(s)NTF(e^s). \tag{3.14}$$

The STF displayed in fig. 3.11, shows the implementation of the example of chapter 2 in a FB topology. The increased high-frequency suppression is immediately visible when comparing to fig. 2.13. A beneficial side-effect of this higher order suppression is that the peaking behaviour just outside the signal band has disappeared. In some cases, it will still be present depending on the aggressiveness of the NTF, but at least it is better suppressed than for the FF topology.

The explicit design of the STF has gained more attention in the scientific community. Proper design could avoid the need for complex high-order overload prevention filters. This is especially important for ADCs used in analog front-ends for wireless/wireline communication, where adjacent channels and interferers should not compromise the dynamic range used for the actual received channel. In [25], a combination of explicit lowpass filtering on the input and highpass filtering on the feedback DAC signal is used in combination with a FF topology. This way the first order STF is extended by the roll-off of this extra lowpass input filter. The overall stability of the NTF is not affected and thus still benefits from the better power efficiency of the FF topology. In [52], the modulator loop is extended with highpass filter feed-forward paths from the global input to the inputs of each integrator section. This way, both for the FF and FB topology, a flat STF frequency response can be achieved. The STF in multi-stage noise

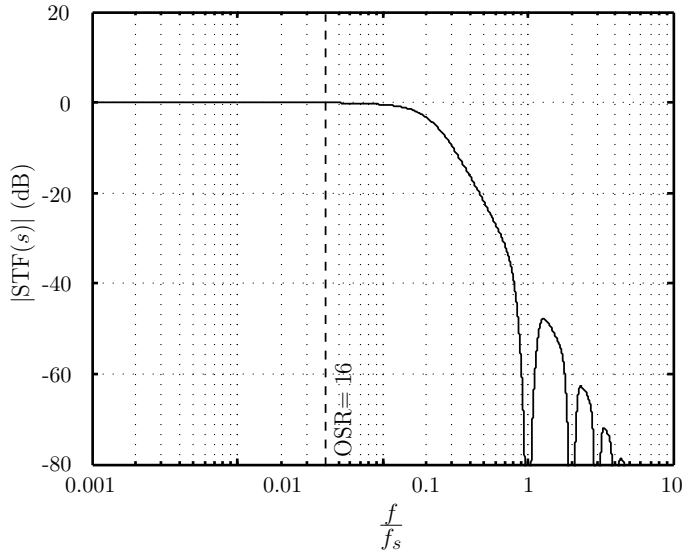

Figure 3.11: Signal transfer function for the CT ΣΔ modulator with third order NTF with poles in Butterworth position, optimized zeros and $\mathcal{H}_\infty = 4$ for the FB topology.

shaping (MASH) CT ΣΔ modulators is investigated in [53]. It is proven that, contrary to previous belief, also the cascaded stages have an influence on the STF behaviour.

3.6 Parasitic Poles and Zeros

The loopfilter of a CT ΣΔ modulator is a continuous cascade of integrator sections. Depending on the actual integrator circuit implementation (single-stage opamp-RC, two-stage opamp-RC with Miller compensation, g_mC, ...), multiple high-frequency parasitic poles and zeros can be present in the loopfilter. As a consequence of the impulse-invariant-transformation, this will also result in extra poles and zeros in the NTF possibly degrading the stability. This is different than for the DT modulator. For switched capacitor circuits, the interfaces between the integrator stages are cleanly separated. This simplifies the design of the DT ΣΔ modulator as correct operation of the individual stages, generally leads to the expected loopfilter

behaviour. For the CT modulator, stability issues can still occur when cascading the individually characterized integrator stages.

When using an active-RC integrator, the limited GBW of the opamp introduces a parasitic pole with time-constant τ_p in the integrator transfer function:

$$ITF_{GBW} = \frac{c_i}{s} \cdot \frac{2\pi f_{GBW}}{s + 2\pi f_{GBW} + c_i} \approx \frac{c_i}{s} \cdot \frac{1}{1 + \frac{s}{2\pi f_{GBW}}} \tag{3.15}$$

$$= \frac{c_i}{s} \cdot \frac{1}{1 + s\tau_p}. \tag{3.16}$$

Due to the oversampled nature, the integrator coefficients are generally much smaller than the opamp GBW and the approximation is justified. Similar to the integrator coefficients, the GBW of an opamp is a combination of a capacitor and a transconductance. For this reason, the variation on the time-constant τ_p will also be in the range of $\pm$ 20 %.

The effect of parasitic integrator poles shows resemblance with the effect of excess loop delay, which also introduces phase shift at higher frequencies. This was identified in [29]. A method is described to approximate the effect of higher order dynamics as extra loop delay. As such, the same strategies as for ELD can be applied to tackle this non-ideality: coefficient tuning and introduction of extra feedback paths.

Part II

Novel Design Strategies for Continuous-Time $\Sigma\Delta$ Modulators

Chapter 4

Robust Design Based on the Nyquist Criterion

4.1 Introduction

Due to the large correspondence between the loop characterization in both DT and CT $\Sigma\Delta$ modulators, pioneer designers of CT modulators thankfully made use of the extensive knowledge on systematic NTF design for DT modulators [5, 6, 8]. This was a logical step, but it did not always lead to the expected system performance. In the previous chapter, several parasitic effects for CT $\Sigma\Delta$ modulators were presented. It should be clear that these effects will lead to modulator designs which will most certainly deviate from the intended design, or in some cases can even be unstable.

So far, design strategies for CT $\Sigma\Delta$ modulators have not enjoyed a lot of attention in literature. In [54] a systematic design strategy for $\Sigma\Delta$ modulators is introduced. It can be used to map to any modulator architecture (FF, FB or MASH) both for DT and CT modulators. It consists of an algorithmic optimization mainly on the system level. However, it does not take into account any of the parasitic effects of CT $\Sigma\Delta$ modulators and, as such it is mainly useful for unconstrained designs. In [24] a different approach was followed. Instead of starting off from a desired NTF, the system design was initiated from the CT modulator architecture. The continuous-time design parameters were optimized to achieve the required performance. To the author's opinion this is definitely the most promising approach. However, not much details about the optimization procedure were given.

In this chapter, we present a first new design strategy for CT ΣΔ modulators [55]. The strategy starts off from a nominal continuous-time system definition, including some of the parasitic effects. The design strategy is based on the work already performed in [18, 56]. It uses the Nyquist criterion, to install a stability robustness figure of merit. In a second phase, optimal design parameters for the nominal system can be searched, such that its stability robustness is maximized. We will show that this new strategy is particularly interesting for constrained systems.

4.2 Nominal System Definition

To illustrate the design strategy we will use the modulator of fig. 4.1 as a test vehicle. It is a third order CT ΣΔ modulator with the loopfilter in a FF topology. Zero spreading is present by the local feedback path with weight g around the second and third integrator.

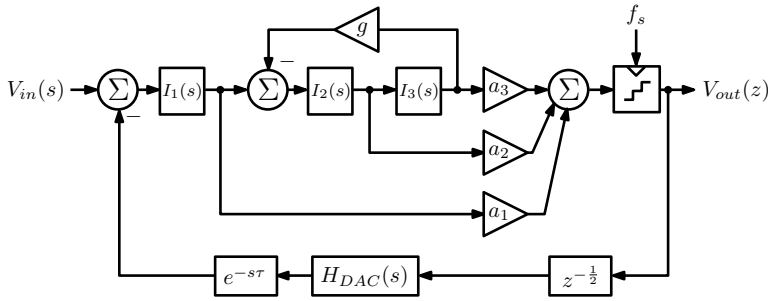

Figure 4.1: Third order FF modulator topology to illustrate the design strategy.

For pure integrator transfer functions $I_i(s)$, the continuous-time loopfilter can be denoted as:

$$H(s) = \frac{a_1c_1(s^2 + c_2c_3g) + a_2c_1c_2s + a_3c_1c_2c_3}{s(s^2 + c_2c_3g)}. \tag{4.1}$$

It is clear that the FF coefficients a_i are only involved in the integrator output scaling. This can be performed afterwards without changing the global loopfilter. It is a tradeoff between the FF coefficients and the integrator coefficients c_i. As such, we will only consider the integrator coefficients as

design parameters, while the FF coefficients will by systematically taken 1 during the system design. Since we have stressed out to insert some of the parasitic effects in the nominal system, a fixed parasitic pole at f_s is included in each integrator transfer function:

$$I_i = \frac{c_i}{s} \cdot \frac{1}{1 + \frac{s}{2\pi f_s}}, \quad \tau_p = \frac{1}{2\pi f_s}. \tag{4.2}$$

Next to this, also a synchronization flip-flop is present which introduces a fixed delay of a half clock cycle $\frac{T_s}{2}$ (clocked on the negative clock edge). On top of this, an extra delay of 10 % of the clock period is added to model the mean process delay for the feedback DAC:

$$\tau = \frac{T_s}{10}. \tag{4.3}$$

A NRZ DAC pulse is chosen. The quantizer unit has a 3-bit resolution and the OSR equals 16. Although this system is defined quite in detail, the principles which will be illustrated hereafter are valid in a broader sense, also for other topological choices.

The equivalent DT loopfilter for the nominal system can be found by means of the IIT:

$$H_{eq}(z) = \mathrm{IIT}\left\{ H(s) \cdot \frac{1 - e^{-s}}{s} \cdot e^{-s\frac{6}{10}} \right\}. \tag{4.4}$$

This DT transfer function will be further used to analyze the stability of the modulator design. By using the IIT, we have now incorporated the information of the extra parasitics that we have added in the nominal system. For example, we already know that by adding ELD, the DT loop order has increased by 1 and our system has become constrained.

On top of this nominal system, parameter variations will be superimposed. In this case the integrator coefficients and the parasitic pole time-constants will still vary with ±20 %. Also, since we consider a converter with a low OSR and a high signal bandwidth, a high speed feedback DAC is present. The delay τ can easily vary with ±50 % due to process variations. These variations will not be considered as a-priori information for the Nyquist-based design strategy. Instead, we will try to optimize the global stability of the nominal system (without parameter variations) in function of the design parameters. Afterwards, the variations will be superimposed to check if the design still remains stable even in the presence of these variations.

4.3 Stability Robustness

4.3.1 Discrete-Time Nyquist Criterion

Similar to continuous-time systems, the stability of a closed-loop discrete-time system can be investigated by means of the open-loop transfer function. The situation is depicted in fig. 4.2. The zeros of the characteristic equation $1 + H_{eq}(z)$ should not be located outside of the unit circle for stability. To evaluate the Nyquist criterion, the Nyquist plot is constructed. This plot evaluates the loopfilter along a specific contour in the complex plane, namely the unit circle: $z = e^{j2\pi f T_s}$, where f goes from $-\frac{f_s}{2}$ to $\frac{f_s}{2}$. The Nyquist criterion defines the following relation:

$$Z = P + N, \tag{4.5}$$

where

- Z is the number of unstable zeros of $1 + H_{eq}(z)$,
- P is the number of unstable poles of $H_{eq}(z)$,
- and N is the net number of counter clockwise encirclements of the critical point -1 in the Nyquist plot.

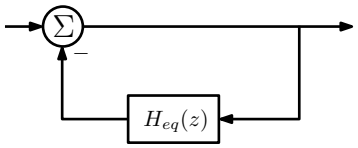

Figure 4.2: Stability for a discrete-time feedback loop.

An example is displayed in fig. 4.3 for our third order test vehicle. In the example the NTF zeros are spreaded inside the signal band. Due to this, the equivalent DT loopfilter $H_{eq}(z)$ contains three resonant poles on the unit circle, which is displayed in the inlet of the figure. In the proximity of these resonant poles the Nyquist contour is slightly adjusted. An infinitesimal encirclement around a resonant pole is provided which will result in a semicircle in the Nyquist plot with infinite radius accompanied by a phase decrease of 180 °. The resonant poles do not account for unstable open loop poles, as such $P = 0$ and there should be no net encirclements of -1 for a stable modulator. In fig. 4.3 this is the case, as the three resonant poles

create 1 clockwise encirclement with infinite radius which is counteracted by the counter clockwise encirclement in the figure. Also note that at $f = \frac{f_s}{2}$ the Nyquist plot ends on the real axis. This is in contrast with CT systems where the Nyquist plot for band-limited systems always ends in the origin for $f \to \infty$.

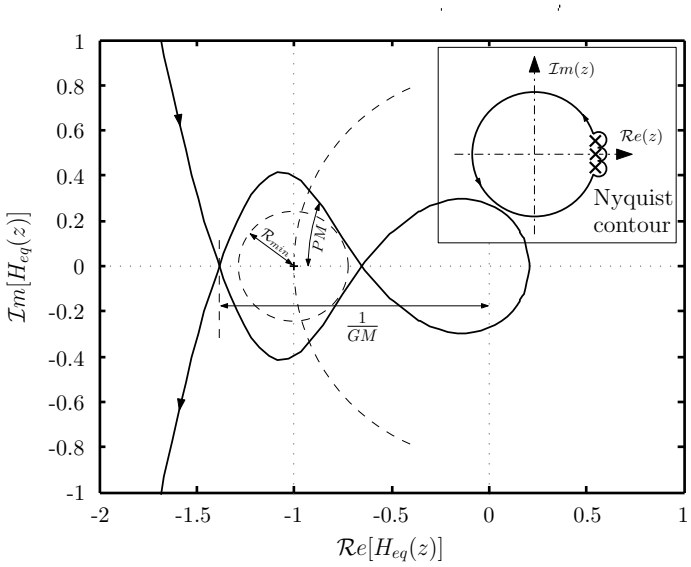

Figure 4.3: Nyquist plot example for the equivalent loopfilter of a third order CT $\Sigma\Delta$ modulator with the architecture of fig. 4.1.

4.3.2 Stability Robustness Figure of Merit

Although we can evaluate stability with the Nyquist criterion, it still defines a binary criterion. A system is either stable or it is unstable. In the context of the expected parameter variations, we are interested in defining a figure of merit which indicates the modulator's stability robustness. From control theory, we are already familiar with two stability margins, phase margin (PM) and gain margin (GM) [57]. They are also indicated in fig. 4.3. PM is defined on the unit circle as the extra phase shift required to make the system unstable. GM is defined on the real axis, as the gain increase or decrease required to make the system unstable. Although these criteria indicate a sound margin for respectively extra phase shift and extra gain in the loop, parameter variations in a CT $\Sigma\Delta$ modulator translate

into more complex combinations of both gain and phase variations. If we look at pure integrator coefficient variations we can see from equation 4.1 that, although the different coefficients will vary in the same direction, the influence is different for the individual terms of the loopfilter numerator. As such it cannot be seen as a pure gain scaling and also introduces extra phase variation. Furthermore, this is only the effect on the analog loopfilter. The IIT which produces the equivalent DT loopfilter also introduces extra gain scaling and phase shift. It will only approximate the continuous-time loopfilter properly for low frequencies. For higher frequencies, where the stability properties of the loop are determined, the approximation will start to divert. Due to the latter, the variation of ELD and of the parasitic poles of the integrators also does not evaluate to a pure phase shift in the discrete-time domain.

The observation of a combined phase and gain shift due to modulator parameter variations has influenced the introduction of a new stability robustness criterion. The minimum distance from the Nyquist plot to the critical point -1 is proposed [18, 55], which we will define as $\mathcal{R}_{min}$. This distance is illustrated in fig. 4.3 and can mathematically be identified as:

$$\mathcal{R}_{min} = \min_{f} |1 + H_{eq}(j2\pi f)|. \tag{4.6}$$

As stability is determined by the number of encirclements of -1, a dangerous situation occurs when the Nyquist plot comes close to this critical point. The parameter variations in a CT $\Sigma\Delta$ modulator will create a family of Nyquist plots, around the nominal Nyquist plot. This illustrated in fig 4.4. On the left hand side, the variations are applied to the nominal modulator of fig. 4.3 with moderate design parameters. We can see the influence for 100 random modulators, with uniform distributed parameter variations. As described above, 20 % variation is included for the integrator coefficients and parasitic poles, and 50 % for the delay variation of the feedback DAC. The nominal system exhibits an $\mathcal{R}_{min}$ value of 0.257. We can see that all the resulting modulators remain stable. A clear eye opening still exists around the critical stability point. This means that the variations could even be more aggressive, before the modulator starts suffering from instability. On the right hand side of fig. 4.4, a more aggressive version of the third order test vehicle architecture is implemented. The nominal modulator only exhibits an $\mathcal{R}_{min}$ value of 0.157 in this case. The system is only marginally stable anymore for the same parameter variations. This can be seen from the fact that the eye opening in the Nyquist plot is practically closed. Although all modulators still have their NTF poles within the unit circle, for some

samples small additional variations will definitely draw them to instability. From these two examples, it can be seen that a larger value of $\mathcal{R}_{min}$ for the nominal modulator leads to increased stability robustness against parameter variations.

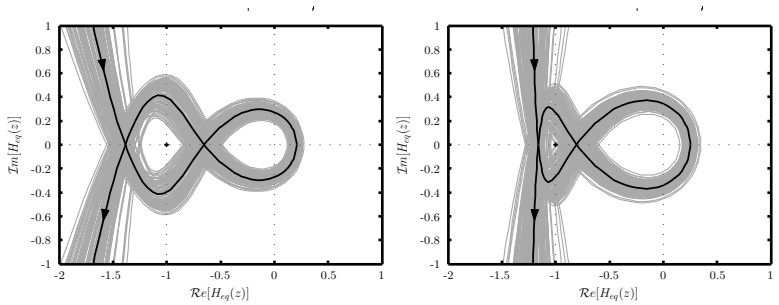

Figure 4.4: Nyquist plots due to parameter variations for (left) the modulator from fig. 4.3 with moderate design parameters and (right) a more aggressive implementation with decreased stability robustness. The gray curves are the Nyquist plots due to parameter variations, the black curve is the nominal Nyquist plot.

4.3.3 Relation to $\mathcal{H}_\infty$ Design

Surprisingly the value of $\mathcal{R}_{min}$ can also be linked to $\mathcal{H}_\infty$, the maximum out-of-band gain of the NTF, as:

$$\mathcal{H}_\infty = \max_f |NTF(e^{j2\pi f})| = \Big[\min_f |1 + H_{eq}(e^{j2\pi f})|\Big]^{-1} = \frac{1}{\mathcal{R}_{min}}. \qquad (4.7)$$

As a consequence, the $\mathcal{R}_{min}$ value is practically located in the interval $[0, 1]$, since $\mathcal{H}_\infty$ is always lower bounded by 1. We know from previous chapters that higher values for $\mathcal{H}_\infty$ give rise to better in-band noise suppression but also to a lower value of the MSA. Now we also see that a higher out-of-band gain gives rise to lower stability robustness. This is intuitively clear as better performance must comply with a more aggressive and hence more sensitive modulator. The design strategy from [5] using $\mathcal{H}_\infty$ as design parameter, is therefore also in line with optimizing stability robustness. The difference to our design strategy is that it proposes a fixed NTF pole constellation to

attain the same goal. Also it originates from DT $\Sigma\Delta$ modulator design, and hence can only be used for unconstrained designs.

4.4 Design Strategy

The design strategy that we introduce, is based on the optimization of the $\mathcal{R}_{min}$ value for the nominal modulator. We have found that this optimization is numerically difficult, especially for higher modulator orders. This is partially due to the fact that the $\mathcal{R}_{min}$ value cannot be determined analytically. Gradient-based optimization did not perform well in practical cases, therefore we have used the genetic optimization algorithm *Differential Evolution* [58]. Genetic optimization is based on the biological concept of survival of the fittest. An initial population of several modulators is used to start breeding several generations. A crossover step combines individuals from the current generation (parents), and generates new individuals (children) which contain properties of the both parents. Once in a while, a mutation step also randomly changes the inherited material to guarantee more coverage over the parameter space. The next generation is preserved from the individuals with the best stability robustness (highest $\mathcal{R}_{min}$ values). After a fixed number of generations, the optimum is acquired as the best individual from the final generation.

4.4.1 $\mathcal{R}_{min}$ Optimization for CT $\Sigma\Delta$ Modulators

A flowchart for the design strategy is displayed in fig. 4.5. The genetic optimization runs within an iteration loop, where we increase the requested peak SQNR by 1 dB after each optimization. The optimization itself starts off from a random population. The size of the population is chosen as twice the number of design parameters. After each iteration, the initial population is randomly regenerated, but it is also extended with the optimal modulators of the 3 previous iterations (with lower peak SQNR values). By choosing the initial SQNR value low enough, the resulting modulator from the first iteration is not very aggressive and the genetic optimizer will definitely find a solution in this case. The actual genetic optimization routine runs for 50 generations. The fitness value $\mathcal{F}$ for each individual is the core function to determine the optimal nominal modulator. The population members are tested against following criteria for being considered as a valid solution:

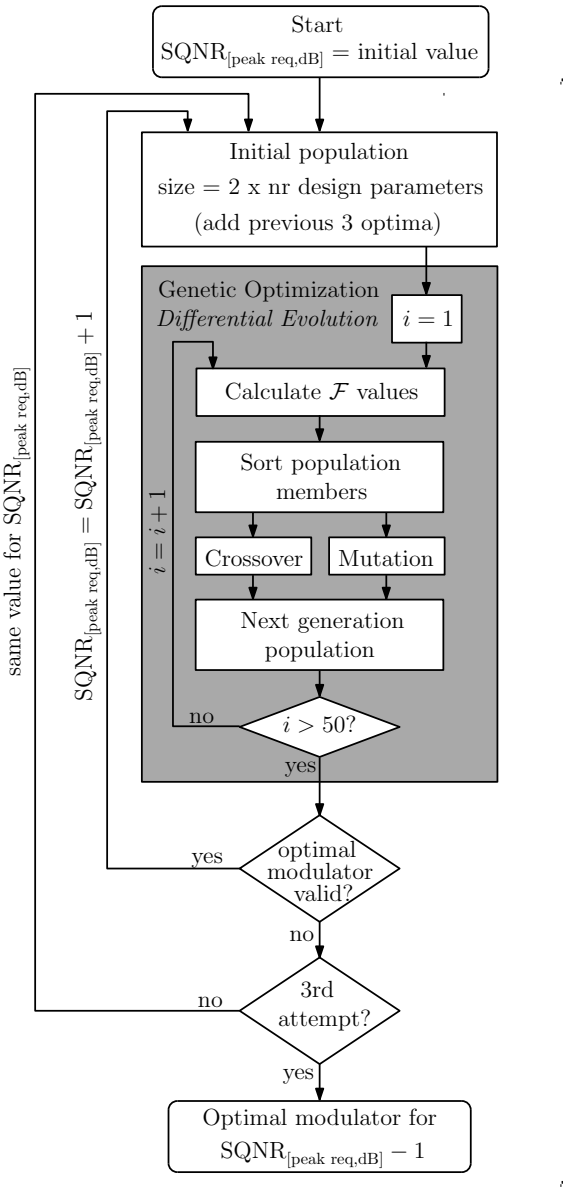

Figure 4.5: Flowchart describing the design strategy based on the Nyquist criterion.

1. The modulator should be stable (have its NTF poles within the unit circle).
2. The modulator should have a reasonable MSA $\geq \frac{1}{\sqrt{2}}$ to be practically usable. As optimization of $\mathcal{R}_{min}$ will generate a lower NTF out-of-band gain, this will automatically lead to more favourable MSA values.
3. The modulator should attain a $\text{SQNR}_{[\text{peak,dB}]} > \text{SQNR}_{[\text{peak req,dB}]}$.

This is resembled in the fitness value $\mathcal{F}$ for each population member:

$$\mathcal{F} = \begin{cases} +\infty & \text{unstable or MSA} < \frac{1}{\sqrt{2}}, \\ \frac{\text{SQNR}_{[\text{peak req,dB}]} - \text{SQNR}_{[\text{peak,dB}]}}{\text{SQNR}_{[\text{peak req,dB}]}} & \frac{\text{SQNR}_{[\text{peak,dB}]}}{\text{SQNR}_{[\text{peak req,dB}]}} < 1, \\ -\mathcal{R}_{min} & \text{valid solution.} \end{cases} \tag{4.8}$$

The *Differential Evolution* algorithm is a minimization algorithm, therefore the fittest member is identified by the lowest $\mathcal{F}$ value. The first two acceptance criteria (stability and MSA criterion), are implemented as hard binary criteria, by assigning an infinite positive value in the case when they are not met. From experience, we found that it was better to install the SQNR criterion as a dynamic criterion in the fitness function. If the modulator attains a too low peak SQNR value, the fitness function is assigned with a term which equals the relative distance from the required SQNR. This way, the violation of the SQNR is favourised compared to the hard binary criteria for stability and MSA. This gives better directions to the optimizer so that the chance of finding a solution in later cross-overs will be more likely. The fitness function will result in a small positive number in this case. Finally, when all acceptance criteria are met, the fitness function is assigned with the inverse of $\mathcal{R}_{min}$. Indeed, it was the purpose all along to optimize the robustness stability. This will result in a negative value for the fitness function between -1 and 0. Only this last category of modulators are valid solutions from the optimization routine. The optimum is selected as the individual with the highest $\mathcal{R}_{min}$ value amongst this category.

Due to the iteration loop, optimal modulator parameters will arise for each increasing value of $\text{SQNR}_{[\text{peak req,dB}]}$. The higher the SQNR performance we require from the modulator, the harder it will become to optimize the $\mathcal{R}_{min}$ value. Hence, we expect the optimum $\mathcal{R}_{min}$ to decrease in function of the required SQNR. If we require too high SQNR requirements, no valid

solutions will be found anymore. This will mainly be due the fact that the MSA criterion cannot be met anymore. The global iteration loop stops if 3 attempts at a certain SQNR value did not lead to any valid solution anymore.

4.5 Design Examples

In this section the design strategy will be applied to third order design examples. To illustrate the advantage of using the Nyquist based $\mathcal{R}_{min}$ criterion, also a comparison is made with the optimization of phase margin as robustness criterion.

4.5.1 Third Order Modulator in Feedforward Topology

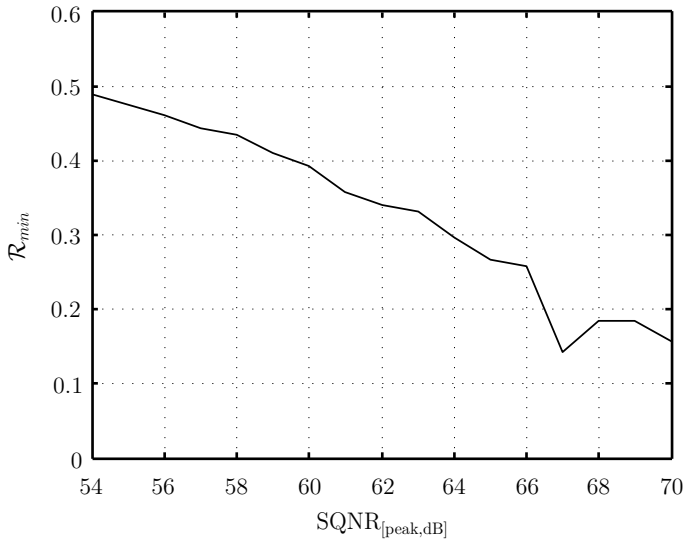

Figure 4.6: Third order CT $\Sigma\Delta$ design example: $\mathcal{R}_{min}$ value in function of the peak SQNR for the optimal nominal modulator.

In this example, the nominal modulator follows the architecture of fig. 4.1. There are 4 design parameters, namely the 3 integrator coefficients c_i and the local feedback coefficient g. The feedback DAC delay parameter τ has a nominal value of $\frac{T_s}{10}$. Also a nominal parasitic pole at f_s is present for

the integrators (according to equation (4.2)). These last two parameters are not considered as design parameters. The design algorithm of fig. 4.5 was applied to these boundary conditions, starting off from a required SQNR of only 54 dB. The optimized $\mathcal{R}_{min}$ values for the nominal modulator in function of the required peak SQNR are displayed in fig. 4.6.

As predicted, the $\mathcal{R}_{min}$ values show a global decreasing trend in function of the performance. The question now remains which nominal modulator to choose to be tolerant to the defined parameter variations. Therefore, parameter variations are applied to evaluate the robustness. For this example the integrator coefficients and parasitic poles are varied by $\pm 20\%$ and the feedback DAC delay τ is varied by $\pm 50\%$. We choose to evaluate the nominal modulator which achieves a peak SQNR of 66 dB ($\mathcal{R}_{min} = 0.257$) and the extreme optimization with a peak SQNR of 70 dB ($\mathcal{R}_{min} = 0.157$).

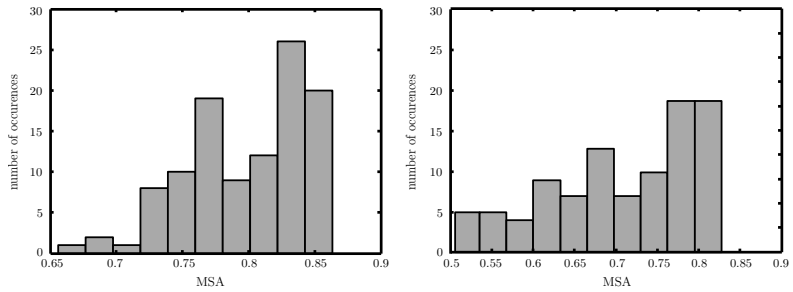

Figure 4.7: Histogram for the maximum stable amplitude due to parameter variations for (left) the nominal modulator with 66 dB performance and (right) the more aggressive nominal modulator with 70 dB performance.

A family of 100 randomly perturbated modulators is generated. On top of that also the corner cases of the variation space are included (8 extra corner cases in this example). The family of resulting Nyquist plots for these 2 optimal nominal modulators were already displayed in fig. 4.4. There, we concluded that the more aggressive nominal modulator is on the edge of instability. This is even more confirmed when we evaluate the maximum stable amplitude. In fig. 4.7, histograms are shown for the MSA in both cases. As the nominal modulator achieves a MSA higher than $\frac{1}{\sqrt{2}}$ (due to the design algorithm), we require the MSA to stay above 0.5 for practical use of the modulator. In the left hand figure, this is the case for all 108 perturbated modulators. All MSA values remain quite confined around the target value. On the right hand side, we can see that the spread in the maximum stable

amplitude has increased. Also, from the 108 resulting modulators, only 98 achieved an MSA above 0.5. Modulators with an MSA below 0.5 have not been displayed in the histogram. Moreover, even though all resulting modulators in this case still have their NTF poles within the unit circle, the resulting MSA values for the most aggressive instances became negative according to equation 2.22. This means that these modulators have become practically unusable.

Table 4.1: Optimal parameters for the third order design example using the Nyquist criterion based $\mathcal{R}_{min}$ optimization.

c_1	c_2	c_3	g	MSA		$\text{SQNR}_{\text{peak}}$	
				nom	min	nom	min
0.879	0.198	0.443	0.308	0.802	0.65	66 dB	57.4 dB

The 66 dB optimization has led to the highest performance nominal modulator which, subjective to parameter variations, was still practically usable (stable and MSA values above 0.5). The design parameters for this optimization are displayed in table 4.1.

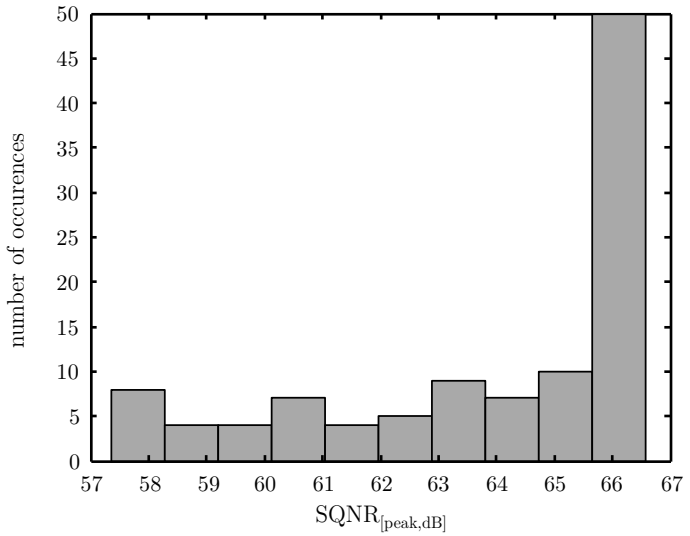

Figure 4.8: Histogram for the peak SQNR due to parameter variations for the nominal third order modulator with 66 dB performance.

Of course, the variations will also influence the peak SQNR performance. In fig. 4.8, a histogram for the peak SQNR is shown. We can see that the performance can drop as low as 57.4 dB. The nominal modulator almost has the best performance. This is because for larger integrator coefficients the in-band quantization noise will decrease, but at the same time the MSA will also decrease due to a more aggressive modulator.

Fig. 4.9 shows the effect of the parameter variations on the resulting optimal nominal NTF. The edge of the signal band for an OSR of 16, is indicated by the dashed vertical line. The variation in the SQNR can be assigned to the large spread in NTF value there. Also, at higher frequencies the variations will increase the out-of-band gain, which will result in a lower MSA value for those specific modulators.

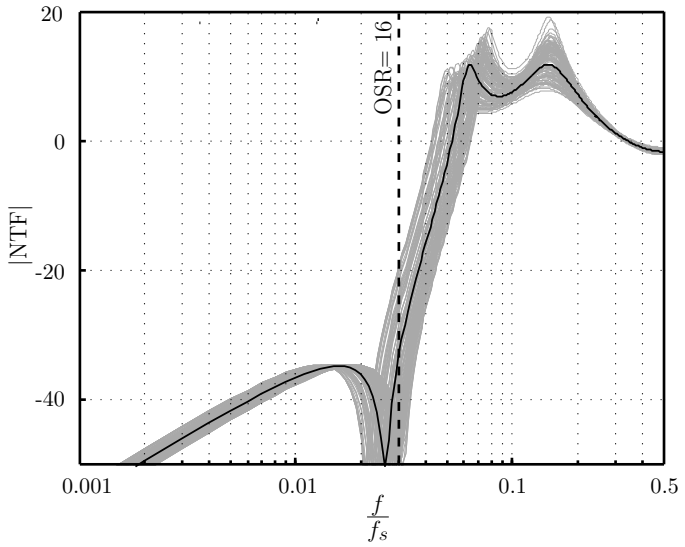

Figure 4.9: Third order design example NTFs due to parameter variations. The nominal modulator is plotted in black.

Extensive time-domain simulations were carried out to obtain the $\mathrm{SQNR}_{\mathrm{peak}}$ for a significant number of perturbated systems. Also, all the corner points of the variation space were added (where all parameters have an extreme variation). For this purpose a Simulink model of the modulator was constructed. A single tone of frequency $\frac{f_s}{4\mathrm{OSR}}$ is applied. Fig. 4.10 shows the result of a the specific modulator where $\delta_{IC} = -20\,\%$; $\delta_{\tau} = -50\,\%$ and $\delta_{\tau_p} = -20\,\%$. This modulator variation gives rise to a MSA of 0.85 and

the minimum peak SQNR of 57.4 dB. The left hand figure shows the output spectrum of the modulator when an input amplitude equal to the MSA is applied. The black curve shows the simulated output spectrum, while the gray curve indicates the design strategy prediction. Good correlation was acquired. The resulting SQNR from the simulation is 57.6 dB. On the right hand side, a dynamic range plot for the specific modulator is displayed.

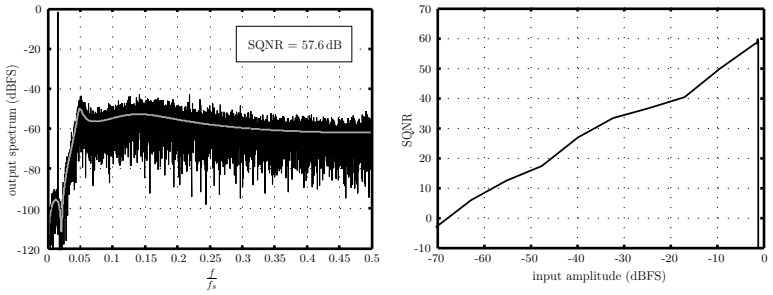

Figure 4.10: Time-domain simulation results for the optimal third order modulator with $\delta_{IC} = -20\,\%$; $\delta_{\tau} = -50\,\%$ and $\delta_{\tau_p} = -20\,\%$: (left) the output spectrum together with the system model prediction and (right) the dynamic range of this specific modulator.

4.5.2 Comparison to Phase Margin Design

To support the statement of using the $\mathcal{R}_{min}$ criterion, we have repeated this design example under identical conditions, but now using the phase margin as optimization criterion. As expected, also the phase margin will drop in function of the required peak SQNR. To make a fair comparison, we have also selected the resulting modulator with a nominal $\text{SQNR}_{\text{peak}}$ of 66 dB. This modulator achieves a phase margin of 25 °in contrast to the previous optimization example where the phase margin was only 21 °. The resulting Nyquist plots due to the variations are shown in fig. 4.11. We can see that due to the phase margin optimization, the nominal Nyquist plot is already very close to the critical point -1 on the real axis. As a consequence, some of the perturbated modulators will have their NTF poles outside of the unit circle. From the 108 samples, only 91 were stable and/or had an MSA which exceeds 0.5.

When we calculate the $\mathcal{R}_{min}$ value for the nominal modulator a value of 0.05 appears. Compared to the previous example where the nominal modulator

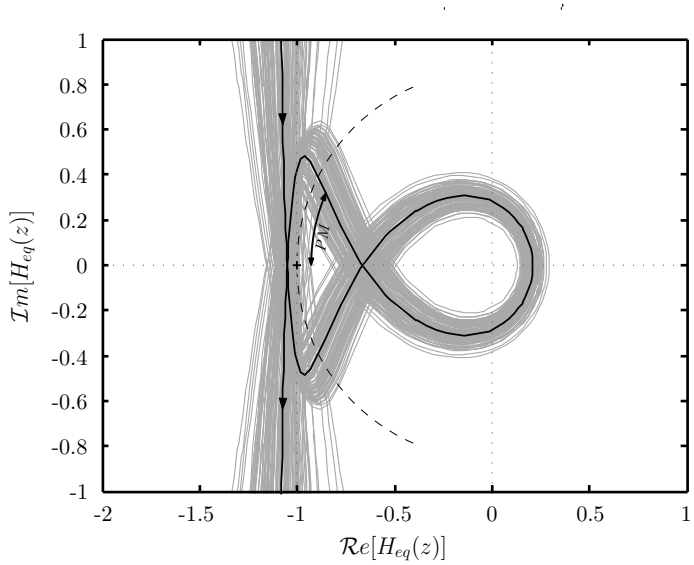

Figure 4.11: Nyquist plots due to parameter variations for the third order modulator using the phase margin as the optimization criterion for the design strategy. The gray curves are the Nyquist plots due to parameter variations, the black curve is the nominal Nyquist plot.

achieves a $\mathcal{R}_{min}$ value of 0.257, we can conclude that the $\mathcal{R}_{min}$ criterion is clearly a better criterion for stability robustness of CT $\Sigma\Delta$ modulators than the phase margin.

4.5.3 Third Order Modulator in Feedforward Topology with Direct Feedback Path

From chapter 3, we know that a possible solution to avoid the constraintness of the system is the introduction of an extra direct feedback path [46]. This feedback path is situated directly at the input of the quantizer as illustrated in fig. 4.12. An extra design parameter d is now present. If we repeat the Nyquist based $\mathcal{R}_{min}$ optimization with the same boundary conditions, the optimal nominal modulator achieves an $\mathcal{R}_{min}$ value of 0.41. Table 4.2 shows the resulting design parameters.

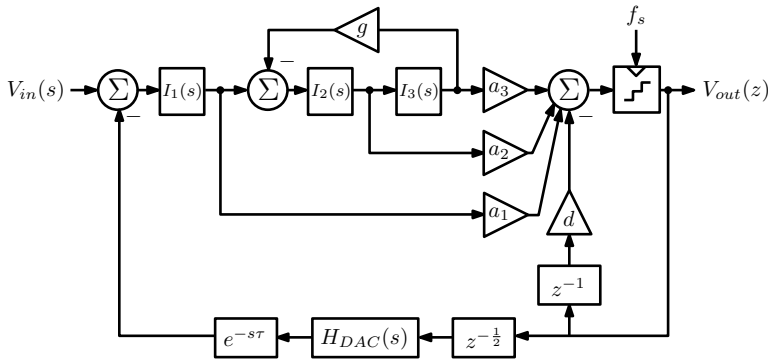

Figure 4.12: Third order FF modulator topology with extra direct feedback path.

Table 4.2: Optimal parameters for the third order design example with direct feedback path using the Nyquist criterion based $\mathcal{R}_{min}$ optimization.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
2.122	0.503	0.43	0.113	1.1	0.78	0.61	81 dB	72.7 dB

We choose the optimization with a nominal $\text{SQNR}_{\text{peak}}$ of 81 dB as final solution. This optimization still leads to modulators with an MSA above 0.5. The histogram for both the MSA and the $\text{SQNR}_{\text{peak}}$ for a family of 108 modulators subjected to variations, is shown in fig. 4.13. Due to the extra design parameter d, which avoids a constrained design, we can see that the robustness of the nominal modulator is already higher than the first example. It is clear that better performance can be achieved. A minimum SQNR of 72.7 dB can be found. This is a significant increase compared to the minimum peak SQNR of 57.4 dB without the extra feedback path. As such, it is worthwhile installing this extra direct feedback path. In contrast to an increase in modulator order to boost the performance, where an extra integrator coefficient is introduced, the feedback path does not include an extra inaccuracy in the system. The parameter is only subjective to mismatch, which we identified as a negligible effect for the loopfilter. This

will lead to a better controllability of the modulator, in the context of the parasitic effects experienced by CT $\Sigma\Delta$ modulators.

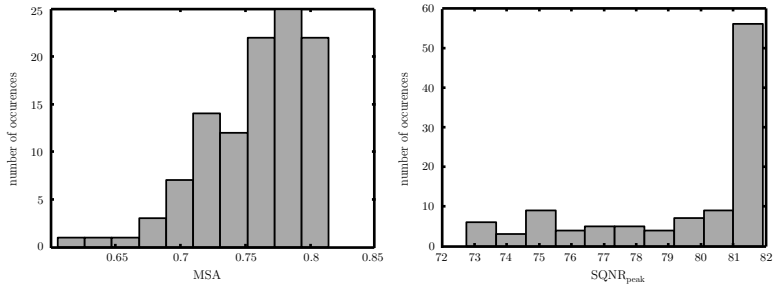

Figure 4.13: Histograms for the nominal modulator with 81 dB performance subjected to parameter variations (left) histogram for the maximum stable amplitude and (right) histogram for the peak SQNR.

Fig. 4.14 shows the effect of the parameter variations on the nominal NTF. Here we can also clearly see the impact of the extra design parameter when comparing to fig. 4.9. The NTF suppression in the signal band is much better than without the direct feedback path. The out-of-band gain of approximately 20 dB is comparable to the first example. As the MSA is mainly determined by this out-of-band behaviour, these values are quite similar between table 4.1 and table 4.2.

Again, extensive time-domain simulations were carried out to obtain the $\text{SQNR}_{\text{peak}}$ for a significant number of perturbated systems. Fig. 4.15 shows the result for the specific modulator which attains the lowest peak SQNR. The variations for this modulator are $\delta_{IC} = -20\,\%$; $\delta_{\tau} = -50\,\%$ and $\delta_{\tau_p} = +20\,\%$. This modulator variation gives rise to an MSA of 0.77. The left hand figure shows the output spectrum of the modulator when an input amplitude equal to the MSA is applied. The resulting SQNR from the simulation is 73.1 dB, which is even slightly better than the design strategy prediction of 72.7 dB. On the right hand side, a dynamic range plot for the specific modulator is displayed.

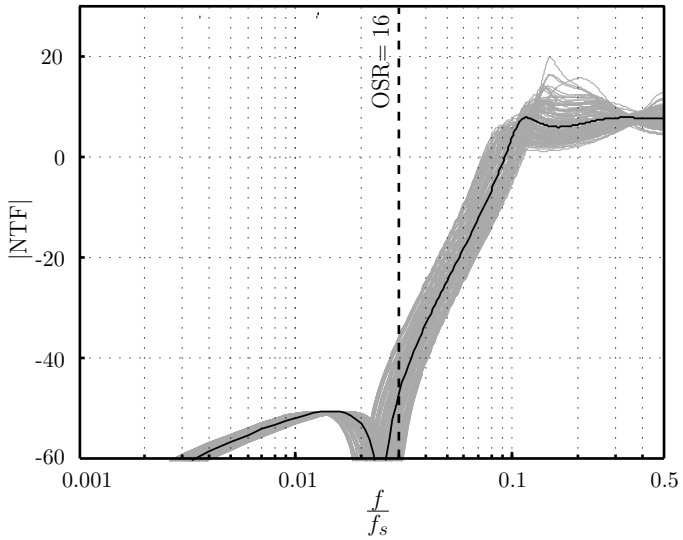

Figure 4.14: Third order design example with direct feedback path NTFs due to parameter variations. The nominal modulator is plotted in black.

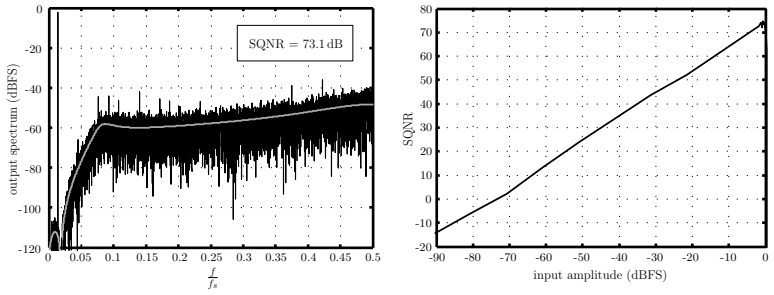

Figure 4.15: Time-domain simulation results for the third order modulator with direct feedback path with $\delta_{IC} = -20\,\%$; $\delta_{\tau} = -50\,\%$ and $\delta_{\tau_p} = +20\,\%$: (left) the output spectrum together with the system model prediction and (right) the dynamic range of this specific modulator.

Chapter 5

The $\mathcal{S}$-figure

5.1 Introduction

In the previous chapter a first design strategy was introduced based on the Nyquist criterion. This strategy allows to design CT $\Sigma\Delta$ modulators, robust to any kind of parameter variations. Furthermore, it can also deal with constrained modulators, which lack the freedom of implementing any NTF possible. The robustness is only optimized for the nominal modulator (without any parameter variations). This means that the resulting optimal design has to be subjected to the variations experienced by the modulator afterwards. In most cases however, the variations can be well defined a-priori. For example, in the previous chapter we have installed a maximum relative variation for the integrator coefficients, the parasitic poles of the integrators and the feedback DAC delay. It should be clear that by utilizing this information, a more targeted modulator design could be achieved.

In this chapter a new design strategy is introduced which does take into account the a-priori knowledge of the variation spread. We will introduce a new figure of merit, the $\mathcal{S}$-figure [4]. It expresses the relative degree in which a specific modulator is able to meet all the performance requirements, even in the presence of predefined parameter variations. This way we can optimize the designed modulator to achieve a guaranteed performance over the whole parameter variation range.

5.2 Design Framework

The design framework that we will use for this new design strategy is very similar to the one from the previous chapter. The main difference lies in the fact that the parameter variation spread is a key part of the framework. It consists of three elements: a nominal system model, normalized variations on some of the system parameters and finally the performance requirements. These three elements are combined into the $\mathcal{S}$-figure.

5.2.1 Nominal System Definition

As a test vehicle, we will reuse the modulator architecture from section 4.2. Similar to the Nyquist criterion based design strategy, the principles explained further on are valid in a broader sense, also for other topological choices.

5.2.2 Normalization of the Parameter Variations

We will focus on the variation of the integrator coefficients to elaborate on the definition for the normalized variations. Formally we can write for the integrator coefficients:

$$-\delta_{IC,max} \leq \delta_{IC} \leq \delta_{IC,max}, \tag{5.1}$$

where $\delta_{IC,max}$ equals 20 %. An important step is the introduction of a normalized version of this variation:

$$\Delta_{IC} = \frac{\delta_{IC}}{\delta_{IC,max}}, \tag{5.2}$$

such that,

$$-1 \leq \Delta_{IC} \leq 1. \tag{5.3}$$

The normalized parameter range will further on be correlated to the value of the $\mathcal{S}$-figure.

5.2.3 Performance Requirements

The performance requirements can initially also be taken over from the previous chapter. Of course, a hard requirement remains stability of the resulting modulator (all its NTF poles should be within the unit circle). Next to that, also the requirement for a maximum stable amplitude larger than $\frac{1}{\sqrt{2}}$ seemed to make sense. It prevents the fact that theoretically stable modulators, which are in fact practically unstable due to quantizer overloading, are retained. A minimum peak SQNR is also required. The main difference in the SQNR requirement is that not only the nominal modulator should achieve this requirement, but also the whole family of modulators which arise from the parameter variations.

Next to this, performance requirements are considered in a broader sense here. In fact, no limitations are posed, and all possible performance requirements can be combined into the $\mathcal{S}$-figure. Later on, we will show examples where clock jitter and the behaviour of the STF are also part of the design. This is again a difference to the Nyquist based design strategy, where only robustness in terms of the Nyquist plot was taken into account.

5.3 The $\mathcal{S}$-figure

In this section we introduce the $\mathcal{S}$-figure, a new figure-of-merit to quantify the robustness of a CT $\Sigma\Delta$ modulator. We will start off by choosing the system parameters from table 4.1. The nominal peak SQNR equals 66 dB and we propose a guaranteed peak SQNR of 60 dB for this design. In this example, we will only subject the modulator to integrator coefficient variations. It is instructive to represent this graphically, by drawing the performance boundaries on the Δ_{IC} axis (fig. 5.1). The valid range for the integrator coefficients is in the Δ_{IC} interval $[-1, 1]$. The performance requirements for stability, maximum stable amplitude and guaranteed peak SQNR, which were posed in the previous chapter, are represented by their boundaries as dashed vertical lines in the figure. The regions in gray, indicate the violation of 1 or more design requirements.

To the left hand side, when the integrator coefficients become smaller, we expect the peak SQNR to drop. In this case, when the relative variation of the integrator coefficients becomes -0.79, the peak SQNR of 60 dB cannot be guaranteed anymore. To the right hand side, the integrator coefficients rise, and the NTF becomes more aggressive. We expect both the stability and the MSA boundary to eventually be broken. The MSA requirement is

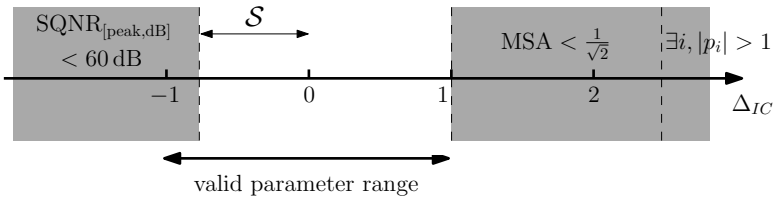

Figure 5.1: Graphical representation of the performance boundaries on the Δ_{IC} axis for a 3rd-order $\Sigma\Delta$ modulator design with only one parameter variation.

only broken outside the valid parameter range, when $\Delta_{IC} = 1.011$. For the NTF poles p_i to cross the unit circle, even higher variations can be tolerated ($\Delta_{IC} = 2.4$). As such, this specific design example will remain stable over integrator coefficient variations of $\pm 20\,\%$. However, it is not possible to meet all the requirements over the entire variation range. We define the $\mathcal{S}$-figure as the absolute value of the minimum normalized variation, that will cause one of the performance boundaries to be crossed. In this case, the $\mathcal{S}$-figure is connected to breaking the SQNR requirement and equals 0.79.

A different parameter selection for the system is given by: $c_1 = 0.8836$, $c_2 = 0.1724$, $c_3 = 0.4723$, $g = 0.4864$. These parameters were obtained by performing an optimization on the $\mathcal{S}$-figure. The nominal NTF reaches a peak SQNR of only 61.6 dB here, which is less than in the previous case. Fig. 5.2 again shows the graphical representation of the performance boundaries. We get a completely different image here. The distance to breaking the stability boundary is not shown in the figure anymore, as this only happens for $\Delta_{IC} = 2.8$. Both the distances to the peak SQNR and MSA boundary are approximately equal. This means that the design parameter selection is quite optimal, as the nominal system is perfectly centered between the two most stringent performance boundaries. The resulting $\mathcal{S}$-figure equals 1.05. The modulator is robust against the full 20 % variation of the integrator coefficients and even has an extra margin for 5 % larger variations.

Generally, striving for an $\mathcal{S}$-figure equal to 1 should always be the goal. Larger $\mathcal{S}$-figures are non-optimal in a sense that the modulator could achieve more stringent performance requirements (e.g. a higher guaranteed peak SQNR). There is still margin to sustain even larger parameter variations. This is the case for the example here. However the extra performance increase here is expected to be negligible as $\mathcal{S}$ is reasonably close to 1. On

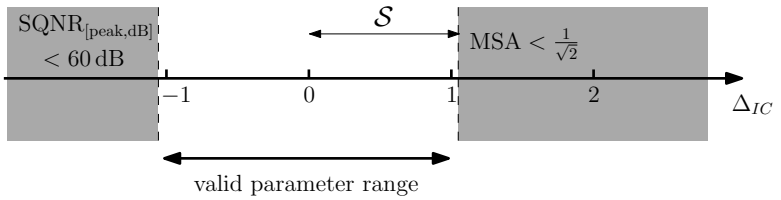

Figure 5.2: Graphical representation of the performance boundaries on the Δ_{IC} axis for a 3rd-order $\Sigma\Delta$ modulator design with only one parameter variation and optimized nominal design parameter selection.

the other hand, an $\mathcal{S}$-figure below 1 is definitely out of the question, as the modulator is not able to meet all requirements over the full variation range.

5.3.1 The $\mathcal{S}$-figure in Multiple Dimensions

So far, only one parameter variation was present, which allowed an easy linear interpretation of the $\mathcal{S}$-figure. Here we will extend the $\mathcal{S}$-figure to multiple dimensions. A similar graphical representation as in the previous section is shown in fig. 5.3 for the case where there are two parameter variations Δ_1 and Δ_2 and three performance requirements. In the origin we have the nominal system, which should meet the performance specifications by definition. The performance boundaries are again indicated by the dashed lines. Consider now the vector $\vec{v_1}$ which makes an angle θ_1 with the Δ_1 axis. If we increase the norm of this vector, we will cross design requirement 2 at the point $(\Delta_{1,\vec{v_1}};\Delta_{2,\vec{v_1}})$. We identify the maximum absolute value of these two coordinates as the "local $\mathcal{S}$-figure" for the direction θ_1, in this case:

$$\mathcal{S}_{local,\theta_1} = \max\left[|\Delta_{1,\vec{v_1}}|;|\Delta_{2,\vec{v_1}}|\right] = |\Delta_{2,\vec{v_1}}|. \tag{5.4}$$

We can repeat this procedure for all other angles. From the previous chapter, we already know that especially the corner points of the variation space are interesting to analyze. For these angles both coordinates change equally when increasing the vector norm in that direction. This is for example the case for the direction θ_2. Design requirement 3 is crossed in this direction and the local $\mathcal{S}$-figure equals:

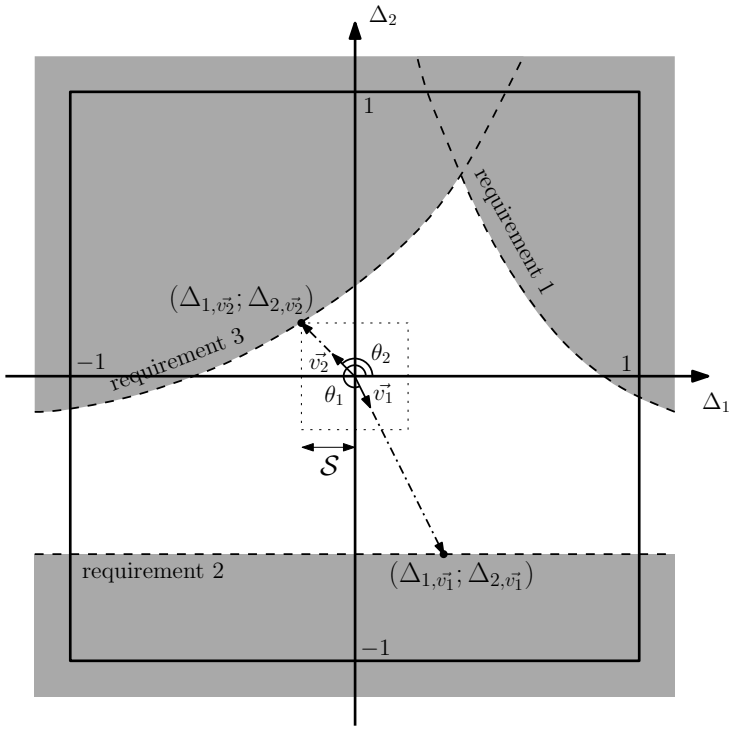

Figure 5.3: Graphical representation of the $\mathcal{S}$-figure in a 2D parameter variation situation.

$$\mathcal{S}_{local,\theta_2} = |\Delta_{1,\vec{v_2}}| = |\Delta_{2,\vec{v_2}}|. \tag{5.5}$$

The $\mathcal{S}$-figure is defined as the minimum of all these "local $\mathcal{S}$-figures":

$$\mathcal{S} = \min_{\forall i} \left[\mathcal{S}_{local,\theta_i}\right]. \tag{5.6}$$

In two dimensions, the $\mathcal{S}$-figure equals half of the side of the largest inner square, which can be drawn around the origin in the variation plane without breaking the performance requirements. If the normalized parameter variations remain smaller than $\mathcal{S}$ the system will definitely satisfy all the specifications. The concept can be extended to 3 or more dimensions where the inner square then becomes a cube or a hypercube.

5.3.2 Calculating the $\mathcal{S}$-figure

The $\mathcal{S}$-figure is one of the variants of the "worst case distance" methodology described in [59–61]. Obviously, determining this $\mathcal{S}$-figure is non-trivial. There are many possible ways to calculate it. Summarizing, there are two important aspects. First, we need an efficient algorithm to calculate the "local $\mathcal{S}$-figure" for a given direction. By investigating only one direction, this has become a scalar problem, which can always be solved as follows: we start from the origin and we gradually increase the vector norm until the corresponding system violates the design requirements. In our implementation we first made a rough sweep, which determines an upper and lower boundary for $\mathcal{S}_{local,\theta_i}$. Then we use a bisectional (binary search) algorithm to obtain a more accurate result. Second, we need to scan all the possible directions, to find the worst-case "local $\mathcal{S}$-figure". Obviously, this procedure would be numerically intensive. We therefore make the assumption that this worst-case point always lies in the direction of one of the corner points of the search space. E.g. in the 2D example of fig. 5.3 the location of the $\mathcal{S}$-figure coincides with the direction of vector $\vec{v_2}$ at an angle of 135 °. Increasing Δ_2 and decreasing Δ_1 both deteriorate requirement specification 3. Empirically, we have found that this assumption is valid for each of the examples considered in this chapter. This extremely simplifies the problem and provides a fast and effective way of determining the robustness of a CT $\Sigma\Delta$ modulator. In fact, this is only possible by choosing the square variant from [61] (using the ℓ_∞ norm). This way, we really consider the worst case parameter variation combinations, without making any assumptions about the statistics between these variations. For our 2D example it means that we only have to execute the algorithm for finding the "local $\mathcal{S}$-figure" 4 times. The resulting $\mathcal{S}$ is selected as the minimum of these 4 values.

5.4 Design Strategy

From the discussion above, it is clear that this $\mathcal{S}$-figure is an unambiguous figure of merit to assess the robustness of a CT $\Sigma\Delta$ modulator against foreseeable imperfections, and hence it can be used as an optimization target. Finding the most robust modulator now boils down to maximization of the $\mathcal{S}$-figure in function of the design parameters. We can reuse most of the algorithm described in the previous chapter. It was slightly adapted for this optimization, which is displayed in fig. 5.4. Again, we use the genetic optimization algorithm *Differential Evolution* [58].

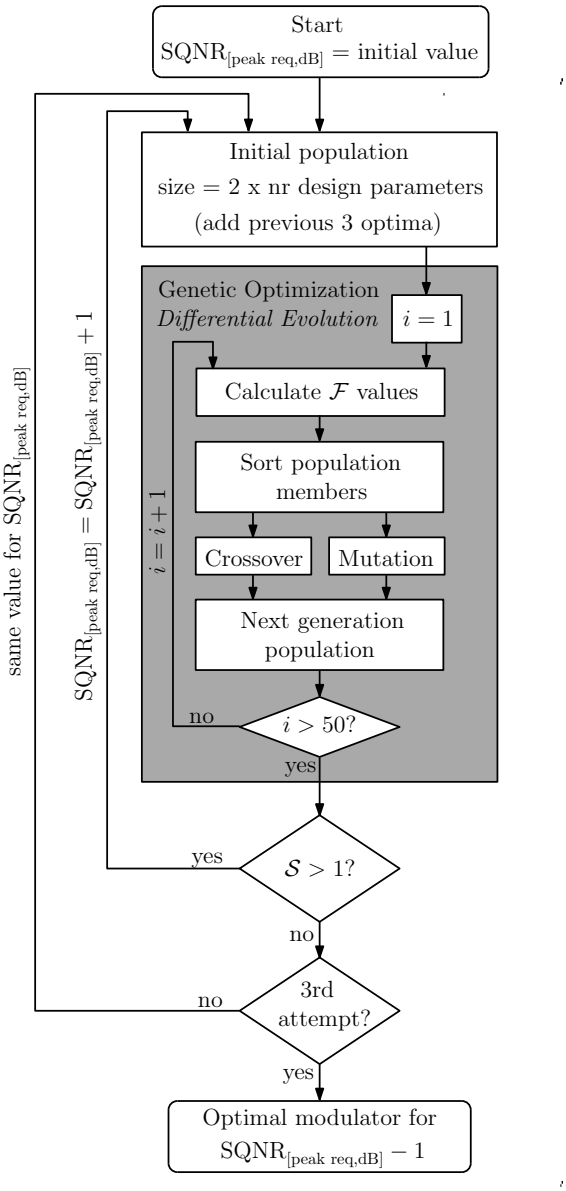

Figure 5.4: Flowchart describing the design strategy based on the $\mathcal{S}$-figure.

For now we will only consider the three requirements that we have claimed so far in this dissertation. The resulting modulator should be stable, have a MSA larger than $\frac{1}{\sqrt{2}}$ and have a peak SQNR requirement. Later on, we will see in the design examples how to incorporate other requirements in the design strategy using the $\mathcal{S}$-figure.

The global iteration loop, where we increase the requested peak SQNR by 1 dB after each optimization, is still present. The global objective is to end up with the modulator design which has an $\mathcal{S}$-figure as close as possible to, but larger than 1. The fitness value $\mathcal{F}$ for each population member is defined as:

$$\mathcal{F} = \begin{cases} +\infty & \text{unstable or MSA} < \frac{1}{\sqrt{2}}, \\ \frac{\text{SQNR}_{[\text{peak req,dB}]} - \text{SQNR}_{[\text{peak,dB}]}}{\text{SQNR}_{[\text{peak req,dB}]}} & \frac{\text{SQNR}_{[\text{peak,dB}]}}{\text{SQNR}_{[\text{peak req,dB}]}} < 1, \\ -\mathcal{S} & \text{valid solution.} \end{cases} \tag{5.7}$$

Again the dynamic criterion for the peak SQNR is contained within the fitness value. For valid solutions, maximizing the $\mathcal{S}$-figure is now the goal. It is important to notice that the validity of the solutions is not only checked for the nominal system, but for all the corner points where the $\mathcal{S}$-figure is evaluated. As such, all performance requirements are guaranteed over the whole parameter variation space.

5.5 Design Examples

In this section we will provide the results of the $\mathcal{S}$-figure design strategy, applied to several examples of different modulator architectures. We will determine the optimal parameters for only third order CT $\Sigma\Delta$ modulators. As a reference, the optimal design parameters for both second and third order modulators are bundled in appendix A. For all design examples we fix the OSR at 16, the number of quantizer bits at 3 and we introduce parasitic poles at f_s in the integrator transfer functions, according to equation (3.15). Besides the variation of the integrator coefficients, also the normalized variations for the feedback DAC delay and the parasitic pole location are introduced (similar to the previous chapter):

$$\Delta_\tau = \frac{\delta_\tau}{\delta_{\tau,max}} \tag{5.8}$$

$$\Delta_{\tau_p} = \frac{\delta_{\tau_p}}{\delta_{\tau_p,max}}, \tag{5.9}$$

where $\delta_{\tau,max}$ equals 50 % and $\delta_{\tau_p,max}$ equals 20 % just like the integrator coefficient variation.

5.5.1 Third Order Modulator in Feedforward Topology

In this design example we repeat the optimization that we also performed in section 4.5.1, but now using the design strategy based on the $\mathcal{S}$-figure. The modulator is mapped on the architecture of fig. 4.1. The usual performance requirements are installed: stability and a guaranteed maximum stable amplitude of a least $\frac{1}{\sqrt{2}}$. The optimization will increase the SQNR for as long as the $\mathcal{S}$-figure remains just above 1. A guaranteed peak SQNR performance of 59 dB is found. The resulting optimal design parameters are displayed in table 5.1.

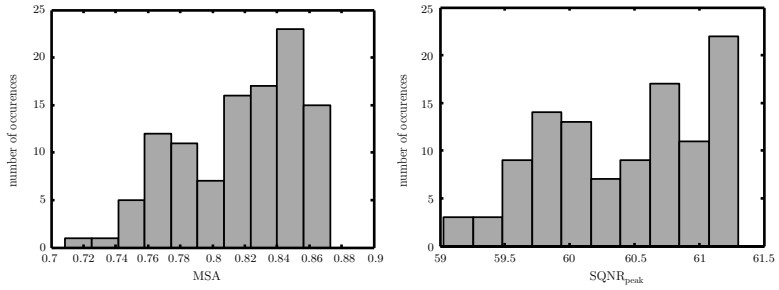

Figure 5.5: Histograms for the modulator with 59 dB guaranteed performance subjected to parameter variations (left) histogram for the maximum stable amplitude and (right) histogram for the peak SQNR.

The histogram for both the MSA and the $\text{SQNR}_{\text{peak}}$ for a family of 108 modulators subjected to variations, is shown in fig. 5.5. We can indeed

Table 5.1: Optimal parameters for the third order design example using the $\mathcal{S}$-figure optimization.

c_1	c_2	c_3	g	MSA		$\text{SQNR}_{\text{peak}}$	
				nom	min	nom	min
0.828	0.181	0.402	0.536	0.82	0.71	60.7 dB	59 dB

verify that all modulators attain a guaranteed performance of at least 59 dB. The MSA is also larger than $\frac{1}{\sqrt{2}}$ in all cases.

Fig. 5.6 shows the effect of the parameter variations on the NTF. We can see that the nominal NTF is quite similar to the one from fig. 4.9. Subjected to variations however, the out-of-band properties are more beneficial here. Also, the zero spreading coefficient is at a higher frequency. This results in a variation for the SQNR of only a few dB.

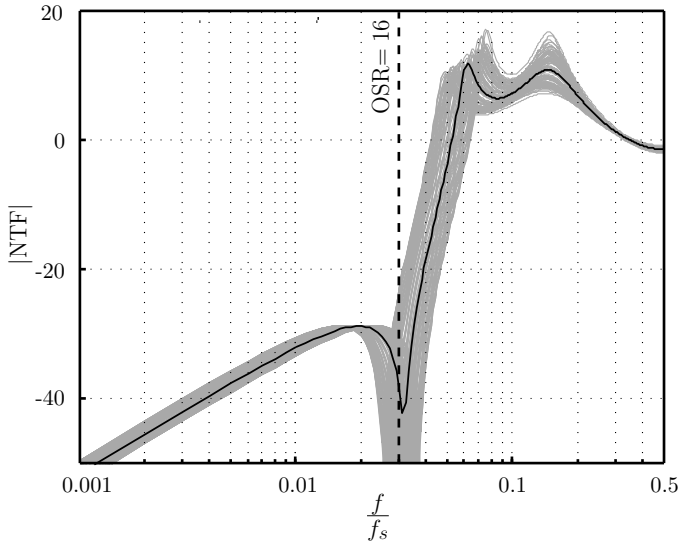

Figure 5.6: Third order design example NTFs due to parameter variations. The nominal modulator is plotted in black.

Extensive time-domain simulations were carried out to obtain the $\text{SQNR}_{\text{peak}}$ for a significant number of perturbated systems. Fig. 5.7 shows the result

for the specific modulator which attains the minimum peak SQNR of 59 dB. The variations for this modulator are $\delta_{IC} = +20\,\%$; $\delta_{\tau} = +50\,\%$ and $\delta_{\tau_p} = +20\,\%$. These variations gives rise to an MSA of 0.71. The left hand figure shows the output spectrum of the modulator, when an input amplitude equal to the MSA is applied. The black curve shows the simulated output spectrum while the gray curve indicates the design strategy prediction. The resulting SQNR from the simulation is 58.97 dB, which is in good agreement with the design strategy prediction. On the right hand side, a dynamic range plot for the modulator is displayed.

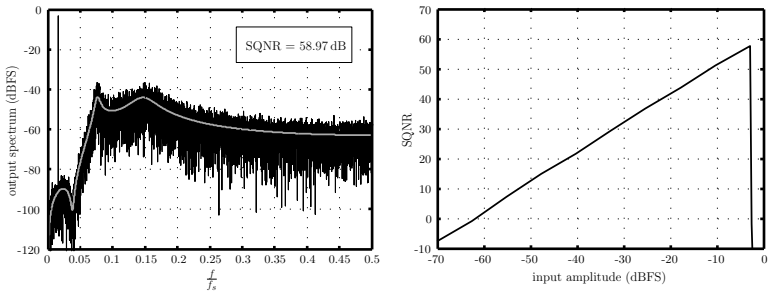

Figure 5.7: Time-domain simulation results for the third order modulator with $\delta_{IC} = +20\,\%$; $\delta_{\tau} = +50\,\%$ and $\delta_{\tau_p} = +20\,\%$: (left) the output spectrum together with the system model prediction and (right) the dynamic range of this specific modulator.

5.5.2 Third Order Modulator in Feedforward Topology with Direct Feedback Path

Similar to the previous chapter, we extend the system with the direct feedback path to increase the performance. The modulator is now mapped on the architecture of fig. 4.12. The resulting optimal design parameters using the $\mathcal{S}$-figure design strategy are displayed in table 5.2.

Fig. 5.8 shows the effect of the parameter variations on the NTF. Again the nominal modulator NTF is quite similar to the one from fig. 4.14. The main difference lies again in the out-of-band behaviour due to parameter variations, which is much lower here. Again, the zero spreading coefficient is optimized in such a way that the SQNR variation is limited to only a few dB.

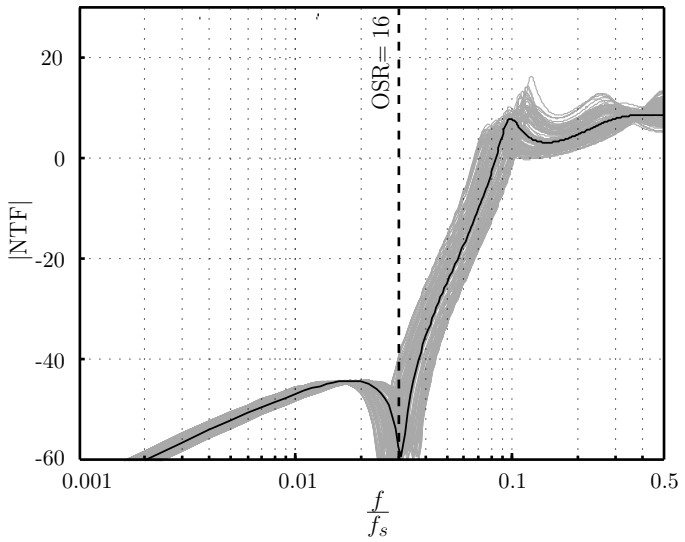

Figure 5.8: Third order design example with direct feedback path NTFs due to parameter variations. The nominal modulator is plotted in black.

Table 5.2: Optimal parameters for the third order design example with direct feedback path using the $\mathcal{S}$-figure optimization.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
2.114	0.414	0.47	0.194	1.132	0.78	0.71	76 dB	74.1 dB

Fig. 5.9 shows the time-domain simulation result for the specific modulator which attains the minimum peak SQNR of 74.1 dB. The variations for this modulator are $\delta_{IC} = -20\,\%$; $\delta_\tau = -50\,\%$ and $\delta_{\tau_p} = -20\,\%$. This gives rise to an MSA of 0.74. The left hand figure shows the output spectrum of the modulator when an input amplitude equal to the MSA is applied. The black curve shows the simulated output spectrum while the gray curve indicates the design strategy prediction. The resulting SQNR from the simulation is 73.6 dB, which is in good agreement with the design strategy prediction. On the right hand side, a dynamic range plot for the specific modulator is

displayed.

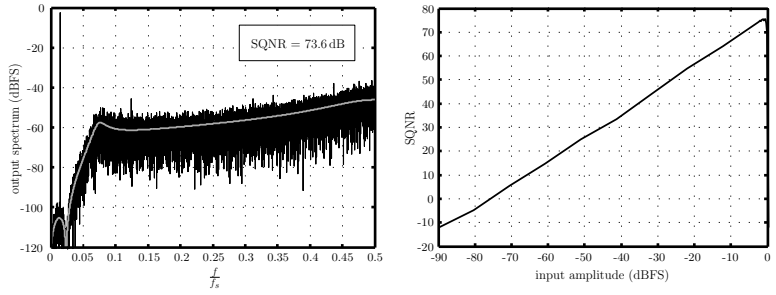

Figure 5.9: Time-domain simulation results for the third order modulator with direct feedback path with $\delta_{IC} = -20\,\%$; $\delta_{\tau} = -50\,\%$ and $\delta_{\tau_p} = -20\,\%$: (left) the output spectrum together with the system model prediction and (right) the dynamic range of this specific modulator.

5.5.3 Third Order FF Modulator with Direct Feedback Path and Coefficient Trimming

In chapter 3, we saw that a general way to tackle the large integrator coefficient variations is to introduce trimmable devices on chip [26, 33]. We propose a new variation spread of 5 % for the integrator coefficients, which should be easily achievable with on-chip trim circuitry:

$$-0.05 \leq \delta_{IC} \leq 0.05. \tag{5.10}$$

Table 5.3: Optimal parameters for the third order design example with direct feedback path and coefficient trimming using the $\mathcal{S}$-figure optimization.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
2.491	0.48	0.56	0.102	1.19	0.75	0.71	83.3 dB	82.2 dB

The same optimization as for the previous case was performed and the resulting optimal modulator parameters are shown in table 5.3. It is clear that the impact of trimming (even with this modest accuracy) is very large. The guaranteed peak SQNR has increased to 82 dB. This can also be seen in fig. 5.10, where the effect of the parameter variations on the NTF is shown.

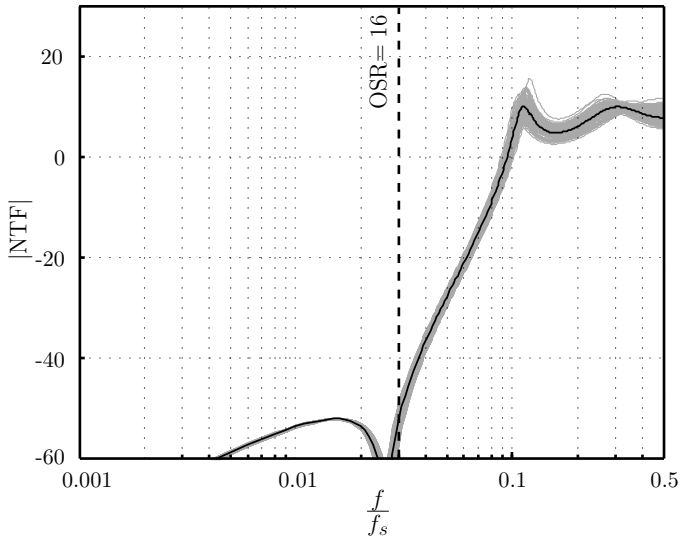

Figure 5.10: Third order design example with direct feedback path and integrator coefficient trimming: NTFs due to parameter variations. The nominal modulator is plotted in black.

5.5.4 Adding Robustness to Clock Jitter

The design strategy using the $\mathcal{S}$-figure can easily be extended to also take into account the effect of clock jitter. For this, we just have to modify the calculation of the peak SQNR, to include the effect of in-band jitter noise according to equation (3.7). Suppose now that we want to design a modulator that is tolerant to a very high level of wideband clock jitter with an effective value $\sigma_{\Delta T_s}$ up to 1% of the clock period T_s. We keep the trimming condition of the previous example. The optimal modulator parameters are summarized in table 5.4.

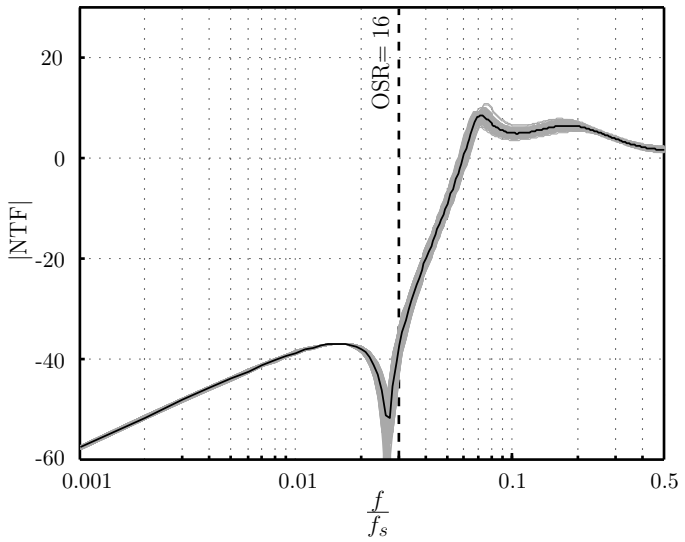

Figure 5.11: Third order design example with direct feedback path and integrator coefficient trimming: NTFs due to parameter variations. This modulator is robust against wideband clock jitter. The nominal modulator is plotted in black.

Table 5.4: Optimal parameters for the third order design example with direct feedback path and coefficient trimming using the $\mathcal{S}$-figure optimization, which is robust against wideband clock jitter.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
1.074	0.275	0.351	0.29	0.424	0.85	0.83	62 dB	61.7 dB

It is clear that a lot of performance is lost compared to the case without wideband jitter. The guaranteed peak SQNR merely reaches a value of 61.7 dB anymore. The resulting NTFs due to the parameter variations are plotted in fig. 5.11. A low out-of-band gain is maintained over all variations (particularly near $\frac{f_s}{2}$). This is consistent with [49], where it was shown that this is indeed a requirement for low clock jitter sensitivity.

5.5.5 Controlling the STF

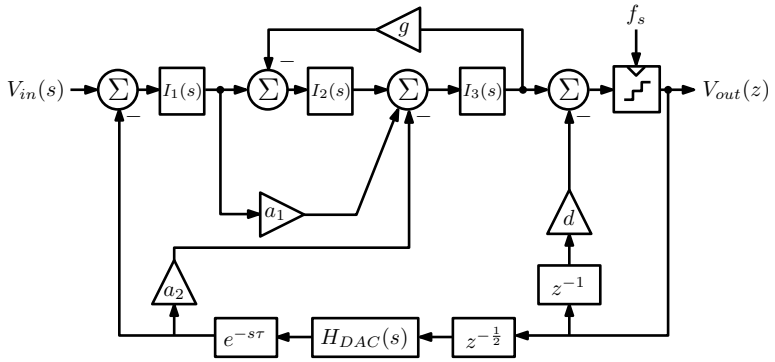

Figure 5.12: Third-order CT ΣΔ modulator architecture with the loopfilter in a hybrid feedforward/feedback topology.

The previous examples all used the FF topology, which is more sensitive to out-of-band peaking of the STF. The control of the peaking behaviour to an acceptable level is important, as it allows relaxation of the ADC pre-filter. In this example we propose the modulator topology of fig. 5.12, which is also used in [33]. This hybrid feedforward/feedback topology compromises a tradeoff between second-order anti-aliasing behaviour and reduced out-of-band peaking by introducing an extra feedback path. Again, we choose the FF/FB coefficients equal to 1 and thus perform a loopfilter optimization. The parameter variations assume 5 % variation for the integrator coefficients due to trimming. The performance requirements for stability, MSA and SQNR are extended with an extra specification to limit the out-of-band STF peak to 2 dB:

$$\max_f |STF(j2\pi f)| < 2\,\text{dB}. \tag{5.11}$$

For comparison, the previous 3 examples gave a worst-case STF out-of-band peak of 18.3, 22.6, 22.4 and 15.1 dB respectively. The resulting optimal modulator parameters for this optimization are given in table 5.5. Clearly, controlling the STF has to be paid for with a performance penalty. The guaranteed peak SQNR was found to be 67 dB.

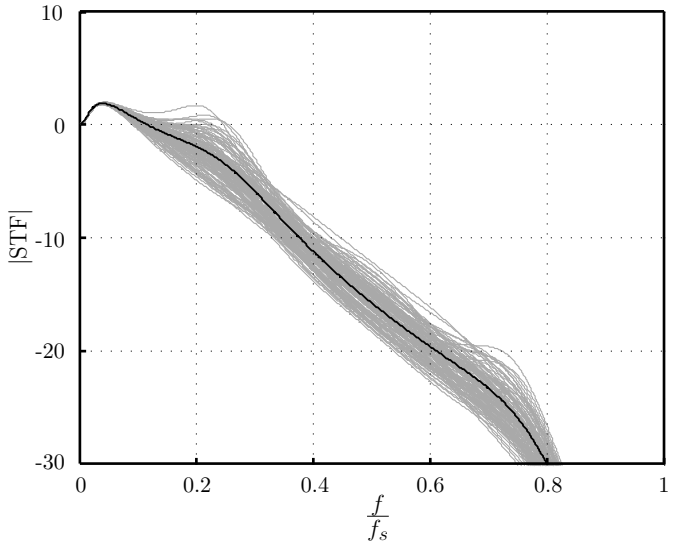

Figure 5.13: STFs with parameter variation influence for the optimal hybrid 3rd-order with controlled STF behaviour.

Table 5.5: Optimal parameters for the third order design example with direct feedback path and coefficient trimming using the $\mathcal{S}$-figure optimization. This modulator has an STF peaking below 2 dB.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
0.373	0.113	2.075	0.098	1.13	0.78	0.75	68.3 dB	67 dB

Fig. 5.13 shows the resulting STFs under influence of parameter variations. The STF has unity gain in the signal band. For higher frequencies the anti-aliasing performance has a second order profile dropping at 40 dB per decade. The out-of-band peaking is indeed limited to 2 dB as required. This is also confirmed in a time-domain simulation. For the worst-case STF peaking modulator ($\delta_{IC} = +20\,\%$; $\delta_{\tau} = -50\,\%$ and $\delta_{\tau_p} = +20\,\%$), a simulation is performed with a multitone signal over the whole Nyquist band to identify the STF. This is shown in fig. 5.14. The gray curve indicates the STF predicted by the design strategy. We can see good correlation between

the single-tone peaks and the theoretical envelope.

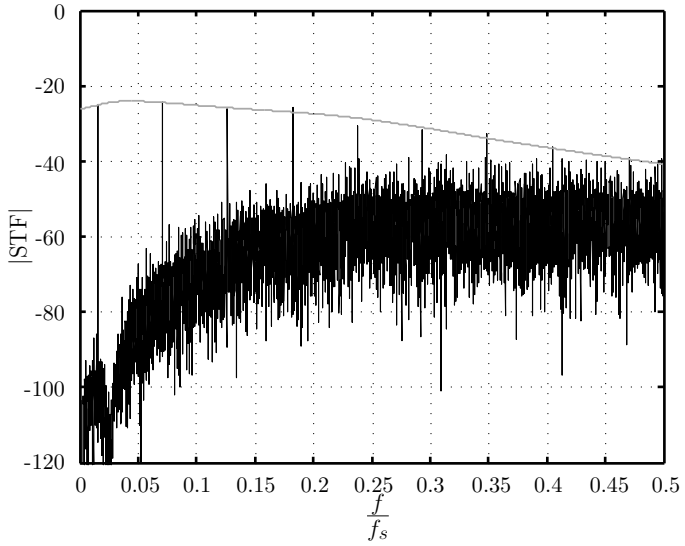

Figure 5.14: Time-domain simulation results for STF of the optimal hybrid 3rd-order ($\delta_{IC} = +20\,\%$; $\delta_{\tau} = -50\,\%$ and $\delta_{\tau_p} = +20\,\%$). The black curve shows the simulation multitone output. The gray curve is the system model prediction.

5.6 Comparison to Robust Design based on the Nyquist Criterion

If we compare the results of the $\mathcal{S}$-figure design strategy with the corresponding results from the previous chapter, we can see great resemblance in the guaranteed values for both the MSA and the peak SQNR. Indeed, comparing the guaranteed MSA and peak SQNR of table 4.1 with table 5.1, shows that the results from the Nyquist based design strategy are only slightly lower than when using the $\mathcal{S}$-figure. The same accounts when comparing table 4.2 with table 5.2. On one hand this is a good sign, as it indicates that both design strategies lead to sensible results. On the other hand we can also see from the tables that the $\mathcal{S}$-figure design strategy not

only performs systematically better, but that mainly the variation on the results is more confined. The peak SQNR variation is only a few dB here, while for the Nyquist-based design strategy variations of nearly 10 dB can be identified. Due to a better boundary condition setting, it is clear that the optimization for the $\mathcal{S}$-figure can find a superior solution. The Nyquist criterion based design strategy can be seen as a more conservative approach, when boundary conditions cannot be narrowly defined. On top of that, the Nyquist based design strategy focuses on optimizing only the stability robustness, defined in the Nyquist plot by the $\mathcal{R}_{min}$ criterion. The $\mathcal{S}$-figure design strategy can be used for any kind of performance criterion, which can be included in the framework.

Part III

Novel Architectures for Continuous-Time $\Sigma\Delta$ Modulators

Chapter 6

Time-Encoding

6.1 Introduction

In the previous chapters, high bandwidth, high resolution continuous-time $\Sigma\Delta$ converters were obtained by combining a low oversampling ratio with multibit quantization. In today's deep sub-micron CMOS technology with reduced voltage headroom, two components in the conventional CT $\Sigma\Delta$ modulator tend to become more difficult to design. The first difficulty is formed by the multibit DAC in the feedback path. Its linearity must be equal to the full modulator's resolution. Therefore, calibration or dynamic element matching techniques are required [41, 43, 44]. A second difficulty arises in the multibit flash quantizer, where the number of comparators rises exponentially with the number of quantizer bits. In deep sub-micron technologies the decrease in supply voltage tends to be more aggressive than the increase of matching properties of MOS devices. As such, the area of the devices at the input stage of the comparators has to be increased to suffice the input-referred offset specification of the quantizer unit. This generally leads to non-minimum length devices and thus a limitation of the operation speed due to the parasitic input capacitance. A solution for this problem can be the introduction of offset calibration techniques [62, 63]. In [64], an offset averaging technique is introduced by spreading the offset of the individual comparators over several decision levels. It is shown that this lowers the global input-referred offset. Besides the flash topology, also other topologies have been presented as quantizer for a $\Sigma\Delta$ modulator such

as the use of 2-step quantization [65, 66], the use of a tracking ADC [67, 68] or a low-resolution successive approximation (SAR) ADC [69].

In this chapter, time-encoding is employed as a promising technique to avoid the main issues from multibit quantization, while preserving multibit performance. Essentially, the multibit quantization is replaced by some kind of quantization in time. As such, this solution is considered to be very well suited for today's ultra deep sub-micron technology which should be able to provide ample time resolution due to their multi-GHz switching ability. In the first section we focus on VCO-based quantization. Next, pulsewidth modulation (PWM) is introduced as a means of time-encoding in the feedback DAC. Time-encoding can also be combined in both the quantizer and the feedback DAC, for example in self-oscillating $\Sigma\Delta$ modulators. This is the subject of the rest of the chapter. Special attention is given to synchronous self-oscillating modulators based on a delay element in the feedback path. The chapter ends with a conspectus on the jitter performance of self-oscillating $\Sigma\Delta$ modulators.

6.2 VCO-Based Quantization

6.2.1 Principle of Operation

The first ideas for using a voltage-controlled oscillator (VCO) as a time-encoding quantizer were proposed in [70–72]. An interesting publication is [73], where these concepts were first used in a real wide-bandwidth CT $\Sigma\Delta$ modulator prototype. Based on this publication, the operation principle of the VCO-based quantizer is illustrated in fig. 6.1. The VCO-based quantizer consists of the actual VCO core and a digital counter. The input voltage modulates the VCO frequency. A digital counter is present which counts the number of positive VCO crossings within each sample period interval. To provide a quantized value of the input, the counter is reset at the beginning of each clock period. In the figure, the input value is displayed as a signal which has been already sampled. In reality this signal will vary continuously, but only at a very slow pace due to the oversampled nature of a $\Sigma\Delta$ modulator. The VCO is usually implemented with a ring-oscillator. Hence, this type of quantizer is well suited for integration in ultra deep sub-micron CMOS technologies, as it only uses components which are digital in nature and have increased time-resolution with each new technology node.

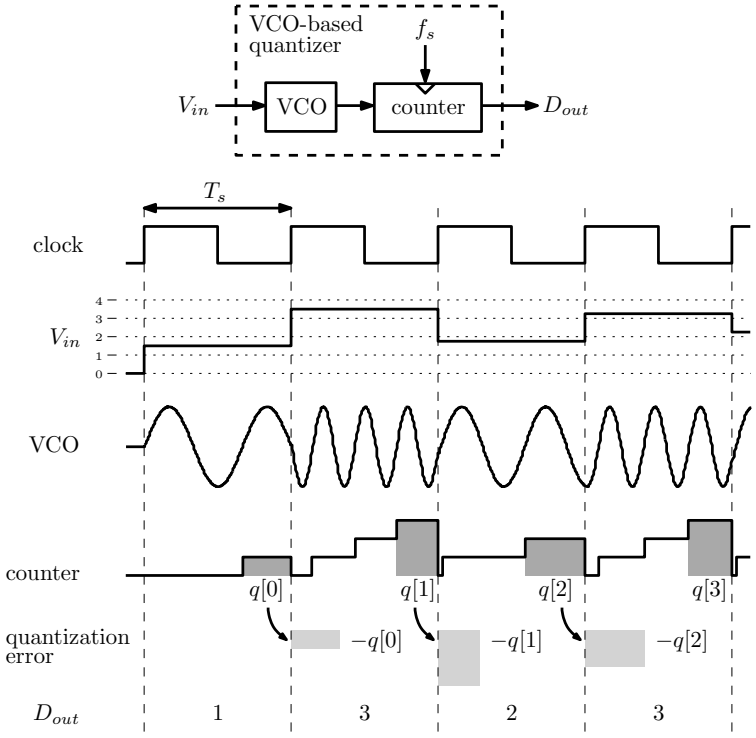

Figure 6.1: Principle of operation of a VCO-based quantizer based on [73].

An important property of the VCO-based quantizer is the implicit first-order quantization noise shaping. This is due to the fact that the actual quantization occurs in the phase domain. The input-dependent phase state of the VCO can be written as:

$$\phi_{VCO}(t) = \int_{\tau=0}^{\tau=t} 2\pi K_V V_{in}(\tau) \mathrm{d}\tau, \tag{6.1}$$

with K_V the VCO sensitivity parameter in Hz/V. The digital counter reacts to the crossings of this phase signal with multiples of 2π. The phase signal is quantized at the end of each clock period with a quantization error $q[n]$:

$$\hat{\phi}_{VCO}[n] = \int_{\tau=0}^{\tau=nT_s} 2\pi K_V V_{in}(\tau)\mathrm{d}\tau + q[n]. \tag{6.2}$$

Due to the reset operation at the beginning of each clock cycle, the effective output code D_{out} is the discrete-time differentiation of the quantized phase signal:

$$\begin{aligned} D_{out}[n] &= \hat{\phi}_{VCO}[n] - \hat{\phi}_{VCO}[n-1] &(6.3)\\ &= \int_{\tau=(n-1)T_s}^{\tau=nT_s} 2\pi K_V V_{in}(\tau)\mathrm{d}\tau + q[n] - q[n-1]. &(6.4)\end{aligned}$$

This reveals the implicit first-order quantization noise shaping. This important advantage of the VCO-based quantizer can also be seen from fig. 6.1. The quantization error per sample is displayed as the gray rectangle at the end of each sample period. Only the counter is reset at beginning of a new clock period while the internal phase signal of the VCO just continues based on the previous state. The end state of the previous sample is transferred as an inverse initial condition in the current sample. This brings us to the same conclusion. The operation in the frequency domain is illustrated in the block diagram of fig. 6.2.

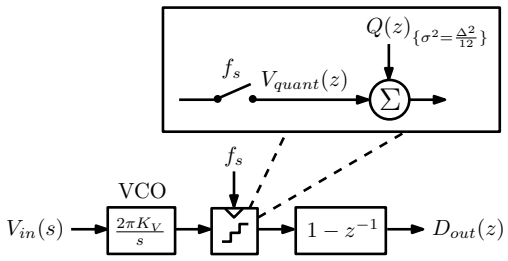

Figure 6.2: Block diagram for the VCO-based quantizer in the frequency domain.

6.2.2 Improved Architecture

The implementation of fig. 6.1 is problematic due to the reset operation of the counter. If one of the VCO phase edges happens to be close to the reset

pulse, information can get lost due to subtle gate delay differences in the digital logic. This would kill the first-order noise shaping behaviour. An improved architecture is proposed in [73, 74] (see fig. 6.3). In this architecture, all the internal states of the ring oscillator are used to make the quantization decision.

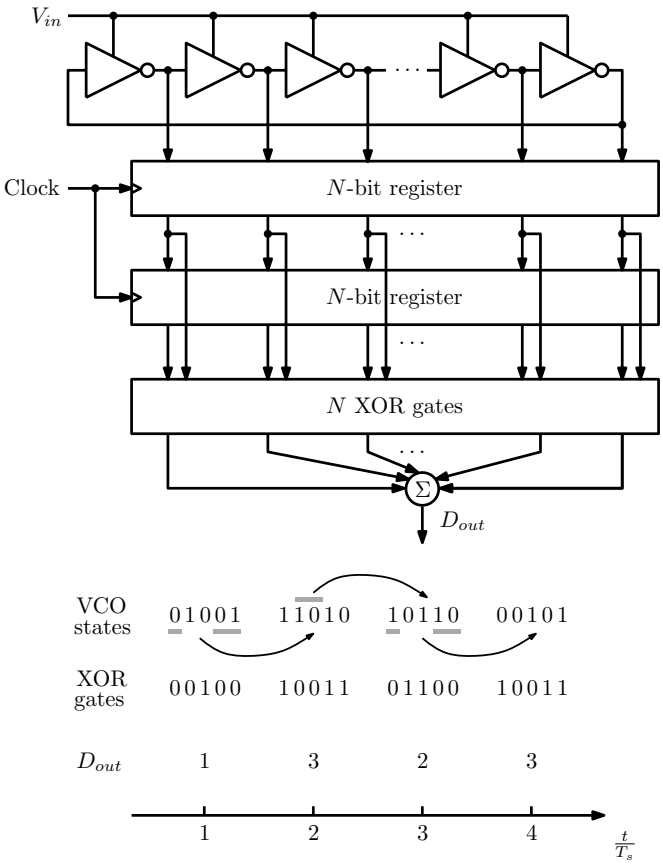

Figure 6.3: VCO-based quantizer with a multiphase ring oscillator.

An example is shown in the figure for a 5-stage ring oscillator. The quantized output value is made up by an XOR operation on two subsequent states of the ring oscillator. This coincides with a digital differentiation on the phase state of the oscillator. A boundary condition in this architecture is that the number of state changes per sample cannot exceed the number of ring

oscillator stages. This leads to the condition that:

$$f_s > 2f_{VCO,max}. \tag{6.5}$$

A beneficial side-effect from this architecture is the circular thermometer encoded quantizer output value. This coincides with the circular pointer of the DWA algorithm [43, 44]. As such, implicit dynamic element matching is present at the output of this type of VCO-based quantizer.

6.2.3 CT $\Sigma\Delta$ modulators with a VCO-based Quantizer

The bottleneck for using a VCO-based quantizer lies in its modest linearity properties. The voltage to frequency conversion in a current-starved ring oscillator will be in the order of 5-6 bit. As such, the VCO-based quantizer is hardly used as a standalone ADC, but instead can be incorporated as the quantizer of a $\Sigma\Delta$ loop (see fig.6.4). In [73] a second order CT loopfilter, of which one of the integrators is implemented with a passive stage, is combined with a 5-bit VCO-based quantizer. In total, a third order noise shaping profile is acquired due to the VCO-based quantizer. The prototype achieves 12-bit linearity in a 20 MHz bandwidth.

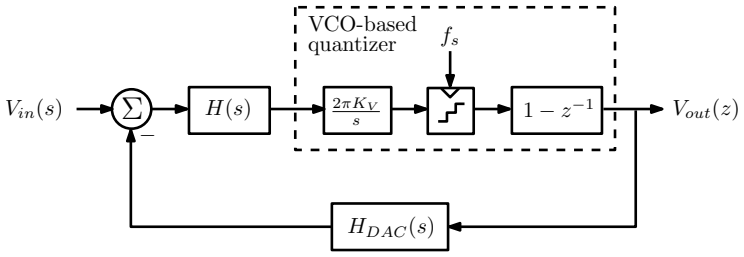

Figure 6.4: CT $\Sigma\Delta$ modulator with a VCO-based quantizer.

In [74], the linearity is improved by installing a first order feedback path around the VCO-based quantizer using the quantized phase signal. This way, the first order differentiation of the quantization noise disappears, but it is exchanged with a suppressed input signal due to the VCO integrator operation. An extra drawback is that also the implicit DEM property of the output codes is removed.

6.3 Pulsewidth Modulation in the Feedback DAC

The multibit feedback DAC signal can be encoded in the time domain by using pulsewidth modulation. The idea is illustrated in fig. 6.5, where a comparison is made with the NRZ and RZ DAC pulses. The clock period is subdivided into the required number of time quantization intervals. A single element DAC is present, of which the quantized activation time determines the feedback value. For the same net charge to be fed back, the single element current must equal the total current of the NRZ DAC or half of the total current of the RZ DAC. The generation of the quantized time intervals usually involves more complex frequency synthesis strategies. Either a higher frequency clock is necessary, either a very clean multiphase clock signal.

In [75], a 3-bit PWM feedback DAC is used in the outer feedback loop of a 5th order continuous-time $\Sigma\Delta$ modulator. For the generation of the different clock phases, an on-chip LC tank VCO is co-integrated. This oscillator includes a complementary injection-locked frequency divider (CILFD) to ensure multi-phase digital signals with low time-domain jitter noise. Jitter sensitivity is identified in this paper as the most severe drawback of PWM-based feedback. This can intuitively be seen from fig. 6.5. The jitter influence of two clock edges is involved in the feedback signal error, which is similar to the case of the RZ pulse. Furthermore, the signal amplitude level always remains equal to the total current of the equivalent NRZ DAC.

Of course the advantage of the PWM-based feedback DAC lies in the increased resolution in the time domain. This way static delay errors due to process and Monte Carlo variations can be better controlled than the matching between the individual current source units from the NRZ DAC. An approximate equation for the linearity improvement of the PWM versus NRZ DAC is proposed [75]:

$$\frac{\mathrm{SNDR}_{\mathrm{NRZ}}}{\mathrm{SNDR}_{\mathrm{PWM}}} = \frac{2}{B}\frac{\sigma^2_{\Delta T_{\%}}}{\sigma^2_{\Delta I_{\%}}}, \tag{6.6}$$

where B is the number of quantizer bits, and $\Delta T_{\%}$ and $\Delta I_{\%}$ represent the relative clock phase deviation and relative unit current source deviation for the PWM and NRZ DAC respectively. The equation appears due to the fact that for the extreme feedback values, the deviation of all B unit current sources is involved for the NRZ DAC while in all feedback cases only 2 clock phase deviations are involved for the PWM DAC. As the relative timing

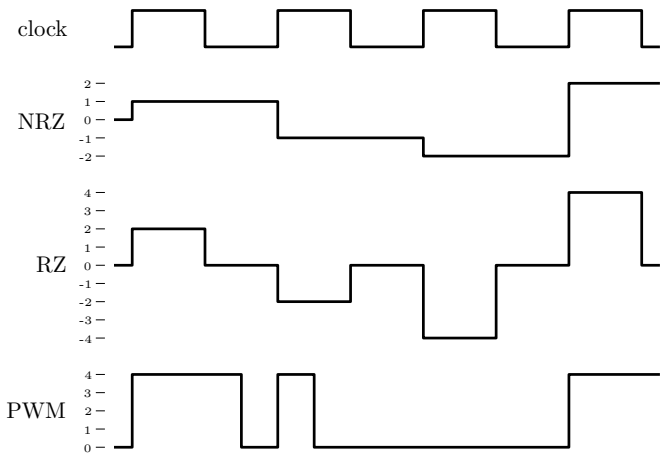

Figure 6.5: Illustration of the PWM multibit feedback DAC as opposed to the more common NRZ and RZ feedback DAC pulses.

variations are smaller than the current source mismatch in deep sub-micron technologies, the PWM DAC outperforms the conventional NRZ DAC.

6.4 Self-Oscillating $\Sigma\Delta$ Modulators

The two previous sections each proposed a solution for avoiding a multibit implementation for either the quantizer or the DAC. In this section both ideas are combined. In contrast to the VCO-based quantizer where the oscillation is clearly limited to the VCO core, here it is extended to the full $\Sigma\Delta$ loop. The CT $\Sigma\Delta$ will be designed in such a way that it operates in a limit cycle mode. The oscillation is sustained by using only a single-bit quantizer (comparator). The low-frequency input will modulate the output oscillation mode in a way similar to PWM encoding.

Originally, limit cycles in $\Sigma\Delta$ were regarded as undesired oscillations in the output signal at high frequencies [76]. They originate from the non-justified assumption of white quantization noise, particularly in low-order $\Sigma\Delta$ modulators with single-bit quantizers [21, 77]. The problem was alleviated in multibit $\Sigma\Delta$ modulators, since the multibit quantizer reduces the correlation of the quantization error with the modulator input signal. In [78], the asynchronous CT $\Sigma\Delta$ modulator is introduced. Here, the limit cycle

is no longer considered as a parasitic effect, but instead it is deliberately introduced in the loop. The basic architecture consists of a feedback configuration of a continuous-time loopfilter and a hysteresis comparator. As it is a non-clocked comparator, the output of the loop remains an analog signal, but which is quantized to only two levels. Therefore the loop is followed by an external sampler. The loop configuration shows great resemblance with a self-oscillating power amplifier (SOPA) [79]. In [80], the sampler is also incorporated into the loop. This gives the extra advantage that the errors from the sampling operation also get shaped with the NTF. The architecture is identical to a conventional single-bit CT ΣΔ modulator, but the loopfilter and comparator hysteresis are designed in such a way that the system deliberately operates in a self-oscillation mode. Next to the use of a hysteresis comparator, adding delay in the feedback path of the modulator can also be used to control the self-oscillation. In the following, we will focus on delay-based self-oscillating ΣΔ modulators.

6.4.1 Delay-Based Self-Oscillating ΣΔ Modulators

Fig. 6.6 shows the basic architecture for the delay-based self-oscillating ΣΔ modulator. Similar to a conventional single-bit modulator, it consists of a continuous loopfilter $H(s)$, a comparator clocked at f_s and a single-bit feedback DAC. To obtain the self-oscillation, we add a digital delay in the modulator feedback path. This way, we obtain a very well controlled self-oscillation at much lower frequency than the sample frequency f_s. This self-oscillation, which is an integer fraction of the sample frequency f_s, will serve as the carrier for the pulsewidth modulation of the output signal.

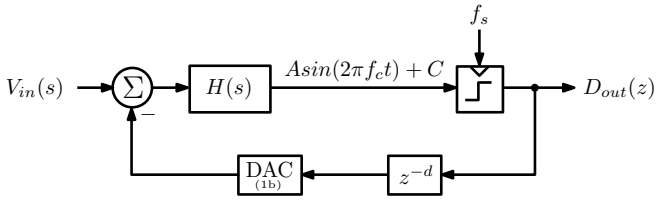

Figure 6.6: Self-oscillating CT ΣΔ modulator with digital delay in the feedback path.

The system shown in fig. 6.6 is non-linear due to the presence of the comparator and therefore hard to analyze. In [80] the describing function theory

is proposed as a way to linearize such systems. The system is described by considering the behaviour for a superposition of different kinds of signals at the comparator input. For each type of signal the comparator is linearized. In our case, the comparator input can contain two types of signals: we will consider a high-frequency contribution ($\propto \sin(2\pi f_c t)$) from the self-oscillation and a low-frequency contribution from the input signal $V_{in}(s)$. It is assumed that the frequency of the input signal is sufficiently smaller, such that it can be approximated as a constant C in the time scope of the self-oscillation.

System Behaviour for the Self-Oscillation Mode

To investigate the self-oscillation mode, we set the input signal $V_{in}(s)$ equal to zero. Since the loop should be designed to sustain a stable self-oscillation mode, the output signal should then be a square wave signal of frequency f_c. This signal is lowpass filtered through the loopfilter $H(s)$. Therefore only the first order harmonic is considered. This way, we have a sine wave with amplitude A and frequency f_c appearing at the input of the quantizer. This is shown in fig. 6.6. To simplify the analysis we will now assume that the sampling frequency of the comparator is infinite. Of course this can not be achieved in practice, but this corresponds to what ultimately could be achieved after technology scaling. The assumption is necessary to apply the describing function theory.

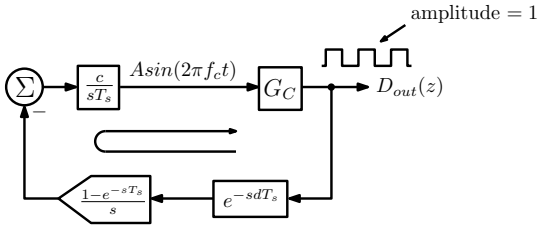

Figure 6.7: Block diagram for the self-oscillation mode: simplified first-order system with infinite sampling frequency.

To obtain a very simple analytic result, we will first assume that the loopfilter is a first-order integrator, later on we will do the analysis properly with the exact loopfilter. Taking into account that we use a NRZ pulse for the feedback DAC, this results in the block-diagram of fig. 6.7. The

Barkhausen stability criterion states that we will have an oscillation where the loop has a 180° phase shift. We immediately obtain, for our simple integrating loopfilter, that the oscillation frequency equals:

$$f_c = \frac{f_s}{4(d+\frac{1}{2})}, \tag{6.7}$$

where the $\frac{1}{2}$ term originates from the delay of the NRZ DAC-pulse (see equation (2.44)). The oscillation frequency is accurately controlled by the digital delay in the loop. For a zero-delay system, which coincides with a conventional delay-less CT ΣΔ modulator, the self oscillation appears at $\frac{f_s}{2}$ as expected.

Moreover, even the amplitude of the oscillation is accurately controlled by the designer. This can be understood by noting that the overall output is a square wave with an amplitude equal to 1 (see fig. 6.7) and a well controlled frequency f_c. The describing function theory [81] provides a linearized quantizer gain which is function of the self-oscillation amplitude A:

$$G_C = \frac{4}{\pi A}. \tag{6.8}$$

The gain originates from the contribution of the fundamental sine wave component in the Fourier series of a square wave of amplitude 1. The Barkhausen amplitude criterion can now be applied for the self-oscillation frequency found in (6.7):

$$\begin{aligned} A &= \frac{4}{\pi}\left|\left(\frac{1-e^{-sT_s}}{s}H(s)\right)\right|_{s=j2\pi f_c} && (6.9)\\ &\approx \frac{4}{\pi}\left|H(j2\pi f_c)\right|. && (6.10) \end{aligned}$$

The approximation can be made because the oscillation frequency is at least a factor of 4 lower than the sampling frequency. For the simplified first-order system from fig. 6.7, the amplitude could be further calculated as:

$$A \approx \frac{4}{\pi}\cdot\frac{c}{2\pi f_c T_s} = \frac{8c}{\pi^2}\left(d+\frac{1}{2}\right). \tag{6.11}$$

Adding delay not only reduces the self-oscillation frequency, but will also increase the self-oscillation amplitude. This can be seen as a general statement as the loopfilter will always have integrator operation, even for more complex filter topologies.

Note that the previous analysis is only an approximation because of two reasons. First, only the fundamental frequency of the self-oscillation is taken into account and second, the effect of sampling is ignored. However, the approximation provides a simple means for a good understanding of the underlying mechanism. Sampling causes the output oscillation frequency to be an even integer fraction of f_s:

$$f_c = \frac{f_s}{M}, \quad \text{with } M \text{ even.} \tag{6.12}$$

Indeed, without any input signal the mean output value should still remain zero. The effect of sampling in the comparator is illustrated in fig. 6.8. The figure shows the effect of sampling on the fundamental tones at both $\frac{f_s}{2}$ and $\frac{f_s}{4}$.

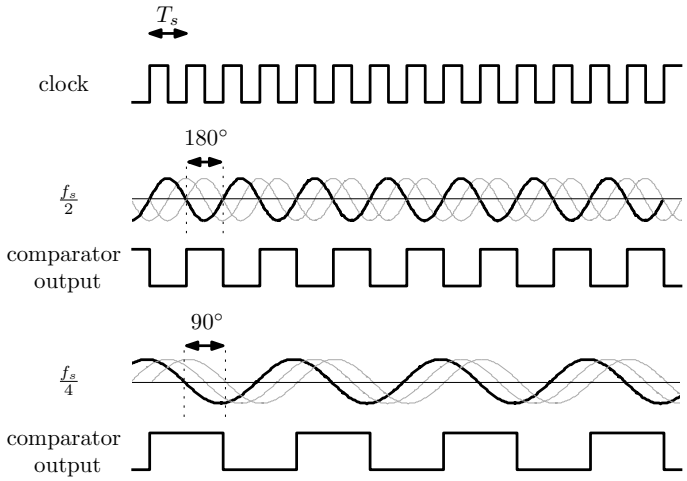

Figure 6.8: Phase uncertainty in a clocked comparator.

For the $\frac{f_s}{2}$ oscillation a phase shift up to 180° gives rise to the same comparator output signal. For the $\frac{f_s}{4}$ oscillation this is a maximum phase shift

of 90°. The effect of sampling can thus be incorporated by modeling it as a phase uncertainty in the loop. The phase shift uncertainty is linked to the self-oscillation subharmonic number. In general, for the phase shift $\Delta\phi$ accounts:

$$\Delta\phi = \frac{360^\circ}{M}, \quad \text{with } M \text{ even.} \tag{6.13}$$

Using this knowledge, a more detailed analysis of self oscillation of the loop can be made by using a graphical interpretation of the Barkhausen criterion [80]. An example with a unit delay in the feedback loop of a second order self-oscillating ΣΔ modulator is shown in fig. 6.9. The Nichols plot representation is used to visualize the amplitude and phase of the loop. The plot is organized in such a way that the crossings with the 180° phase line coincide with the amplitude of the fundamental tone of the self-oscillation at the comparator input. Furthermore, for each even integer fraction of the sample frequency, phase uncertainty is added by extending the phase according to equation (6.13).

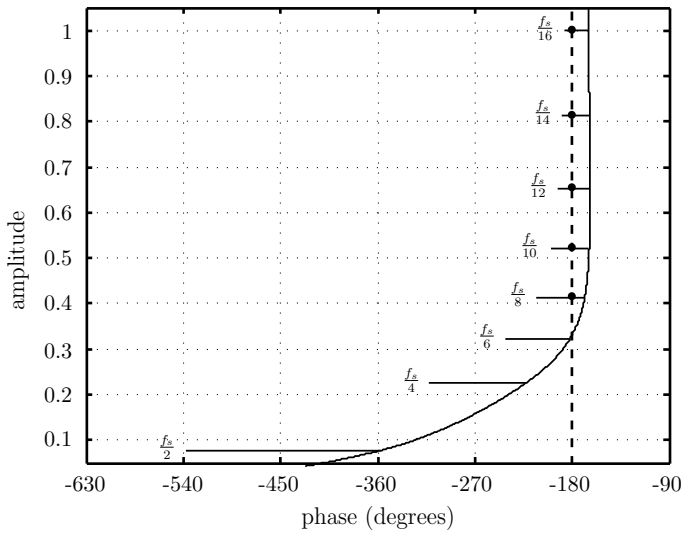

Figure 6.9: Nichols plot of a second order self-oscillating ΣΔ modulator.

Although the approximation from equation (6.7) would predict a self oscillation tone at $\frac{f_s}{6}$, the more accurate second-order filter behaviour and the clocked comparator give rise to oscillations starting from $\frac{f_s}{8}$. Assuming that the comparator reference level coincides with the analog output range of the loopfilter, oscillations with amplitude above 1 are not shown, as they would oversteer the system. It can be seen that multiple oscillation modes are possible. In practice, the system will operate in the mode which complies with the most high-frequent solution. Indeed, for a conventional $\Sigma\Delta$ modulator, the output also oscillates at $\frac{f_s}{2}$ for a zero-input signal.

The existence of the self-oscillation is fundamental for the circuit-level requirements. While in a conventional $\Sigma\Delta$ modulator the integrators require parasitic poles which are beyond the sample frequency f_s, here the loopfilter only has to process signals that are of the order of the self-oscillation frequency (much lower than f_s). As a result of this, we expect that the requirements on the opamp GBWs will remain quite moderate and hence a significant reduction in current consumption can be achieved.

System Response to the Input Signal

To analyze the response to the input signal, we can observe the comparator output. This is shown in fig. 6.10(a). From the figure it is clear that the comparator output signal consists of a pulsewidth modulated version of its input signal. This way, we can consider two components in the comparator output signal: a component at a high frequency (the self-oscillation component) and a component at low frequency (the signal component). Since we are now interested in the response to the input signal, we can associate a best-fit gain G_S for the low-frequency signal component. Again this best-fit gain is provided by the describing function theory [81]:

$$G_S = \frac{2}{\pi A}. \tag{6.14}$$

It is important to notice that this low-frequency gain is dependent on the amplitude of the high-frequency oscillation, as such it can be linked to the evaluation of equation (6.9).

Due to the pulsewidth modulation of the oscillation, spectral tones around the self-oscillation frequency will appear in the output spectrum. Furthermore, from the previous section, we know that sometimes multiple self-oscillation modes are possible. The input signal tends to add to the amplitude of the self oscillation [80]. If the input power is large enough, the self-

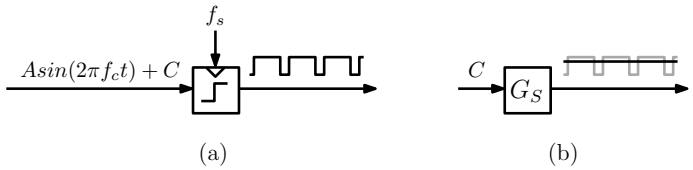

Figure 6.10: Comparator behaviour for the input signal: (a) comparator output in a system with a self-oscillation and (b) its low-frequency approximation.

oscillation could jump to a lower frequency. As such, the input signal bandwidth should be low enough compared to the possible self-oscillations.

To study the low-frequency behaviour of the system we could now just plug the linear model for the comparator in the system model of fig. 6.6. However, we would then obtain a system without quantization noise and hence obtain an infinite resolution for the associated A/D converter. In this system, the quantization noise originates from the discretisation in time of the output waveform. The basic mechanism is elaborated in fig. 6.11 for a ΣΔ modulator with a self-oscillation at $\frac{f_s}{8}$. The figure shows the unsampled comparator output waveform $x(t)$ and its zero-order-held version $y(t)$. Without quantization, $y(t)$ should have the same shape as the input signal $x(t)$. Still there is half a clock cycle delay between $x(t)$ and $y(t)$ which is caused by the delay of the ZOH-pulse. To separate the quantization effect from this delay effect, we introduce the time-shifted signal $y'(t)$. It is clear that $y'(t)$ can only change at a falling clock edge. This causes a quantization error $q(t)$, which consists of a set of consecutive pulses. As is common for quantization noise, the next step is to assume that q is a zero mean white noise sequence. To calculate the power σ_Q^2, we note that each pulse in the $q(t)$ waveform has a magnitude of ± 2 and a duration between $\pm T_s/2$. Moreover, during each period of the self-oscillation, 2 such pulses occur. This way:

$$\sigma_Q^2 = 4\frac{1}{12}\frac{2f_c}{f_s} = \frac{2}{3}\frac{f_c}{f_s}. \tag{6.15}$$

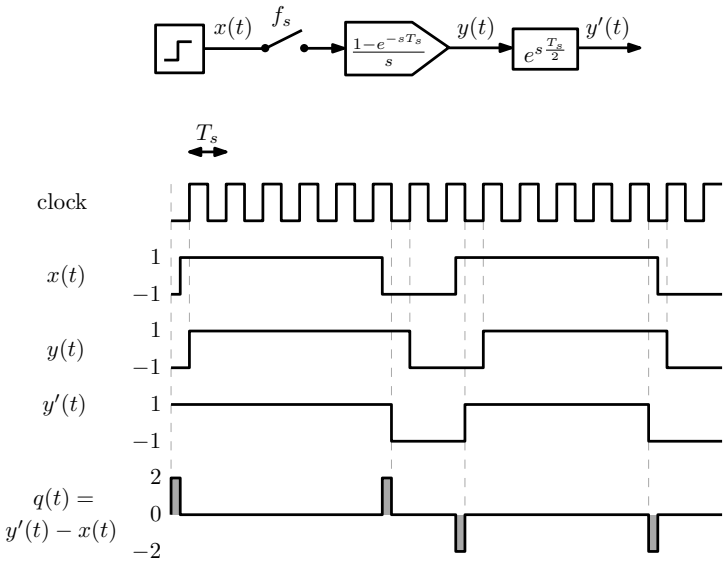

Figure 6.11: Illustration of quantization noise in a time-encoding self-oscillating modulator.

6.4.2 Modeling of a Self-Oscillating ΣΔ Modulator

Prior work on pulsewidth modulated and limit cycle ΣΔ modulators tried to set up an equivalence with a conventional multibit CT ΣΔ modulator [78,80, 82]. The system could be compared to a conventional modulator operating at a sample frequency of $2f_c$ (a conventional modulator would have a limit cycle at $\frac{f_s}{2}$), and a multibit quantizer with $\frac{f_s}{f_c}$ levels. The OSR would be similarly defined with respect to the signal bandwidth f_b:

$$\mathrm{OSR} = \frac{f_c}{f_b}. \tag{6.16}$$

This way, using equation (6.15), the in-band noise for a plain oversampling converter could be written as:

$$\mathrm{IBQN}_{[\mathrm{OSR}]} = \frac{2}{3}\frac{f_c}{f_s}\frac{2}{f_s}f_b = \frac{4}{3}\left(\frac{f_c}{f_s}\right)^2\frac{1}{\mathrm{OSR}}. \tag{6.17}$$

Next to the effect of oversampling, also a 6 dB decrease per octave can be identified for the ratio $\frac{f_s}{f_c}$. This is compliant with the decrease of quantization noise power by increasing the number of bits in a multibit quantizer and hence the equivalence accounts. However, this equivalence is only an approximation and neglects several aspects of the actual self-oscillating CT ΣΔ modulator. Furthermore, the self-oscillation frequency f_c should still be much higher than the signal bandwidth f_c (OSR large enough) for the spectral broadening due to pulsewidth modulation not to interfere in the signal band.

An alternative model that is derived through the describing function theory is shown in fig. 6.12. It is based on the low-frequency linearization and quantization noise mechanism outlined above. In this model the comparator is replaced by its best-fit gain, calculated according to equation (6.14). The quantization noise is modeled as white noise with a variance according to equation (6.15).

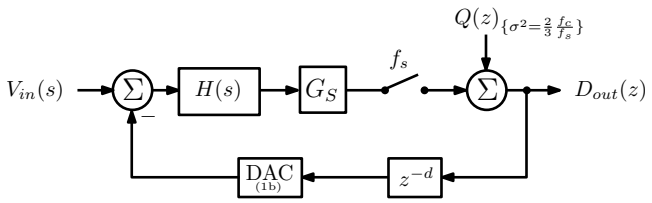

Figure 6.12: Low-frequency linearized model for analysis of the self-oscillating ΣΔ modulator.

6.4.3 Jitter Performance of Self-Oscillating ΣΔ Modulators

Clock jitter was described in chapter 3 as a phenomenon which affects the performance of CT ΣΔ modulators because it introduces a random component in the DAC feedback signal. For conventional modulators, the jitter performance was clearly influenced by the modulator loopfilter. Indeed, the more aggressive the loopfilter, the higher the energy of the out-of-band quantization noise and thus the switching activity. In the case of self-oscillating ΣΔ modulators, such an analysis is not needed because the switching activity is well controlled and signal independent: i.e. the output waveform switches twice per period of the self-oscillation. As such the output is affected by a white jitter error with a variance:

$$\sigma^2_{\text{jitter,SO}} = 4\frac{\sigma^2_{\Delta T}}{T_s^2}\frac{2f_c}{f_s}. \tag{6.18}$$

Since this jitter is white and occupies the band from DC to $f_s/2$, obviously most of the jitter is outside the signal band. For a signal bandwidth f_b this leads to an in-band noise variance due to jitter:

$$\text{IBN}_{[\text{jitt,SO}]} = 4\frac{\sigma^2_{\Delta T}}{T_s^2}\frac{2f_c}{f_s}\frac{2}{f_s}f_b = 16\frac{\sigma^2_{\Delta T}}{T_s^2}\left(\frac{f_c}{f_s}\right)^2\frac{1}{\text{OSR}}. \tag{6.19}$$

Again, for a fixed OSR the jitter noise decreases by 6 dB per octave in function of the self-oscillation frequency to sample frequency ratio.

Chapter 7

A 5-MHz, 11-bit Self-Oscillating $\Sigma\triangle$ Modulator with a Delay-Based Phase Shifter in 0.025 mm^2

7.1 Introduction

The increased attention for self-oscillating $\Sigma\Delta$ modulators has recently led to the publication of measurement results from several prototypes. Common to all these prototypes is the reduced system complexity due to the use of only a single bit comparator. The sample frequency can therefore be chosen close to the technological process limit, while the loopfilter components only have to operate at the self-oscillation frequency. Also the digital part of the modulator loop is quite simple as only 1-bit signals have to be fed back. Besides the reduced design complexity, especially the area of the resulting modulators is quite impressive in comparison to conventional multibit modulators. In [80], an asynchronous $\Sigma\Delta$ modulator is designed, based on a hysteresis comparator. In this type of modulator, the actual sampling operation occurs outside of the loop. A first and second order prototype are designed, that achieve an outstanding 70 dB signal-to-noise ratio (SNR) performance in a bandwidth of 8 and 12 MHz respectively. The designs were processed in a 0.18 µm CMOS technology and occupy a mere area of 0.05 mm^2. In [82] a third order delay based self-oscillating $\Sigma\Delta$ modulator was implemented. The prototype achieves an SNDR of 65 dB for a

6.4 MHz bandwidth mode and 58 dB SNDR for a 17 MHz bandwidth mode. The area is only 0.1 mm^2 in a 0.13 µm CMOS technology.

In this chapter, the results of a second order self-oscillating ΣΔ modulator prototype are reported [83, 84]. A delay-based implementation is chosen to sustain the self-oscillation. An additional key element in this design, is the use of a feedback finite-impulse-response digital-to-analog converter (FIR-DAC) which reduces the jitter sensitivity and further relaxes the slewing requirements of the first operational amplifier in the loop. The prototype modulator is fabricated in a 0.18 µm CMOS technology and achieves a dynamic range (DR) of 66 dB for a 5 MHz bandwidth. Due to the low complexity of the circuit, the modulator core area is only 0.025 mm^2. The power consumption of the modulator equals 6 mW.

7.2 System Level Design

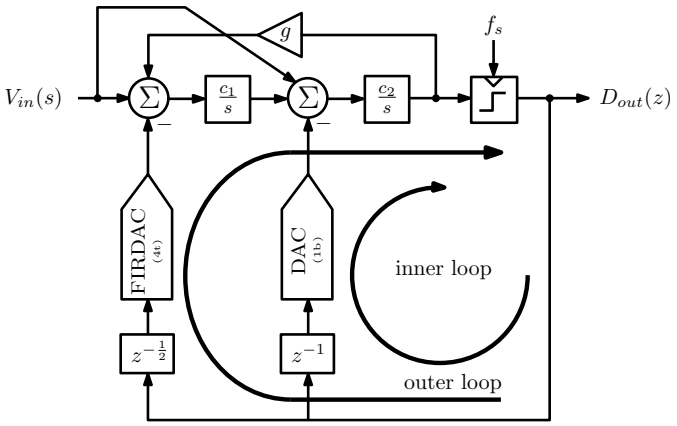

Figure 7.1: Block diagram of the self-oscillating ΣΔ modulator.

Fig. 7.1 shows the block diagram of the second order system that we have implemented. The system-level and corresponding circuit-level parameters can be found in table 7.1. In the structure 2 loops can be considered. The inner loop dominates at high-frequency and controls the self-oscillation. The integrator coefficients are chosen such that they are well below the self-oscillation frequency. One unit delay is introduced in the inner loop to supply enough phase shift for the self-oscillation. This delay is readily

implemented by inserting 1 additional flip-flop in the loop. According to equation (6.7), this would lead to a self-oscillation frequency of $\frac{f_s}{6}$. However, there is a small phase shift due to the outer loop as well. This way, the overall loop exhibits a phase shift of 180° at a frequency of $\frac{f_s}{7.8}$. Since the zero-input limit cycles are constrained to integer fractions of the sampling frequency, this leads to a self-oscillation frequency of $\frac{f_s}{8}$. This was also illustrated in fig. 6.9 from the previous chapter, where the Nichols plot for this system implementation was displayed.

Table 7.1: Second order self-oscillating ΣΔ modulator prototype parameters

Parameter	System level value	Circuit level value
$c_1/(2\pi)$	$0.05 f_s$	42.5 MHz
$c_2/(2\pi)$	$0.05 f_s$	42.5 MHz
g	0.0046	0.0046
f_s		850 MHz
f_c	$f_s/8$	106.25 MHz
f_b	$f_s/170$	5 MHz

The outer loop dominates at low-frequency. Its task is to provide sufficient loop gain to suppress the quantization noise. It has half a clock cycle delay as well, to relax the settling requirements of the comparator. In addition to this, a uniform 4-tap finite-impulse-response digital-to-analog converter is included here:

$$H_{\text{FIRDAC}}(z) = \frac{1}{4}\left(1 + z^{-1} + z^{-2} + z^{-3}\right). \tag{7.1}$$

This FIR filter serves multiple purposes. First it reduces the high-frequency gain of the outer loop. This way, the interaction with the inner loop is minimal and the self-oscillation is mainly determined by the inner loop. The large self-oscillation component is heavily reduced in the outer loop. This way, the first opamp does not have to process fast slewing signals and hence its requirements are significantly relaxed. Finally, this filter improves the jitter sensitivity of our modulator [85, 86]. Due to the averaging effect of the 4-taps FIRDAC the overall jitter variance is reduced by a factor 4 compared to equation (6.18):

$$\sigma^2_{\text{jitter,SO,4t-FIRDAC}} = \frac{\sigma^2_{\Delta T}}{T_s^2}\frac{2f_c}{f_s}. \tag{7.2}$$

The number of taps L in the FIR-filter was the result of a co-optimization process with the first-integrator gain c_1. In terms of performance, both L and c_1 should be as high as possible. However increasing L and c_1 reduces the loop stability. Therefore the selected values for L and c_1 are a compromise of performance versus stability.

To further enhance the noise shaping capability of the loop, local feedback (through the branch with the coefficient g) is added. This way, an optimized zero is implemented [5]. Finally, a feed-in path from the input is also present to reduce to output swing of the first integrator [22].

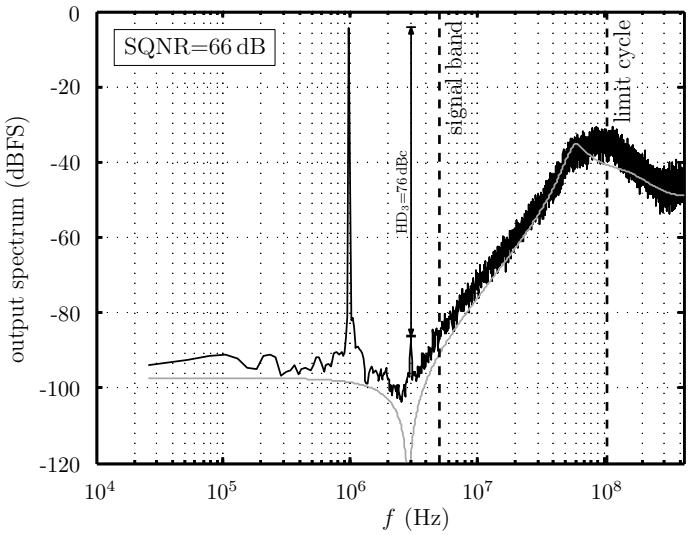

Figure 7.2: Simulated output spectrum for a -4.3 dBFS input signal on the system model (8× averaged 32k FFT).

A system-level simulation was performed with a commercially available continuous-time simulator (Simulink). It was found that the simulation was quite tricky. The simulator time step had to be set to a very small value to avoid additional time-domain quantization effects which caused the results to be unreliable. A resulting simulated output spectrum for a -4.3 dB input relative to full scale (dBFS), is shown in Fig. 7.2. The signal band and the nominal oscillation frequency are indicated by two vertical lines. Clearly, the output contains a lot of content around the oscillation frequency. Due to the pulsewidth modulation of the oscillation mode, spectral broadening appears around $\frac{f_s}{8}$.

The resulting signal-to-quantization-noise ratio (SQNR) equals 66 dB. The calculated noise spectrum according to the low-frequency linearized model from fig. 6.12 is superimposed on the figure. The linearized model underestimates the in-band noise by roughly 3.5 dB and predicts an SQNR of nearly 70 dB. This deviation is due to the fact that the amplitude of the self-oscillation is assumed to be fixed in the calculation. It was found in the simulation that the amplitude increases slightly if a non-zero input signal is applied to the modulator. As a result the effective comparator gain (and hence also the modulator loop gain) is reduced, leading to a degraded performance. Still the matching between the simulated and calculated spectrum can be considered reasonable in the low-frequency band. Because of the non-linear nature of the system, a third-order harmonic is also present at -78 dB relative to the carrier (dBc). This non-linearity can also be understood by noting that the actual low-frequency comparator gain G_S depends on the magnitude of the low-frequency signal component (see equation (6.14)). This way, this non-linear behaviour is inherent to this type of modulator. Of course this non-linearity is reduced by the loop gain and hence the design of the loopfilter greatly affects this undesired component. In our case the non-linearity was sufficiently suppressed to obtain an accuracy in the order of 12 bit.

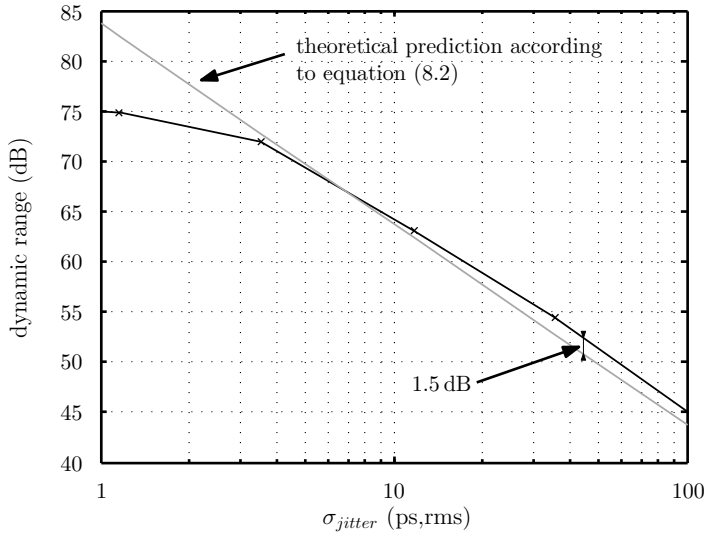

Figure 7.3: Simulated dynamic range vs. jitter rms value for white jitter.

A simulation result of the jitter performance for our modulator is shown in

fig. 7.3. In the simulation model, white jitter was applied to the modulator clock and the corresponding dynamic range was determined. This was repeated for increasing values of the jitter rms value. The result is plotted together with the predicted dynamic range according to equation (7.2). Despite of the simplicity of the derived equation, it matches reasonably well (within 1.5 dB) with the simulation result.

7.3 Circuit Level Design

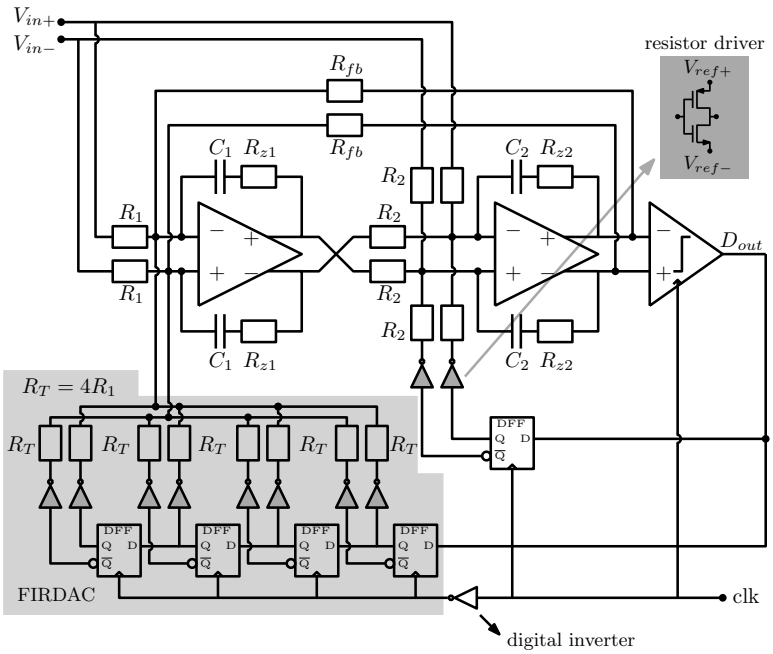

Figure 7.4: Toplevel schematic of the active-*RC* opamp based loopfilter and the switched-resistor feedback DACs.

The prototype is designed for a 5 MHz bandwidth and a clock frequency of 850 MHz. The clock frequency limitation lies in the maximum speed of the digital cells in the target 0.18 µm CMOS process. The resulting limit cycle is 8 times lower than the clock frequency at 106.25 MHz. The circuit-level parameters are shown in table 7.1. The toplevel schematic is illustrated in

fig. 7.4. The integrators are implemented with active-RC feedback opamps, where a small R_z resistor is added to compensate for the finite GBW of the opamp feedback loop. No RC time constant tuning or trimming was incorporated. A local feedback path is formed by the resistors R_{fb} to install an NTF zero in the signal band. A clocked comparator drives the feedback signals, which are implemented using resistive DACs. They are digitally controlled by standard cell D-flip-flops who trigger a resistor driver which switches either to V_{ref+} or V_{ref-}. The FIRDAC is formed by a 4-tap shift register. To install the half clock cycle delay in the outer loop, this shift register operates on the negative clock edge.

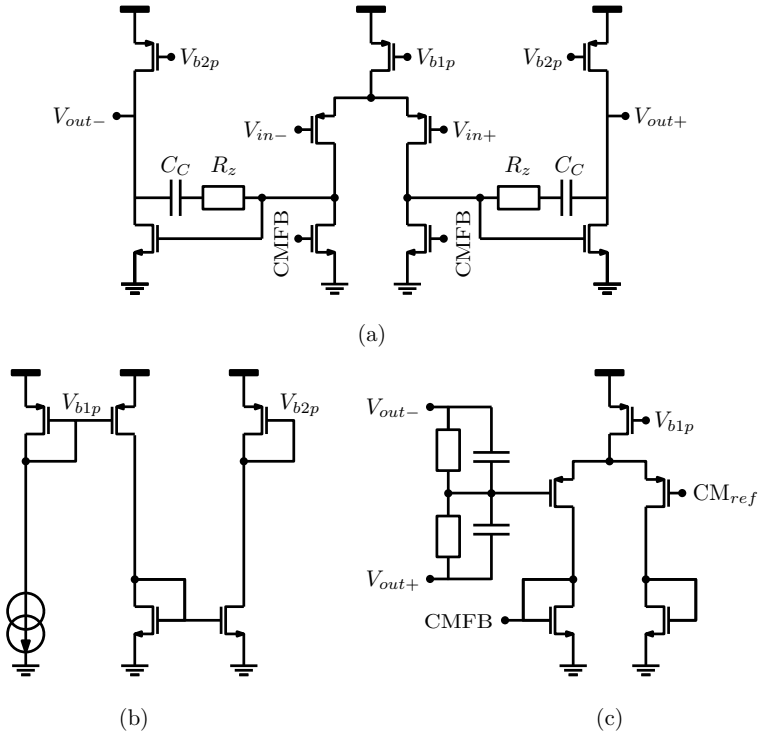

Figure 7.5: Circuit implementation for the opamp: (a) Miller compensated two-stage operational amplifier, (b) the bias circuit for the opamp and (c) the CMFB auxiliary amplifier.

Although the circuit is clocked at 850 MHz, in principle the analog circuits don't have to be sized for this speed. Basically, it is sufficient that the

circuits are capable to process the limit cycle (at 106.25 MHz). This way, quite conventional circuit design techniques could be used for the opamps. To drive the resistive loads, a two-stage Miller compensated opamp topology is used for both integrators. Fig. 7.5 shows the schematic of this opamp. The common-mode feedback (CMFB) control signal is applied at the NMOS transistors in the first stage. The common-mode voltage is sensed with a resistive voltage divider at the outputs and compared to a reference value using an auxiliary amplifier. The opamp was designed to obtain a phase margin of at least 70°. This resulted in a GBW of about 1 GHz, which is definitely enough for this modulator. The opamps in both integrators are basically identical designs. But due to the different drive requirements between the opamp in the first versus the second integrator, an impedance scaling was applied for the second opamp. All transistor widths and the compensation capacitor are decreased by a factor 2 compared to the first opamp. For power optimization, the first integrator was designed for a thermal noise level approximately 6 dB above the quantization noise level.

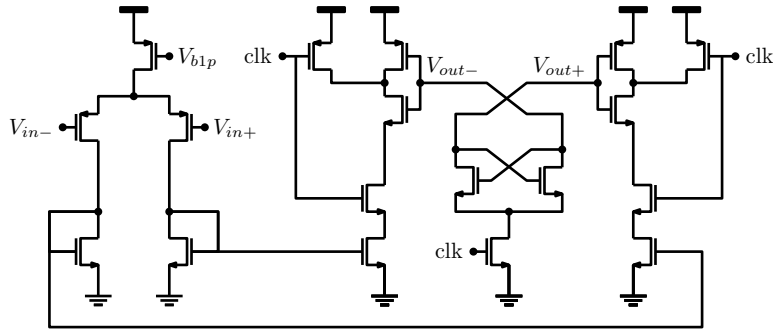

Figure 7.6: Schematic of the comparator consisting of a pre-amplifier and a latch.

The clocked comparator is displayed in fig. 7.6 and is a downscaled version of the circuit that was used in [87]. It consists of a pre-amplifier followed by a latch. The pre-amplifier is a simple PMOS differential pair loaded with ordinary active load NMOS devices to suppress the offset of the clocked latch.

Note that this system is highly portable to a more advanced technology. We could then use a higher clock frequency and adjust the number of digital delays in the inner loop to obtain the same limit cycle. That way, we would

have obtained a nearly equivalent system but with less quantization noise and hence improved performance. Since the circuits in the loop essentially would have to process the same limit cycle, this should not affect the speed requirements on the building blocks (opamps).

7.4 Experimental Results

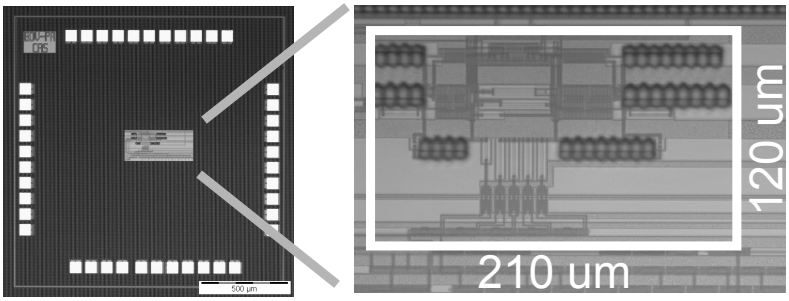

Figure 7.7: Microphotograph of the 0.18 µm CMOS prototype. Left: entire pad-limited die, right: the actual modulator circuit.

Fig. 7.7 shows a microphotograph of the prototype chip fabricated in a single-poly six-metal layer 0.18 µm digital CMOS process. It is shown on the left and is obviously pad-limited. One of the reasons for this, is that the digital outputs are brought off the chip as a parallel 16-bit bus. Internally a shift register is present to convert the 1-bit output stream at 850 MHz to a parallel stream at a 16 times lower rate. The modulator core is shown on the right. It fits in a rectangle of only 0.025 mm^2. From the photograph it is clear that the layout is not dense at all. This is because not much effort was spent to minimize the area. The power consumption is 6 mW from a 1.8 V supply voltage for f_s equal to 850 MHz. The analog blocks (opamps, comparator) consume 5 mW, while the digital blocks consume 1 mW. These digital blocks include clock drivers, the flip-flops in the FIRDAC, and also the shift register that is used to buffer the data out.

A measured output spectrum is shown in fig. 7.8. The input conditions are similar to fig. 7.2 (-4.3 dBFS input tone). A full scale input corresponds to a sine wave with a differential amplitude of 1.8 V. High correlation between the measured spectrum and the simulated spectrum can be observed. The resulting SNR equals 61.1 dB. Also second-order and third-order distortion appear at -57 dBc and -70 dBc respectively. Especially the second-order

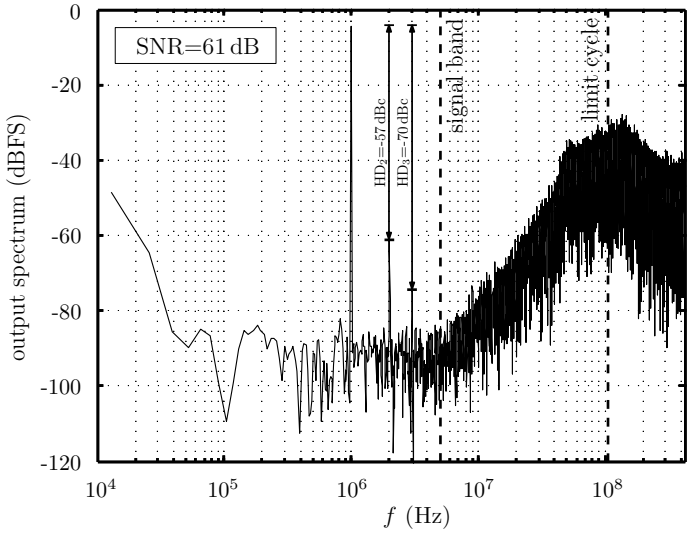

Figure 7.8: Measured output spectrum for a 1 MHz, -4.3 dBFS input signal (64K FFT).

distortion is worrying as it limits the signal-to-noise and distortion ratio (SNDR) of the modulator. Imbalance in the differential behaviour of the system was found to be the cause of this distortion. This is due to the fact that the negative side of the differential DAC is driven by the $\overline{Q}$ output of the standard cell flip-flop, while the positive side of the differential DAC is driven by the Q output (see fig. 7.4). Since the standard cell flip flop is internally asymmetric, the $\overline{Q}$ and the Q output have different gate delays and rise/fall times. This creates a systematic difference between the positive side and the negative side of the DAC. However, this is a non fundamental problem which can be fixed in future designs. From the spectrum also an offset can be observed. Based on measurements on the 10 samples that we received, we found that this offset has a systematic component ($\approx 6\,\text{mV}$ input referred) and a random part ($\sigma \approx 9\,\text{mV}$ input referred). The random offset is caused by limited transistor matching in the first opamp. The systematic offset is caused by the imbalance in the feedback FIRDAC.

In fig. 7.9 the SNR, SNDR and the SNDR without the inclusion of the second-order distortion are shown in function of the input amplitude. The peak SNR of 61.1 dB is found for the -4.3 dBFS input. Even for a full scale input the SNR is still 50.2 dB. However, distortion becomes quite large then,

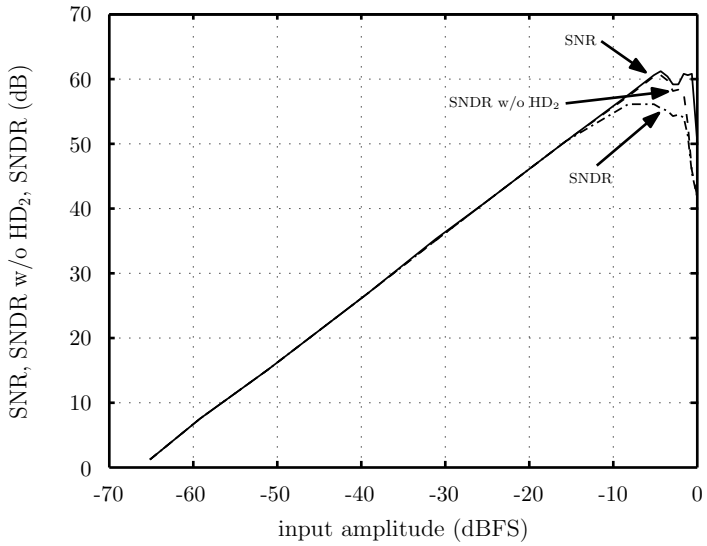

Figure 7.9: SNR (solid), SNDR (dashed-dotted) and the SNDR without second-order distortion (dashed) in function of the input amplitude.

which lowers the SNDR to 41.8 dB. As one can see, second-order distortion is clearly dominant as the SNDR already starts dropping at much lower input signal levels compared to the situation where second-order distortion was neglected. The dynamic range of the modulator equals 66 dB which corresponds to an 11-bit resolution.

Based on the power consumption, signal bandwidth and attained bit resolution we can estimate a figure of merit (FOM) for our prototype [88]:

$$\text{FOM} = \frac{P}{2 f_b 2^B} = 360\,\text{fJ/conversion}. \tag{7.3}$$

A performance summary can be found in table 7.2.

The jitter performance of the prototype was measured as well. For this purpose a low-jitter pulse generator (Agilent 81134A) was modulated through its delay-control input with a noise signal and used as the modulator clock. Under this condition the dynamic range for a 1 MHz input signal was determined. This procedure was repeated for increasing effective values of the jitter. The result is shown in fig. 7.10. It is clear that the dynamic range

Table 7.2: Prototype performance summary

Technology	0.18µm CMOS
Clock frequency	850 MHz
Bandwidth	5 MHz
Power consumption	5 mW analog
	1 mW "digital"
Dynamic range	66 dB
Peak SNR	61.1 dB
Peak SNDR	56.1 dB
Peak SNDR without HD_2	60.6 dB
Converter Area	0.025 mm^2

remains unaffected over a wide range of jitter values. For an effective value of 35 ps,rms the performance drops with 3 dB. For very large values of the jitter, clock pulses that are shorter than 1 ns start to occur. This leads to timing violations in the digital cells. This causes bit errors, leading to a very steep drop of the dynamic range. The white jitter limit according to equation (7.2) is shown as well in the figure. Surprisingly the measured dynamic range is nearly an order of magnitude *better* than the calculated value. This turns out to be due to the fact that the jitter in our measurement setup is not white but has a limited bandwidth of about 50MHz.

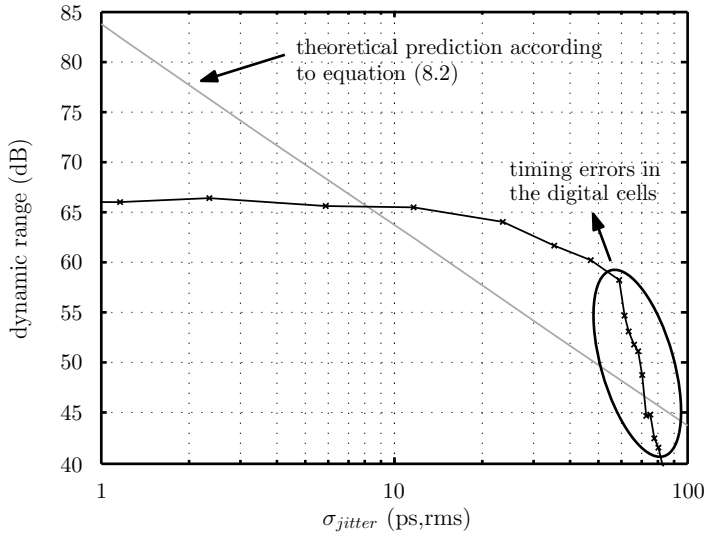

Figure 7.10: Measured DR vs. jitter effective value for a jitter bandwidth of approximately 50 MHz.

Part IV

Closing Remarks

Chapter 8

Conclusion

8.1 Overall Summary

An overall summary can be found at the beginning of this work, both in English and Dutch. This gives a complete overview of the work performed in this dissertation.

8.2 Improvements and Future Research

- The design strategies developed for robust CT $\Sigma\Delta$ modulators could be extended to the domain of bandpass and quadrature bandpass $\Sigma\Delta$ modulators. This is an interesting topic in the context of ADCs for communication standards. Clearly, these are more challenging cases than the conventional lowpass case. It can be understood from the fact that all problems for lowpass CT $\Sigma\Delta$ modulators also occur here. But in addition to this, the modulator performance is very sensitive to the accurate position of the center frequency.
- The system modeling of CT self-oscillating $\Sigma\Delta$ modulators needs some refinement. Indeed, the design of the discussed prototype is actually ad hoc. There are still significant gaps in the tradeoffs between linearity and modulator performance. Also, there are several architectural paths which have not been explored. For example the use of hysteresis-based self-oscillating $\Sigma\Delta$ modulators is expected to provide improved

noise shaping performance, although this may come at the cost of less good control of the self-oscillation frequency. Note that in the discussed prototype, a very stable limit cycle is obtained, because it is controlled by a digital delay in the feedback loop.

- An important next step would be to investigate the overall robustness of self-oscillating $\Sigma\Delta$ modulators. I hope that many of the techniques that were developed for conventional modulators, can also be applied for this class of modulators. However, the current techniques assume that the modulator can be treated as a linear system, whereas due to the non-linear behaviour of the self-oscillating $\Sigma\Delta$ modulator, several of the techniques will need to be revised.

Part V

Appendices

Appendix A

Optimal Coefficients for CT $\Sigma\Delta$ Modulators Based on the $\mathcal{S}$-figure

Optimal design parameters for CT $\Sigma\Delta$ modulators, based on the $\mathcal{S}$-figure design strategy from chapter 5, are given in this appendix. We focus on second and third order designs. The results displayed here are for modulators which contain a 3-bit quantizer, have an OSR of 16 and a NRZ feedback DAC pulse. The results can easily be extended to a different number of quantizer bits. A performance increase/decrease by 6 dB compared to the results displayed here has to be accounted for every quantizer bit change. For a different OSR, the local feedback coefficient can in first order be scaled with the ratio of the desired OSR compared to 16. For a lower OSR than 16, we expect the signal band to interfere even more with the high-frequency behavior of the NTF. In that case, the optimization would have to be re-evaluated. For higher OSRs, the performance increase in first order follows the basic $\Sigma\Delta$ properties of SQNR increase in function of the modulator order (see also fig. 2.7).

All design examples include parasitic poles at f_s in the integrator transfer functions, according to equation (3.15). Next to this, also a synchronization flip-flop is present which introduces a fixed delay of a half clock cycle $\frac{T_s}{2}$ (clocked on the negative clock edge). On top of this, an extra delay of $\tau = \frac{T_s}{10}$ is added to model the mean process delay for the feedback DAC. In general we consider variations for the integrator coefficients, the parasitic pole time-constants and the feedback DAC delay. The usual performance requirements are installed: the modulator should be stable and attain a guaranteed MSA of at least $\frac{1}{\sqrt{2}}$.

A.1 Second Order Designs

A.1.1 Second Order Modulator in Feedforward Topology

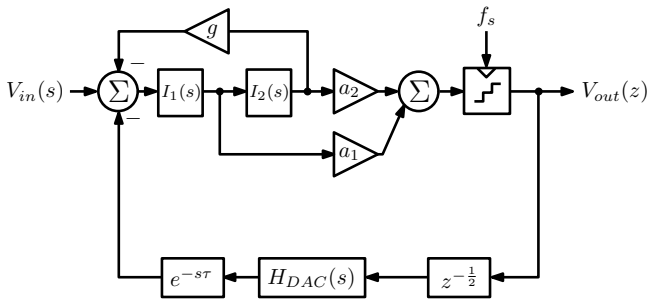

Figure A.1: Second order FF modulator topology.

Following variations apply for the system architecture of fig. A.1:

$$\delta_{IC,max} = 20\,\% \tag{A.1}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.2}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.3}$$

Table A.1 shows the results of the $\mathcal{S}$-figure optimization.

Table A.1: Optimal parameters for the second order design example using the $\mathcal{S}$-figure optimization.

c_1	c_2	g	MSA		$\text{SQNR}_{\text{peak}}$	
			nom	min	nom	min
0.553	0.290	0.137	0.858	0.743	51.2 dB	49.5 dB

A.1.2 Second Order Modulator in Feedforward Topology with Direct Feedback Path

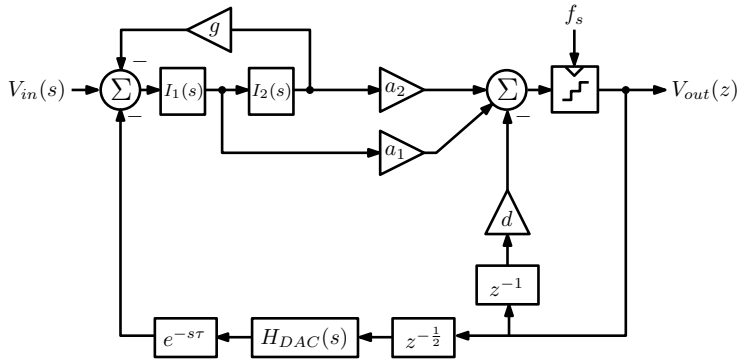

Figure A.2: Second order FF modulator topology with direct feedback path.

Following variations apply for the system architecture of fig. A.2:

$$\delta_{IC,max} = 20\,\% \tag{A.4}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.5}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.6}$$

Table A.2 shows the results of the $\mathcal{S}$-figure optimization.

Table A.2: Optimal parameters for the second order design example with direct feedback using the $\mathcal{S}$-figure optimization.

c_1	c_2	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
				nom	min	nom	min
1.731	0.513	0.024	1.11	0.798	0.722	65.1 dB	62.3 dB

A.1.3 Second Order FF Modulator with Direct Feedback Path and Coefficient Trimming

This example uses the same system architecture of fig. A.2. Following variations apply:

$$\delta_{IC,max} = 5\,\% \tag{A.7}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.8}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.9}$$

Table A.3 shows the results of the $\mathcal{S}$-figure optimization.

Table A.3: Optimal parameters for the second order design example with direct feedback path and coefficient trimming using the $\mathcal{S}$-figure optimization.

c_1	c_2	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
				nom	min	nom	min
1.992	0.644	0.011	1.2	0.767	0.728	69.4 dB	68.2 dB

A.1.4 Second Order FB Modulator with Direct Feedback Path and STF control

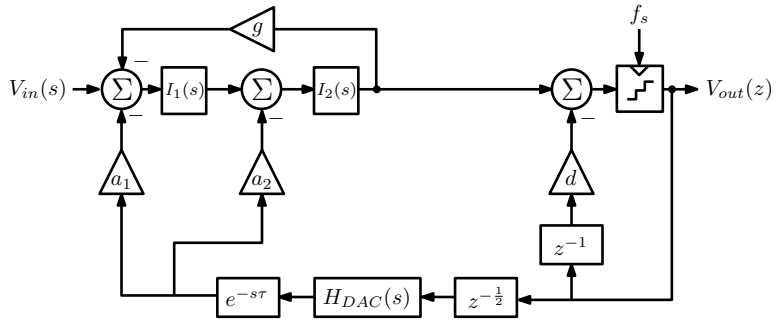

Figure A.3: Second order FB modulator topology for controlled STF peaking.

Following variations apply for the system architecture of fig. A.3:

$$\delta_{IC,max} = 5\,\% \tag{A.10}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.11}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.12}$$

Table A.4 shows the results of the $\mathcal{S}$-figure optimization.

Table A.4: Optimal parameters for the second order FB design example with direct feedback path and coefficient trimming using the $\mathcal{S}$-figure optimization. This modulator has a controlled STF peaking below 2 dB.

c_1	c_2	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
				nom	min	nom	min
0.392	2.048	0.0183	1.203	0.774	0.72	65.6 dB	64.2 dB

In this example, the modulator is in a FB topology because the performance requirements are extended with an extra specification to limit the out-of-band STF peak to 2 dB:

$$\max_f |STF(j2\pi f)| < 2 \text{ dB}. \tag{A.13}$$

A.2 Third Order Designs

A.2.1 Third Order Modulator in Feedforward Topology

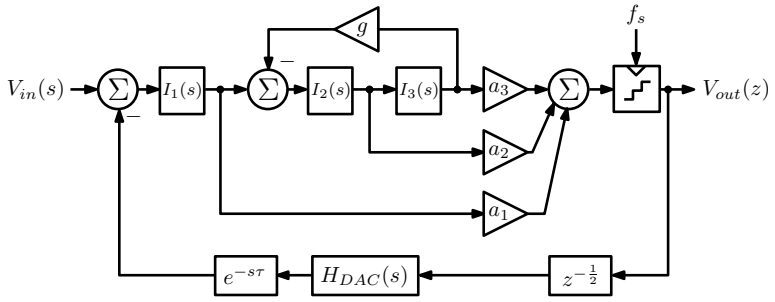

Figure A.4: Second order FF modulator topology.

Following variations apply for the system architecture of fig. A.4:

$$\delta_{IC,max} = 20\,\% \tag{A.14}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.15}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.16}$$

Table A.5 shows the results of the $\mathcal{S}$-figure optimization.

Table A.5: Optimal parameters for the third order design example using the $\mathcal{S}$-figure optimization.

c_1	c_2	c_3	g	MSA		$\text{SQNR}_{\text{peak}}$	
				nom	min	nom	min
0.828	0.181	0.402	0.536	0.82	0.71	60.7 dB	59 dB

A.2.2 Third Order Modulator in Feedforward Topology with Direct Feedback Path

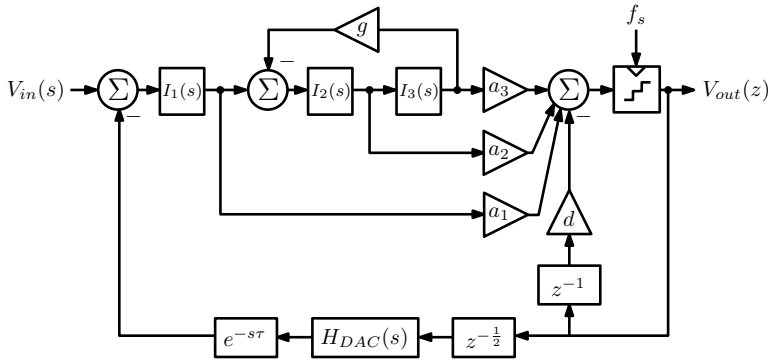

Figure A.5: Third order FF modulator topology with direct feedback path.

Following variations apply for the system architecture of fig. A.5:

$$\delta_{IC,max} = 20\,\% \tag{A.17}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.18}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.19}$$

Table A.6 shows the results of the $\mathcal{S}$-figure optimization.

Table A.6: Optimal parameters for the third order design example with direct feedback using the $\mathcal{S}$-figure optimization.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
2.114	0.414	0.47	0.194	1.132	0.78	0.71	76 dB	74.1 dB

A.2.3 Third Order FF Modulator with Direct Feedback Path and Coefficient Trimming

This example uses the same system architecture of fig. A.5. Following variations apply:

$$\delta_{IC,max} = 5\,\% \tag{A.20}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.21}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.22}$$

Table A.7 shows the results of the $\mathcal{S}$-figure optimization.

Table A.7: Optimal parameters for the third order design example with direct feedback path and coefficient trimming using the $\mathcal{S}$-figure optimization.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
2.491	0.48	0.56	0.102	1.19	0.75	0.71	83.3 dB	82.2 dB

A.2.4 Third Order Hybrid FF/FB Modulator with Direct Feedback Path and STF control

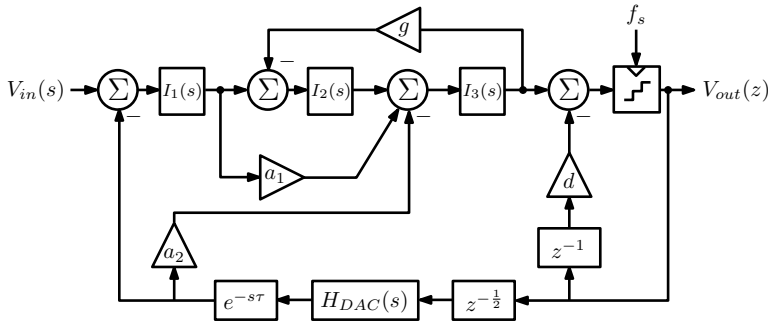

Figure A.6: Third order hybrid FF/FB modulator topology for controlled STF peaking.

Following variations apply for the system architecture of fig. A.6:

$$\delta_{IC,max} = 5\,\% \tag{A.23}$$
$$\delta_{\tau,max} = 50\,\% \tag{A.24}$$
$$\delta_{\tau_p,max} = 20\,\%. \tag{A.25}$$

Table A.8 shows the results of the $\mathcal{S}$-figure optimization.

Table A.8: Optimal parameters for the third order hybrid FF/FB design example with direct feedback path and coefficient trimming using the $\mathcal{S}$-figure optimization. This modulator has a controlled STF peaking below 2 dB.

c_1	c_2	c_3	g	d	MSA		$\text{SQNR}_{\text{peak}}$	
					nom	min	nom	min
0.373	0.113	2.075	0.098	1.13	0.78	0.75	68.3 dB	67 dB

In this example, the modulator is in a hybrid FF/FB topology because the performance requirements are extended with an extra specification to limit the out-of-band STF peak to 2 dB:

$$\max_f |STF(j2\pi f)| < 2 \text{ dB}. \tag{A.26}$$

Bibliography

[1] C. E. Shannon, "Communication In the Presence of Noise," *Proc. Institute of Radio Engineers*, vol. 37, no. 1, pp. 10–21, 1949.

[2] W. R. Bennett, "Spectra of Quantized Signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446–472, 1948.

[3] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters*. IEEE Press, 1996.

[4] B. De Vuyst, P. Rombouts, and G. Gielen, "A Rigorous Approach to the Robust Design of Continuous-Time ΣΔ modulators," *IEEE Trans. Circuits Syst.-I*, vol. 58, no. 12, pp. 2829–2837, 2011.

[5] R. Schreier, "An Empirical Study of High-Order Single-Bit Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 40, no. 8, pp. 461–466, 1993.

[6] J. G. Kenney and L. R. Carley, "Design of Multibit Noise-Shaping Data Converters," *Analog Integrated Circuits and Signal Processing*, vol. 3, no. 3, pp. 259–272, 1993.

[7] R. Schreier, "The ΔΣ toolbox," *http://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox*.

[8] B. E. Boser and B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, 1988.

[9] P. Rombouts, J. De Maeyer, and L. Weyten, "A 250-kHz 94-dB Double-Sampling ΣΔ Modulation A/D Converter With a Modified Noise Transfer Function," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1657–1662, 2003.

[10] S. Rabii and B. A. Wooley, "A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783–796, 1997.

[11] A. R. Feldman, B. E. Boser, and P. R. Gray, "A 13-Bit, 1.4-MS/s Sigma-Delta Modulator for RF Baseband Channel Applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1462–1469, 1998.

[12] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 3.3-V, 15-bit, Delta-Sigma ADC with a Signal Bandwith of 1.1 MHz for ADSL Applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 927–936, 1999.

[13] K. Vleugels, S. Rabii, and B. A. Wooley, "A 2.5-V Sigma-Delta Modulator for Broadband Communications Applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1887–1899, 2001.

[14] R. Gaggl, A. Wiesbauer, G. Fritz, C. Schranz, and P. P., "A 85-dB Dynamic Range Multibit Delta-Sigma ADC for ADSL-CO Applications in 0.18-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1105–1114, 2003.

[15] P. Balmelli and Q. Huang, "A 25-MS/s 14-b 200-mW ΣΔ Modulator in 0.18-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2161–2169, 2004.

[16] del Río, R. and de la Rosa, J. M. and Pérez-Verdú, B. and Delgado-Restituto, M. and Domínguez-Castro R. and Medeiro, F. and Rodríguez-Vázquez A., "Highly Linear 2.5-V CMOS ΣΔ Modulator for ADSL+," *IEEE Trans. Circuits Syst.-I*, vol. 51, no. 1, pp. 47–62, 2004.

[17] L. Yao, M. S. J. Steyaert, and W. Sansen, "A 1-V 140 µW 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, 2004.

[18] J. De Maeyer, *Efficient Architectures for A/D-Converters in Discrete and Continuous Time*. PhD Thesis, University of Ghent, 2006.

[19] J. Tuxal, *Automatic Feedback Control System Synthesis*. McGraw-Hill Book Company, Inc., 1955.

[20] J. A. Cherry and W. M. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 46, no. 4, pp. 376–389, 1999.

[21] E. J. van der Zwan and E. C. Dijkmans, "A 0.2-mW CMOS ΣΔ Modulator for Speech Coding with 80 dB Dynamic Range," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1873–1880, 1996.

[22] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband Low-Distortion Delta-Sigma ADC Topology," *Electron. Lett.*, vol. 37, no. 12, pp. 737–738, 2001.

[23] R. H. M. van Veldhoven, "A Triple-Mode Continuous-Time ΣΔ Modulator With Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2069–2076, 2003.

[24] Patón, S. and Di Giandomenico, A. and Hernández, L. and Wiesbauer, A. and Pötscher, T., "A 70-mW 300-MHz CMOS Continuous-Time ΣΔ ADC With 15-MHz Bandwidth and 11 Bits of Resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1062, 2004.

[25] Philips, K. and Nuijten, P. A. C. M. and Roovers, R. L. J. and van Roermund, A. H. M. and Muñoz Chavero, F. and Tejero Pallarés, M. and Torralba, A., "A Continuous-Time ΣΔ ADC With Increased Immunity to Interferers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2170–2178, 2004.

[26] Yan, S. and Sánchez-Sinencio, E., "A Continuous-Time ΣΔ Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, 2004.

[27] J. De Maeyer, P. Rombouts, and L. Weyten, "Nyquist-Criterion Based Design of a CT ΣΔ-ADC with a Reduced Number of Comparators," *INTEGRATION, the VLSI journal*, vol. 42, pp. 61–67, 2009.

[28] V. Peluso, P. Vancorenland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 900-mV Low-Power ΣΔ A/D Convertor with 77-dB Dynamic Range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, 1998.

[29] M. Ortmanns, F. Gerfers, and Y. Manoli, "Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time ΣΔ Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 51, no. 6, pp. 1088–1099, 2004.

[30] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits," *IEEE Trans. Circuits Syst.-I*, vol. 52, no. 11, pp. 2358–2368, 2005.

[31] F. Gerfers, M. Ortmanns, and M. Y., "A 1.5-V 12-bit Power-Efficient Continuous-Time Third-Order ΣΔ Modulator," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1343–1352, 2003.

[32] B. Xia, S. Yan, and E. Sánchez-Sinencio, "An *RC* Time Constant Auto-Tuning Structure for High Linearity Continuous-Time ΣΔ Modulators and Active Filters," *IEEE Trans. Circuits Syst.-I*, vol. 51, no. 11, pp. 2179–2188, 2004.

[33] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS Continuous-Time ΣΔ ADC With 20-MHz Signal Bandwith, 80-dB Dynamic Range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, 2006.

[34] S. Pavan and N. Krishnapura, "Automatic Tuning of Time Constants in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 54, no. 4, pp. 308–312, 2007.

[35] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching Properties of MOS Transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, 1989.

[36] S. Hausser, S. Majoni, H. Schligtenhorst, and G. Kolwe, "Mismatch in Diffusion Resistors Caused by Photolithography," *IEEE Trans. Semicond. Manufacturing*, vol. 16, no. 2, pp. 181–186, 2003.

[37] J. Shyu, G. C. Temes, and F. Krummenacher, "Random Error Effects in Matched MOS Capacitors and Current Sources," *IEEE J. Solid-State Circuits*, vol. 19, no. 6, pp. 948–955, 1984.

[38] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1057–1066, 1986.

[39] D. W. J. Groeneveld, H. J. Schouwenaars, H. A. H. Termeer, and C. A. A. Bastiaansen, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1517–1522, 1989.

[40] K. Falakshahi, C. Ken Yang, and B. A. Wooley, "A 14-bit, 10-Msamples/s D/A Converter Using Multibit ΣΔ modulation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 607–615, 1999.

[41] I. Galton and P. Carbone, "A Rigorous Error Analysis of D/A Conversion with Dynamic Element Matching," *IEEE Trans. Circuits Syst.-II*, vol. 42, no. 12, pp. 763–772, 1995.

[42] L. R. Carley, "A Noise-Shaping Coder Topology for 15+ Bit Converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 267–273, 1989.

[43] R. Baird and T. Fiez, "Linearity Enhancement of Multibit ΔΣ A/D and D/A Converters Using Data Weighted Averaging," *IEEE Trans. Circuits Syst.-II*, vol. 42, no. 12, pp. 753–762, 1995.

[44] R. Schreier and B. Zhang, "Noise-Shaped Multibit D/A Converter Employing Unit Elements," *EL*, vol. 31, no. 20, pp. 1712–1713, 1995.

[45] J. De Maeyer, P. Rombouts, and L. Weyten, "Adressing static and dynamic errors in unit element multibit-DACs," *Electron. Lett.*, vol. 39, no. 14, pp. 1038–1039, 2003.

[46] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, and Y. Manoli, "A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma-Delta Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 55, no. 11, pp. 3480–3487, 2008.

[47] S. Pavan, "Excess Loop Delay Compensation in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 55, no. 11, pp. 1119–1123, 2008.

[48] J. A. Cherry and W. M. Snelgrove, "Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 46, no. 6, pp. 661–676, 1999.

[49] K. Reddy and S. Pavan, "Fundamental Limitations of Continuous-Time Delta-Sigma Modulators Due to Clock Jitter," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 10, pp. 2184–2193, 2007.

[50] T. Song, Z. Cao, and S. Yan, "A 2.7-mW 2-MHz Continuous-Time ΣΔ Modulator With a Hybrid Active-Passive Loop Filter," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 330–341, 2008.

[51] S. Luschas, R. Schreier, and H. Lee, "Radio Frequency Digital-to-Analog Converter," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1462–1467, 2004.

[52] J. De Maeyer, J. Raman, P. Rombouts, and L. Weyten, "Controlled behaviour of STF in CT ΣΔ modulators," *Electron. Lett.*, vol. 41, no. 16, pp. 896–897, 2005.

[53] M. Keller, A. Buhmann, F. Gerfers, M. Ortmanns, and Y. Manoli, "On the Implicit Anti-Aliasing Feature of Continuous-Time Cascaded Sigma-Delta Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 12, pp. 2639–2645, 2007.

[54] O. Bajdechi, G. E. Gielen, and J. H. Huijsing, "Systematic Design Exploration of Delta-Sigma ADCs," *IEEE Trans. Circuits Syst.-I*, vol. 51, no. 1, pp. 86–95, 2004.

[55] B. De Vuyst, P. Rombouts, J. De Maeyer, and G. Gielen, "The Nyquist Criterion : A Useful Tool for the Robust Design of Continuous-Time $\Sigma\Delta$ Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 57, no. 6, pp. 416–420, 2010.

[56] J. De Maeyer, P. Rombouts, and L. Weyten, "Nyquist Criterion Based Design of Continuous Time $\Sigma\Delta$ Modulators," *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, pp. 2501–2504, 2006.

[57] G. Franklin, J. Powell, and M. Workman, *Digital Control of Dynamic Systems*. Addison Wesley Longman Inc., 1997.

[58] R. Storn and K. Price, "Differential Evolution - A Simple and Efficient Heuristic for Global Optimization over Continuous Spaces," *Journal of Global Optimization*, vol. 11, no. 4, pp. 341–359, 1997.

[59] H. E. Graeb, C. U. Wieser, and K. J. Antreich, "Design Verification Considering Manufacturing Tolerances by Using Worst-Case Distances," *Design Automation Conference*, pp. 86–91, 1992.

[60] K. J. Antreich, H. E. Graeb, and C. U. Wieser, "Circuit Analysis and Optimization Driven by Worst-Case Distances," *IEEE Trans. on Computer-Aided Design of Integrated Circuits Syst.*, vol. 13, no. 1, pp. 57–71, 1994.

[61] K. J. Antreich and H. E. Graeb, "Circuit Optimization Driven by Worst-Case Distances," *Proc. IEEE Int. Conf. Computer Aided Design*, pp. 166–169, 1991.

[62] B. Razavi and B. A. Wooley, "Design Techniques for High-Speed, High-Resolution Comparators," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1916–1926, 1992.

[63] K.-L. Wong and C.-K. Yang, "Offset Compensation in Comparators with Minimum Input-Referred Supply Noise," *JSSC*, vol. 39, no. 5, pp. 837–840, 2004.

[64] P. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s Flash ADC in 0.18- μm CMOS Using Averaging Termination," *JSSC*, vol. 37, no. 12, pp. 1599–1609, 2002.

[65] J. De Maeyer, P. Rombouts, and L. Weyten, "Efficient Multibit Quantization in Continuous-Time ΣΔ Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 4, pp. 757–767, 2007.

[66] S. Lindfors and K. A. I. Halonen, "Two-Step Quantization in Multibit ΔΣ Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 48, no. 2, pp. 171–176, 2001.

[67] Dörrer, L. and Kuttner, F. and Greco, P. and Torta, P. and Hartig, T., "A 3-mW 74-dB SNR 2-MHz Continuous-Time ΔΣ ADC With a Tracking ADC Quantizer in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2416–2427, 2005.

[68] F. Colodro and A. Torralba, "Continuous-Time Sigma-Delta Modulator With a Fast Tracking Quantizer and Reduced Number of Comparators," *IEEE Trans. Circuits Syst.-I*, vol. 57, no. 9, pp. 2413–2425, 2010.

[69] M. Ranjbar, A. Mehrabi, O. Oliaei, and F. Carrez, "A 3.1 mW Continuous-Time ΔΣ Modulator With 5-Bit Successive Approximation Quantizer for WCDMA," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1479–1491, 2010.

[70] M. Hoven, A. Olsen, L. T. S., and C. Toumaze, "Delta-Sigma Modulators Using Frequency-Modulated Intermediate Values," *JSSC*, vol. 32, no. 1, pp. 13–22, 1997.

[71] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "The Architecture of Delta Sigma Analog-to-Digital Converters Using a Voltage-Controlled Oscillator as a Multibit Quantizer," *TCASII*, vol. 46, no. 7, pp. 941–945, 1999.

[72] R. Naiknaware, H. Tang, and T. Fiez, "Time-Referenced Single-Path Multi-Bit ΔΣ ADC using a VCO-Based Quantizer," *TCASII*, vol. 47, no. 7, pp. 596–602, 2000.

[73] M. Z. Straayer and M. H. Perrot, "A 12-bit, 10-MHz Bandwith, Continuous-Time ΣΔ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, 2008.

[74] M. Park and M. H. Perrot, "A 78 dB SNDR 87 mW 20 MHz Bandwith Continuous-Time ΔΣ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, 2009.

[75] C.-Y. Lu, M. Onabajo, V. Gadde, Y.-C. Lo, C. H.-P., V. Periasamy, and J. Silva-Martínez, "A 25 MHz Bandwidth 5th-Order Continuous-Time Low-Pass Sigma-Delta Modulator With 67.7 dB SNDR Using Time-Domain Quantization and Feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1795–1808, 2010.

[76] R. Gray, "Spectral Analysis of Quantization Noise in a Single-Loop Sigma-Delta Modulator with DC Input," *TCOM*, vol. 37, no. 6, pp. 588–599, 1989.

[77] D. Reefman, J. Reiss, and M. Sandler, "Description of Limit Cycles in Sigma-Delta Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 52, no. 6, pp. 1211–1223, 2005.

[78] E. Roza, "Analog-to-Digital Conversion via Duty-Cycle Modulation," *IEEE Trans. Circuits Syst.-II*, vol. 44, no. 11, pp. 907–914, 1997.

[79] T. Piessens and M. Steyaert, "Highly Efficient xDSL Line Drivers in 0.35-μm CMOS using a Self-Oscillating Power Amplifier," *JSSC*, vol. 38, no. 1, pp. 22–29, 2003.

[80] S. Ouzounov, A. Hegt, and A. van Roermund, "Sigma-Delta Modulators Operating at a Limit Cycle," *IEEE Trans. Circuits Syst.-II*, vol. 53, no. 5, pp. 399–403, 2006.

[81] A. Gelb and W. E. Vander Velde, *Multiple-Input Describing Functions and Nonlinear System Design.* McGraw-Hill, 1968.

[82] E. Prefasi, L. Hernandez, S. Paton, A. Wiesbauer, R. Gaggl, and E. Pun, "A 0.1 mm^2, Wide Bandwith Continuous-Time $\Sigma\Delta$ ADC Based on a Time Encoding Quantizer in 0.13-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2745–2754, 2009.

[83] B. De Vuyst and P. Rombouts, "A 5-MHz 11-Bit Self-Oscillating $\Sigma\Delta$ Modulator with a Delay-Based Phase Shifter in 0.025 mm^2," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1919–1927, 2011.

[84] ——, "A 5-MHz 11-bit Delay-Based Self-Oscillating $\Sigma\Delta$ modulator in 0.025 mm2," *Proc. IEEE Custom Integ. Circuits Conf. (CICC)*, pp. 1–4, 2010.

[85] O. Oliaei, "Sigma-Delta Modulator With Spectrally Shaped Feedback," *IEEE Trans. Circuits Syst.-II*, vol. 50, no. 9, pp. 518–530, 2003.

[86] F. Colodro and A. Torralba, "New Continuous-Time Multibit Sigma-Delta Modulators With Low Sensitivity to Clock Jitter," *IEEE Trans. Circuits Syst.-I*, vol. 56, no. 1, pp. 74–83, 2009.

[87] J. De Maeyer, P. Rombouts, and L. Weyten, "A Double-Sampling Extended-Counting ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 411–418, 2004.

[88] R. Walden, "Analog-to-Digital Converter Survey and Analysis," *IEEE J. Selected Areas in Communications*, vol. 17, no. 4, pp. 539–550, 1999.