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Lateral Charge Transport in the Carbon-doped Buffer in AlGaN/GaN-on-Si HEMTs

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***Abstract*—Dynamic R_{ON} and ramped substrate bias measurements are used to demonstrate size and geometry dependent dispersion in power transistors. This is due to a novel lateral transport mechanism in the semi-insulating carbon-doped GaN buffer in AlGaN/GaN HEMTs. We propose that the vertical field generates a 2D hole gas at the bottom of the GaN:C layer, with hole flow extending outside the isolated area. The device-to-device variation is due to a combination of widely spaced preferential leakage paths through the structure and lateral transport from those paths to trapping sites. The spread of the 2DHG outside the active area of the device strongly affects the result of substrate ramp measurements producing major differences between single and multifinger devices. In dynamic R_{ON} recovery measurements, single-finger devices show large device-to-device variation, with multifinger devices showing a small variation with the transient comprising the superposition of the recovery transient of multiple small single-finger devices.**

***Index Terms*—GaN-on-Silicon, HEMTs, current collapse, dynamic R_{ON}, power transistors, 2D Hole Gas**

I. Introduction

GaN based high-electron-mobility transistors (HEMTs) are being actively developed for high power, high voltage switching applications [1, 2]. By using a 2-D electron gas (2DEG) in GaN based heterojunctions and by benefiting from the high bandgap of GaN and its related alloys, low on-resistance (R_{ON}) and high blocking voltages can be realized at the same time [3, 4]. When employing standard approaches to improve the lateral breakdown strength, such as intentional incorporation of carbon (C) dopants, dynamic on-resistance (a time dependent on-resistance resulting from charge storage in either surface or bulk traps that can affect the performance of the device during switching) degrades significantly [5]–[8] impacting the power device efficiency. Surface trapping can be very effectively controlled by the use of field plates [9], but bulk trapping is inherent in all single-heterojunction HEMTs due to the necessity to include deep-level dopants in the GaN buffer to control bulk leakage and short-channel effects [10, 11]. Carbon has a complex range of deep levels in the gap, but the most important is an acceptor sitting 0.9 eV above the valence band [12]. With some compensation, this means that the buffer is weakly p-type with a low hole density, and hence high resistivity, giving long time constants for charging processes (a hole density of only 10^4 cm^{-3} was inferred in [13]). Charge trapping in the buffer leads to significant current collapse. Thus, it is necessary to understand the charge storage and transport in the various layers of the buffer to predict the long term stability of these devices. Substrate bias experiments provide an excellent tool to study charge trapping and transport in the buffer and effectively distinguish surface and bulk induced current collapse [14-16]. Monitoring the substrate bias dependence of the channel conductivity, and its dispersion as the ramp-rate and temperature are varied, allowed a model for the transport within each layer within the buffer to be constructed [13, 17-19]. Substrate bias ramps have been used to link buffer leakage in the upper part of the epitaxy to dynamic R_{ON} dispersion [20, 21].

Interpretation of substrate measurements has normally used the assumption that all transport is vertical and so 1-D models are appropriate. However, deviations from the 1D behavior have previously been observed locally within the device associated with enhanced leakage under contact regions [13] impacting transport within the isolated area. In this work, dynamic R_{ON} and back-bias measurements were used to investigate transport and trapping in the buffer and show that lateral conduction within the buffer can occur outside the isolated device region. An important consequence is that the assessment of single-finger test devices is not necessarily characteristic of the behavior of multiple-finger transistors and cannot accurately represent trapping issues in such devices. The proposed model to explain this behavior is that the vertical field results in the formation of a 2-D hole gas (2DHG) layer at the heterojunction between the bottom of the GaN:C layer and the AlGaN based strain relief layer (SRL). 2DHGs have been widely discussed as occurring at GaN based heterojunctions and have been exploited in active devices [22]-[26]. Here we show for the first time that a parasitic 2DHG within the buffer can also have a strong impact on the substrate bias dependence. As a result, the substrate biasing technique, which is an important tool in understanding trapping behavior in these devices, must be used with caution as it can give inconsistent results between single-finger and multiple-finger transistors. Interestingly the 2DHG had a more limited effect on dynamic R_{ON} due to the local sinking of holes by the source contact, although clear device size dependence was still apparent.

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II. Experimental Details

Devices were processed as part of the development of a 650V GaN power process. Sheet resistance of the 2DEG is ~400 Ohm/sq. Hall mobility and 2DEG density are ~1750 cm^2/Vs and ~$9x10^{12}$ cm^{-2} respectively. The MISHEMT devices use a Si_3N_4 gate dielectric and show excellent performance and cross-wafer uniformity. The devices have pinch-off voltage of ~−7V and no evidence of surface current collapse [27]–[29]. The epitaxial layer structure, as shown schematically in Fig. 1, used an undoped channel region, an intentionally carbon doped GaN buffer (GaN:C), an Al(Ga)N based strain relief layer (SRL) with heterojunction at the GaN:C to SRL interface, all grown on 6-inch p-type Si.

The device structure and measurement setups are shown in Fig. 1. Two experiments were undertaken: firstly, a conventional drain transient measurement to evaluate dynamic R_{ON}, and secondly a substrate bias ramp. Dynamic R_{ON} measurements were undertaken at room temperature (RT) and 80ºC. All the devices tested had gate and source field plates thereby strongly reducing or eliminating surface trapping effects. They were biased in the off-state with V_{GS} = −10V and V_{DS} = 100V for 1000 seconds before switching to the on-state with V_{GS}= 0V, V_{DS}= 1V. This corresponds to a "worst case" V_{DS} for dynamic R_{ON} measurement in this technology [29, 30, 31]. The on-state current, I_{DON}, was then recorded for 1000s allowing the device to return towards equilibrium. Three different transistors were used for the study: single finger, two finger and multifinger power devices, having the same intrinsic source to drain geometry apart from gate width. The single-finger transistor has a drain on only one side (S-G-D arrangement) and a gate width of 100µm and implant isolated active area of 100×50µm. The 2-finger transistor is symmetric to the drain electrode, again has 100µm wide fingers, and is a S-G-D-G-S sub-cell of the large power transistor. The power transistor has multiple wider fingers with an active area of 2.75×1mm.

The substrate ramp uses the change in conductivity of the 2DEG in the HEMT as a ramped substrate-bias is applied to the silicon wafer to monitor changes in the vertical electric field in the buffer below the 2DEG [13, 17]. Changes in the channel conductivity (with V_{GS}=0V) can then be used to quantify bulk charge storage and trapping. The ramped voltage generates a vertical displacement current through the "leaky dielectric" buffer. The ramprate of ~1V/s is chosen so that the displacement current is comparable to the thermally generated leakage current of typical carbon doped GaN and hence will display dispersion associated with transport in that layer. Fig. 1(c) shows the lumped-element representation of the device structure including the primary vertical leakage paths and capacitances normally used to interpret substrate bias experiments assuming 1D conduction [11, 13-19]. Only negative substrate bias, V_{SUB}, is considered here since this corresponds to the polarity experienced under the drain in a transistor under OFF state conditions. The substrate ramp experiments were carried out with a maximum of 0.1V on the drain and with the gate grounded. All three types of device were tested.

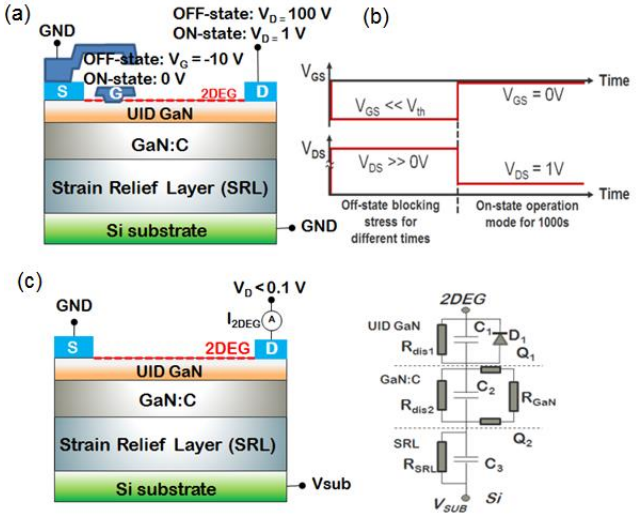
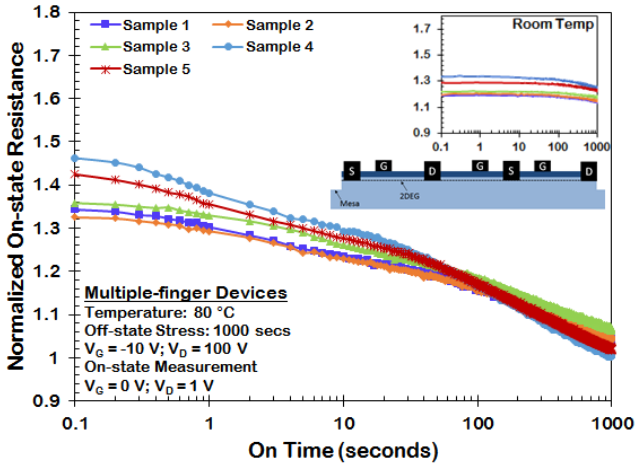


Fig. 1: Schematic cross-section of the AlGaN/GaN HEMT power transistor with (a) dynamic R_{ON} and (b) back-biasing experimental details (c) 1D lumped-element representation of the device structure [16].

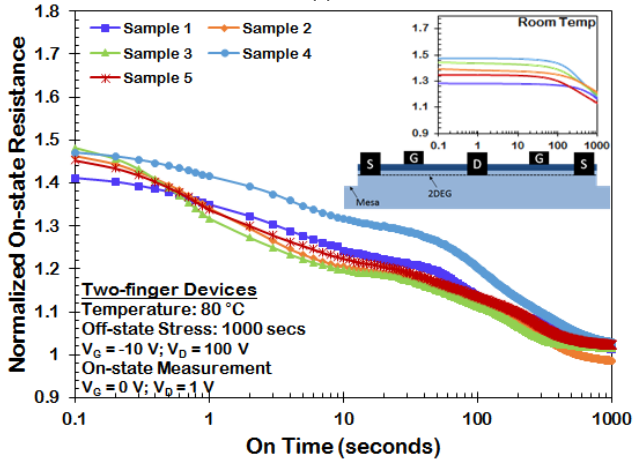
III. Experimental Results

Fig. 2 shows the dynamic R_{ON} measurements for the three device types, normalized to on-state resistance value before stress, at room temperature (inset) and 80ºC. Several samples (five shown) of each kind have been measured to give an indication of the device-to-device variation. The room-temperature measurements for the large devices in Fig. 2(a) show saturation at short times, with the measurement range extending over 4 decades in time insufficient to observe full recovery at that temperature after 1000s [31]. However, when comparing measurements collected at RT and 80°C, the data suggests that the broad distribution of time constants actually extends over at least 6 decades in time for all the tested devices, with very similar behavior seen in all devices. Pulsed measurements of comparable wafers reported in [29] showed similar magnitude dynamic R_{ON} 4ms after stress. By contrast, the single-finger devices in Fig. 2(c) show a summation of a small number (two or three) of individual time-constant responses that are different in each device but with those time constants are distributed over the same 6 decades, indicating that the large multi-finger device behavior is a superposition of multiple small single-finger devices having discrete and distributed time constants. The two-finger devices shown in Fig. 2(b) show behavior that is intermediate between that seen in the single finger and the large devices. We note that pulse IV measurements at room temperature using 1µs ON, 1ms OFF pulses at V_{DS}=50V showed less than 10% current collapse on these devices.

Complementary substrate-bias experiment results are shown in Fig. 3. Fig. 3a shows the 2DEG conductivity normalized to initial conductivity and the vertical leakage through the structure with respect to the substrate voltage for three large transistors. Ramping the substrate bias applied to the silicon resulted in a change in the electric field below the 2DEG and hence a change in 2DEG channel charge and I_D. The ramp rate was sufficiently slow for the silicon substrate to be in equilibrium and was considered as a metallic back



(a)



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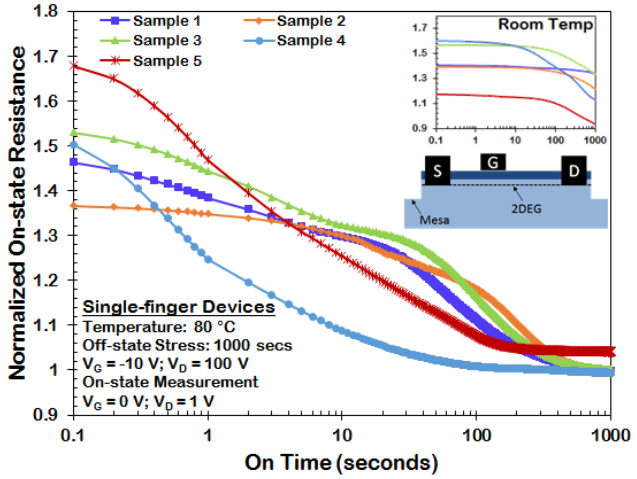
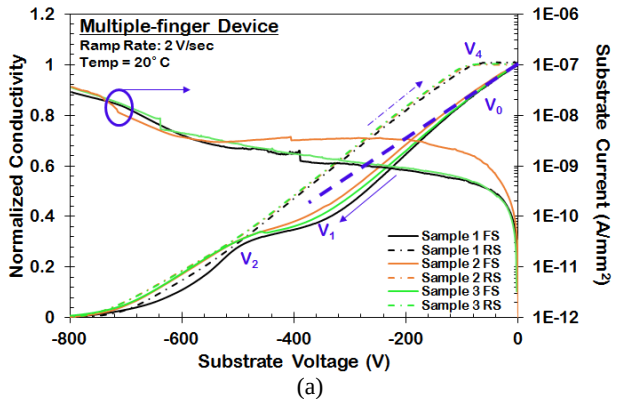


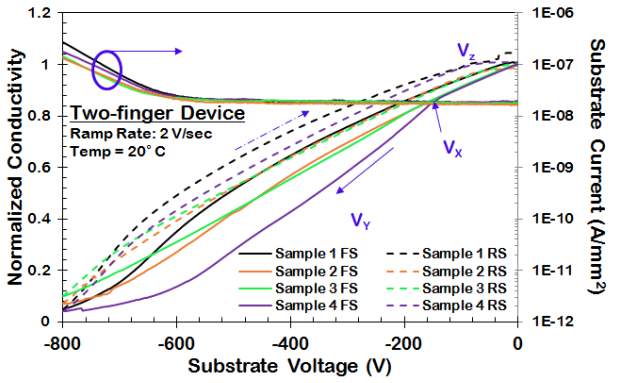
(c)

Fig. 2: On resistance after switching from off-state (V_{GS} =−10V, V_{DS} = 100V) to on-state (V_{GS} = 0, V_{DS}= 1V) of five samples of each of (a) multiple-finger, (b) two-finger and (c) single-finger devices at room temperature. The measurements are normalized to the on resistance before stress.

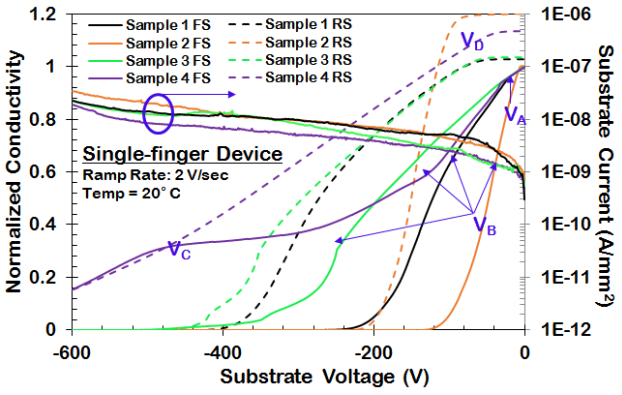
contact. As the device is ramped from 0V to −800V at 2V/s, initially the structures demonstrated a capacitive behavior corresponding to the epitaxial stack behaving as an insulator ie the current dropped linearly with voltage at a rate consistent with the expected Si back-gate extrapolated pinch-off voltage of ~ −730V, blue dashed line. Another way of looking at this



(a)



(b)



(c)

Fig. 3: Sheet conductivity (left axis) and vertical leakage current (right axis) of (a) three AlGaN/GaN multiple-finger power transistors, (b) four two-finger power transistors and (b) four single-finger power transistors during a ramp of the substrate bias from 0 to -V_{SUB} and back to 0V. The sheet conductivity measurements are normalized to the drain current before substrate at V_{SUB} = 0V. (FS: Forward Sweep = 0 to −V_{SUB}; RS: Reverse Sweep = −V_{SUB} to 0V)

is that the back-gate transconductance (the rate of change of 2DEG conductivity with substrate voltage) was constant in this region. At V_0, the conductivity started decreasing at a faster rate before starting to saturate at voltage V_1. The transconductance increased again at V_2 leading to pinch-off at around −800V. On the return sweep significant hysteresis was observed between −500V and 0V. The saturation observed at V_4 led to a return to almost the same 2DEG conductivity at 0V as initially. This indicates almost no net stored charge after bias stress. The basic behavior is apparently very similar to that observed in [13] with positive charge storage between V_1 and V_2 and its neutralization

between V_4 and 0V. The device to device variation for these large devices was minimal. In contrast to the multiple-finger devices, the single-finger transistors showed very high device-to-device variability in their response despite very similar pre-substrate stress channel carrier density across the wafer (<10% variation). Fig. 3c shows the substrate bias dependence for four indicative transistors illustrating the range of behaviors observed. All the devices started out with a capacitive behavior, but beyond voltage V_A, the back-gate transconductance increased significantly by a factor between 1× and 7× compared to the large devices. Most devices went directly to pinch-off at only −100 to −400V, but a small proportion showed a saturation and pinch-off more similar to that seen in the larger devices. On the return sweep, all the devices showed indications of positive charge storage after reaching 0V i.e. the normalized channel current had increased. The two-finger transistors (Fig. 3b), show an intermediate behavior between the multiple-finger and single-finger devices but were closer in behavior to that of the large devices. Most of these samples showed primarily capacitive behavior, while one of the samples (sample 4) had an increased back-gate transconductance at V_X. On reverse sweep, all the samples showed only small amounts of positive charge storage after reaching 0V.

IV. Discussion

The results shown in the previous section presents a contrasting picture between the dynamic R_{ON} and substrate bias experiments. While the dynamic R_{ON} experiments showed that the large multiple-finger device behavior is a superposition of multiple small single-finger devices, the substrate bias experiments showed a dramatic effect of device size.

In the substrate bias experiment results, in all the devices, up to V_0, V_A, or V_X at about −50 to −100V bias, capacitive coupling dominated, which in terms of the equivalent circuit shown in Fig. 1c indicates that resistive leakage is less than the displacement current of $C_{TOT}\, dV_{SUB}/dt$, where C_{TOT} is equal to the series capacitance of C_1, C_2 and C_3. However for the single-finger devices there was a large increase in back-gate transconductance for $|V_{SUB}|>|V_A|$ which varied from device to device. In terms of the 1D transport model presented in Fig. 1(c) the behavior can be explained in two ways: a) an increase in leakage through the SRL (drop in R_{SRL}), which however was not observed in Fig. 3, or b) by an increase in the capacitance between the 2DEG and the Si, which cannot be explained with the 1D model. However, if we relax the 1D assumption, Fig. 4 shows how such an apparent leakage/capacitance increase could arise associated with the creation of a low resistance lateral leakage path. This lateral conductive path would leave C_1, C_2 unchanged but would increase C_3 and hence increase the back-gate transconductance. Given the device epitaxial structure (shown in Fig. 1(a)),, a plausible candidate for this path is a 2DHG at the heterojunction at the top of the SRL. As the field across the epitaxial stack increases, thermally generated holes within the GaN:C layer will flow vertically leaving ionized acceptors in the GaN:C layer and forming a hole accumulation layer at the heterojunction. In this case, the threshold V_{SUB} for its creation

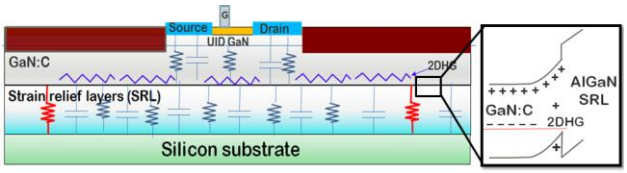


Fig: 4: Schematic diagram showing the location of the 2DHG at the bottom of the GaN:C layer where the band-offset between the GaN:C and SRL creates a blocking junction. Widely spaced preferential leakage paths are shown through the SRL.

seems to be −50 to −100V. The inset to Fig. 4 shows schematically the resulting band diagram at the bottom of the C-doped GaN layer. The 2DHG can form provided the heterojunction is sufficiently high to form a blocking barrier, with the threshold voltage, V_{T2DHG}, for formation of the 2DHG determined by polarization charge and compensating donor (not acceptor) density. Note that V_{T2DHG} has no first order dependence on the carbon acceptor density as long as it is greater than the donor density. The implantation used for isolation only damages about the top hundred nanometers of the structure, suppressing the 2DEG channel, but has no impact below this, meaning that the 2DHG can extend outside the active device area and in principle an unrestricted spread of the 2DHG could occur into the implant isolated area extending over the entire wafer. This allows the original assumption of a 1D current flow to be relaxed, and results in an increase in the SRL capacitance, C_3, and hence an increase in the back-gate transconductance, as was observed especially for the single-finger devices. In practice, the implied increase in C_3 is limited and different in each device, suggesting that the distance that the holes flow laterally is also limited and different for each device. This distance can be very roughly estimated based on the observation that the back-gate transconductance of the single-finger devices varied between 1× and 7× larger than the value for the large device. Hence, and since C_1,C_2>>C_3, it can be inferred that the area over which the holes spread is roughly between 1× and 7× larger than the single-finger transistor isolated area. That active area is 5000μm^2 so the area would increase up to 35,000μm^2 or a circle of diameter ~200μm. So, charge flows up to 50-100μm outside the isolated device area. To explain the variability seen in Fig. 3c, it can be postulated that the leakage through the SRL is dominated by leakage along discrete extended defects whose separation is comparable to, or larger than the isolated area of the small single-finger devices. It is now well known that leakage in GaN P-N diodes occurs along dislocations with high screw component [32] and here we assume that a small proportion of those paths dominates the leakage. These randomly separated discrete leakage paths with separation ~100μm would provide a source of electrons which could neutralize the spreading 2DHG and pin its potential closer to the Si substrate as shown schematically in Fig. 4. So every individual small single-finger device would have a different spread of 2DHG around that device giving rise to the device-to-device variation. This increased area and hence SRL capacitance, C_3, will result in an increase in the field dropped in the UID GaN layer and result in the early pinch-off of the device (as seen in Fig. 3c). The positive charge seen after the return ramp to 0V would correspond to the hole charge stored

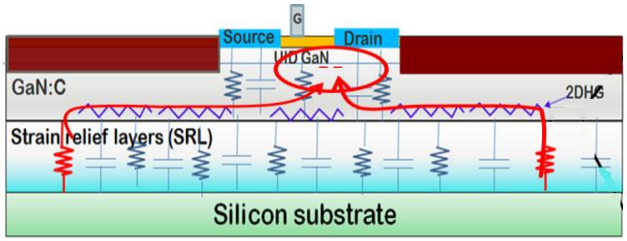


Fig. 5: Schematic representation of the hole transport path during the on-state recovery transient. The negative ionized carbon acceptor charge exposed during the off-state stress is circled [24], as is the single extended-defect leakage path which allows holes to flow from the contacts.

outside the isolated area flowing back into the active device. It is important to note that the current flowing along each vertical leakage path needed to pin the 2DHG potential is very small and only needs to exceed the displacement current which for our ramprate is only ~0.3pA.

In the case of the multi-finger large devices, the maximum lateral hole flow distance outside the active area would be much smaller than the mm-scale active device dimension so it would apparently behave as a 1D structure, with the lateral spreading effect of the 2DHG having little impact. We assume that most of the threading vertical leakage paths would intersect an Ohmic contact and would act as a resistive potential divider between the contact and substrate potentials, and so would not have any strong impact on the potential of the 2DHG. Hence in the large devices, other features of the ramps seen in Fig. 3(a) can be interpreted using the straightforward 1D transport model of Fig. 1c employed in [17]. So the positive charge storage in the buffer seen between V_1 and V_2 can be attributed to hole leakage from the 2DEG channel via a non-Ohmic band-to-band leakage path possibly by a trap-assisted- tunneling process although other possibilities exist [33, 34]. For voltages above $|V_2|$ where the leakage through the SRL exceeds the substrate ramp induced displacement current, leakage could occur more uniformly by a mechanism such as electron tunneling from the Si substrate, however it is more likely that the preferred path would be along extended defects, including those leakage paths inferred to be present from the measurements on single-finger devices.

The situation for the dynamic R_{ON} measurement is quite different from the substrate ramp, and the impact of the 2DHG is likely to be small. When the device is biased in the OFF state positive and negatively charged regions will form in the buffer in response to the vertical and lateral electric fields [30]. The key difference from the substrate ramp is that in OFF state the source contacts will act as a sink for any free holes since there is a forward biased diode between the GaN:C and that contact. Depending on the size of the leakage path between the drain and the GaN:C layer, holes may flow laterally outside the active area in the case of the single finger device, however in general any exposed positive charge in the buffer is likely to be principally in the form of ionized donor charge. When the device is switched to the ON-state, the recovery transient shown in Fig. 2 results from the neutralization of the stored negative charge located between gate and drain (and which is responsible for the dynamic R_{ON}), presumably as ionized carbon acceptors. The carbon doped layer is p-type so the process of neutralizing the excess ionized acceptors will require lateral hole transport within that layer [13, 17, 29]. We propose that in this process variant the large device-to-device variation in the on-state recovery transient observed in the single-finger devices results from the wide variation in distance that the holes have to drift/diffuse from the vertical leakage paths that will act as sources of holes in the ON-state. Fig. 5 shows schematically the transport process that would be involved in the recovery transient when there are two extended-defect leakage paths located outside the active area. The different distances that the holes must flow from a preferential leakage path to the ionized acceptors would result in a different recovery time associated with each leakage path and provide an explanation for the device-to-device variation observed. For large devices, the leakage paths would almost all reside within the device active area but would still provide the source of holes in the ON-state with superposition resulting in the small device-to-device variation.

V. Conclusions

This work demonstrates size and geometry dependent dispersion in power transistors. We interpret this as showing clear evidence for a lateral transport mechanism outside the device isolated area in GaN:C doped HEMTs. We propose that the device-to-device variation is due to a combination of widely spaced (100µm scale separation) leakage paths through the structure and lateral transport from those paths to trapping sites. A 2DHG is present in the buffer, created only when there is an applied vertical field, that augments the lateral charge transport within the carbon doped GaN layer. The spread of the 2DHG outside the active area of the device strongly affects the result of substrate ramp measurements producing major differences between single and multifinger devices. In dynamic R_{ON} recovery measurements, single-finger devices show large device-to-device variation, with multifinger devices showing a small variation with the transient comprising the superposition of the recovery transient of multiple small devices. It is clear, that understanding dynamic R_{ON} dispersion can require not only a full understanding of the point defect deep acceptor and donor density together with any sheet charge layers within the epitaxy, but also the distribution and leakage properties of the extended defects.

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