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Tan, T. H., Mitchell, S. J. N., McNeill, D. W., Wadsworth, H., Strahan, S., & Bailie, I. (2017). Medium Doped Non-Suspended Silicon Nanowire Piezoresistor using SIMOX substrate. In International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES): Proceedings (pp. 189-193). IEEE . DOI: 10.1109/ICAEES.2016.7888036

Published in:
International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES): Proceedings

Document Version:
Peer reviewed version

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Medium Doped Non-Suspended Silicon Nanowire Piezoresistor using SIMOX substrate

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***Abstract*—This paper reports on the enhanced piezoresistive effect in *p*-type <110> silicon nanowires, fabricated using a top down approach. The silicon nanowire width is varied from 100 to 500nm with thickness of 200 nm and length of 9µm. It is found that the piezoresistive effect increases when the nanowire width is reduced below 350 nm. Compared with micrometre sized piezoresistors, silicon nanowires have produced up to 50% enhancement. Silicon nanowire with cross-section of (100 × 200 nm) with doping concentration of 3.2×10^{18} cm^{-3} has produced a gauge factor of 150. The extracted gauge factors are compared with other silicon nanowire experimental publications. The enhancement in piezoresistive effect by employing non-suspended silicon nanowire is beneficial for new MEMS pressure sensors with medium doping concentrations.**

Keywords — Piezoresistive devices; piezoresistance; nanowires; silicon; MEMS.

I. Introduction

Nowadays, silicon MEMS pressure sensors are employed for wide range of monitoring and control applications, ie. environmental, industrial, aircraft, and automotive [1]–[3]. In the automotive sensor market, the demand for tyre pressure sensors has risen rapidly since the introduction of legislation in USA by The National Highway Traffic Safety Administration (NHTSA) making tyre pressure monitoring systems (TPMS) mandatory in vehicles [4]. However, existing pressure sensors require improvements in terms of sensitivity, size, power consumption and temperature dependency [5], [6]. Recently, silicon nanowires have attracted significant attention due to reported enhancement in piezoresistivity. It has been reported that the piezoresistance effect increases with decreasing nanowire dimensions and doping concentrations [7]–[13].

Research on piezoresistance in silicon nanowires was first published by T. Toriyama *et al.*[7] with an enhancement of 55% being reported. This was followed by the discovery of what was termed "giant piezoresistance" (3676% enhancement) by He and Yang [8]. Nanowire devices fabricated by T. Toriyama *et al.* [7] and He and Yang *et al.* [8] both had a suspended structure. K. Reck *et al.* [9] produced *p*-type silicon nanowires from 140nm to 480nm wide on solid substrates. They observed an enhancement of 633% in piezoresistance for the smallest nanowire of 140nm width and 200nm thickness under compressive stress.

T. T. Bui *et al.* [10] studied the effect in *p*-type silicon nanowires with width 35-480 nm in tension. A 60% enhancement in piezoresistance was observed for the smallest nanowires of 35nm width, 40nm thickness and 2µm length. T. Barwicz *et al.* [11] investigated *p*-type silicon nanowire in <100> and <110> orientations. An average of 230% enhancement in piezoresistance was observed for the smallest nanowire in <110> orientation and in compression.

A number of publications have shown the enhanced sensitivity of silicon piezoresistors [12]–[14]. Overall, the piezoresistance coefficient has been found to increase with decreasing nanowire doping and cross-sectional area. In addition, higher piezoresistance enhancement was observed in compression rather than in tension. Piezoresistance was also greater for suspended or free standing silicon nanowires.

In this work we investigate the design of silicon nanowire sensors using top down technology. The operating range of piezoresitive pressure sensors is limited by the noise factor, especially at low doping levels. In order to produce a silicon nanowire that has lower noise level yet enhanced sensitivity, we propose to design our nanowire based on two critical parameters: medium doping and width less than 350 nm. A non-suspended structure is chosen in this nanowire fabrication to minimize the fabrication process steps.

Electron Beam Lithography (EBL) is chosen as the top down fabrication technology to enable nanowires with a range of widths to be fabricated on the same chip. The thickness of nanowire structure is controlled at 200 nm which is achieved by employing very thin silicon-on-insulator (SOI) wafers. For preliminary experimental testing, the four point bending approach is employed to produce uniaxial stress. In order to avoid excessively high resistance values, medium doping concentrations were selected.

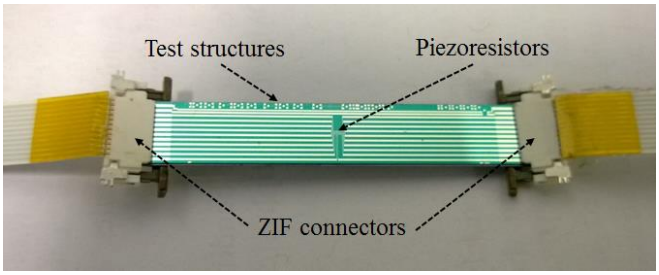

Fig. 1. Photograph of silicon beam array.

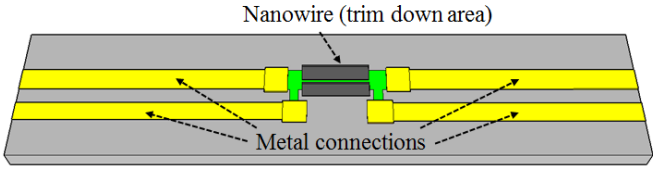

Fig 2. Silicon nanowire 3D layout (not to scale).

II. Design of Silicon Nanowire

The silicon test beams used in our work, are 40mm long, 6.5mm wide and 400µm thick, with each carrying 6 *p*-type piezoresistors (Figure 1). The thickness and width of the chip are defined based on the dimension of the Zero Insertion Force connector (ZIF) which creates a simple plug and measure method [15], [16]. Flat flexible cable is employed to establish electrical connections to the test chip to minimize measurement error. Several test structures are included at one edge of the silicon beam to enable electrical characterization of key process and device parameters.

All six piezoresistors are located at the center surface region of the silicon chip as this area will experience uniform stress when using the four-point bending fixture. Each of the piezoresistors will have a different width but have the same length of 9µm. The variation of width is realized by employing electron beam lithography (EBL) to trim micrometre sized resistors to the desired nanometre width. The trimming will be performed by reactive ion etching (RIE). All piezoresistors are oriented in the <110> direction. Each resistor is designed to enable 4 terminal resistor measurements and eliminate contact resistance effects (Figure 2).

The resistance change for a piezoresistor can be derived as the function of the longitudinal and transverse stress as below [17]–[20]:

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \tag{1}$$

Applying a uniaxial stress along the <110> direction, the relative resistance change for a piezoresistor can be simplified to [15], [16], [21]–[23]

$$\frac{\Delta R}{R} \cong \pi_l \sigma_l \tag{2}$$

The gauge factor (GF), a common measure of the sensitivity of a sensor is defined as

$$GF = \frac{\Delta R / R}{\varepsilon} \cong \frac{\pi_l \sigma_l}{\sigma_l / E} \cong \pi_l E \tag{3}$$

where ε is the strain, E is the young's modulus of silicon. The young's modulus of Silicon is taken as 170 GPa [15], [16], [21]–[23].

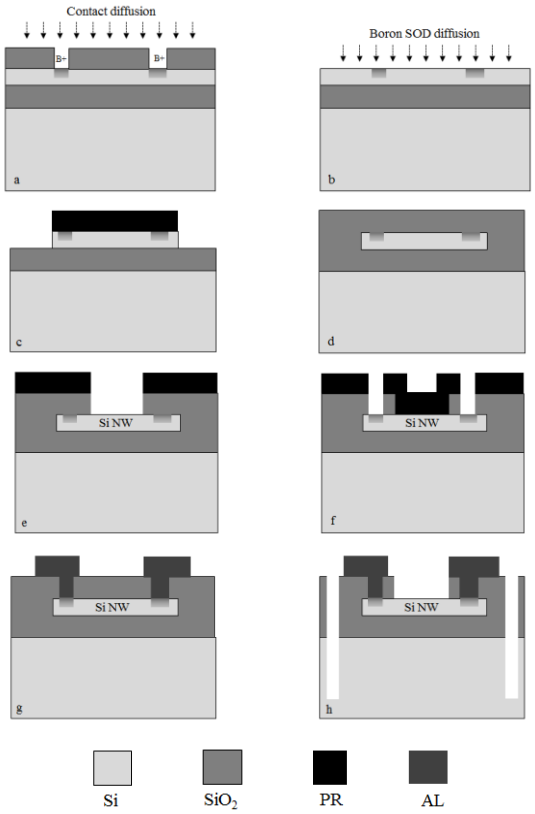

Fig 3. Illustration of fabrication process steps. SOI starting wafer with 200 nm thick device and 375 nm thick buried oxide. (a)boron contact solid source diffusion. (b) boron spin on dopant diffusion. (c) removal of non-resistor area. (d) PECVD oxide deposition. (e) EBL, PECVD oxide RIE etch & Silicon NW HBr RIE etching. (f) contact windows opening. (g) Aluminium deposition; (h) silicon trench etching.

III. Fabrication Of Silicon Nanowire

The silicon nanowire fabrication process consists of 8 main steps (Figure 3). A *p*-type 100 mm diameter SOI wafer, (100) orientation, thickness of 525µm, sheet resistance of 10-20 ohm.cm is used as starting material. The silicon device and buried oxide layers are 200nm and 375nm thick, respectively.

a. First, 600nm of oxide is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). This is used as a mask for solid source boron diffusion of the contact regions.
b. After boron diffusion, the PECVD oxide is stripped. A further boron diffusion from a spin on dopant source is then performed to produce doping concentration less than 1×10^{20}cm^{-3} for the piezoresistor regions.
c. A photo mask is applied to protect resistor regions and the non-resistor areas are removed using reactive ion etching (HBr RIE etching). This step ensures that individual resistors are completely isolated.
d. Approximately 300nm of PECVD oxide is deposited to

protect the silicon device layer during nanowire triming.

e. E-beam lithography is conducted to define the nanowire width, ranging from 100 to 500nm. PMMA photoresist is coated and patterned on the oxide layer. PECVD oxide mask is RIE etched, followed by RIE silicon etching using HBr to trim the resistor to nanometre dimensions.
f. Next, PMMA photoresist is stripped and contact windows wet etched through the PECVD oxide,
g. This is followed by evaporation and patterning of aluminium (approximately 1µm).
h. Finally, deep reactive ion etching, (DRIE) of silicon is performed to create silicon beams from a full device wafer.

An SEM image of the four terminal nanowire piezoresistor configuration is shown in figure 4a, with Figure 4b providing a closer view of the same nanowire with 169nm width and 9µm length.

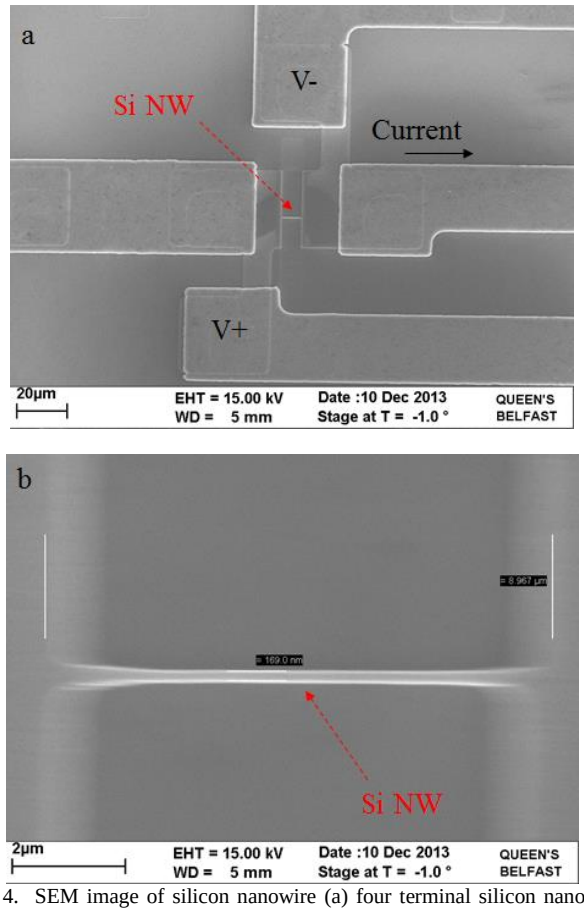

Fig. 4. SEM image of silicon nanowire (a) four terminal silicon nanowire piezoresistor with aluminium metal connections; (b) length 9µm, width 169nm and 200nm thick.

IV. Four Point Bending Apparatus

In this work, four point bending (4PB) apparatus is employed to produce uniform and uniaxial stress along the <110> direction of the piezoresistors [15], [16], [21]–[23]. Figure 5 illustrates the apparatus used. Load weights are used to exert downward force onto the silicon test beam where the displacement is monitored using a Differential Variable Reluctance Transducer (DVRT). The 4PB fixture consists of a base block containing two blades separated by a distance of 28mm and a sliding top block where two inner blades are separated by a distance of 14mm. The fixture is made from the thermoplastic material Acetal (Delrin) which is substantially stable in the temperature range from 0 to 100ºC. Figure 6a and 6b show the silicon beam under no load and 15N load force respectively. Deflection of the test beam can be observed in figure 6b, with the centre of the beam undergoing pure bending.

Horizontal alignment of the chip is achieved by visual inspection. Linear bearings are employed to minimize friction as the top block moves downwards. The stress (σ) at the centre is derived as [15], [16], [21]–[23]

$$\sigma = \frac{3Fa}{wt^2} \quad (1)$$

where F is force, a is inner separation, w is width and t is the thickness of the silicon beam. Deflection is given by [15], [16], [21]–[23]

$$\delta = \frac{\left(12aL - 16a^2\right)aF}{4Et^3w} \quad (2)$$

where L is the length of the beam, and E is the Young's modulus of silicon.

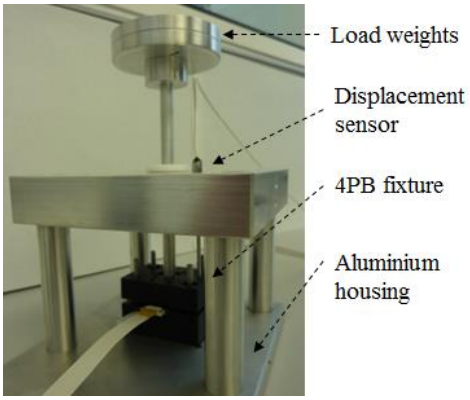

Fig. 5. Photograph of the setup using load weights force application Method.

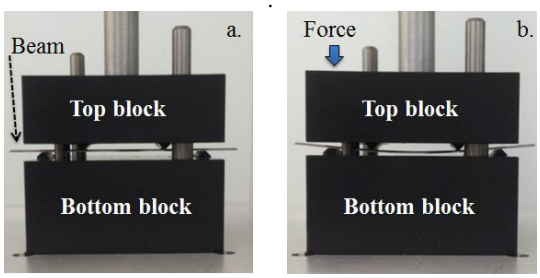

Fig. 6. Photograph of 4PB fixture. (a) zero load (b)15N load.

V. Results And Discussion

Silicon nanowires with width ranging from 100 to 500nm were fabricated and characterised to determine any enhancement of the piezoresistive effect. An Agilent B1500A semiconductor device parameter analyzer was used to characterize the devices. Based on sheet resistance

TABLE I
SILICON NANOWIRE EXPERIMENTAL WORK COMPARISONS (ESTIMATION)

Research group	*w* (nm)	t (nm)	*l* (μm)	ρ (cm^{-3})	Stress application	Structure	Maximum Enhancement (%)	Gauge Factor (Estimated value)
Toriyama *et al.*[7]	53-333	53-65	3	9.0×10^{19}	Tensile	Suspended	55	82
R. He *et al.* [8]	50-350	50-350	2	5.8×10^{16}	Compressive	Suspended	3676	5000
K. Reck *et al.*[9]	140	200	2.8-9.6	4.1×10^{16}	Compressive	Non-suspended	633	770
T. T. Bui *et al.*[10]	35-480	40	2	1.2×10^{18}	Tensile	Non-suspended	60	90
T. Barwicz *et al.*[11]	5-113	23-45	0.4	1.0×10^{15}	Compressive	Non-suspended	230	493
A. Koumela *et al.*[14]	40-50	38-160	0.35-5	5×10^{17}	Compressive	Non-suspended	64	75
A. Koumela *et al.*[14]	40-50	38-160	0.35-5	5×10^{17}	Compressive	Suspended	200	235
Our work (NW)	100-500	200	9	3.2×10^{18}	Compressive	Non-suspended	50	150
Our work (bulk)	20 μm	200	500	3.2×10^{18}	Compressive	Non-suspended	--	99

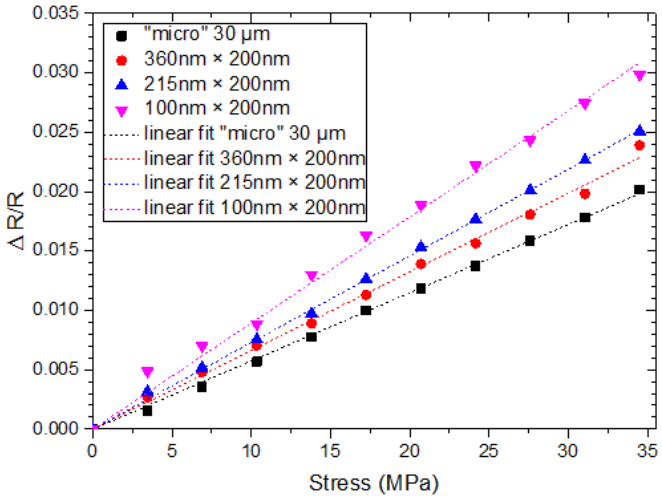

Fig. 7. The relative change in resistance as a function of stress for silicon nanowire at $3.2\times10^{18}cm^{-3}$ doping concentrations.

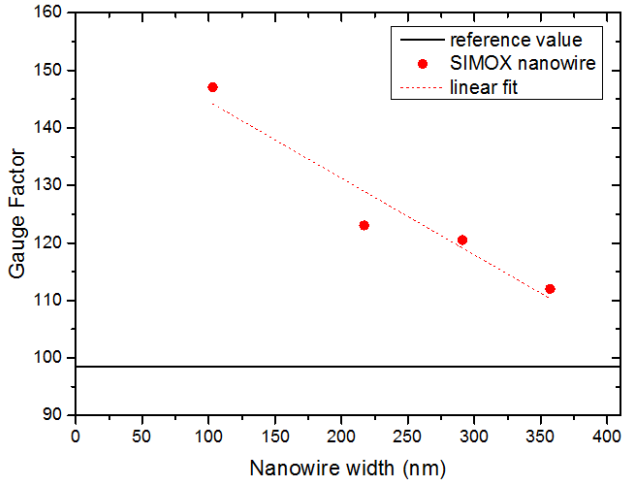

Fig. 8. The gauge factor (GF) as a function of width for silicon nanowire at $3.2\times10^{18}cm^{-3}$ doping concentrations at 3N (34.5MPa).

measurements, the silicon nanowires with 1×10^{19} cm^{-3} boron spin on diffusion have an approximate surface doping concentration of 3.2×10^{18} cm^{-3}.

The relative change in resistance as a function of stress is depicted in figure 7. A linear relationship between resistance change and applied stress up to 34.50 MPa (3 N load force) can be observed. The nanowire widths are estimated from measured resistance values and verified by electron microscopy. The gradient of the graph and hence the piezoresistance effect can be seen to increase as the width of nanowire decreases below 400 nm. The smallest nanowire (100 × 200 nm) has produced sensitivity enhancement of approximately 50%.

Using equation (2), the longitudinal piezoresistance coefficient (π_l) can be extracted. A micrometre sized resistor used as the reference has a longitudinal piezoresistance coefficient (π_l) of $57.97 \times 10^{-11}Pa^{-1}$. The highest longitudinal piezoresistance coefficient, 86.52×10^{-11} Pa^{-1} is observed on nanowires with cross-section of (100 × 200nm). Figure 8 shows the extracted gauge factor as a function of width. The estimation of gauge factor (*GF*) is performed using equation (3). In our work, non-suspended silicon nanowires with cross-section of (100 × 200 nm) produced a gauge factor of approximately 150 compared with the reference value of 99 for a micrometer sized device. This represents an approximately 50% enhancement. The result shows that enhancement is significant when the width of piezoresistor is below 350nm as reported by other researchers [7]–[11], [14].

Table 1 summarizes the publications on silicon nanowires (Si NW) research work and provides comparison with our work. Our experimental results are comparable with other recent publications on non-suspended silicon nanowires at medium doping level. It is also observed that the highest gauge factor of ~5000 was reported by He and Yang using bottom up nanowire in the <111> direction [8]. For top down fabricated silicon nanowires in the <110> direction, K. Reck et al. has produced the nanowire with the highest gauge factor of ~770 [9] however at much lower doping concentrations. Overall, greater enhancement in piezoresistance effect is observed for silicon nanowires with width of less than 100 nm, thickness of less than 50 nm, low doping level and compressive stress. However, top down nanowires with dimensions of less than 100 nm are not investigated in this work as they are less feasible for high volume fabrication due to the limitation of conventional fabrication technology.

VI. CONCLUSION

In this work, *p*-type non-suspended medium doped silicon nanowire piezoresistors were fabricated by a combination of boron spin on dopant diffusion, electron beam lithography, and RIE. Test samples were diced into silicon beams to be tested in a four point bending apparatus. The smallest piezoresistor width was 100nm, and the thickness was 200nm. The extracted $\pi_{l[110]}$ and gauge factor increase significantly as nanowire dimensions are reduced below 350 nm. An enhancement of 50% relative to micrometre sized devices is obtained in the case of 100nm wide

piezoresistors. Such enhancement in sensitivity of non-suspended devices is beneficial for sensors that are required to operate in harsh mechanical environments, such as tyre pressure sensors.

ACKNOWLEDGMENT

T H Tan would like to thank Schrader Electronics Ltd. for sponsorship of this project.

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