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CIRCUIT-AWARE DESIGN OF ENERGY-EFFICIENT MASSIVE MIMO SYSTEMS

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ABSTRACT

Densification is a key to greater throughput in cellular networks. The full potential of coordinated multipoint (CoMP) can be realized by massive multiple-input multiple-output (MIMO) systems, where each base station (BS) has very many antennas. However, the improved throughput comes at the price of more infrastructure; hardware cost and circuit power consumption scale linearly/affinely with the number of antennas. In this paper, we show that one can make the circuit power increase with only the square root of the number of antennas by circuit-aware system design. To this end, we derive achievable user rates for a system model with hardware imperfections and show how the level of imperfections can be gradually increased while maintaining high throughput. The connection between this scaling law and the circuit power consumption is established for different circuits at the BS.

1. INTRODUCTION

We consider a cellular network where each BS communicates with K unique single-antenna user equipments (UEs). Interference coordination is a major limiting factor in these systems but can be handled in the spatial domain by CoMP methods, where several antennas, N , are deployed at each BS [1]. The massive MIMO paradigm, where $N \gg K$, has gained particular traction in recent years [2], because it allows for distributed interference coordination and brings robustness to having imperfect channel state information (CSI).

Two important practical issues with the deployment of large antenna arrays are the increased hardware cost and circuit power consumption [3]—these scale linearly/affinely with N unless we redesign the network with these two issues in mind. Low-cost energy-efficient transceiver equipment suffer from hardware imperfections, which must be modeled properly if accurate conclusions are to be drawn [4–6]. In this paper, we consider an uplink system distorted by multiplicative phase-drifts, additive distortion noise, and noise

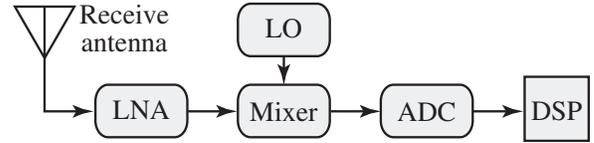


Fig. 1. Block diagram of one antenna branch in a typical receiver. The main hardware components are given, while various filters are also needed.

amplifications. We derive achievable user rates and prove that the level of imperfections can be gradually increased with N . The practical implications of this scaling law are established for three circuits at the BSs: analog-to-digital converter (ADC), low noise amplifier (LNA), and local oscillator (LO). These are the main components of the typical receiver illustrated in Fig. 1.

2. SYSTEM MODEL

We consider the uplink of a network with $L \geq 1$ cells. The flat-fading channel from UE k in cell l to BS j is denoted as $\mathbf{h}_{jlk} \triangleq [h_{jlk}^{(1)} \dots h_{jlk}^{(N)}]^T \in \mathbb{C}^N$ and is modeled as block fading; thus, it is static for a coherence block of T channel uses and has independent realizations between blocks. Each channel is zero-mean circularly symmetric complex Gaussian distributed as $\mathbf{h}_{jlk} \sim \mathcal{CN}(\mathbf{0}, \lambda_{jlk} \mathbf{I}_N)$, where the average channel attenuation $\lambda_{jlk} > 0$ depends on the large-scale fading.

The signal $x_{lk}(t)$ sent by UE k in cell l at channel use t satisfies a power constraint of $\mathbb{E}\{|x_{lk}(t)|^2\} = p_{lk}$ and $\mathbf{x}_l(t) \triangleq [x_{l1}(t) \dots x_{lK}(t)]^T \in \mathbb{C}^K$ is the transmit signal in cell l .

Contrary to most prior works on massive MIMO (e.g., [2] and references therein), the receiver branches at the BSs are assumed to be imperfect. Interestingly, it is shown in [4–6] that imperfect hardware mainly causes multiplicative phase-drifts, additive distortion noise, and noise amplifications. Based on these prior works, the received signal $\mathbf{y}_j(t) \in \mathbb{C}^N$ at BS j at channel use $t \in \{1, \dots, T\}$ in the coherence block is modeled as

$$\mathbf{y}_j(t) = \mathbf{D}_{\phi_j(t)} \sum_{l=1}^L \mathbf{H}_{jl} \mathbf{x}_l(t) + \mathbf{v}_j(t) + \boldsymbol{\eta}_j(t) \quad (1)$$

where $\mathbf{H}_{jl} \triangleq [\mathbf{h}_{jl1} \dots \mathbf{h}_{jlK}] \in \mathbb{C}^{N \times K}$ is the channel from

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$$\text{SINR}_{jk}(t) = \frac{p_{jk} |\mathbb{E}\{\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{h}_{jjk}(t)\}|^2}{\sum_{l=1}^L \sum_{m=1}^K p_{lm} \mathbb{E}\{|\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{h}_{jlm}(t)|^2\} - p_{jk} |\mathbb{E}\{\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{h}_{jjk}(t)\}|^2 + \mathbb{E}\{|\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{v}_j(t)|^2\} + \sigma^2 \xi \mathbb{E}\{\|\mathbf{v}_{jk}(t)\|^2\}} \quad (7)$$

UEs in cell l , while the hardware imperfections are given by:

1. Phase-drift matrix $\mathbf{D}_{\phi_j(t)} \triangleq \text{diag}(e^{i\phi_{j1}(t)}, \dots, e^{i\phi_{jN}(t)})$ where the drift at the n th antenna of BS j at time t follows a Wiener process: $\phi_{jn}(t) \sim \mathcal{N}(\phi_{jn}(t-1), \delta)$. The parameter $\delta \geq 0$ is the variance of the innovations.
2. Additive distortion noise $\mathbf{v}_j(t) \sim \mathcal{CN}(\mathbf{0}, \mathbf{\Upsilon}_j)$ which is independent across time and antennas, such that

$$\mathbf{\Upsilon}_j \triangleq \kappa^2 \sum_{l=1}^L \sum_{k=1}^K p_{lk} \text{diag}(|h_{jlk}^{(1)}|^2, \dots, |h_{jlk}^{(N)}|^2)$$

for a given channel realization. The variance at an antenna is proportional to the received signal power at this antenna and $\kappa \geq 0$ is the proportionality parameter [4].

3. The receiver noise $\boldsymbol{\eta}_j(t) \sim \mathcal{CN}(\mathbf{0}, \sigma^2 \xi \mathbf{I}_N)$ where σ^2 is the fundamental thermal noise power and the parameter $\xi \geq 1$ is the noise amplification factor.

This tractable model of hardware imperfections at the BS is characterized by three parameters: δ , κ , and ξ . We exemplify in Section 4 how these are related to the main hardware components of the BSs which are shown in Fig. 1. In the analysis of this paper, we distinguish between two important cases: a common LO (CLO) on all antennas of a BS and separate LOs (SLOs) with identical properties. In the former case, the phase drifts $\phi_{jn}(t)$ are identical for all $n = 1, \dots, N$, while these drifts are independent when having SLOs.

3. ACHIEVABLE USER RATES AND SCALING LAWS

Next, we provide our main analytic throughput results for the system model in (1). These results are exploited in Section 4 where we describe the individual impact of different hardware components on massive MIMO configurations.

Although the channel is fixed within the coherence block, the effective channels $\mathbf{h}_{jlk}(t) \triangleq \mathbf{D}_{\phi_j(t)} \mathbf{h}_{jlk} \in \mathbb{C}^N$ change due to the phase-drifts. Hence, we need to estimate the channel for each t used for transmission. Suppose pilot sequences that occupy B channel uses are transmitted in the beginning of each coherence block; $\tilde{\mathbf{x}}_k \triangleq [x_{jk}(1) \dots x_{jk}(B)]^T \in \mathbb{C}^B$ is the pilot sequence of UE k in cell j . The following is the linear minimum mean squared error (LMMSE) estimator.

Lemma 1. Let $\boldsymbol{\psi}_j \triangleq [\mathbf{y}_j^T(1) \dots \mathbf{y}_j^T(B)]^T \in \mathbb{C}^{NB}$ denote the received signal at BS j during the pilot transmission. For both a CLO and SLOs, the LMMSE estimate of $\mathbf{h}_{jlk}(t)$ at any channel use $t \geq B$ for any l and k is

$$\hat{\mathbf{h}}_{jlk}(t) = (\lambda_{jlk} \tilde{\mathbf{x}}_{lk}^{\text{H}} \mathbf{D}_{\delta(t)} \boldsymbol{\Psi}_j^{-1} \otimes \mathbf{I}_N) \boldsymbol{\psi}_j \quad (2)$$

where $\mathbf{D}_{\delta(t)} \triangleq \text{diag}(e^{-\frac{\delta}{2}(t-1)}, e^{-\frac{\delta}{2}(t-2)}, \dots, e^{-\frac{\delta}{2}(t-B)})$,

$$\boldsymbol{\Psi}_j \triangleq \sum_{\ell=1}^L \sum_{m=1}^K \lambda_{j\ell m} \mathbf{X}_{\ell m} + \sigma^2 \xi \mathbf{I}_B, \quad (3)$$

$$\mathbf{X}_{\ell m} \triangleq \bar{\mathbf{X}}_{\ell m} + \kappa^2 \mathbf{D}_{|\bar{\mathbf{x}}_{\ell m}|^2}, \quad (4)$$

$$\mathbf{D}_{|\bar{\mathbf{x}}_{\ell m}|^2} \triangleq \text{diag}(|x_{\ell m}(1)|^2, \dots, |x_{\ell m}(B)|^2), \quad (5)$$

\otimes is the Kronecker product, and element (i_1, i_2) of $\bar{\mathbf{X}}_{\ell m}$ is

$$[\bar{\mathbf{X}}_{\ell m}]_{i_1, i_2} = \begin{cases} |x_{\ell m}(i_1)|^2, & i_1 = i_2, \\ x_{\ell m}(i_1) x_{\ell m}^*(i_2) e^{-\frac{\delta}{2}|i_1 - i_2|}, & i_1 \neq i_2. \end{cases} \quad (6)$$

Proof. This LMMSE estimator was derived for SLOs in [6] and the same derivations hold for a CLO. \square

The channel estimates in Lemma 1 are utilized to select receiver filters $\mathbf{v}_{jk}^{\text{H}}(t) \in \mathbb{C}^N$. Using an approach from [7] and [6, Lemma 1], the achievable rate for UE k in cell j is

$$R_{jk} = \frac{1}{T} \sum_{t=B+1}^T \log_2(1 + \text{SINR}_{jk}(t)) \quad [\text{bit/channel use}]$$

where $\text{SINR}_{jk}(t)$ is given in (7) at the top of this page. The expectations in (7) can be computed in closed form if the BS applies maximum ratio combining (MRC): $\mathbf{v}_{jk}(t) = \hat{\mathbf{h}}_{jjk}(t)$.

Lemma 2. If the MRC receive filter is used, then

$$\begin{aligned} \mathbb{E}\{\|\mathbf{v}_{jk}(t)\|^2\} &= N \lambda_{jjk}^2 \tilde{\mathbf{x}}_{jk}^{\text{H}} \mathbf{D}_{\delta(t)} \boldsymbol{\Psi}_j^{-1} \mathbf{D}_{\delta(t)}^{\text{H}} \tilde{\mathbf{x}}_{jk} \\ \mathbb{E}\{\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{h}_{jjk}(t)\} &= \mathbb{E}\{\|\mathbf{v}_{jk}(t)\|^2\} \\ \mathbb{E}\{|\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{h}_{jlm}(t)|^2\} &= \lambda_{jlm} \mathbb{E}\{\|\mathbf{v}_{jk}(t)\|^2\} \\ &+ N \lambda_{jjk}^2 \lambda_{jlm}^2 \tilde{\mathbf{x}}_{jk}^{\text{H}} \mathbf{D}_{\delta(t)} \boldsymbol{\Psi}_j^{-1} \mathbf{X}_{lm} \boldsymbol{\Psi}_j^{-1} \mathbf{D}_{\delta(t)}^{\text{H}} \tilde{\mathbf{x}}_{jk} + N(N-1) \\ &\times \begin{cases} \lambda_{jjk}^2 \lambda_{jlm}^2 \tilde{\mathbf{x}}_{jk}^{\text{H}} \mathbf{D}_{\delta(t)} \boldsymbol{\Psi}_j^{-1} \bar{\mathbf{X}}_{lm} \boldsymbol{\Psi}_j^{-1} \mathbf{D}_{\delta(t)}^{\text{H}} \tilde{\mathbf{x}}_{jk} & \text{if a CLO} \\ \lambda_{jjk}^2 \lambda_{jlm}^2 |\tilde{\mathbf{x}}_{jk}^{\text{H}} \mathbf{D}_{\delta(t)} \boldsymbol{\Psi}_j^{-1} \mathbf{D}_{\delta(t)}^{\text{H}} \tilde{\mathbf{x}}_{lm}|^2 & \text{if SLOs} \end{cases} \\ \mathbb{E}\{|\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{v}_j(t)|^2\} &= \kappa^2 \mathbb{E}\{\|\mathbf{v}_{jk}(t)\|^2\} \sum_{l=1}^L \sum_{m=1}^K p_{lm} \lambda_{jlm} \\ &+ \kappa^2 \sum_{l=1}^L \sum_{m=1}^K p_{lm} N \lambda_{jjk}^2 \lambda_{jlm}^2 \tilde{\mathbf{x}}_{jk}^{\text{H}} \mathbf{D}_{\delta(t)} \boldsymbol{\Psi}_j^{-1} \mathbf{X}_{lm} \boldsymbol{\Psi}_j^{-1} \mathbf{D}_{\delta(t)}^{\text{H}} \tilde{\mathbf{x}}_{jk}. \end{aligned}$$

The expectations for SLOs were previously derived in [6, Theorem 2] and, interestingly, it is only the second order moments that are different with a CLO. Hence, the case with the smallest variance $\sum_{l=1}^L \sum_{m=1}^K p_{lm} \mathbb{E}\{|\mathbf{v}_{jk}^{\text{H}}(t) \mathbf{h}_{jlm}(t)|^2\}$ of interference gives the largest rate for UE k in cell j . This term depends mainly on the pilot sequences and phase drifts, as seen from the expressions in Lemma 2. The only difference

is that $\tilde{\mathbf{X}}_{\ell m}$ with a CLO is replaced by $\mathbf{D}_{\delta(t)}\tilde{\mathbf{x}}_{\ell m}\tilde{\mathbf{x}}_{\ell m}^H\mathbf{D}_{\delta(t)}^H$ with SLOs. These terms are equal when there are no phase drifts (i.e., $\delta = 0$), while the difference grows larger with δ . In particular, the term $\tilde{\mathbf{X}}_{\ell m}$ is unaffected by the time index t , while the corresponding term for SLOs decays as $e^{-\delta t}$ (from $\mathbf{D}_{\delta(t)}$). Hence, we expect SLOs to provide larger user rates than a CLO, because interference reduces faster with t when the independent phase drifts mitigate pilot contamination.

By letting $N \rightarrow \infty$ in Lemma 2, one can obtain closed-form expressions for the asymptotic SINRs. It can be seen that the detrimental impact of hardware imperfections vanishes almost completely as N grows large [6, Corollary 1]. This result holds for any fixed values of the parameters δ , κ , and ξ . It is also possible to increase these parameters with N . This gives a gradual degradation of the circuits' quality at the BS and the scaling should fulfill the following scaling law.

Lemma 3. Suppose the hardware imperfection parameters are replaced as $\kappa^2 \mapsto \kappa_0^2 N^{\tau_1}$, $\xi \mapsto \xi_0 N^{\tau_2}$, and $\delta \mapsto \delta_0(1 + \log_e(N^{\tau_3}))$, for some scaling parameters $\tau_1, \tau_2, \tau_3 \geq 0$ and some initial values $\kappa_0, \xi_0, \delta_0 \geq 0$. If

$$\begin{cases} \max(\tau_1, \tau_2) \leq \frac{1}{2} \text{ and } \tau_3 = 0 & \text{if a CLO} \\ \max(\tau_1, \tau_2) + \frac{\delta_0(t-B)}{2} \tau_3 \leq \frac{1}{2} & \text{if SLOs.} \end{cases} \quad (8)$$

then $\text{SINR}_{jk}(t)$ with MRC has a non-zero limit as $N \rightarrow \infty$.

Proof. This follows along the lines of [6, Corollary 3]. \square

Lemma 3 proves that the circuit design can be relaxed as N increases. By accepting larger distortions we can achieve better energy efficiency in the circuits or lower hardware costs; see Section 4. The scaling law shows that the variances of the additive distortion noise and noise amplification can be increased simultaneously as N to some exponent. The phase-drift variance can scale only for SLOs and only logarithmically with N , since it affects the signal itself. In this case, (8) manifests a trade-off between increasing imperfections that cause additive and multiplicative distortions.

4. SCALING LAW AWARE CIRCUIT DESIGN

We now exemplify what the scaling law in Lemma 3 means for the hardware components at the BS, depicted in Fig. 1.

4.1. Analog-to-Digital Converter (ADC)

The ADC quantizes the received signal to b bit resolution. The quantization error can be included in the additive distortion noise $\mathbf{v}_j(t)$ and contributes to κ^2 with 2^{-2b} [5]. The scaling law in Lemma 3 allows us to increase the variance κ^2 as N^{τ_1} for $\tau_1 \leq \frac{1}{2}$. This corresponds to reducing the resolution of the ADC with $\frac{\tau_1}{2} \log_2(N)$ bits, which allows for substantial cost reduction. For example, we can reduce the ADC resolution by 2 bits if we deploy 256 antennas instead of one. For very large arrays, it is even sufficient to use 1-bit ADCs.

The power dissipation of an ADC, P_{ADC} , is proportional to 2^{2b} [5, Eq. (8)] and can, thus, be decreased as $1/N^{\tau_1}$. If each antenna has a separate ADC, the total power NP_{ADC} still increases with N but proportionally to $N^{1-\tau_1}$ for $\tau_1 \leq \frac{1}{2}$, instead of N , due to the gradually lower ADC resolution.

4.2. Low Noise Amplifier (LNA)

The LNA is an analog circuit that amplifies the received signal. It is shown in [8] that the behavior of an LNA is characterized by the figure-of-merit (FoM) expression

$$\text{FoM}_{\text{LNA}} = \frac{G}{(\xi - 1)P_{\text{LNA}}} \quad (9)$$

where ξ is the noise amplification factor defined in Section 2, G is the amplifier gain, and P_{LNA} is the power consumption of the LNA. For optimized LNAs, FoM_{LNA} is a constant determined by the circuit architecture [8]; thus, FoM_{LNA} basically scales with the hardware cost. The scaling law in Lemma 3 allows us to increase ξ proportional to N^{τ_2} for $\tau_2 \leq \frac{1}{2}$. The noise figure, defined as $10 \log_{10}(\xi)$, can thus be increased by $\tau_2 10 \log_{10}(N)$ dB. For example, we can increase it by 10 dB if we deploy 100 antennas instead of one.

For a given architecture, the invariance of the FoM_{LNA} in (9) implies that we can decrease the power consumption (roughly) proportional to $1/N^{\tau_2}$. Hence, we can make the total power consumption of the N LNAs, NP_{LNA} , increase as $N^{1-\tau_2}$ instead of N by increasing the noise amplification.

4.3. Local Oscillator (LO)

Phase noise in the LOs is the main source of multiplicative phase drifts. If the LOs are free-running, the drifts are modeled by the Wiener process, defined in Section 2, with variance

$$\delta = 4\pi^2 f_c^2 T_s \zeta \quad (10)$$

where f_c is the carrier frequency, T_s is the symbol time, and ζ is a constant that characterizes the quality of the LO [9]. Moreover, the power dissipation P_{LO} in an LO is directly coupled to ζ , such that $P_{\text{LO}}\zeta \approx \text{FoM}_{\text{LO}}$ where the FoM value FoM_{LO} depends on the circuit architecture [9, 10] and naturally on the hardware cost. For a given architecture, we can increase δ and, thereby, decrease the power P_{LO} . The scaling law in Lemma 3 allows us to increase δ proportionally to $(1 + \log_e(N^{\tau_3}))$ when using SLOs. Hence, the power dissipation in the LOs can be reduced as $\frac{1}{1+\tau_3 \log_e(N)}$. This reduction is only logarithmic in N , which stands in contrast to the $1/\sqrt{N}$ scalings for ADCs and LNAs (with $\tau_1 = \tau_2 = \frac{1}{2}$). Since linear increase is much faster than logarithmic decay, the total power NP_{LO} with SLOs increases almost linearly with N . Note that no scalings are allowed when having a CLO.

The LO variance formula in (10) gives other possibilities than decreasing the circuit power. In particular, one can increase the carrier frequency f_c with N by exploiting the scaling law in Lemma 3. This is interesting because massive

MIMO has been identified as a key enabler for operating in millimeter wave bands, in which phase noise is more severe since the variance in (10) increases as f_c^2 . Fortunately, massive MIMO has an inherent resilience towards phase noise.

5. NUMERICAL EXAMPLE

The analytic results are corroborated by simulating a scenario with 16 cells and wrap-around to avoid edge effects; see Fig. 2. Each square cell is 250×250 meters and divided into 8 virtual sectors; each sector contains one uniformly distributed UE (with minimum distance 35 meters). Each sector has an orthogonal pilot sequence from a DFT matrix [6], but the same pilot is reused in the same sector of other cells.

The channel attenuations are $\lambda_{jlk} = 10^{s_{jlk}-1.53}/d_{jlk}^{3.76}$ where d_{jlk} is the distance in meters between BS j and UE k in cell l and $s_{jlk} \sim \mathcal{N}(0, 0.25)$ is a realization of the shadow-fading. The transmit powers are $p_{jk} = -47$ dBm/Hz, the thermal noise power is $\sigma^2 = -174$ dBm/Hz, $B = 8$ is the pilot sequence length, and the coherence block is $T = 500$.

The achievable sum rate is shown in Fig. 3 for a system with either ideal hardware or hardware imperfections given by $b = 8$ bit ADCs, 2 dB noise figure in the LNAs, and LOs with a phase noise variance of $1.6 \cdot 10^{-4}$. This corresponds to $\{\kappa_0, \xi_0, \delta_0\} = \{2^{-8}, 10^{0.2}, 1.6 \cdot 10^{-4}\}$ when we scale the hardware imperfections with N as described in Lemma 3.

We see that the throughput is reduced by hardware imperfections. The loss is larger when the imperfections are increased with N , but the difference essentially vanishes as $N \rightarrow \infty$ if the scaling law for SLOs in Lemma 3 is satisfied. The throughput loss is large when the scaling law is not followed. We observe that SLOs provide higher throughput than a CLO. This is because parts of the interference average out.

6. CONCLUSION

Massive MIMO systems are prone to hardware imperfections in ADCs, LNAs, and LOs. We have shown that these systems have an inherent resilience to such imperfections. The distortions can be increased with N , which allows the circuit power of ADCs and LNAs to increase as \sqrt{N} instead of N . The analysis shows that having a CLO is better in terms of energy efficiency and cost, while SLOs provide higher throughput.

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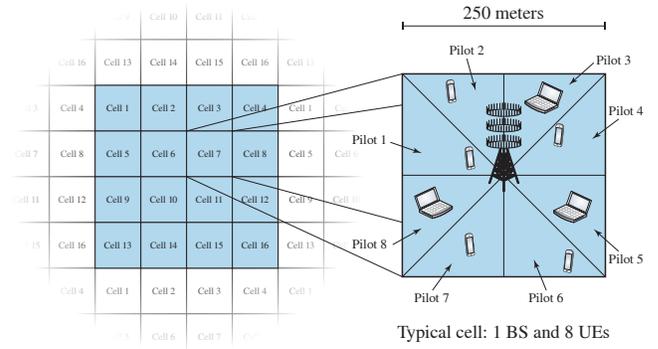


Fig. 2. The simulation scenario consists of 16 square cells with wrap-around to avoid edge effects.

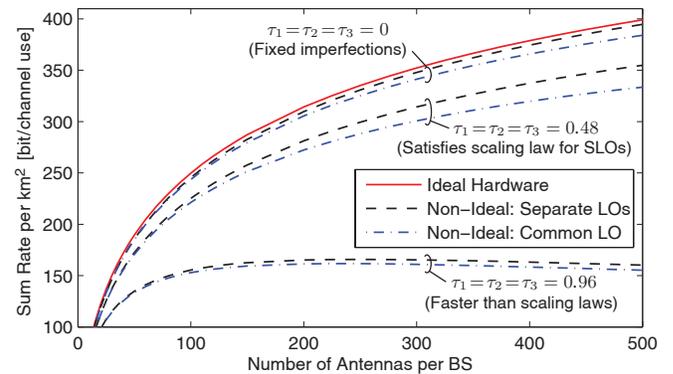


Fig. 3. Sum rate in the 1 km^2 area in Fig. 2 as a function of the numbers of antennas. We consider different hardware imperfections and scaling strategies.

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