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A New Monolithic Approach for Mid-IR Focal Plane Arrays

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ABSTRACT

Antimonide-based photodetectors have recently been grown on a GaAs substrate by molecular beam epitaxy (MBE) and reported to have comparable performance to the devices grown on more expensive InSb and GaSb substrates. We demonstrated that GaAs, in addition to providing a cost saving substrate for antimonide-based semiconductor growth, can be used as a functional material to fabricate transistors and realize addressing circuits for the heterogeneously grown photodetectors. Based on co-integration of a GaAs MESFET with an InSb photodiode, we recently reported the first demonstration of a switchable and mid-IR sensible photo-pixel on a GaAs substrate that is suitable for large-scale integration into a focal plane array. In this work we report on the fabrication steps that we had to develop to deliver the integrated photo-pixel. Various highly controllable etch processes, both wet and dry etch based, were established for distinct material layers. Moreover, in order to avoid thermally-induced damage to the InSb detectors, a low temperature annealed Ohmic contact was used, and the processing temperature never exceeded 180 ˚C. Furthermore, since there is a considerable etch step (> 6 μm) that metal must straddle in order to interconnect the fabricated devices, we developed an intermediate step using polyimide to provide a smoothing section between the lower MESFET and upper photodiode regions of the device. This heterogeneous technology creates great potential to realize a new type of monolithic focal plane array of addressable pixels for imaging in the medium wavelength infrared range without the need for flip-chip bonding to a CMOS readout chip.

1. INTRODUCTION

Imaging at mid-IR wavelengths, and in particular in the medium wavelength infrared (MWIR) region (3-5μm) is of great importance for a number of applications such as gas sensing, medical diagnostics, security and defense [1]. In order to realize an image sensor such as a focal plane array (FPA), each photodiode must be individually addressable using row and column decoding/multiplexing, so that the photo-generated signal can sequentially be transferred out from the array. State-of-the-art FPAs working in the mid-IR require the isolated array of narrow bandgap photodiodes to be hybridized with a CMOS addressing chip, is also known as a read-out integrated circuit (ROIC). Since one-to-one interconnections between photodiodes and corresponding addressing circuits are unavoidable in this approach, indium bump based flip-chip bonding techniques become nearly a necessity in order to achieve this kind of hybridization. Although the hybrid approach has successfully produced very large format and high performance imagers, the commonly used flip-chip bonding technique is not problem-free. First, as a technique that requires many processes at die level such as fabrication of bumps, substrate alignment, epoxy under-filling and substrate thinning, it will dramatically increase the cost of the manufactured FPAs [2]. Moreover, the yield and reliability of indium bump interconnections will become more and more challenging when the technology is scaled for fabrication of large format arrays. Another issue of the hybrid approach arises from the fact that most mid-IR imagers are operated under cryogenic cooling. Due to the large thermal expansion mismatch between common mid-IR sensitive materials and the silicon chips, considerable stress is thus experienced by the interconnections during thermal cycles, resulting in the possibility of connection failure or material cracking in the worst case [3].

On the other hand, monolithic integration of detectors with the ROIC can support mass production by wafer level manufacturing, and has been realized for low cost infrared FPAs based on thermal detectors [4]. However, some early attempts at monolithically integrated, photon detector based mid-IR FPAs made using metal-insulator-semiconductor (MIS) structures were soon abandoned [5][6]. The main bottleneck of these designs is the fundamental difficulty of realizing both light sensing and signal readout functions with narrow bandgap materials (e.g. HgCdTe, InSb), which present either limited signal handling capability or noise problems [7]. Furthermore, MIS detectors are not suitable for

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room temperature operation, something more and more in-demand in the field of photon detector based mid-IR FPAs as it would open up many applications.

We recently reported on a monolithically integrated switchable photo-pixel working in the MWIR range under room temperature, achieved by heterogeneous integration of InSb-based photodiodes onto a GaAs substrate containing active layers for fabricating metal-semiconductor field effect transistors (MESFETs) [8]. In this paper we will detail more material process techniques, particularly focusing on the fabrication challenges and on the solutions we developed for scaling our devices from single pixels to array format.

2. HETEROGENEOUS GROWTH AND CONTROLLABLE ETCHING

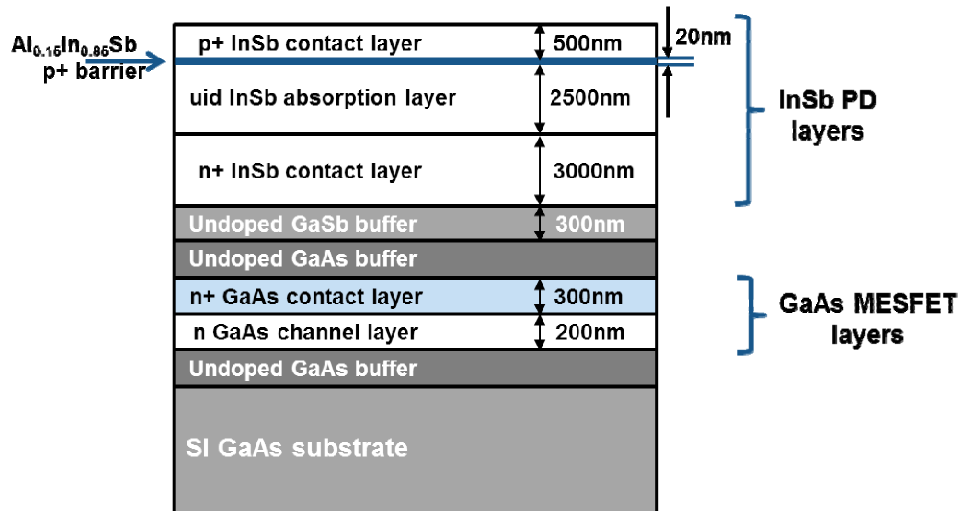

Fig.1. Diagram of the material layer structure used, highlighting the heterogeneous growth of GaAs and InSb device layers on a semi-insulating (SI) GaAs substrate.

The layer structure used for this work, as shown in Fig.1, is grown on a 3-inch semi-insulating (SI) GaAs substrate by MBE. The lower epitaxial layers were designed for implementation of an underlying MESFET to be used for switching. The MESFET includes a 200 nm thick Si doped GaAs channel layer with a donor density (N_d) of 1×10^{17} cm^{-3} and a 300 nm thick heavily doped contact layer with $N_d = 2\times10^{18}$ cm^{-3}. Between the MESFET and the photodiode active layers, a 300 nm undoped GaSb buffer was grown to allow relaxation of the strain introduced by the large lattice mismatch (14.6 %) between GaAs and InSb. Finally, a non-equilibrium InSb photodiode structure was grown, including a 20 nm $In_{0.15}Al_{0.85}Sb$ barrier layer inserted in a standard p-i-n structure. This barrier layer was grown since it has been reported to block the flow of electrons between the non-intentionally doped absorption layer and the highly p-doped contact, hence reducing the dark current and allowing photodiode operation at higher temperature [9]. The highly n-doped contact layer of the InSb photodiode was chosen to be particularly thick (3 µm) in order to further reduce the density of threading dislocations within the absorption layer.

The mesa structures of the photodiodes were defined by standard photolithographic techniques. The sensing area of the InSb photodiodes was masked by photoresist and the surrounding InSb was etched using a citric acid and hydrogen peroxide based wet chemical etching process. The InSb mesa etching offered great selectivity, larger than 30:1 (with InSb etch rates of ~20 nm/min and GaSb etch rates of 0.6 nm/min), thus the etch stopped when reaching the GaSb buffer layer. It was noted that the surface of the GaSb buffer layer showed increased roughness after exposure to the citric acid etchant, as Fig.2 (a) shows. A metal layer composed of titanium and gold (Ti 50nm/Au 150nm) was then deposited by metal evaporation and patterned by lift-off techniques to form the Ohmic contacts to the defined photodiodes. The fabrication of photodiode part was completed with surface passivation, achieved by low temperature inductively coupled

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plasma (ICP) deposition of silicon nitride (SiN_x) and with the opening of via windows on top of the Ohmic contacts by Sulphur hexafluoride (SF_6) based plasma etching in a reactive ion etching (RIE) machine.

The patterned SiN_x passivation layer, shown in Fig.2 (b), also acted as a mask for etching of the GaSb buffer. Standard photoresist developer (Microposit MF-319) was used to selectively remove the GaSb buffer layer. Because the resist developer is designed to avoid any potential attack to most of the semiconductor materials including GaAs, the underlying MESFET active layers were thus exposed with extremely high uniformity and as-grown surface condition.

Except for the wet chemical etch, we also developed a Chlorine-free low-temperature dry etch process in which we achieved low damage anisotropic etching of antimonide-based materials with either 60° positive sloped or nearly vertical etch sidewall profile [10]. In this case, the etching was monitored by a laser interferometer tool, attached to the Plasmalab 100 Inductively Coupled Plasma (ICP) 180 etching tool from Oxford instruments.

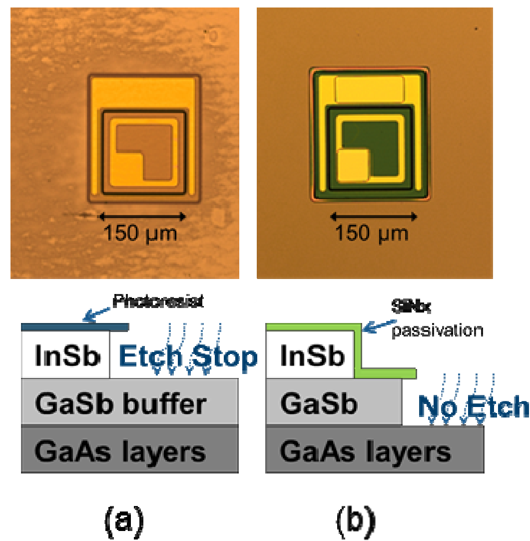

Fig.2. (a) Selective wet etching of InSb using citric acid based etchant (b) Selective wet etching of GaSb using MF-319 which leads to uniform exposure of underlying GaAs layers.

3. LOW THERMAL BUDGET MESFET FABRICATION

The fabrication of the MESFET device started with GaAs buffer etching and mesa isolation etching using a phosphoric acid based etchant. The process steps leading to the GaAs MESFET had to be achieved without exceeding a temperature of approximately 200 ˚C, since this was reported as a starting point for antimony desorption and could potentially introduce degradation to the fabricated photodiodes [11]. This implied that the highest temperature used during MESFET processing, reached during the annealing of Ohmic contacts to GaAs, could not exceed 200 ˚C as well. The use of Pd/Ge/Au layers is the only reported metallization system that can achieve good Ohmic behavior with such a low annealing temperature [12]. We therefore further developed and optimised Ohmic contact structures based on the Pd/Ge/Au system in order to minimize specific contact resistivity, and we achieved a value as small as 1.2×10^{-6} Ω cm. By introducing a superlattice-like Au/Ge stack layer into the Pd/Ge/Au contact layer structure, as shown in Fig. 3 (a), we successfully managed to control the interdiffusion of Au and Ge more precisely by adjusting the relative thickness of the Au and Ge layers in the Au/Ge stack. By comparing standard Pd/Ge/Au contacts with the ones based on the superlattice-like layers for the same total metal thickness and using the same evaporator, we observed an improvement in contact resistivity with factor of 1.5 to 2. Moreover, this developed Ohmic contact process supports annealing with an 180˚C conventional oven and hence can be automatically carried out during later resist preparation steps.

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Following definition of the MESFET source and drain contacts, another lithography step was used to define the gate pattern. The subsequent step was the gate recess etching, conducted with a citric acid based etchant. In order to precisely remove the n+ contact layer and avoid etching of the channel layer, an iterative approach was used. Using a probe station, after each iteration the current flow through the annealed Ohmic contacts was monitored, until the measured current saturated at a calculated value of approximately 30 mA with a bias voltage of 3V. Finally, in this self-aligned gate process, a common Schottky contact metal system, Ti 30nm /Pt 30nm /Au 150nm, was evaporated and then lifted off to form the gate of GaAs MESFET as shown in Fig.3 (b).

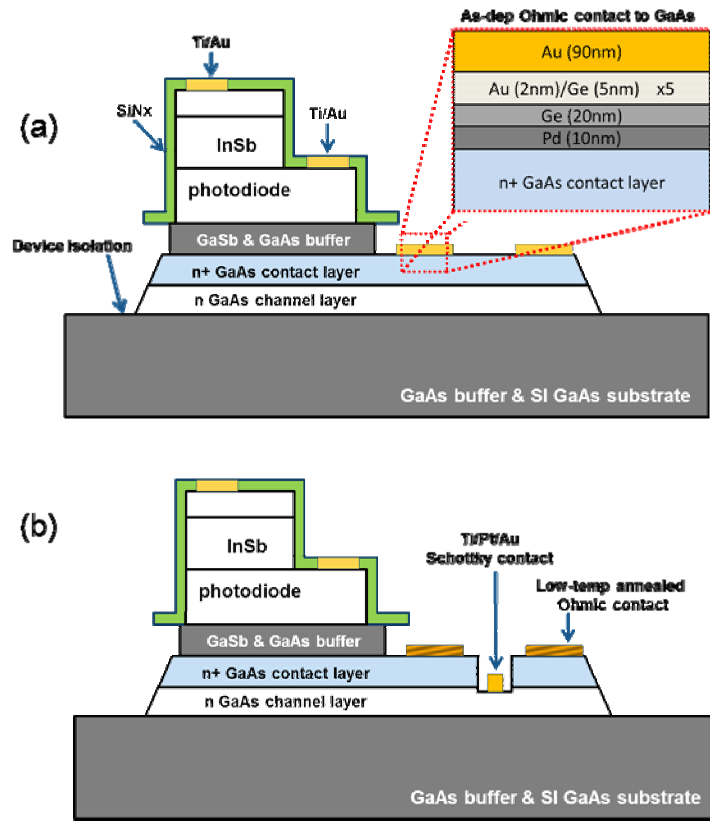

Fig.3. (a) Schematic diagram of a device after mesa isolation etching and Ohmic contact deposition, and the inset diagram shows the Pd/Ge/Au based metallization system used for Low temperature Ohmic contact formation on n+ doped GaAs layer (b) Side-by-side fabricated GaAs MESFET after gate recess etching and Ti/Pt/Au Schottky contact metal evaporation

4. PLANARIZATION AND INTERCONNECTION

The final fabrication step was to make interconnects between the fabricated MESFET and the photodiode and thus form a switchable photo-pixel device. Since there were various considerable mesa steps after etching, the interconnection metal could easily break when trying to straggle directly. As shown in Fig. 4 (a), even with more than 600 nm metal evaporated, the interconnection still cracked at the edge of the mesa due to a near vertical sidewall profile and up to 6 µm step height. To solve this problem we developed an intermediate step using polyimide to provide a smoothing section between the lower MESFET and upper photodiode regions of the device.

Firstly, a 2 µm thick Dupont PI-2545 polyimide layer was spin-cast on to the sample, followed by baking for 6 minutes on a hotplate set at 150˚C. This temperature was chosen to partially cure the polyimide layer and provide a continuous gentle ramping region at the etch mesa step edge. Then, standard electron beam lithography techniques were used to define a pattern in PMMA resist, to be used as a mask for polyimide etching. MF-319 was used as an etchant to open via holes through the polyimide where interconnections were required, e.g. from photodiode Ohmic contact to the MESFET

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Ohmic contact. As shown in Fig. 4 (b), via holes with sizes as small as 8 μm diameters were opened. More importantly, the etched via holes have positively sloped sidewall profile in all directions. Before depositing the interconnection metal, the sample was oven-baked at 180 ˚C for 2 hours in order to fully cure the polyimide and further smooth the etched edges. After this planarization process a 200nm thick Ti/Au metal can easily be used to form the interconnections in between devices without breaking. This is particularly important when making an array ofdevices, given the high number of interconnections and the multiple metal layers desired. A sketched cross-section of the completed photo-pixel device after formation of interconnections is shown in Fig.4 (c).

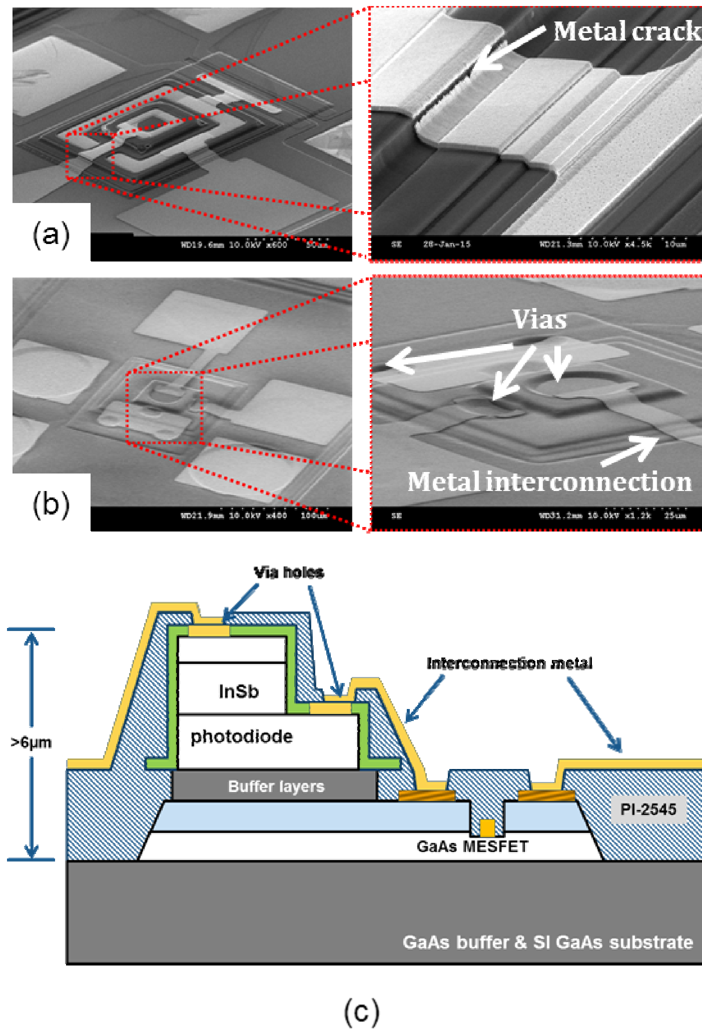

Fig.4. (a) Failed metal interconnection due to etch step height up to 6 μm (b) interconnected devices with polyimide smoothing section applied (c) a sketch of the cross-section of a completed photo-pixel device after formation of interconnections.

5. DEVICE CHARACTERIZATION RESULTS AND DISCUSSION

Fig.5 shows micrographs of two fabricated photo-pixel devices with 45 μm × 45 μm square shaped, and 45 μm diameter circular photodiode active sensing area respectively. Both devices have a depletion mode MESFET switch with 3 μm gate length and 100 μm width. In order to probe the MESFET and photodiode independently when testing the pixel device, five test-point metal pads were made including P, N, Gate, Drain and Source. Note that Drain and N pads are short-circuited by the metal interconnection, thus they are shown as a single node in the circuit diagram of Fig. 5.

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DC behavior of the complete photo-pixel device was measured using an Agilent 4155C semiconductor parameter analyzer. As shown in the equivalent circuit diagram of Fig. 5, the pad P was connected to signal ground which was 0 V. Then the voltage labeled V_{source} was swept from 0.5 V to -0.5 V while the current flow between the P pad and the Source pad was measured as a function of various gate-source voltages V_{gs}. With V_{gs} = 0 V, the MESFET switch is turned on and thus the I-V characteristic follows the photodiode I-V curve, showing a rectifying behavior (see the red trace in Fig.6 (a)). When V_{gs} is decreased so that the MESFET channel is depleted, the measured I-V characteristic shows a fall in the current as V_{source} is swept. V_{gs} = -3.5 V is required to fully pinch-off the channel and turn off the MESFET switch accordingly. Under this biasing condition, only a residue current of a few tens of nA is measured which is close to the value of leakage current flowing to the MESFET gate Schottky contact.

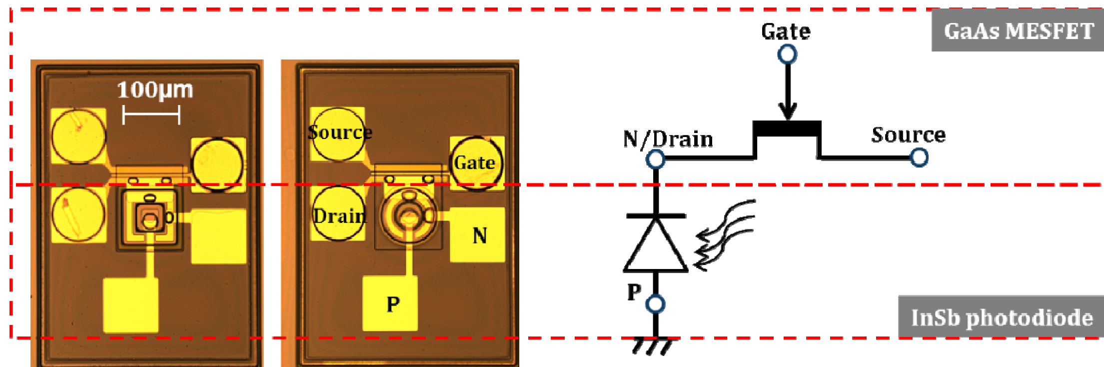

Fig.5. Optical micro graphs and equivalent circuit diagram of the monolithically integrated photo-pixel devices with 45 µm × 45 µm square shaped and 45 µm diameter circular photodiode active sensing area respectively.

We then measured the relative photo-response of the photo-pixel device under mid-IR illumination using a Bruker Vertex 70 FTIR spectrometer. The photo-response was detected using a transimpedance current preamplifier connected to the node Source and without applying a voltage between the P pad and the Source pad during the measurement (i.e. measurements were carried out at zero bias). Similarly to the DC measurement, we obtained a series of spectral scan results with various values of V_{gs} at room temperature and standard atmosphere. When the MESFET is in ON-state, the spectra we obtained spanned the wavelength range from 1.3 µm to 6.7 µm with a peak in the response at 5.1 µm, which is consistent with results from InSb photodiodes operating at room temperature [13]. The absorption of mid-IR radiation caused by CO_2 in the atmosphere is clearly demonstrated by the sudden drop of the curve at approximately 4.2 µm. As shown in Fig. 6 (b), consistently with the DC results the MESFET was capable of controlling the flow of photo-generated carriers in the photo-pixel device, as the measured photo-response decreases in amplitude when V_{gs} is decreased below zero. When the pinch-off point of the MESFET (V_{gs} = -3.5 V) is reached, the photo-response is eliminated and the entire pixel is thus isolated for readout.

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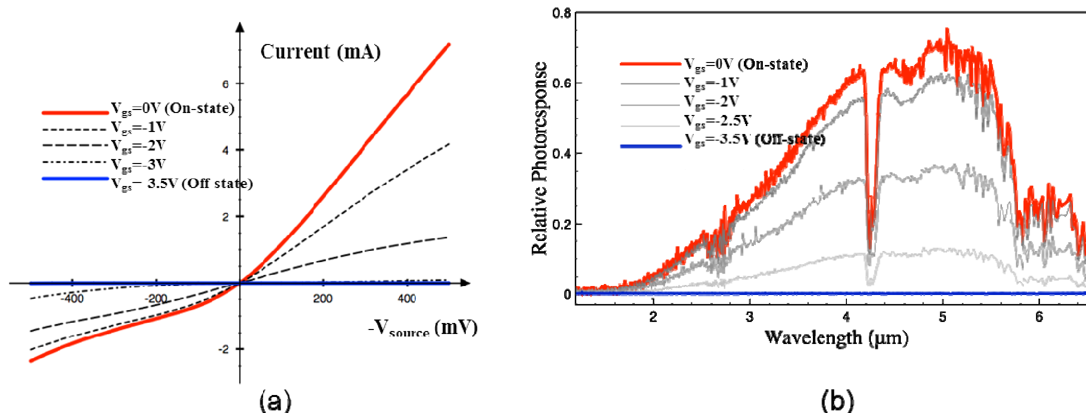

Fig.6. (a) The current–voltage characteristics and (b) the relative spectral response of a typical photo-pixel device with a 45 µm diameter circular InSb photodiode and under various gate bias conditions. The solid red line represents the results obtained when the MESFET switch is turned on while the solide blue line shows the corresponding results when the pixel is switched off.

6. CONCLUSION

We developed a sequence of successful process steps for independent fabrication of an InSb photodiode and a GaAs MESFET side-by-side on the surface of a heterogeneous grown sample. Highly controllable etching processes were developed to selectively expose underlying GaAs active layers with great uniformity. All the processes, including the Ohmic contact formation to GaAs, were achieved without exceeding 180 ˚C and thus no degradation was observed to the InSb photodiodes. Furthermore, metal interconnections between devices were realized by applying a simple planarization process, which can contribute to the formation of a complete readout circuit in an array of the pixel devices. The obtained electrical and optical characterization results have confirmed that the InSb-based photo-pixel was sensitive to mid-IR photons at room temperature, and its photo-response could be eliminated and isolated from its contacts by switching off the co-integrated MESFET.

Similarly to the current flip-chip bonding based hybrid design, this technique supports optimization of detector structures and ROICs separately and hence it can potentially realize a new monolithic approach to make FPAs working in the mid-IR range with wafer level manufacturing capability for cost reduction. So far, a number of groups have developed methods for growing various mid-IR detector structures on GaAs substrate with assistance of GaSb buffer layer and reported to have comparable detection performance as compared to those devices grown on more expensive InSb or GaSb substrates. This includes newly developed HOT detector structures based on materials such as InAsSb and type II InAs/GaSb superlattices [14][15][16]. Our process steps could thus be easily used for alternative semiconductor layer structures, improving the detection performance at high operating temperature.

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