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Optimization Of Transition-Metal Dichalcogenides Based Field- Effect- Transistors Via Contact Engineering

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OPTIMIZATION OF TRANSITION-METAL DICHALCOGENIDES BASED FIELD-EFFECT-TRANSISTORS VIA CONTACT ENGINEERING

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DEDICATION

"To my wife Maheeka, daughter Kiyara, my brother, parents and anyone who loves 2D materials"

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CHAPTER 1:GENERAL INTRODUCTION

1.1 Development of 2D materials beyond Graphene

Two dimensional(2D) materials have demonstrated a wide range of remarkable properties for applications in next generation nano-electronics. Their atomic scale thickness provides higher degree of electrostatic control than bulk materials[1], revealing the possibility for low power electronics devices[2].To date, the most widely studied 2D material is graphene due to its rich physics and potential in device applications including electronics [3, 4], spintronics[5, 6], chemical and biological sensing [7-10], nano-electromechanical systems (NEMS) [11], and energy storage [12]. However graphene does not have a band gap that limits its applications in digital logic devices. A band gap in graphene can be generated by applying high transverse electric fields in bi-layer graphene or shaping graphene into nano-ribbons. However these efforts increase the complexity for device fabrication and also lead to mobility reduction.[13]

Alternatively, another class of 2D materials known as, transition metal dichalcogenides - TMDs (such as MoS_2, $MoSe_2$ and WSe_2) have not only demonstrated many of the "graphene like" properties desirable for electronics applications such as mechanical flexibility, chemical and thermal stability and the absence of dangling bonds, but also have a substantial band gap. As the most studied TMD material to date, MoS_2 has a band gap of ~ 1.8 eV, which makes it a suitable candidate for low power digital logic devices [14]. Just like graphene, TMD materials can be exfoliated from its bulk crystals by mechanical exfoliation method due to the weak van der Waals interactions between layers.

1.2 Challenges in 2D materials based electronics.

1.2.a) Understanding the main challenge

In the early studies of "graphene like" 2D semiconductor, the carrier mobility of few layer and monolayer MoS_2 FETs fabricated on Si/SiO_2 substrates was calculated to be in the range of 0.1-10 $cm^2V^{-1}S^{-1}$.This is orders of magnitude lower than the mobility of graphene. Moreover, it substantially lower than the phonon-limited mobility in bulk MoS2 crystals (which is on the order of 100 $cm^2V^{-1}S^{-1}$) [15-18].In one study byRadisavljevic*et al.* the mobility of monolayer MoS2 was imprved significantly using HfO_2 high -κ dielectric top gating. This was attributed to the screening of Coulomb scattering and modification of Phonon dispersion[19]. In addition to higher mobility, MoS_2 FETs have demonstrated high ON-OFF ratio(10^8), near ideal sub threshold swing (74 mV/decade) and outstanding mechanical flexibility , opening up its ability to use in low power and high performance flexible devices [19-21]. Furthermore MoS_2 FET can be used in novel applications such as as energy harvesting [22, 23] and optoelectronics [24, 25] devices. However, it is not completely clear, to what degree the reported charge impurity screening and phonon dispersion modificationcontributesto the mobility improvement. On the other hand, a studiesbyGhatak*et al.* and Lee *et al.* suggest that the low mobility values reported for MoS_2 FETs fabricated on Si/SiO_2 are largely due to the charge- impurity-induced electron localization [16] and Schottky barrier forms at MoS_2 /metal contact interface respectively [26]. A study by Lin *et al.* shows that mobility increase in polymer electrolyte covered monolayer MoS_2 FETs can be attributed partially to the reduction of contact resistance and partially to the enhancement of the channel mobility [27].

1.2.b) Contact engineering as a solution

The strength of semiconducting 2D TMDs such as MoS_2, $MoSe_2$ and WSe_2 as channel materials lies in their large bandgap, which results in a very high ON-OFF current-ratio and excellent electrostatic integrity [14]. However, large bandgap semiconductors are also known to have difficulties forming Ohmic contacts with metal, while low resistance Ohmic contacts are essential in optimizing the device performance of FETs.

There are typically two types of low resistance Ohmic contacts that can be made between a semiconductor and a metal, (a) very low barrier Schottkycontacts and(b) tunneling contacts. Ideally, an Ohmic contact can be formed if the SB height is zero or negative. For an n-type semiconductor such as MoS_2 and $MoSe_2$, the work function of the metal must be close to or smaller than the electron affinity of the semiconductor to form Ohmic contacts. Bulk MoS_2 as a n-type semiconductor has an electron affinity of ~ 4 eV, and that of atomically thin MoS_2 is expected to be even smaller due to the increased band gap[26, 28]. However, the work function of most commonly used electrode metal ranges from slightly over 4 eV for Al andTi to over 5 eV for Pd and Ni.

In addition, a good electrical contact material also requires high conductivity, chemical, thermal, electrical stability. It is extremely difficult to have stable electrical properties if low work function metals (such as Ca, which has a work function of 2.9 eV) are used, since low-work-function metals oxidize easily, which severely degrades their electrical characteristics. Therefore, it is challenging to find a suitable metal to form very low barrier Schottky contacts to n-type TMDs. For a p-type semiconductor such as WSe_2, the work function of the metal must be close to or larger than the sum of the electron affinity and the bad gap energy, which is similarly

challenging. Although relatively good contacts have been made between the p-doped monolayer WSe_2 and the high work function Pd, a non-negligible SB still appears to be present [29]. Furthermore, the Schottky barrier in reported MoS_2 FET devices with various metal contacts appears to be quite insensitive to the work-function of the contact metal, suggesting the presence of Fermi level pinning (or at least weak pinning) likely due to the metal induced gap states at the metal/MoS_2 interface [30].

1.3 Methods to reduce contact resistance

1.3.1) Metal contacted MoS_2 FETs with Ionic liquid gating.

Aconvenient way to make low -resistance contacts is to make narrow Schottky junctions, where the contact resistance is determined by the tunneling current. As our first approach to improve the contacts of MoS_2FETs,we used Ionic Liquid (IL) gating which forms an electric double layer with high capacitance at MoS_2/metal interface. As a result, IL gated MoS_2 FETs demonstrate high tunneling efficiency and thus low contact resistance due to the strong band bending occuring at MoS_2/metal interface. We successfully observed mobility enhancement, higher ON-OFF ratio for both electrons and holes, near ideal sub-threshold swing and phonon limited behavior.

1.3.2) Highly doped graphene as low-resistance contact material for MoS_2 FETs.

According to Yu *et al.* the work function of graphene can be tuned by electric field effect within the range of 4.5 -4.8 eV for single layer and 4.65-4.75 eV for bilayer graphene using a Si back gate with a 300 nm thick SiO_2 dielectric layer, making graphene an attractive material for low contact barrier electrodes [31]. However, significantly larger range of work function tunability will be needed for achieving true Ohmic contacts for both electrons and holes in

graphene/TMD junctions due to the large band gap of the TMD materials. To resolve this issue, we used ionic liquid gates to more effectively tune the carrier density (thus the work function) of graphene. An ionic liquid gate can induce a high carrier density exceeding 10^{14} cm^{-2} in graphene, which is more than an order of magnitude higher than using a conventional solid-state gate dielectric [32]. Atomically sharp interfaces between graphene and hydrogenated Si as well as between graphene and MoS_2 have been achieved, and a modulation of SB at the graphene/Si junction by a gate voltage has also been demonstrated [33, 34]. The nearly ideal diode ideality factor observed in graphene/Si junctions strongly suggests that high quality graphene/semiconductor contacts free of interface states are achievable using graphene as a contact-electrode material [33].

Furthermore we used Hexagonal Boron Nitride (h-BN) as a bottom dielectric and channel passivation material. The main reason of the channel passivation ids to selectively dope graphene contacts by protecting the channel. h-BN is used due to its atomically smooth surface, which is chemically inert and relatively free of charged impurities and charge traps [35-37].

1.3.3) 2D/2D contacts with slightly doped channel.

For realistic device applications, more permanent, air and thermally stable Ohmic contacts with lower contact resistance are needed. In this respect,we used degenerately doped 2D electrodes along with lightly doped 2D channel. Nb is used as p-dopent and is bound with covalent bond which provides higher air and thermal stability[38]. 2D /2D junctions can be formed with atomically smooth surfaces by Van der Waals assembly of 2D crystals[39, 40].In this study the .01% Nb ($Nb_{0.0001}$ $W_{0.9991}Se_2$) doped $WSe_2$was used as the channel material and .5% ($Nb_{0.005}$ $W_{0.995}Se_2$) degenerately doped samples for contacts. The obtained transport

characteristics include a two probe field-effect mobility of ~ 180 $cm^2V^{-1}S^{-1}$ at room temperature, which increases up to around 700 $cm^2V^{-1}S^{-1}$ at 10 K. We also observed near 10^8 ON/OFF ratio, intrinsic phonon limited behavior and subthreshold swing of 700 mV/dec at room temperature.

CHAPTER 2:EXPERIMENTAL METHODS

In order to achieve higher device performance and intrinsic transport properties for TMDs based FETs, we employed novel contact engineering strategies. This chapter is describes techniques that were used to fabricate devices with each different contact engineering strategies. In addition to standard FET fabrication techniques, we have used a home-built transfer stage to fabricate TMD FETs with 2D contacts.

2.1 Substrate cleaning

The first of the device fabrication process is to prepare clean Si/SiO_2 substrates.For this purpose, degenerately doped Si wafers with 270-290 nm thick$SiO_2$are used as the substrates. When mechanically exfoliated TMDs are transferred on to these substrates, the above mentioned oxide thickness range provides high visibility for monolayer or few layer samples. To remove the particulates on the Si/SiO2 substrates, they were sonicated in Isopropyl Alcohol (IPA) andacetone for 10 minuteseac, where the ultra sonic waves are used to loosen the particles adhering to the surfaces.

Once this is done, thesubstrates are annealed in the annealer at 600^0C for 10 minutes in forming gas(90% Ar and 10% H_2) and cooled down gradually. This helps to eliminate organic residues on the substrate surfaces and thus to thoroughly clean the substrate.

2.2 Sample fabrication with mechanical exfoliation

Next step is to synthesis TMD materials. Ultimately we measure the intrinsic transport properties of TMD channel materials after improvements in contacts. To make sure we get the best TMD channel material, it's necessary to produce clean, uniform high quality

samples.TMDcrystals are composed of vertically stacked layers which are interacting weakly and held together by Vander Waals interactions.[2]

TMDs can be exfoliated into single or few layers by using mechanical exfoliation method.[41] First we place a tiny piece of 2D material on the ultralow residue tape (Ultron system R1007 tape).Then another piece of tape is placed on 2D material and press it using an eraser or thumb.[41]Keeping the bottom tape fixed, slowly peel off the top tape maintaining an angle. Repeat this several times until MoS_2 is thinner enough.[41] Once you have thin enough flakes on the tape, transfer them onto Si/SiO_2 substrates. This will give flakes with wide range of thickness distribution.We can look for samples with desired thickness range under the optical microscope.[41] MoS_2 mono-layers were transferred to degenerately doped silicon substrates covered with 270-nm-thick SiO_2 (Fig. 2.1).

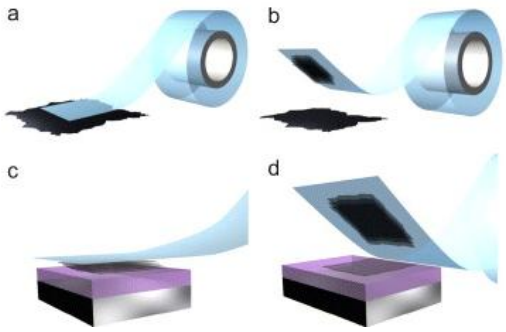


Figure 2.1 : Mechanical exfoliation of 2D material crystals.

To further characterize the MoS_2samples , they are scanned with non contact mode AFM (Park System XE-70) to understand the quality of the sample surface and measure the sample thickness.AFM is a powerful characterization tool that can provide resolution down to sub Å scale measurements. Figure 2.2 shows an optical micrograph of MoS_2 sample and it's further characterized AFM image with sample height distribution.

(a)

(a) (b)

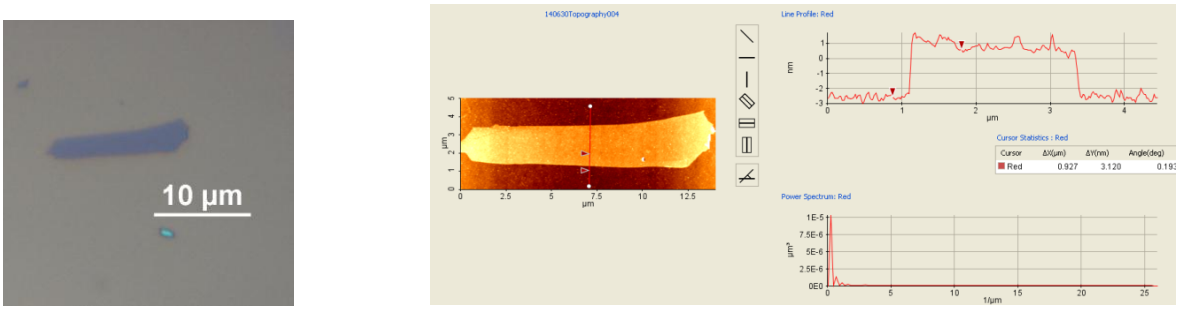


Figure 2.2: (a) A bilayer MoS_2 sample on SiO_2 substrate. **(b)** An AFM image of a sample and it's thickness distribution.

Transferring TMDs directly on to Si /SiO_2substrate was used in the early stage of our research efforts(Chapter 3).Over the time hexagonal Boron Nitride (h-BN) was used as a bottom dielectric to provide an atomicallysmooth surface that is chemically inert and relatively free of charged impurities and charge traps.[42]Furthermore, h-BN was used as a channel passivation layer to selectively dope graphene contacts that will be discussed in detail in chapter 4.In order to transfer h-BN and 2D contacts (will be discussed in chapter 5) we needed a method that can transfer 2D material to a targeted place on the substrate.This challenge was addressed by dry transfer method.A home built setup was used for this purpose and step by step explanation is presented below.

2.3 Dry transfer method

Dry transfer method is extremely important technique which allows to fabricate devices that needed multiple 2D material transfer steps. For instance a typical 2D/2D contacted devices (which will be covered in chapter 6), need this method to transfer h-BN bottom dielectric, the TMD channel, The top passivation and 2D contacts for both drain and source.To transfer a 2D

material on to a substrate, we first have to exfoliate the sample on to a Polydimethylsiloxane (PDMS) patch. PDMS is asilicone based polymer, and for this transfer procedure it's used as an intermediate material for transferring process. This means 2D materials are exfoliated on to PDMS and then transferred on a substrate.

2.3.1) Preparing PDMS.

In-order to make high quality devices it is crucial to use freshly made PDMS. By doing so, we make sure that PDMS residue won't be introduced to the samples. PDMs is prepared using Sylgard 184 silicone elastomer base and curing agent. 7g of elastomer base is added to a freshly chosen plastic cup. Then 0.7 g of curing agent is added and stir using fresh, clean stick until they mixed well. This mixture is placed inside the vacuum for 20 minutes until all the bubbles are gone from the mixture.

Then use a brand new wafer, pour the mixture in to the center and spin coat it with 350 rpm for 35 seconds. Then the pre-coated PDMS should be backed on a hotplate for 80^0C for 30 minutes and another 30 minutes to cool down.

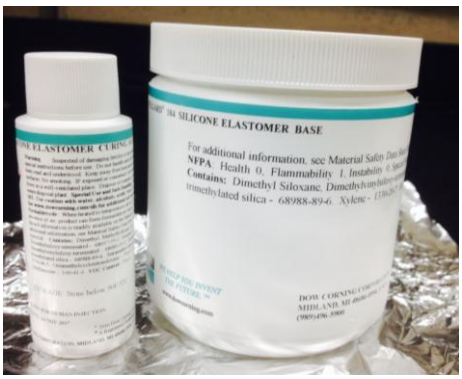


Figure 2.3: Sylgard 184 silicone curing agent and elastomer (respectively from left to right)

2.3.2) Preparing for the transfer.

First the 2D material that we want to transfer has to be exfoliated on to blue tape. Once it was exfoliated up to desired thickness, we look it under the optical microscope and choose a better area. Then we cut PDMS into small patches and place couple of patches on the area of the blue tape that already selected. Then put back the backing of the blue tape and press gently .Transfer the PDMS patches on to a glass slide and search for better samples under the microscope.

Once you find the patch with desired sample, it should be placed on a glass slide(Figure 2.4) along it's shorter edge. This will help to land the sample easily on the targeted position. The farthest end of the PDMS edge from the sample is mount to the glass slide with a scotch tape.

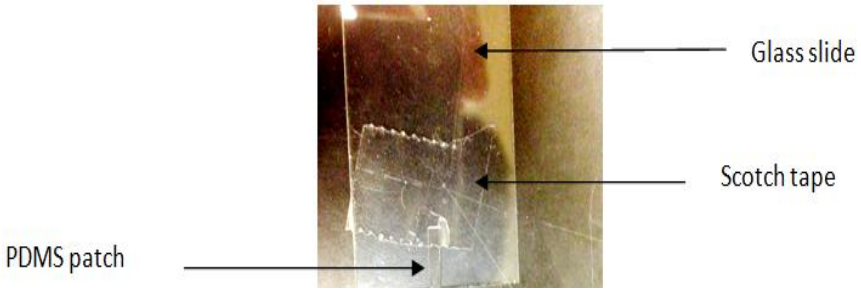


Figure 2.4: A PDMS patch mount on a glass slide and ready to transfer.

2.3.3) Transferring the samples onto substrate.

For transferring we use a transfer stage with a micromanipulator. The transfer stage contains the microscope , a sample stage and a micromanipulator. The slide with the sample patch should be mount on to the micromanipulator as facing the sample towards the sample stage. The substrate should be mount on the stage. Then the glass slide brings on top of the substrate and lower towards the substrate looking from the microscope. When the sample on PDMS is so close to the substrate then we should lower the sample on PDMS patch slowly until

(a) (b)

it completely land on the desired target. Finally we lift the glass slide very slowly until it completely off from the substrate. Now we can have a look under the microscope the sample that we have transferred.

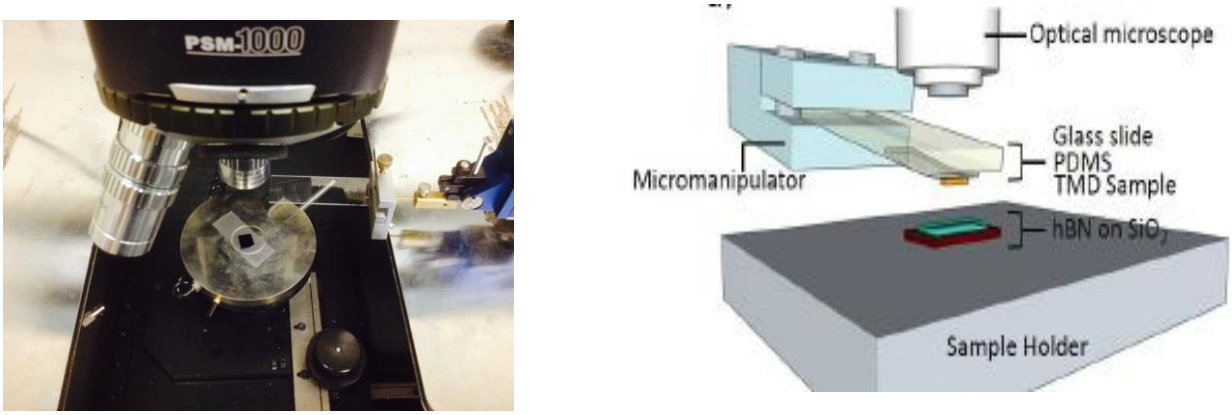


Figure 2.5:(a) A real image of the transfer stage set up.**(b)** A schematic diagram of the ready to use transfer stage.

The following figure elaborates the transfer of each 2D material components in fabricating a 2D/2D contacted device.

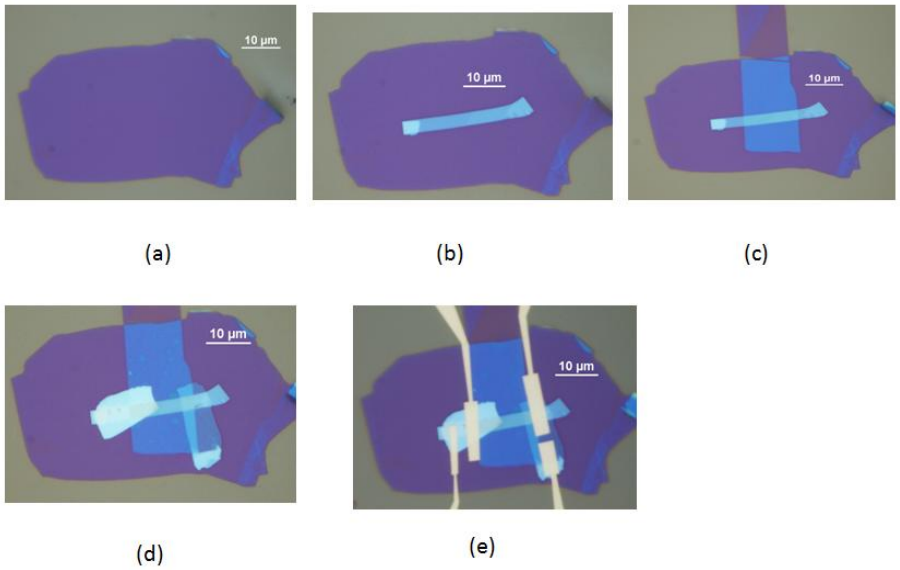


Figure 2.6: The steps of fabricating 2D/2D contacted device. **(a)** Bottom h-BN dielectric transferred on SiO_2 substrate. **(b)** $Nb_{0.0001}$ $W_{0.9991}Se_2$ transferred on h-BN **(c)** Top h-BN

passivation for the channel **(d)** Transferring degenerately doped contacts ($Nb_{0.005}$ $W_{0.995}Se_2$) as drain and source electrodes **(e)** Fabricating metal electrodes for the 2D/2D contacted device.

2.7 Electron beam lithography and metal deposition

Electron beam (e- beam) lithography is a widely used, simple and reliable technique to fabricate nanodevices. A mask (resist) is used to cover the substrate which contains the sample and electron beam is used to pattern customized electrodes. Exposing the resist to electron beam changes the solubility of the resist in the exposed area.

Bilayer resist system is used in our standard e-beam lithography procedure. Two PMMA layers we use are 495 A4 and 950 A2, which have different molecular weights (represented by 495 /950) and concentrations (A4/A2).As the top layer, 950 A2 is used. This is mainly due to its less sensitivity to electron beam since it has higher molecular weight.This creates an undercut profile. PMMA is coated on the substrate using spin coating. A program with 4000 rpm for 45 seconds was used for this purpose. The first PMMA layer to coat is 495 A4which gives around 220 nm of thickness while 950 A2 gives around 80 nm.After each coating step, the substrate is baked in 180^{o}C for 5 minutes.Then silver paint is applied close to the sample area, to fine focus the system before writing the pattern. NPGS (Nano Pattern Generating System) software is used to design and customize the pattern that we need to write. The written patterns have to be developed afterwards. This means the resist will be removed only from the area that was exposed to electron beam, following the designed customized pattern. After writing the pattern using e beam lithography, the very next step is developing, which removes the resist from area that was exposed to e-beam. Developing involves soaking the e-beam patterned sample in 1:3 mixture of MIBK:MEK. Finally the sample is observed under the microscope and take images in different magnifications.

Then we deposit Ti/Au combination on the exposed area using standard metal deposition process. Finally we remove the remaining resist by soaking the sample in Acetone which is called lifting off, and end up with having metal electrodes as we designed.The whole purpose of this procedure is to create electrodes on the TMD samples which are on the Si substrate and construct FETs.

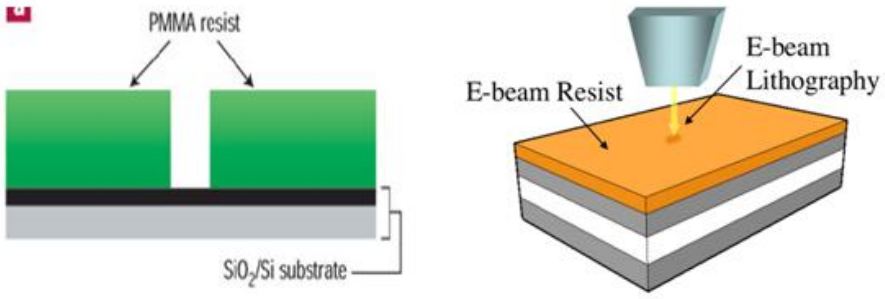


Figure 2.7:(a) Schematic diagram of PMMA resist on SiO_2 /Si substrate. **(b)** E beam lithography to create patterns on the resist.[43]

2.7.1)The main steps of E-beam lithography process

Film preparation

1. Substrate cleaning example procedure (for Silicon substrate):

   (a) Sonicate in Acetone for 20 min;

   (b) Sonicate in IPA for 10 min;

   (c) Annealing at 600^0C for 10 minutes. (Add Ar gas for 2 minutes during this time)

2. Substrate bake: 150^o C for 30 minutes on hotplate
3. PMMA spin: refer to the specific PMMA data sheet (e.g., 495 PMMA A4 3000 rpm film thickness ~ 200 nm)

4. Film bake: refer to the specific PMMA data sheet (e.g., 180^{o}C for 1~1.5 min on hotplate for 495 PMMA)
5. Make a scratch on the sample surface as a reference mark for e-beam adjustment and patterning.

Specimen and SEM Setup

1. Load the sample into the SEM.
2. Optimize sem.
3. Focus on gold particles.
4. Move to appropriate area.
5. Focus on silver particle for fine tuning.
6. Using appropriate program write the pattern on the substrate.

2.7.2) Pattern Development

1. Check the PMMA Data sheet for proper development conditions. Below are several sample procedures for your references. Developer Time Conditions

   MIBK:IPA 1:3 70 seconds for more sensitive features

   MIBK:IPA 1:1 70 seconds for larger features (stronger developer)

   IPA 20seconds
2. Dip the sample into the proper developer solution and swirl constantly for a desired period of time (e.g., 70 seconds).
3. Dip the sample into pure IPA solution or DI water and swirl for 20 seconds to stop the reaction.

4. Quickly wash the substrate with water and dry with Nitrogen gas. Decrease the flow of Nitrogen gas if necessary (for sensitive features).
5. Pour the developer and IPA into proper waste storage containers under the hood.
6. Check the pattern under the optical microscope.

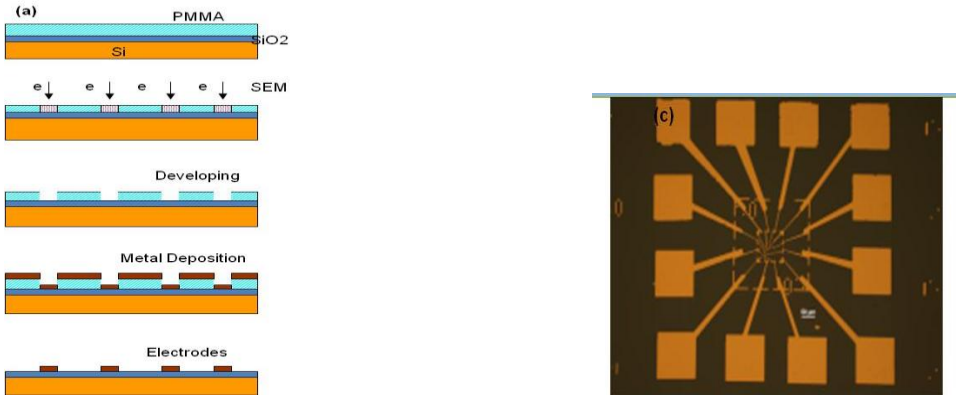
2.8) Metal Deposition

The metal deposition allows to form metal electrodes on the patterns we wrote using lithography. We need to make sure that metals we are using have smaller work functions in order to get good n channel contacts with MoS_2 sample since it forms smaller Schootky barrier.

For metal deposition,Termescal model BJD-1800 E-beam evaporator was used. This includes high vacuum chamber, pumping system (mechanical pump, diffusion pump and automated interlocks) and sources to be targeted by E-beam.[44] In this particular equipment we have 6 pockets to hold sources. The samples should be loaded in to the system and have to wait round 2 hours until the system reaches the pressure lower than 2 X 10^{-6} torr to start the deposition. For out samples we usually use 10nm Ti and 40nm Au as deposition metals. The rate of deposition is used as 1 Å/s for both materials.

Figure 2.8: BJD 1800 E-beam evaporation system for metal deposition[44]

The source metal is evaporated in vacuum and vapor particles move towards the target, condensed back and deposit.[45]Following figure shows the schematic diagrams to illustrate the processes with respect to electron beam lithography and metal deposition. In the next image, the electrodes are shown in after lift-off process using acetone.



(a) **(b)**

Figure 2.9: The schematic diagrams show the integrated processes with electron beam lithography and metal deposition. **(a)** Starting the coating of PMMA to lift-off process. **(b)** The actual electrodes picture ready for electric measurement.

2.8.a) Annealing process

To remove any absorbed impurities from the 2D materials and improve the qulaity of performance, thermal annealing is used. In device fabrication, this helps to reveal the true electrical transport properties of the channel and improve the contacts. In our fabrication process, we used two types of annealing procedures. To clean the Si substrates, the maximum temperature of 600^{o}C for 10 minutes with purging gas (10% Ar and 90% H_2) were used. For this purpose (Ulvac Mila 5000 equipment)was loaded with the Si substrates , turn on the vacuum pump and purge with purging gas for three times. When the annealer starts running ,it reaches the maximum temperature of 600^{o}C and stays there for 10 minutes. During this window, we let

purging gas in for 2 minutes. After staying 10 minutes, the annealer starts to drop its temperature gradually and reach the room temperature. This completes the annealing process for Si substrates. We usually perform this prior to use the Si substrates.

When it comes to anneal fabricated TMD FETs, we make sure to use the maximum temperature of 250^{o}C for 30 minutes. In this case we don't let the purging gas in when it reaches the maximum temperature.

Figure 2.12: Ulvac Mila 5000 annealer

2.9) Doping methods.

After devices are fabricated ,different doping methods are used as contact engineering approach to improve device performance and achieve intrinsic transport properties.

2.9.1) Ionic Liquid (IL) doping.

Ionic liquid is binary organic salts that can foam an electric double layer at IL/Channel interface[46]. This acts like a parallel plate capacitor. Once the devices are fabricated, small droplet of DEME-TFSI IL (Supplied from Sigma Aldrich 727679) is applied using micro-manipulator. In order to apply IL gating efficiently we make sure that the IL drop covers the ing area (The contact area generally) with minimum spreading and the gate electrode with the maximum spreading. In the below we have a schematic diagram and a real image to demonstrate how it looks like after IL gating is applied.

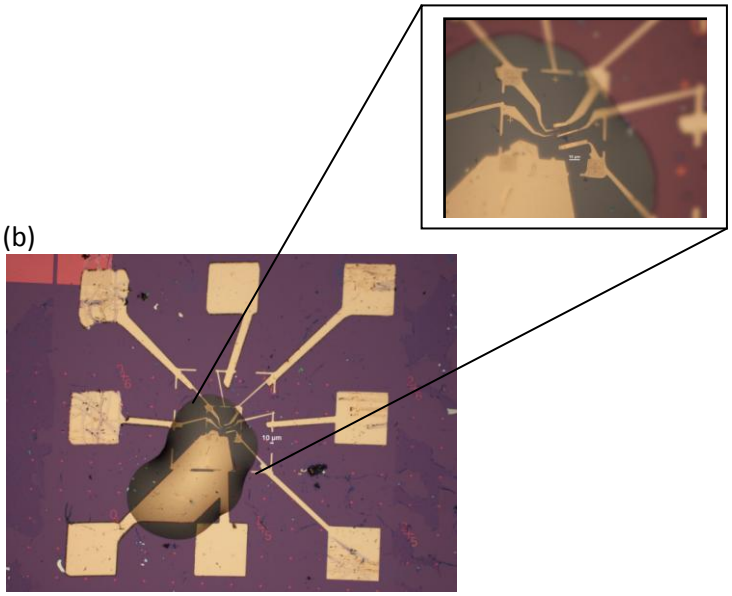


Figure 2.11: An optical micrograph of a metal contacted MoS_2device after application of IL gating at 10X and 50 X magnification.

2.9.2) Benzyl Vioilogen doping method

Air stable doping of 2D materials is really important for electronic and optoelectronic applications as well as to understand the intrinsic channel bahvior by improving the contacts.[47] Benzyl Viologen (B.V) is a surface charge transfer donor which can be used to dope graphene or other TMDs. In our study we use B.V to highly dope the electrodes of grapehe contacted MoS_2 FETs. According to the literature MoS_2 can be doped up to the degenerate doping level using B.V doping method.[47]This method is even attractive since the B.V can easily spin coat on the device and can be reversibly removed using Toluene.[48]

The B.V solution is prepared as follows. First 8 mg of Benzyl Violgen dichloride (powder) is measured and put in to a clean small bottle. Then 2.5 ml of De-ionized water (D.I

Water) is added in to the same bottle. Then the mixture of B.V powder and D.I water is shaked gently until they mixed properly. Once the B.V powder is dissolved completely the final solution looks colorless(Figure 2.10 (a)).Then 2.5ml of Toluene is added to the prepared B.V solution using a pipette. Toluene doesn't dissolve with the prepared B.V mixture, so it forms as a layer on Top.(Figure 2.10(b)).Then 50 mg of Sodium Borohydride ($NaBH_4$) is added to the solution (Figure 2.10(c)).This first enters to the Toluene layer and start to react with the B.V solution in the bottom. This is kept for a day and the top Toluene layer is extracted by a pipette and put in a clean container.(Figure 2.10 (d)).For a B.V solution prepared with above mentioned recipe, we will get a B.V solution with 60mM concentration.

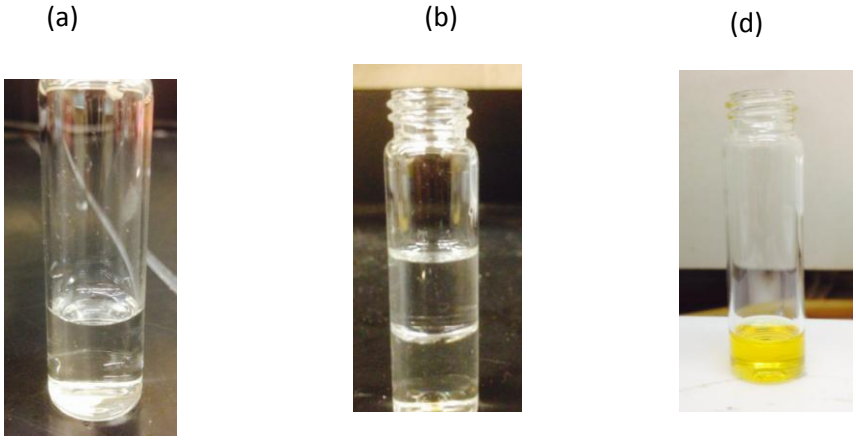
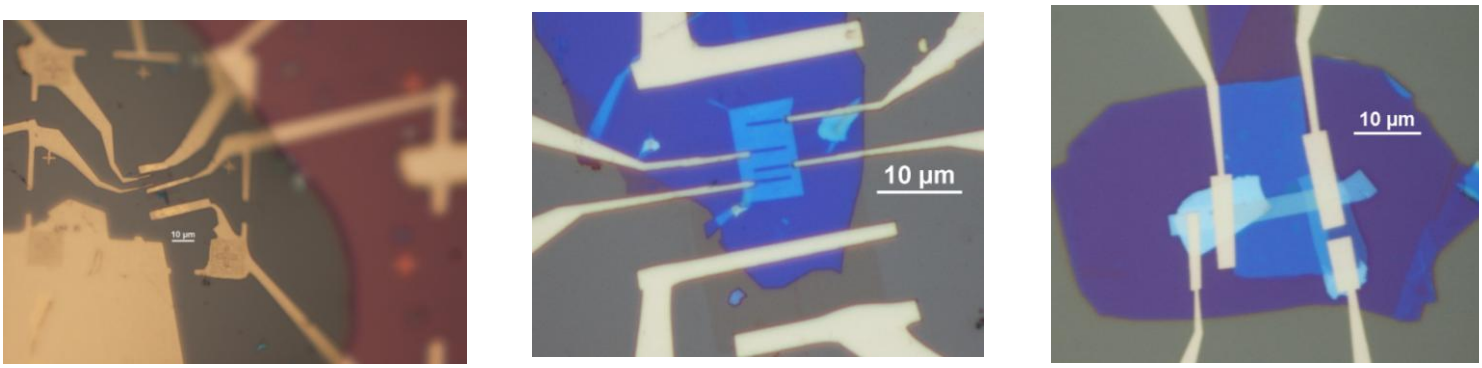


Figure 2.10: The step by step preparation process of B.V solution.**(a)** B.V powder is mixed with D.I water **(b)** After Toluene is added **(c)** Right after $NaBH_4$ is added **(d)**After extracting Toluene layer with B.V which is ready to use for doping

2.10) The summary of devices types that are fabricated for each project



(a) (b) (c)

Figure 2.13 : The type of contact engineering approaches used to improve device performances. **(a)** Metal contacted MoS_2 FET with IL gating **(b)** The highly doped graphene contacted MoS_2 FET with h-BN passivation **(c)** 2D/2D contacted WSe_2 FET with h-BN passivation.

CHAPTER 3 : IMPROVED PERFORMANCE IN FEW LAYER MOS_2 FETs VIA IONIC LIQUID GATING.

3.1 Introduction

In the quest for flexible electronics in the "post-silicon" era, graphene has attracted much attention due to unsurpassed carrier mobility and high thermal conductivity,[49-52] combined with excellent chemical and thermal stability down to the nanometer scale.[53] The major drawback is the absence of fundamental band gap, which makes semimetallic graphene unsuitable for conventional digital logic applications. Sustained efforts to engineer a band gap in graphene have either caused severe mobility degradation or require prohibitively high bias voltages.[54-57]

Molybdenum disulfide (MoS_2), a layered transition-metal dichalcogenide (TMD), has emerged as a viable alternative to graphene, as it combines a semiconducting gap with mechanical flexibility, chemical and thermal stability and absence of dangling bonds. The single-layer MoS_2 consists of a molybdenum monolayer sandwiched between two sulfur monolayers. The fundamental band gap changes from an ≈1.2 eV wide indirect gap in the bulk to a direct gap of ≈1.8 eV in single-layer MoS_2.[14, 58] Similar to graphene, single MoS_2 layers can be extracted from bulk crystals by a mechanical cleavage technique due to relatively weak interlayer interaction with an important van der Waals character.[15] Besides conventional field effect transistors (FETs), the use of MoS_2 has been proposed for applications such as energy harvesting[22, 23] and optoelectronics.[24, 25] Recently, integrated circuits based on MoS_2 transistors have also been demonstrated, which is a significant step toward the application of MoS_2 in high-performance low-power nanoelectronics.[59] However, the room temperature

carrier mobility in single- and few-layer MoS_2 FETs fabricated on Si/SiO_2 substrates was found to be very low, typically in the range of 0.1 -10 $cm^2V^{-1}s^{-1}$.[12, 17, 21] This mobility is not only orders of magnitude lower than that of graphene, but also substantially lower than the phonon-limited mobility in the bulk system,[15-18, 30] which is of the order of 100 $cm^2V^{-1}s^{-1}$. The interface between the MoS_2 channel and the SiO_2 gate dielectric has been considered as one of the primary factors limiting carrier mobility.[16] A substantial mobility enhancement to over 200 $cm^2V^{-1}s^{-1}$ and 500 $cm^2V^{-1}s^{-1}$ has been reported for HfO_2 and Al_2O_3 capped monolayer and multilayer MoS_2 FETs, respectively, which was attributed to high-κ dielectric screening of charged impurities that reduces scattering at the channel/dielectric interface.[60, 61] There are also rising concerns that the mobility in these devices might have been substantially overestimated.[62]

For large band-gap semiconductors such as MoS_2,a significant Schottky barrier may form at the metal/semiconductor contact, yielding a high contact resistance.[14],[63] Lee *et al.* showed in their study of MoS_2 flakes produced by liquid exfoliation that the mobility in MoS_2 FETs could be largely underestimated due to the Schottky barriers at the MoS_2/metal contacts.[64] In the presence of a substantial Schottky barrier, the extrinsic mobility is also expected to degrade with decreasing temperature due to the reduced thermionic emission current and thermally assisted tunneling current, as was recently observed by Ghatak*et al* in atomically thin MoS_2 FETs.[16] In agreement with recent predictions,[24] Das *et al*. has demonstrated a significant mobility enhancement by reducing the Schottky barrier height using a low work function contact metal, which further indicates that the performance of MoS_2 FETs can be strongly influenced by the metal/semiconductor contacts.[26]

In order to optimize the performance of MoS_2 FETs, it is crucial to use low resistance Ohmic contacts. There are typically two types of low resistance contacts that can be made between a semiconductor and a metal: (a) Schottky contacts with a very low barrier height and (b) highly transparent tunneling contacts. Ideally, an Ohmic contact can be formed if the Schottky barrier height is zero (or negative). Contacts with low Schottky barrier height (≈30 meV) have been achieved in multilayer MoS_2 by using Scandium as a low work function contact metal.[65] However, the tunability of the Schottky barrier height may be reduced by Fermi level pinning.[30] Alternatively, highly transparent tunneling contacts can be fabricated by heavily doping the semiconductor in the contact region. This approach fails for MoS_2, since ionized impurity doping would substantially damage the structural integrity of the atomically thin channel. As an alternative, surface doping with strongly oxidizing NO_2 molecules has been used to narrow the Schottky barrier thickness for hole injection and thus reduce the contact resistance of WSe_2 FETs.[66]

In this article, we report electrostatic doping using an ionic-liquid (IL) gate as a viable approach to achieve low resistance MoS_2/metal tunneling contacts. We demonstrate(i) significant improvement in the performance of few-layer MoS_2 FETsand (ii) high carrier mobility in the MoS_2 channel that is limited by phonons. Ionic liquids are binary organic salts that can form electric double layers at the ionic-liquid/solid interface and thus act as nano-gap capacitors with extremely large capacitance. As we show in the following, the Schottky barrier can be drastically reduced in ionic-liquid-gated FETs (IL-FETs) of MoS_2. We observe a significant increase of the tunneling efficiency that can be attributed to strong band bending at the MoS_2/metal interface, provided by the thin electrical double layer with a high capacitance. As a result, our nanometer-

thick MoS_2 IL-FETs exhibit a significantly enhanced extrinsic mobility that exceeds 60 $cm^2V^{-1}s^{-1}$ at 250 K, in contrast to $\mu<5$ $cm^2V^{-1}s^{-1}$ measured in the Si-back-gate configuration without ionic liquid. The MoS_2 IL-FETs further exhibit ambipolar behavior with a high current ON/OFF ratio exceeding 10^7 for electrons and 10^4 for holes, and a near ideal subthreshold swing (SS) of ~50 mV/decade at 250 K. More significantly, the mobility in few-layer MoS_2 IL-FETs increases from ~100 $cm^2V^{-1}s^{-1}$ to ~220 $cm^2V^{-1}s^{-1}$ as the temperature decreases from 180 K to 77 K, which is in good agreement with the true channel mobility derived from our four-terminal measurements. The temperature dependence of the mobility behaves as $\mu \sim T^{-\gamma}$ with $\gamma \approx 1$, indicating that the mobility is predominantly limited by phonon scattering in this case.

3.2 Results and discussion

Atomically thin MoS_2 flakes were produced from a bulk crystal by a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrates covered with a 290 nm-thick thermal oxide layer.[15, 67] An optical microscope was used to identify thin flakes, which were further characterized by non-contact mode atomic force microscopy (AFM). In the present study, we focus on bilayer and few-layer (2-7 layers corresponding to 1.3-5 nm thickness) samples, since the yield of bilayer and few-layer flakes was found to be much higher than that of single-layer MoS_2. Moreover, few-layer MoS_2 also tends to form lower Schottky barriers (thus smaller contact resistance) than single-layer samples.[30, 65]MoS_2 IL-FET devices were fabricated by first patterning the source, drain and gate electrodes, consisting of 5 nm of Ti covered by 50 nm of Au, using standard electron beam lithography and electron beam deposition.[56] A small droplet of the DEME-TFSI ionic liquid (Sigma Aldrich 727679) was then carefully applied onto the devices using a micromanipulator under an optical microscope,

covering the MoS_2 layer and the source, drain and gate electrodes.[68] The ionic liquid gate forms by self-assembly. DEME-TFSI has been chosen for its large electrochemical stability window (>3 V at room temperature).

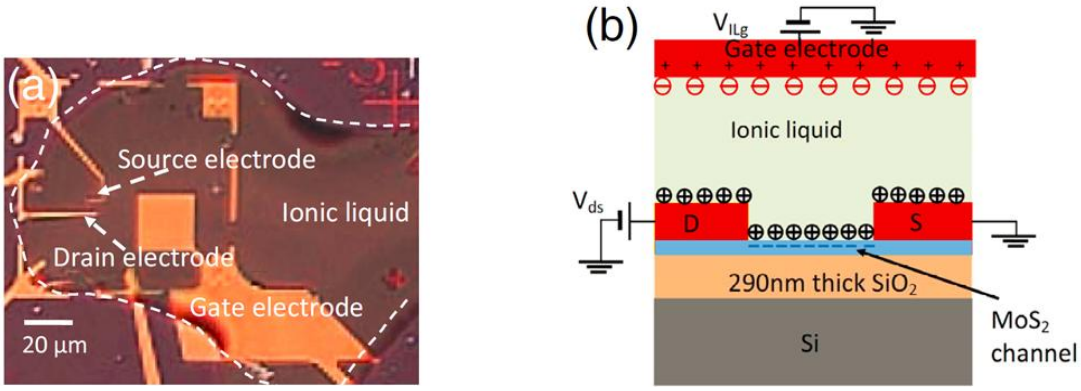


Figure 3.1.(a) Optical micrograph of a typical ionic-liquid-gated MoS_2 FET. The contour of the ionic liquid drop covering the MoS_2 channel and the in-plane gate-electrode are marked by white dotted lines. The scale bar is 20 µm. **(b)** Schematic illustration of the working principle of an ionic-liquid-gated MoS_2 FET.

Figure 3.1a shows a micrograph and figure 3.1b the schematic of a typical ionic-liquid-gated MoS_2 device. Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station after dehydrating the ionic liquid under high vacuum (~1×10^{-6}Torr) for 48 hours. This thorough removal of the remaining moisture turned out to be important to preventing the formation of chemically reactive protons and hydroxyls through the electrolysis of water.[69] Most measurements on ionic-liquid-gated devices were carried out at 250 K or below to further reduce the possibility of any chemical reactions between the ionic liquid and MoS_2.[70] As shown schematically in figure 1.1b, negative ions in the ionic liquid accumulate near the gate electrode and positive ions accumulate near the MoS_2 channel when a positive voltage is applied to an ionic-liquid-gate-electrode near the device channel. The scenario reverses when a negative voltage is applied to

the gate. In both cases, electric double layers form at the interfaces between the ionic liquid and solid surfaces.[71] To ensure that nearly all of the gate voltage appears as potential drop across the ionic-liquid/channel interface, the surface area of the gate electrode is 1-2 orders of magnitude larger than the total area of the transport channel plus parts of the drain/source electrodes, which are immersed in the ionic liquid.[72] Downscaling of the ionic liquid gated devices can be achieved by simultaneously reducing the surface area of the gate electrode and covering a large part of the drain/source electrodes with an insulating overlayer.[73]

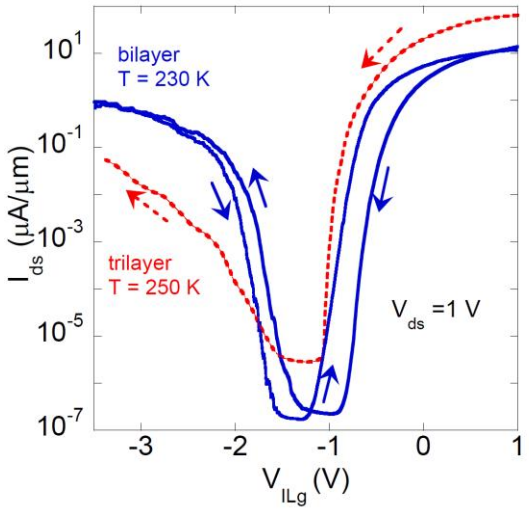


Figure 3.2. Transfer characteristics of representative bilayer and trilayer MoS_2 ionic-liquid-gated FETs measured at the drain-source bias V_{ds} = 1 V.

We have measured several ionic-liquid-gated bilayer and few-layer MoS_2 FETs and observed consistent results. Fig. 3.2 shows the transfer characteristics of two representative devices measured at a drain-source voltage of 1 V. Both the bilayer and trilayer devices exhibit ambipolar behavior, with the current ON/OFF ratio exceeding 10^7 for electrons in both devices. The observed ON/OFF ratio for holes was 10^6 in the bilayer and 10^4 in the trilayer device. Ambipolar behavior has been previously observed in ion-liquid-gated thicker MoS_2 flakes

(>10 nm) by Zhang *et. al.*[70] However, their ON/OFF ratio was less than 10^3 for both electrons and holes, presumably due to the relatively large "OFF" state current passing through the interior of the crystal beneath the channel surface. This current ON/OFF ratio is much lower than the typical values between 10^4 and 10^7, which are desired for digital logic devices.[60] It is worth pointing out that our observation of hole conduction in bilayer and few-layer MoS_2 is rather surprising in view of the large Schottky barrier height (~1 eV) for the hole-channel.[30] Our results suggest that holes are injected into the MoS_2 channel primarily by thermally assisted tunneling rather than by thermionic emission.[74]The tunneling rate is increased significantly for both electrons and holes in presence of the extremely thin (~1 nm) dielectric layer formed by the ionic-liquid gate, which significantly reduces the thickness of Schottky barrier through strong band bending near the contacts at high gate voltages. Since the formation of an electrical double layer on the MoS_2 contacts near the edge of the metal electrodesis conformal, the thickness of the contact Schottky barrier can be reduced very effectively by the ionic liquid gate down to the electrostatic screening length in the ionic liquid (~1 nm).[75] The asymmetry between electron and hole transport can be attributed to

1)a larger Schottky barrier height for the hole channel that reduces thermally assisted tunneling,

2) a slight preference for the adsorption of positive ions on MoS_2, as discussed later, and

3)intrinsic*n*-doping of the transport channel.

All of these effects tend to favor electron *vs.*hole transport, shifting the transfer curves toward the negative gate-voltage direction. The lower asymmetry between electron and hole transport (observed when the gate voltage was swept from positive to negative), causing a more balanced ambipolar character of the bilayer MoS_2 device, may be attributed to a slightly lower degree of

intrinsic *n*-doping in the bilayer flake.[72] The hysteresis in the transfer characteristics could be attributed to the charge injection at the interfaces between the channel and the substrate as well as the slow motion of the ions at low temperature.[70, 76]

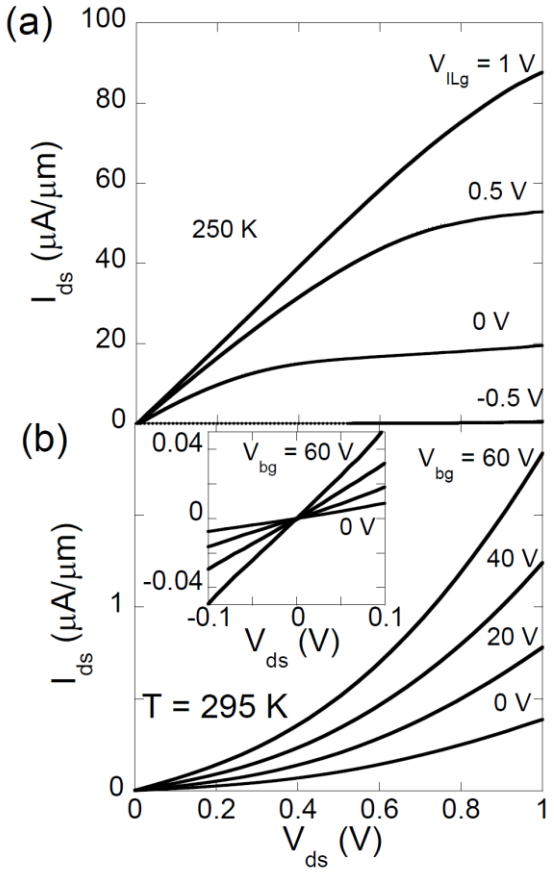


Figure 3.3. Comparison of the output characteristics of the trilayer MoS_2 device used in Fig. 2, measured in the ionic-liquid-gate and back-gate (without ionic liquid) configurations. **(a)** Drain-source current I_{ds} as a function of the drain-source bias V_{ds} at ionic-liquid-gate voltages between -0.5 and 1 V. **(b)** I_{ds} as a function of V_{ds} at selected back-gate voltages between 0 and 60 V before the ionic liquid was deposited. The **inset in (b)** shows the magnified low-bias region in this panel.

Low contact resistance is an important prerequisite to realize the full potential of MoS_2 as a channel material for FETs. Since the Schottky barrier for holes is larger than for electrons, the contact resistance in the hole channel is higher than in the electron channel. To optimize the

device performance, we next focus on the electron channel only and study the impact of ionic-liquid-induced Schottky barrier thinning on its electrical characteristics. Fig. 3.3 shows the output characteristics of a trilayer MoS_2 device that was measured both with an ionic-liquid-gate and a back-gate with no ionic liquid present. As shown in Fig. 3.3a, the drain current in the ionic-liquid gate voltage range of $0<V_{ILg}< 1$ V exhibits linear dependence at low drain-source voltages and starts to saturate at higher V_{ds}. The current saturation at high V_{ds} can be attributed to the channel pinch-off of the FET. In sharp contrast to these data, the same device, when measured in the back-gate configuration without ionic liquid, exhibits strongly non-linear (upward turning) I_{ds}–V_{ds}behavior, suggesting the presence of a significant Schottky barrier at the contacts (Fig. 3.3b). Furthermore, the total resistance calculated from the slope of the I_{ds} - V_{ds} characteristics in the low-bias region is over two orders of magnitude larger for the Si back-gate configuration (2×10^6 Ω at V_{bg} = 60 V, see the inset of Fig. 3.3b) than for the ionic-liquid-gate configuration (1×10^4 Ω at V_{ILg} = 1 V), providing further evidence that ionic-liquid gating significantly reduces the contact resistance by thinning the Schottky barrier. Note that linear I_{ds}-V_{ds} dependence at small bias voltages ($V_{ds}< 0.1$ V, shown in the inset of Fig. 3b) is only a necessary, but not a sufficient condition for a low-resistance Ohmic contact. Linear current-voltage behavior may also be due to the thermally assisted tunneling current, especially at small drain-source voltages.[65]

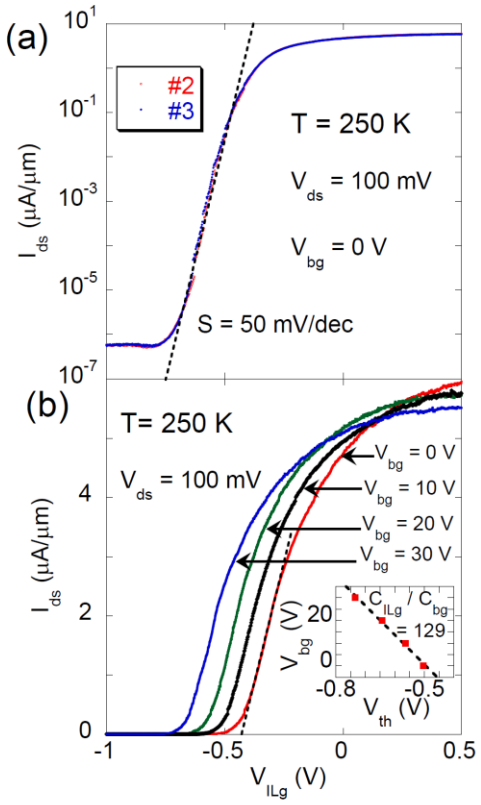


Figure 3.4.(a) Transfer characteristics of the identical trilayer MoS_2 device in two separate runs, where the ionic-liquid-gate voltage was swept at V_{ds} = 100 mV, V_{bg} = 0 V and T = 250 K. **(b)** Transfer curves of the identical ionic-liquid-gate device measured at various back-gate voltages between 0 and 30 V. The **inset in (b)** shows the back-gate voltage *vs.* the threshold voltage of the transfer curves.

The observed drastic reduction of the contact resistance by ionic-liquid gating opens up the possibility of investigating channel-limited device parameters in nanometer-thick MoS_2 devices. Fig. 3.4a shows the transfer characteristics from two separate measurements of the same trilayer MoS_2 device at T= 250 K, for V_{ds}= 0.1 V and V_{bg} = 0 V. The high reproducibility of the transfer curves indicate that charged ions in the ionic liquid are electrostatically accumulated at the gate/electrolyte and MoS_2/electrolyte interfaces without any noticeable chemical reactions. The transfer characteristics also remain essentially unchanged at different gate voltage sweeping rates. Furthermore, the subthreshold swing (SS) reaches the theoretical limit of kT/e ln (10) =

50 meV/decade at T = 250 K corresponding to a gate efficiency of ~1. Such a high gate efficiency can be attributed to the large electric-double-layer capacitance of the ionic-liquid gate. The near ideal subthreshold swing also further indicates that the ionic-liquid gate creates highly transparent tunneling contacts.[77]

To extract the carrier mobility, we first estimated the ionic-liquid gate capacitance by measuring I_{ds}*versus*V_{ILg} of the same trilayer device at various fixed back-gate voltages, as shown in Fig. 4b. As the back-gate voltage is stepped up from the 0 to 30 V, the threshold voltage V_{th} of the I_{ds}-V_{ILg} curves systematically shifts in the negative V_{ILg} direction, while the slope of the I_{ds}-V_{ILg} curves remains nearly constant in the linear region. The small crossover between the I_{ds}-V_{ILg} curve measured at V_{bg} = 30 V and corresponding measurements at lower back-gate voltages may be due to the hysteretic effect. The ionic-liquid gate capacitance per unit area is estimated to be C_{ILg} ~ 1.55×10^{-6} Fcm.$^{-2}$ This estimate is based on the observed change of the threshold voltage ΔV_{th} in response to the change of the back-gate voltage ΔV_{bg} using the relationship $C_{ILg}/C_{bg} = \Delta V_{bg}/\Delta V_{th}$. We used $C_{bg} = 1.2\times10^{-8}$ Fcm^{-2} for the capacitance per unit area between the channel and the back gate and the value $\Delta V_{bg}/\Delta V_{th}$ = 129, determined from the linear fit shown in the inset of Fig. 4b. Using the expression $\mu = L/W\times dI_{ds}/dV_{ILg}/(C_{ILg}V_{ds})$, we estimated the low-field field-effect mobility of ~293 cm^{2}V^{-1}s^{-1} using L= 3.3 μm for the channel length and W = 1.0 μm for the channel width, dI_{ds}/dV_{tg} for the slope of I_{ds}-V_{ILg} curve in the linear region at V_{bg} = 0 V, and C_{ILg} ~1.55×10^{-6} F/cm^{-2}. Note that the value C_{ILg} ~ 1.55×10^{-6} F/cm^{-2} is about 4-5 times smaller than the C_{ILg} value determined by Hall measurements ($C_{ILg,H}$ ~ 7.2×10^{-6} Fcm^{-2}) on much thicker MoS_2 flakes[70]. The discrepancy may arise from the dependence of the quantum capacitance on the carrier density. The total capacitance $C_{ILg,}$ consisting of the electrostatic

capacitance C_e of the electric double layer and the quantum capacitance C_q of the MoS_2 channel, which are connected in series ($1/C_{ILg} = 1/C_e + 1/C_q$). $C_{ILg,}$ is likely dominated by C_q due to the extremely large electrostatic capacitance of the DEME-TFSI ionic liquid gate,[69] which can be as high as 100 μF/cm^2. Since C_q is a measure of the average density of states (DOS) at the Fermi level, whichincreases with increasing carrier density, the value of C_q may also increase with the carrier density.[14] As a result, the C_q is expected to be smaller in the low carrier density region near the threshold voltage than in the higher carrier density region [above n_{2D}~1×10^{13} cm^2 as determined from $n_{2D} = C_{ILg,H}(V_{ILg,H} - V_{th})$], where the field-effect mobility is determined. This may lead to a possible underestimate of the total capacitance and thus an overestimate of the mobility. Using the capacitance $C_{ILg,H}$ = 7.2 μFcm^{-2} determined by Hall measurement in multilayer flakes (> 10 nm) at high carrier densities, the low limit of the field-effect mobility in our ionic-liquid-gated trilayer MoS_2 device is determined to be 63 cm^{2}V^{-1}s^{-1}, consistent with the Hall mobility measured in ionic-liquid-gated MoS_2 multiplayer flakes and with the mobility of multiplayer MoS_2 on SiO_2 measured in a four-probe configuration.[70, 78] We conclude that the actual extrinsic field-effect mobility lies likely between 63 cm^{2}V^{-1}s^{-1} and 293 cm^{2}V^{-1}s^{-1}, which is 1-2 orders of magnitude higher than the mobility observed in typical Si-back-gated monolayer and few-layer MoS_2 FETs. This indicates the reported mobility ranging between 0.1–10 cm^{2}V^{-1}s^{-1} in monolayer and few-layer MoS_2 FETs has been largely limited by the contact resistance. [15, 16, 60]

It is also worth noting that our ionic-liquid-gated MoS_2 channel is in a highly electron-doped state with a threshold voltage of $V_{th} \approx 0.5$ V at $V_{ILg} = 0$ V, which may be attributed to a higher concentration of positive than negative ions adsorbed in the vicinity of MoS_2. A large

negative threshold voltage shift was also observed in high-κ dielectric passivated monolayer and multiplayer MoS_2 FETs, which could be attributed to the presence of a large amount of fixed positive charges in the dielectric layer, which have likely accumulated during the low temperature atomic layer deposition process.[60, 61] Similar to the molecular ions adsorbed on the MoS_2 surface in ionic-liquid gated devices, these fixed charges in the thin high-κ dielectric layer could also reduce the Schottky barrier thickness, and thus contribute to the reported mobility enhancement. Also in carbon nanotube FETs, modest surface molecular doping has been shown to significantly reduce the Schottky barrier thickness, leading to a substantially enhanced tunneling current.[79]

To elucidate the transport mechanisms in the few-layer MoS_2 channel that was electrostatically doped by the ionic liquid, we measured the I_{ds}-V_{bg} relationship in a different MoS_2 device (3.3 nm or 5 layers thick) between 77 and 180K, after the device had been quickly cooled from 250 K to 77 K at a fixed V_{ILg} = 0 V. Below the freezing point of the ionic liquid (≈200 K), the carrier charge density induced by the presence of positive ions, which preferentially enriched the vicinity of MoS_2, remained practically constant. The carefully chosen value V_{ILg} = 0 V of the ionic-liquid gate voltage allowed the creation of highly transparent tunneling contacts due to the adsorption of positive ions (implying *n*-doping), while the carrier density in the MoS_2 channel was kept low enough to allow an efficient reduction to zero by the back gate (see Fig. 3.5a). As shown in the inset of Fig. 3.5a, the I_{ds}-V_{ds} characteristics are highly linear in the entire V_{ds} and V_{bg}range even at 77 K, indicating highly transparent contacts with thin Schottky barriers. To confirm that it is the electrostatic surface doping that is responsible for the drastic reduction of the contact resistance, we compared the device characteristics before the

ionic liquid was added and after it was removed, following the completion of all electrical measurements. We observed nearly identical output characteristics in both cases (data not shown). Consequently, we may exclude the possibility of electrochemical doping or any other type of irreversible electrochemically induced degradation of the MoS_2 channel.

To avoid possible complications arising from the interplay between the ionic-liquid gate and the back gate, we performed I_{ds} -V_{bg} measurements only at temperatures below the freezing temperature of the ionic liquid in order to suppress changes in the capacitance between the back-gate and the MoS_2 channel. In our previous study of polymer-electrolyte-gated monolayer-thick MoS_2 FETs, we attributed the beneficial influence of the polymer-electrolyte gate on the I_{ds}-V_{bg} curves to a significant improvement of the carrier mobility.[80] However, the extent of mobility enhancement was overestimated by neglecting the additional ionic-liquid capacitance that was induced by the back-gate voltage. In addition, capacitive coupling between the back and top gates through the large top-gate bonding pad may also lead to a significant underestimate of the back-gate capacitance in conventional dual-gated FET devices,[62] thus causing a nominal overestimate of the mobility. Unlike in conventional top-gated (or dual-gated) devices, where the top-gate electrode is directly on top of the channel, inducing capacitive coupling, the metal gate electrode used in the ionic-liquid gate, shown in Fig. 3.1a, is located within the plane of the device and separated by several tens of micrometers, causing no change in the capacitance. As a result, the ionic-liquid gate electrode in our devices is capacitively decoupled from the transport channel and the back-gate in the temperature range between 77 and 180 K, ruling out the possibility of any stray capacitance arising from the gate electrode that may inadvertently cause a nominal increase in the back-gate capacitance. Our I_{ds}-V_{bg} measurements with a floating and

grounded ionic-liquid gate, shown in Fig. 3.5a, yield identical results, indicating that the ionic-liquid gate electrode has no effect on the back-gate capacitance when the ionic liquid is frozen.

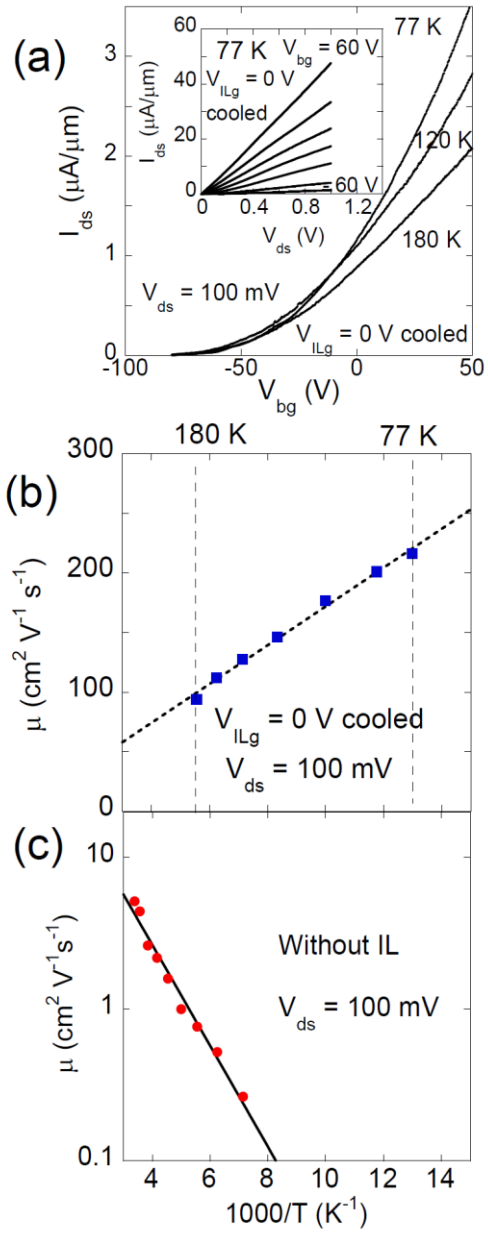


Figure 3.5.(a) Transfer curves of a 3.3 nm thick (5 layer) MoS_2 FET measured in the back-gate configuration with the drain-source bias V_{ds} = 100 mV and the ionic-liquid-gate voltage kept at 0 V. The observations in the temperature range between 77 and 180 K were performed after the device had been cooled down from 250 to 77 K. **The inset in(a)** shows the output characteristics of the device measured at back-gate voltages between -60 and 60 V at T = 77 K. **(b)**

Temperature dependence of the field-effect mobility extracted from the transfer characteristics in (a). **(c)** Temperature dependence of the field-effect mobility of the same device before the ionic liquid was added.

Figures 3.5(b-c) show the temperature dependence of the low-field field-effect mobility extracted from the I_{ds}-V_{bg} curves in Fig. 3.5a. These data are compared to the expected mobility in the same device with no ionic liquid present using the expression $\mu = L/W \times dI_{ds}/dV_{bg}/(C_{bg}V_{ds})$. For this estimate, we used L= 4.5 μm, W = 0.7 μm, and $C_{bg} = 1.2 \times 10^{-8}$ Fcm^{-2} for the back-gate capacitance. The field-effect mobility with no ionic liquid present was observed to decrease from 5 cm^{2}V^{-1}s^{-1} to 0.3 cm^{2}V^{-1}s^{-1} as the temperature decreased from 295 K to 140 K, following a simple activation temperature dependence depicted in Fig. 5c. In this case, the mobility decreases much more rapidly than if it were limited by scattering from charged impurities.[81] This suggests that the charge transport behavior is largely limited by the Schottky barriers at the contacts and does not reflect the intrinsic behavior of the carrier mobility. We can extract an effective Schottky barrier height of $\Phi \sim 66$ meV from the temperature dependence of the extrinsic mobility $\mu \sim \exp(-\Phi/k_B T)$ in Fig. 5c. This is lower than published theoretical estimates for an ideal interface,[25] possibly due to band bending induced by an applied gate voltage. In sharp contrast to this behavior, the mobility in presence of the ionic-liquid gate increases from ~100 cm^{2}V^{-1}s^{-1} to ~ 220 cm^{2}V^{-1}s^{-1} as the temperature decreases from 180 K to 77 K at a carrier concentration between 7×10^{12} and $< 9 \times 10^{12}$ cm^{-2} [determined from $n_{2D} = C_{bg}(V_{bg} - V_{th})$], following a $\mu \sim T^{\gamma}$ dependence with $\gamma \approx 1$. We conclude that in this case, the mobility is limited by the intrinsic behavior of the channel. Of course, dielectric screening in the ionic-liquid gate could nominally increase the capacitive coupling.[81] Still, the observed qualitative change from thermally activated to "metallic" behavior caused by an ionic liquid gate, which acts as a top

dielectric layer below the melting temperature, cannot be simply attributed to a possible underestimation of the back-gate capacitance. Extrapolating the $\mu \sim T^{\gamma}$ fit with $\gamma \approx 1$ to the temperature T=250 K yields a mobility value of $\mu \approx 70$ $cm^2V^{-1}s^{-1}$, in good agreement with the mobility measured in the ionic liquid gate configuration at 250 K. This provides further evidence that the mobility measured in the back gate configuration is unlikely an artifact due to the underestimation of back gate capacitance. Moreover, as discussed in more detail below, our four-terminal measurements on a similar MoS_2 device show that the presence of the frozen ionic liquid, which forms an additional dielectric layer on top of the devices, does not substantially change the capacitance of the back-gate measurements.

Low-field field-effect channel mobility in this temperature range is affected by various scattering mechanisms, including scattering by acoustic phonons, optical phonons, as well as long range and short range disorder that is present both in the bulk and near the surfaces of the channel. Kaasbjerg*et al*. showed theoretically that the mobility due to acoustic and optical phonon scattering in monolayer MoS_2 increases with decreasing temperature following a $\mu \sim T^{-\gamma}$ dependence, where the exponent γ depends on the dominant scattering mechanism.[82] At relatively low temperatures (< 100 K) , acoustic phonon scattering dominates, resulting in $\gamma = 1$. At higher temperatures, optical phonon scattering starts to dominate, and the exponent $\gamma > 1$ should cause a stronger temperature dependence of the mobility. On the other hand, the disorder-limited mobility decreases with decreasing temperature.[82, 83] In our few-layer devices, the observed exponent ($\gamma \approx 1$) in the expression $\mu \sim T^{-\gamma}$ for the temperature dependence of the mobility coincides with that of transport dominated by acoustic-phonon scattering. In this case, however, the mobility values are substantially lower than what would be expected from acoustic-

phonon-limited mobility, and the temperature was high enough to excite not only acoustic, but also optical phonons. This behavior can be understood in a likely scenario, where the top ionic-liquid dielectric quenches phonon modes and thus reduces the γ value.

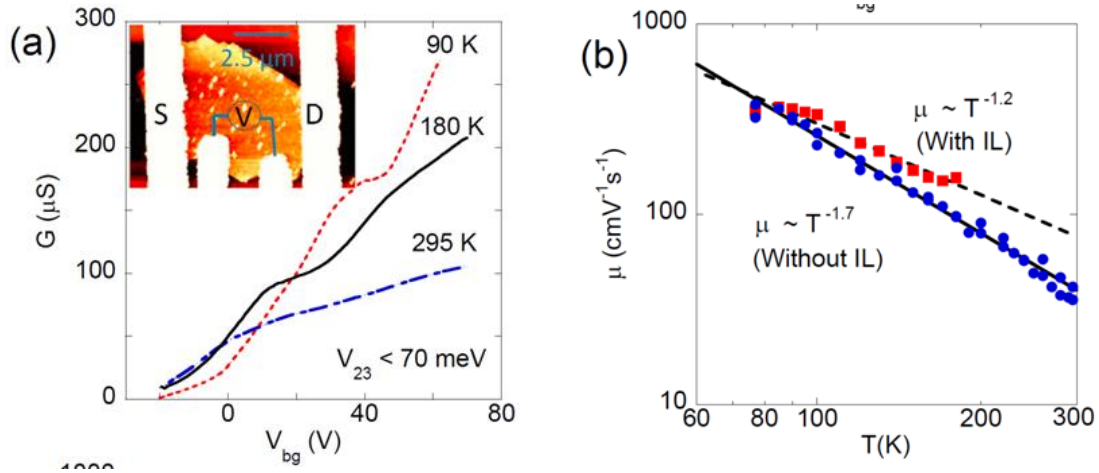


Figure 3.6. Four-terminal electron transport in a back-gated 8 nm thick MoS_2 FET with and without ionic liquid. **(a)** Conductance as a function of back-gate voltage measured at different temperatures with no ionic liquid present. The inset shows an AFM image of the four-terminal device. **(b)** Temperature dependence of the true channel mobility derived from the four-terminal measurements in presence and absence of the ionic liquid.

In order to verify that the extrinsic mobility of our ionic liquid gated MoS_2 FETs approaches the true channel mobility, we also performed four-terminal measurements. An AFM image of the four-terminal device is shown in the inset of Fig. 3.6a. We measured the conductance $G = I_{ds}/V_{inner}$, where V_{inner} is the potential difference across the voltage probes, at a fixed drain-source bias while sweeping the back-gate voltage. $V_{inner}$is kept below 70 mV during the measurement. Fig. 3.6a shows the conductance *versus* back-gate voltage of an 8 nm thick MoS_2 flake measured at various temperatures, with a back-gate voltage of up to V_{bg} = 70 V. Under these conditions, we expect a charge carrier concentration of $n_{2D} = C_{bg}(V_{bg} - V_{th}) \sim 6.8 \times 10^{12}$ cm^{-2} at V_{bg} = 70 V, where the threshold voltage $V_{th} \approx$ -20 V. The field-effect mobility can be

extracted from the G*vs.*V_{bg} curves in the 60 <V_{bg}< 70 V range using the expression $\mu = L_{inner}/W \times (1/C_{bg}) \times dG/dV_{bg}$, where L= 3.0 μm is the distance between the two voltage probes, W = 5.0 μm, and $C_{bg} = 1.2 \times 10^{-8}$ Fcm^{-2} is the back-gate capacitance. The steps in the conductance may be caused by the back-gate tuning of the voltage contacts. The voltage electrodes are very wide in our geometry, and their separation is only about twice their width. In this case, the effective distance between them may change with applied gate-voltage. Fig. 6b shows the temperature dependence of the true channel mobility with and without the frozen ionic liquid as a dielectric capping layer. Before the ionic liquid was added, we observed a mobility increase from ≈ 40 cm^{2}V^{-1}s^{-1} at 300 K to ≈ 390 cm^{2}V^{-1}s^{-1} at 77 K following a $\mu \sim T^{-\gamma}$dependence with $\gamma \approx 1.7$ in the entire temperature range, in good agreement with theoretical predictions for an MoS_2 monolayer.[82] Although our 8 nm thick sample is much thicker than a monolayer, back-gating has the strongest effect on the bottom MoS_2 layers. Moreover, charge screening also reduces the number of charge carriers in the top layers, especially at high back-gate voltages.[65, 84] The relatively low overall mobility values in this device may be attributed to additional extrinsic scattering mechanisms such as impurity scattering and scattering off surface polar optical phonons of the SiO_2 gate dielectric.[82] Interestingly, the overall mobility of the device with the ionic liquid is similar to that without the ionic liquid in the temperature range between 77 and 180 K, indicating that the ionic liquid as a capping top dielectric does not substantially impact the back gate capacitive coupling when it is frozen. On the other hand, the temperature dependence of the mobility weakens upon adding the ionic liquid, following a $\mu \sim T^{-\gamma}$dependence with $\gamma \approx 1.2$ for 77 < T < 180 K. This weaker temperature dependence of the channel mobility μ in presence of ionic liquid dielectric capping is consistent with that of the extrinsic mobility shown

in fig. 5b, which can be attributed to phonon mode quenching caused by the ionic-liquid dielectric.[81] Note that the extrinsic mobility values in fig. 3.5b, which include the contact resistance, are in good agreement with the true channel mobility values in fig. 3.6b. This is a further demonstration that ionic liquid gating effectively creates highly transparent electrical contacts and reveals the intrinsic channel-limited device properties of MoS_2 FETs. This finding shows that the previously reported low mobility of Si-back-gated MoS_2 FETs, ranging typically between 0.1 – 10 $cm^2V^{-1}s^{-1}$, may not represent the intrinsic channel property, but was rather limited by non-ideal contacts, as pointed out by Popov *et al*.[63] It also demonstrates that phonon-limited mobility can be achieved without substantially reducing the disorder near the channel/dielectric interface.

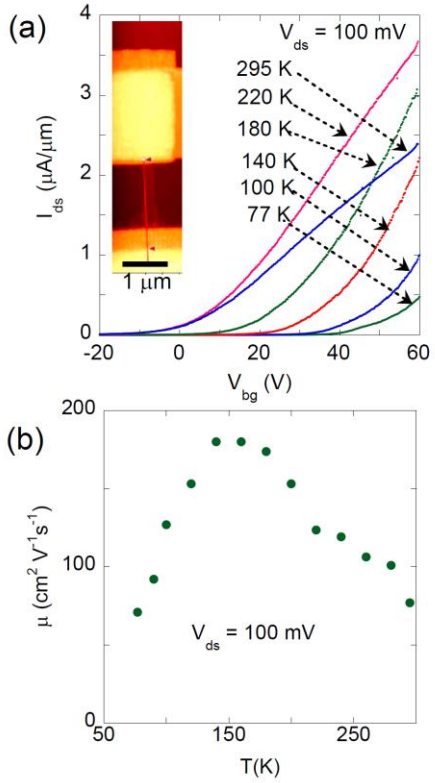


Figure 3.7:(a) Transfer characteristics of a back-gated 5 nm thick MoS_2 FET measured at the drain-source bias V_{ds} = 100 mV, for various temperatures. **The inset of (a)** shows an AFM image of the device with its electrical contacts covered by HSQ while large portion of the channel is bare. **(b)** Field-effect mobility of the device as a function of temperature.

Since the carriers induced by the ionic-liquid gate are close to the top surface of the MoS_2 channel, the interface properties in these devices may be different from back-gated devices with no ionic liquid, where the carriers are closer to the bottom surface. To rule out the possibility that the drastic difference in mobility between MoS_2 devices with and without an ionic liquid gate arises from differences at the channel/dielectric interface, we measured another few-nanometer thick (5 nm or ~7 layers) back-gated MoS_2 with patterned *n*-doping. As shown in the inset of Fig. 3.7a, both the electrical contacts and a small section of the channel near each electrode are covered by a 50 nm thick layer of positive resist (hydrogen silsesquioxane, HSQ), defined by standard electron beam lithography at a dose of 200 $\mu C/cm^2$, while the large portion of the channel is not covered by HSQ. At low degrees of cross-linking obtained at low electron beam dosages, Si-H bonds in HSQ are readily broken and release hydrogen, increasing electron density in MoS_2 near the contacts.[85] Consequently, HSQ covered contact regions are *n*-doped, while the bare channel region remains undoped. Fig. 3.7a shows selected transfer curves of the back-gated device at temperatures between 77 and 295 K, from which the field-effect mobility can be extracted. As shown in Fig. 3.7b, the mobility increases from ~ 75 $cm^2V^{-1}s^{-1}$ to ~ 180 $cm^2V^{-1}s^{-1}$ as the temperature drops from 295 K to 140 K, suggesting that mobility in this temperature range is largely limited by phonon scattering. Below 140 K, the mobility starts decreasing with decreasing temperature, which can be attributed to the reduction of the thermally assisted tunneling current through a Schottky barrier. Since the main difference between this device and other back-gated, few-nanometer-thick MoS_2 FETs is the *n*-doping of the contacts, the observed

high mobility at room temperature and its phonon-limited temperature dependence above 140 K can be attributed to the Schottky barrier thinning by the surface doping in the contact regions, which is albeit not as effective as ionic-liquid gating. The slightly lower mobility in the ionic-liquid gated device (Fig. 5b) than in the HSQ contact-doped device (Fig. 7b) above 140 K may be attributed to the presence of added charge impurities from the ionic liquid.[86] This finding unambiguously demonstrates that the observed mobility enhancement in ionic-liquid-gated MoS_2 FETs is not an interface effect and cannot be simply attributed to the reduction of charge scattering in the transport channel.

3.3) Conclusions

In conclusion, we report the fabrication of ionic-liquid-gated MoS_2-based field-effect transistors with significantly higher mobilities than reported in comparable back-gated devices. We attribute the observed mobility enhancement to the ionic liquid, which acts as an ultrathin dielectric that effectively reduces the Schottky barrier thickness at the MoS_2/metal contacts by strong band-bending. The substantially reduced contact resistance in ionic-liquid-gated bilayer and few-layer MoS_2 FETs results in an ambipolar behavior with high ON/OFF ratios, a near-ideal subthreshold swing, and significantly improved field-effect mobility. Remarkably, the mobility of a 3-nm-thick MoS_2 FET with ionic-liquid-gating was found to increase from ~ 100 $cm^2V^{-1}s^{-1}$ to ~ 220 $cm^2V^{-1}s^{-1}$ as the temperature decreased from 180 K to 77 K. This finding is in quantitative agreement with the true channel mobility measured by four-terminal measurement, suggesting that the mobility is predominantly limited by phonon-scattering. It is remarkable that the high mobility has not been degraded by the presence of both long range disorder (*e.g.* from charged impurities) and short range disorder (*e.g.* interface roughness scattering) at the

MoS_2/SiO_2 and MoS_2/ionic-liquid interface. The effect of Schottky barrier thinning on the performance of MoS_2 FETs was further verified by patterned *n*-doping of the contact regions using HSQ. More detailed studies of MoS_2 FETs with HSQ doped contacts are underway. Our study of ionic-liquid-gated MoS_2 FETs clearly demonstrates that previously observed low mobility values in monolayer and few-layer MoS_2 devices were largely caused by the large contact resistance. We found that phonon-limited mobility can be recovered through Schottky barrier thinning even in the presence of non-ideal channel/dielectric interfaces. We also surmise that the reported drastic mobility improvement in high-κ dielectric-capped MoS_2 FETs may be partially attributed to the Schottky barrier thinning caused by the doping of the fixed charges in the thin dielectric layer in addition to dielectric screening.

CHAPTER 4: IMPROVED PERFORMANCE IN H-BN ENCAPSULATED MOS_2 FETs CONTACTED BY HIGHLY DOPED GRAPHENE ELECTRODES.

4.1 Introduction

In the previous chapter, we have reported significant improvement of electrical contacts in few-layer MoS_2 devices by drastically reducing the SB thickness using an ionic liquid (IL) gate.[87] However, the improved charge injection efficiency using this method is still fundamentally limited by the height of the Schottky barrier. For example, the contact resistance of our IL-gated MoS_2 is still significantly higher for the hole channel than for the electron channel due to the relatively large SB height for the valence band. As mentioned earlier, the Schottky barrier height may be reduced by selecting metal electrodes with a low work function (for n-type semiconductors) or a high work function (for p-type semiconductors). Yet it has proven to be extremely challenging to find metals with a proper high or low work function that also exhibit a high conductivity and a high chemical, thermal and electrical stability. Furthermore, the expected benefit of the proper work function for lowering the SB may be drastically reduced by Fermi level pinning.[30, 88] In particular, a recent theoretical study shows that partial Fermi level pinning is present at the metal/TMD contacts for a variety of metals with the work functions spanning a wide range.[89]

In this work, we use graphene as electrode material with a tunable work function to overcome the above limitations of metal electrodes to contact few-layer MoS_2 FETs. For one, graphene is mechanically strong, flexible and thermally stable, which is desirable for flexible electronics applications. Even more importantly, the work function of graphene can also be tuned

by chemical or electrostatic doping to minimize the SB height at the graphene/semiconductor interface.[31, 33] By using the extremely large electric double layer (EDL) capacitance of an IL gate, the work function of graphene at the graphene/WSe_2 interface can be modulated within an enormously large range. By using Ionic liquid (IL) as an electrostatic dopen we were able to tune the graphene Fermi level in a wide range to achieve both n (towards conduction band minimum) and p (towards valance band maximum) of MoS_2 channel. In addition to electrostatic doping with IL gating ,an air stable, surface charge transfer electron donor Benzyl Viologen (B.V) was used to achieve n-type behavior for the entire temperature range from 77K to room temperature. These graphene contacted MoS_2 FETs showed remarkable stability in both air and the vacuum.[47] Unlike conventional chemical doping methods, B.V dopant molecules can be reversibly removed using toluene[47]. Even though devices based on graphene-TMD heterostructures have been reported previously,[34, 90, 91] the operation principle of our MoS_2 FETs with lateral graphene contacts is qualitatively different from the previously reported graphene-based field-effect tunneling transistors (FETTs) and vertical field-effect transistors (VFETs). Whereas transport in FETTs and VFETs based on graphene/TMD heterostructures is modulated by the vertical transport barrier at the graphene/TMD junctions, the graphene/TMD junctions in our devices serve as optimum drain and source contacts to lateral MoS_2 FETs. We also emphasize that high n (p) doping is crucial to achieve a sufficiently low (high) graphene work function that is needed for making low resistance contacts to the conduction (valence) band of MoS_2. Although back-gated MoS_2 FETs with graphene contacts have also been reported recently, achieving such a large modulation of the work function is not possible with a back gate alone.[92-95]

The electrical transport measurements carried out for the Graphene contacted MoS_2 FETs demonstrate that when the temperature decreases from 160K to 77K , extrinsic field effect mobility for IL gated devices(with V_{ILg} = -3V) increases from ~ 150 $cm^2V^{-1}S^{-1}$ to ~ 350 $cm^2V^{-1}S^{-1}$ for electron channel. Following a similar behavior, the same device with B.V doping (Concentration of 60 mM)measured in the same temperature range the mobility increases from ~ 125 $cm^2V^{-1}S^{-1}$ to ~260 $cm^2V^{-1}S^{-1}$.With both doping methods the two probe extrinsic transport shows phonon limited behavior. Four probe measurements were carried out to understand the intrinsic transport behavior and scattering mechanism. These devices were measured with and without doping and results clearly concludethat ,the doping doesn't affect the intrinsic transport properties for the graphene contacted MoS2 FETs with h-BN encapsulation.

4.2 Experimental details, results and discussions

4.2.1 Fabrication of graphene contacted MoS_2 FETs encapsulated my h-BN

To fabricate graphene contacted MoS_2 FETs, atomically thin MoS_2 flakes were produced from a bulk crystal by a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrates covered with a 290 nm thick thermal oxide layer.[67, 80, 87, 96] An optical microscope was used to identify thin flakes, which were further characterized by non-contact-mode atomic force microscopy (AFM). In the present study, we focus on few-layer samples with 4-12 layers corresponding to 3-8 nm thickness. Samples containing only few layers can be produced more easily and sustain larger drive currents than MoS_2 monolayers, while at the same time maintaining a relatively large ON/OFF ratio and a small *c*-axis interlayer resistance in comparison to thicker samples.[31,] [83, 97] Next, we deposited a thin hexagonal boron nitride (h-BN) crystal (10–50 nm thick; mechanically exfoliated from commercially

available h-BN crystals) onto a few layer MoS_2 flake to cover its middle section. While performing the deposition using a home-built precision transfer stage, we made sure that the two ends of the MoS_2 remained exposed to form electrical contacts. Passivating the MoS_2 channel by h-BN enables us to tune separately the SB height at the graphene drain/source contacts using the IL gate and the chemical potential of the channel using the Si back gate. We chose h-BN as the MoS_2 channel passivation layer, because of its atomically smooth surface that is chemically inert and relatively free of charged impurities and charge traps.[35-37]To form drain and source contacts, we transferred patterned CVD grown monolayer graphene on top of the h-BN covered MoS_2 flake. Subsequently, we fabricated metal electrodes, consisting of 5 nm of Ti covered by 50 nm of Au, as electrical contacts to the graphene electrodes using standard electron beam lithography (EBL) and electron beam deposition.[56] During the same fabrication step, a large metal electrode was fabricated to serve as an IL gate electrode. Finally, we removed selectively graphene on top of the h-BN covered MoS_2 channel by EBL patterning and oxygen plasma etching.

4.2.2 Characterization of highly doped graphene

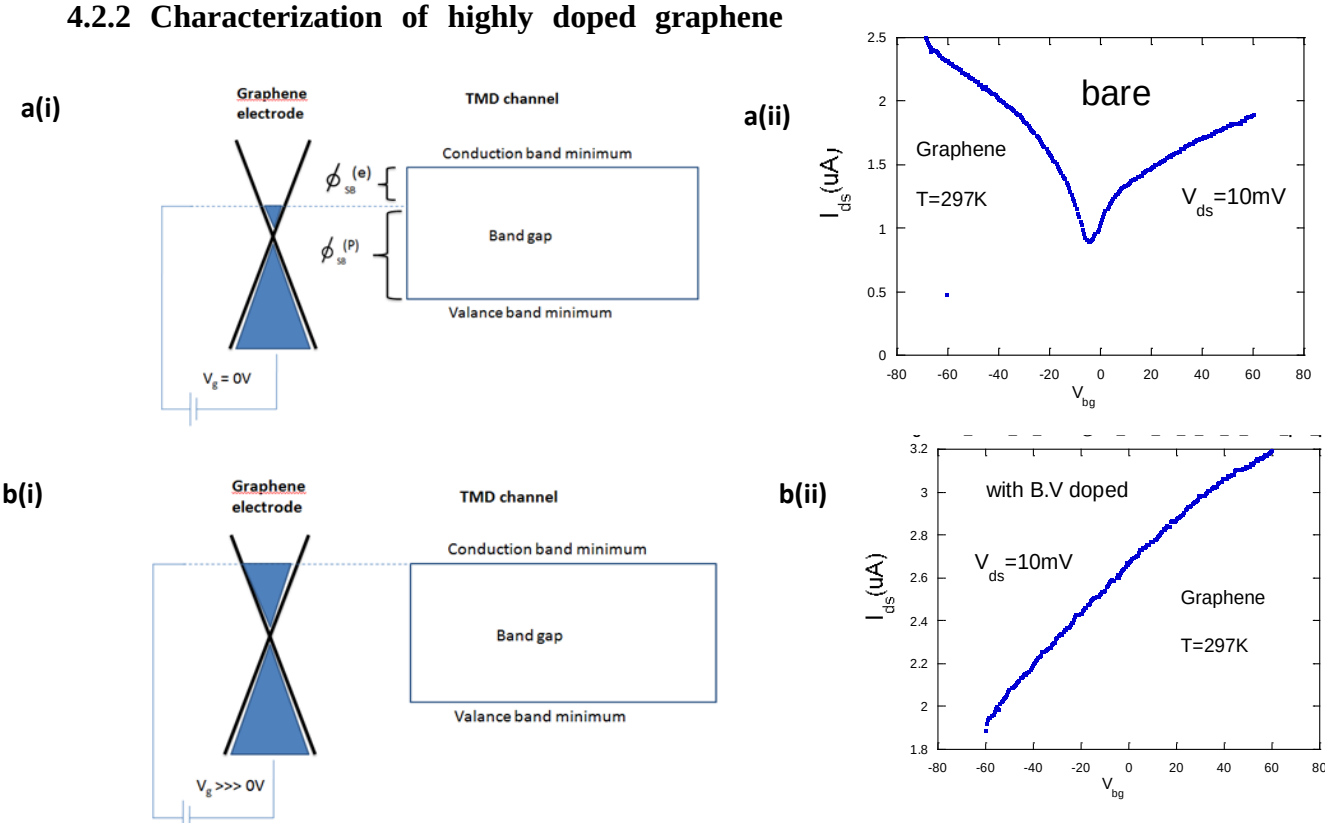


Figure 4.1: Graphene transfer outputs and corresponding schematic diagramme at graphene/MoS2 heterostuture**.** **(a) -(i)**The schemetic band diagramme of the graphene/ MoS_2heterostructure before doping. **(a)-(ii)** The transfer curve measured at 297K and Vds = .01 V without doping.**b-(i)** The band giagramme after B.V doping is applied **(b)-(ii)** The Transfer curve after graphenen is doped with B.V

Figure 4.1(a) (ii) shows the transfer curve of graphene without any doping method. For this case the Dirac point of graphene is close to -5V of back gate voltage with V_{ds} = 0.01V. After B.V doping the Dirac point is shifted extremely towards the negative gate voltage indicating that the B.V doping highly doped the graphene contacts. In this particular case the B.V solution with concentration of 60 mM was used.

4.2.3 Output characteristics with and without doping.

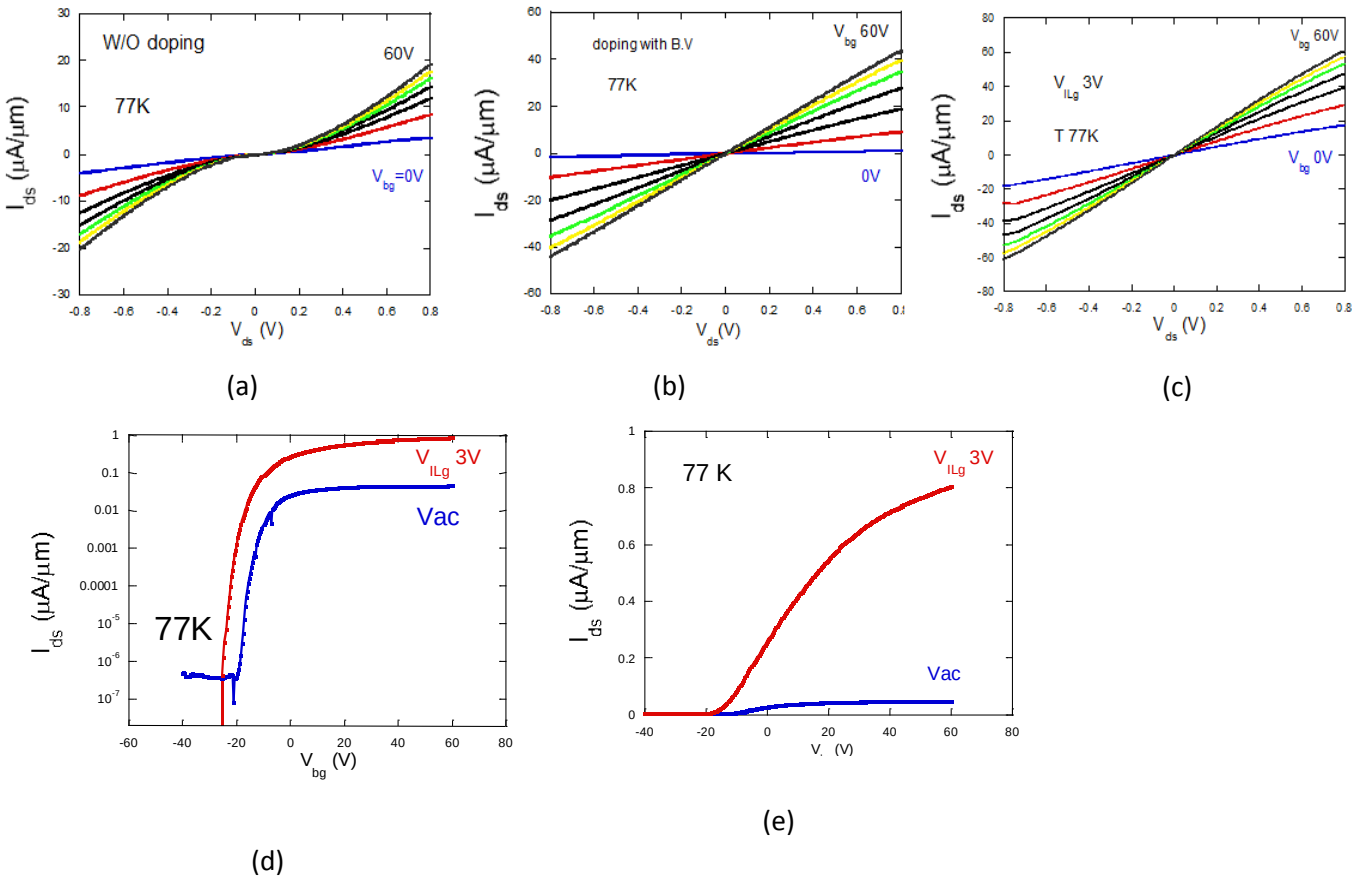


Figure 4.2: (a-c) Output characteristics of the device without any doping, with B.V doping and IL gating of 3V.Each graph shows the I-V curves from -0.8 V to 0.8V **.(d)** I_{ds} as a function of V_{bg} at V_{ds}= .01V and T=77K for without doping and with V_{ILg} 3V in logarithmic scale. The inset shows linear curves of the same graph.

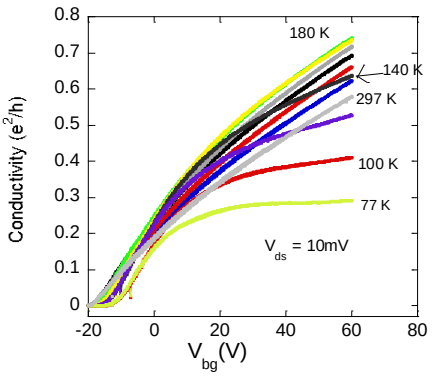
Figure 4.2 (a-c) show the output characteristics of two terminal graphene contacted MoS_2 FET with channel thickness of 9 nm and length to the width ratio of channel (L/W)= 2.5/4.1.This device was fabricated on h-BN to provide high quality bottom gate dielectric. Top of the channel is covered with another piece of h-BN to make sure that both electrostatic and chemical doping won't dope the channel. Doping the channel could degrade the mobility due to the scattering of carriers. This scattering originates from the disorder which introduced by dopant molecules/Ions. The output and transfer characteristics of this device was measured for the entire temperature range, from 77K to 297K for the cases of without doping, with Ionic liquid gating and with B.V doping. In Figure 4.2 (a) the device output characteristics were shown as I_{ds} Vs V_{ds} for fixed backgate voltages at 77K without doping. This reveals the quality of the contact at graphene-MoS_2 hetero-structure. The strong non-linear behavior (turning upward), suggesting the presence of a significant Schottky barrier at the contacts. In sharp contrast to this, the same device measured with ionic liquid gating with V_{ILg} = 3V and B.V doping (Figure 4.2 b-c) show linear behavior for every fixed back gate voltage. The maximum current recorded to be 20μA/μm for the device without doping and it increased up to 40 uA/um while with V_{ILg} = 3V, it was increased to 60uA/um at V_{ds} = 1V for V_{bg} = 60V. Both n doping methods improved the contacts at 77K for electron channel by reducing the contact resistance, mainly lowering the Schottky barrier height. The Figure 4.2 (a-c) clearly demonstrate how the device without doping initially showed non -linear behavior and with each doping level the contacts were improved

even at low temperature as 77K.When the graphene contacts are doped with appropriate doping, the contact resistance can be reduced. The Fermi level of graphene is below the conduction band minimum and the n doping helps to tune the graphene Fermi level towards the conduction band minimum. This reduced the SB height significantly and leads to achieve low resistance Ohmic contacts. Even at V_{ds} = 1V and V_{bg} =60V, we don't see any sign of saturation, indicating that expanding V_{ds} can provide higher ON- current.

Figure 4.2 (d) shows the transfer characteristics of the same device measured at 77K with V_{ds} = 0.01V with and without IL gating. The device without doping shows very low I_{ds} current at high back gate voltage which indicates the existence of significant SB height. In this case the achieved current is mainly due to the carriers thermally excited over the SB or tunneled at the band edge or by the thermally assisted tunneling current which is the combination of first two mechanisms. When a high back gate voltage is applied, then the electrons tunneled in to the conduction band due to the band bending occur at graphene/MoS_2 interface due to the thinning of SB. In addition, the back gate voltage introduce higher carrier density to graphene electrodes. This allows the Fermi level of graphene to shift towards the conduction band minimum and lower the SB height at high positive gate voltage. It's imperative to reduce Schootky barrier height further which leaves behind a significant contact resistance that hinders the intrinsic properties of MoS_2 device. To reduce the contact resistance, high positive IL gating (V_{ILg} = 3V) was applied to the work function tunable graphene electrodes. This significantly increased the I_{ds} current and slightly lower the threshold voltage which indicates that we successfully lower the schotkby barrier height. The maximum current was increased from .04 to 0.8 µA/µm after IL gating and the ON/OFF ratio of the device reaches 10^7. The figure 4.2 (e) clearly demonstrates

the increment of I_{ds} since it represent the both curves in linear region. The reduction of threshold voltage can be explained as the drop of activation energy that the carriers needed to inject in to the conduction band. These observations associate with the changing of SB height with IL gate modulation. The higher electron density introduced by positive IL gate voltage changes the Fermi level of graphene level towards the conduction band minimum making the SB height smaller. The graphene electrodes are selectively doped due the top h-BN passivation which eliminates the doping of channel. The reduction of SB height at drain and source contacts provide low resistance Ohmic contacts for the device. This can be also attributedby the mobility incensement of each case. The device without doping shows 42.23 $cm^2V^{-l}S^{-1}$ and after IL gating the mobility increased up to 350 $cm^2V^{-1}S^{-1}$ at 77.

4.2.4 The transfer characteristics with and without doping.



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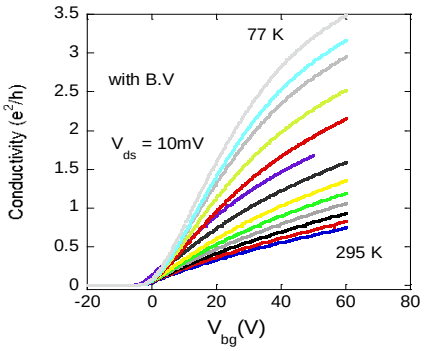

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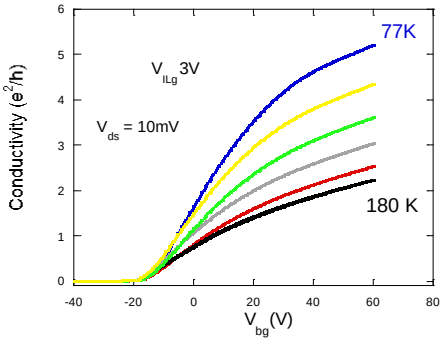

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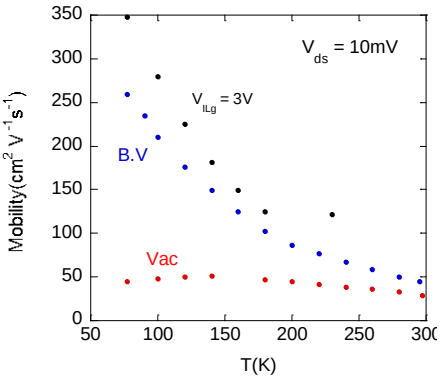


d

Figure 4.3: (a-c) Two terminal conductivity as a function of back gate voltage, at each temperature for cases of without doping, with B.V doping and IL gating of 3V. **(d)**The temperature dependence of two terminal field effect mobility for each case of doping and without doping.

The obtained low resistance contacts with highly n doped graphene electrodes opened up the possibility to investigate the intrinsic channel properties of MoS_2 FETs. Figure 4.3 (a-c) show the two probe conductivity curves of the device, characterized in figure 4.3 , as a function of back gate voltage. These curves were measured for a wider temperature range of 295 K to 77K for the cases of without doping and B.V doping. For IL gating the devices were measured below 160 K to make sure IL is frozen and the electric double layer capacitance remain the same for the entire temperature range when we sweep the back gate voltage. The definition of the conductivity is given by $\sigma = \frac{I_{ds}}{V_{ds}} \times \frac{L}{W}$ where L and W are channel length and width respectively.The conductivity of the device without any doping method with increasing temperature, increases up to 180K, and start to drop for the rest of the temperature range. This can be explained as the clear existence of a Schootky barrier below 180 K and the transport mechanism is dominated by thermally assisted tunneling current. For the temperature range from 180K and above the conductivity is mainly limited by phonons. However this does not necessary mean the carrier transport is not limited by Schootky barrier. This may also include the thermally assisted tunneling current especially at higher temperature range. The linear region of the conductivity curves were used to extract the two probe mobility. The mobility was plotted as a function of temperature as shown in figure 4.3 (d).With both IL and BV doping the temperature dependence of conductivity curves are in metallic region. At 77K with V_{ds} = 10mV the maximum current at V_{bg}60 V with BV doping , increased up to 3.5 µA/µm from 0.3 µA/µm.

With IL gating the maximum current under the same conditions as earlier , recorded as 5.125 μA/μm. In short the maximum I_{ds} current increase more than 10 times with both BV and V_{lLg} = 3V, which clearly indicated that the contacts resistance becomes significantly smaller with highly doped graphene contacts even at a very low temperature. Figure 4.3 (d) shows the two probe mobility as a function of temperature for each case. The mobility was extracted by using the linear region of transfer curves and using the expression $\mu = \left(\frac{1}{C_{bg}}\right) \times (\frac{d\sigma}{dV_{bg}})$. For the case without doping the mobility remains pretty much same, close to 50 $cm^2V^{-1}S^{-1}$. If we observe closely it can be seen that the mobility increases slightly up to 180K and start to decrease for the higher temperatures. This is a similar trend that we observed in the transfer curves. For the cases with both B.V and IL gating the mobility decreases with increasing temperature with higher values , strongly suggest that we successfully achieved low resistance contacts which reveals intrinsic channel properties limited by phonon scattering. It's important to mention that the selectively doping only the contacts and providing high quality atomically thin dielectric surface with h-BN passivation are crucial in order to achieve high mobilities with lower threshold voltage by reducing charge impurity scattering and interface traps.

4.2.5) Four terminal measurements

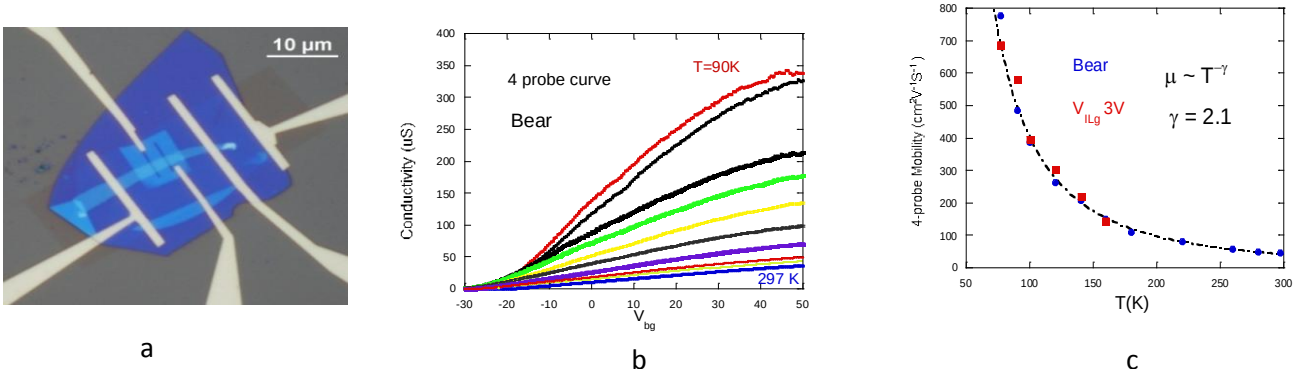


Figure 4.4: (a) The optical micrograph image of a four terminal graphene contacted MoS_2 FET, using h-BN as bottom and top passivation dielectric. The scale bar is 10um.**(b)**4- probe conductivity as a function of $V_{bg}$for fixed temperatures without doping. **(C)** The four probe conductivity as a function of temperature. The blue data points correspond to device without doping and red data points mean device with Ionic liquid gating 3V.

4 probe measurements were carried out for the graphene contacted MoS_2 FETs to understand the intrinsic channel properties and scattering mechanism. The figure 4.4 (a) shows the optical micrograph image of the device that used in this study. The 4 probe device consist of Drain (D), Source (S) and two inner electrodes ,V_1 and V_2.The inner probes V_1 and V_2 were used to measure the voltage V_{ds} while D and S were used to measure the I_{ds}. For the calculations , the separation of V_1 and V_2 is taken as the channel length. The average width of the channel running from D to S, considered as the channel width. The 4 probe conductivity was measured as a function of back gate voltage (V_{bg}) for fixed temperatures for the range of 90K to 297K. When the temperature decreases the maximum conductivity (at V_{bg} = 50 V) increases as expected in true channel behavior. The linear region of the curves were used to extract the mobility.

4.2.6) Important of h-BN passivation for better device performance.

The phonon limited mobility decreases with increasing temperature following a power law dependence, similar to MoS_2 devices fabricated on SiO_2 and Al_2O_3 substrates as reported in the literature. However, the gamma is much large than on oxide substrate, but it is consistent with a recently work on h-BN encapsulated MoS_2. The large gamma indicates reduced interface and substrate scatterings due to charged impurities. Further improving the contacts such as using ionic liquid gating does not affect the intrinsic channel mobility of h-BN encapsulated devices measured in a 4-probe configuration.

4.3 Conclusions

In summary we have used graphene as a work function tunable electrode material to achieve low resistance Ohmic contacts for MoS_2 FETs for n-channel. Using this approach we can lower the Schootky barrier height and achieve intrinsic channel behavior . The contacts are good for a wide range of temperature from 77K to 300K.We successfully achieved 10^7 high ON/OFF ratio nearly ideal sub threshold swing .We used both electrostatic doping (DEME-TFSI) and more air stable molecular doping (Benzyl viologen) to dope the graphene electrodes. Ultra clean h-BN was used as a bottom dielectric and top passivation layer to provide atomically smooth high quality dielectric media , eliminate charge impurity scattering and to protect the channel. The four probe measurements (with devices covered with hBN) reveal that the doping use to improve for contact engineering, doesn't affect the intrinsic transport properties.

CHAPTER 5: WSe_2 FETs WITH DIFFERENT CHANNEL DOPING LEVELS

5.1 Introduction

While low resistance contacts have been achieved using IL gating and highly doped graphene as the contact material, more air and thermally stable contacts with even lower contact resistance will be needed for practical applications. In conventional Si-based electronic devices, low-resistance Ohmic contacts are achieved by selective ion implantation of the source/drain regions before making metal contacts. This is an effective method since the barrier width between semiconductor and metal decreases with the carrier density. Unfortunately, this method cannot be implemented for 2D layered semiconductor channels due to their ultrathin bodies. Various alternative doping methods such as surface charge transfer [47, 98, 99] and substitution [38, 100]doping have been used to reduce the contact resistance of TMD devices. However, most of these doping methods suffer from air, thermal or long term instability.

In this chapter, we investigate the charge transport in FETs with WSe_2 channel that is substitutionally doped by Nb at different concentrations ranging from 0.01% to 0.5%, where the substitution of W by Nb introduces holes to the WSe_2channel. While heavy doping is needed for drain and source contacts, light *n*- and *p*-doping is desired for *n*-type and *p*-type transistors, respectively. On the one hand, doping the channel can lead to highly transparent metal/semiconductor contacts. On the other hand, the carrier mobility is reduced due to the impurity scattering introduced by dopants. We have systematically studied how the contact resistance and channel mobility are affected by the doping concentration. WSe_2 samples with

three different levels of Nb doping are prepared: 0.5%, 0.05% and 0.01% ($Nb_{0.005}W_{0.995}Se_2$, $Nb_{0.0005}W_{0.9995}Se_2$ and $Nb_{0.0001}W_{0.9999}Se_2$) for this study.

5.2 Transport properties of WSe_2 samples with different doping levels.

5.2.1. Fabricating metal contacted WSe_2 FETs with heavily *p*-doped channel

The electrical transport properties of WSe_2 channels with 0.5% and 0.05% Nb doping are studied by fabricating FETs with metal contacts, where the doping level is sufficiently high to make highly transparent tunneling contacts with metal electrodes. First, Nb doped WSe_2 ultrathin flakes were produced by mechanical exfoliation and subsequently transferred onto degenerately doped Si substrate with 290 nm thick SiO_2. High quality thin samples were identified under an optical microscope. These selected samples are further characterized by Park System atomic force microscopy (AFM)**.** Metal electrodes, consisting of 10 nm of Ti and 50 nm of Au, were fabricated to contact the doped WSe_2 samples using standard electron beam lithography (EBL) and electron-beam deposition.

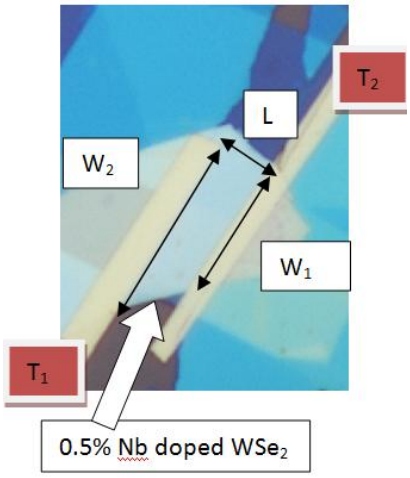


Figure 5.1: Optical micrograph of a metal contacted 0.05% Nb doped WSe_2 device.

5.2.2Electrical transport properties of degenerately (0.5% Nb) doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) samples

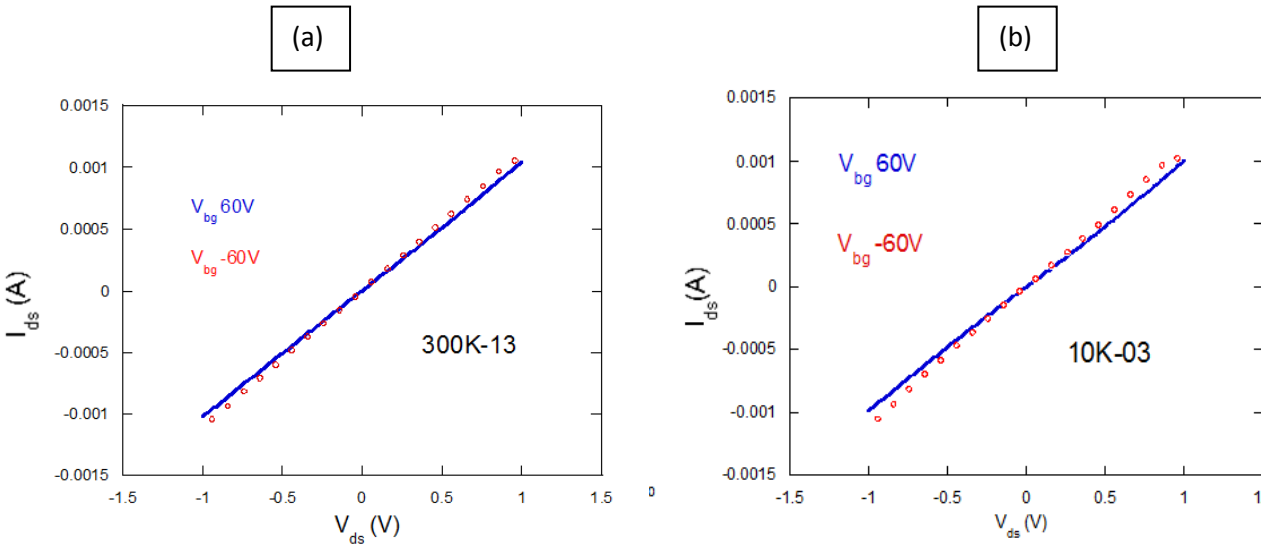


Figure 5.2.I_{ds}(V) Vs $V_{ds}$of$Nb_{0.005}$ $W_{0.995}Se_2$ measured at V_{bg}= -60 and 60V at **(a)** 300K and**(b)**10K.

Figure 5.2 shows I_{ds}-V_{ds} characteristics of a degenerately *p*-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) device with Ti/Au contacts measured at 300K and 10 K. The linearity of the I_{ds}-V_{ds} characteristics down to 10 K indicates Ohmic behavior, which is ascribed to the highly transparent contacts between heavily doped WSe_2 and Ti/Au metal electrode. The I_{ds} only slightly increases as the gate voltage changes from 60 V to -60 V, indicating heavy *p*-doping. The I_{ds}-V_{ds} characteristics also show weak temperature dependence, indicating absence of carrier freeze-out, which is consistent with degenerate doping.

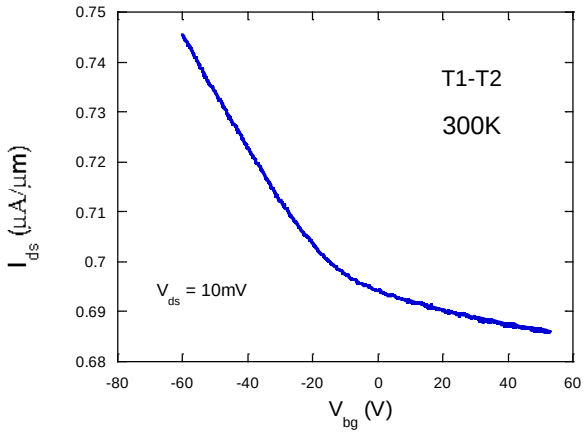


Figure 5.3: The transfer curve of the $Nb_{0.005}W_{0.995}Se_2$ FET at 300K and V_{ds} = 10mV.

To further understand the gate dependanc and extract the field effect mobility, the transfer curve of the device was measured at V_{ds} = -10 mV at room temperate as shown in Figure 5.3. From the slope of the transfer curve in the high V_{bg} region, the two probe field-effect mobility for the $Nb_{0.005}W_{0.995}Se_2$ device is estimated to be ~ 4 $cm^2V^{-1}S^{-1}$ at 300K.

The relatively low mobility of the $Nb_{0.005}W_{0.995}Se_2$ device can be attributed to increased charge impurity scattering in the channel caused by the Nb dopants. In such highly doped devices, the contact resistance is rather small. In our previous study, a very low contact resistance of ~0.20 $k\Omega\mu m$ is obtained in $Nb_{0.005}W_{0.995}Se_2$ devices with Ti/Au contacts, which is nearly temperature independent.[101] Therefore, the low mobility in our $Nb_{0.005}W_{0.995}Se_2$ device is limited by the charged impurity scatting in the channel rather than by the contacts. The low mobility and weak gate dependence in $Nb_{0.005}W_{0.995}Se_2$ devices severely limit the device performance. Therefore, WSe_2 with lower doping concentration is needed as the channel material.

5.3.Characterizing 0.05% Nb doped WSe_2 ($Nb_{0.0005}W_{0.9995}Se_2$) samples.

5.3.1.Electrical transport properties of $Nb_{0.0005}$ $W_{0.9995}Se_2$ samples.

(a) (b)

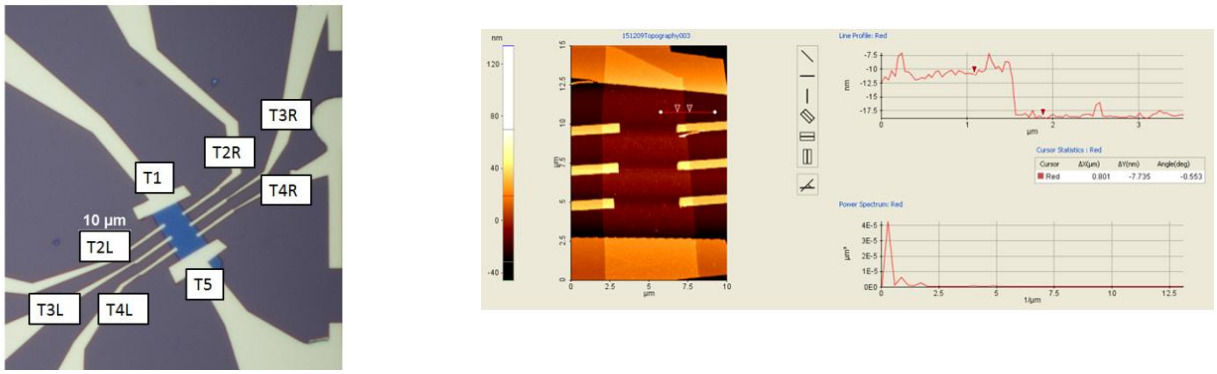


Figure 5.4: (a) The optical micrograph of Hall bar device **(b)** The AFM image of the Hall bar device and its thickness variation across the channel.

Figure 5.4 shows an optical micrograph and an AFM image of a Hall bar device consisting of a 7.7 nm thick $Nb_{0.0005}$ $W_{0.9995}Se_2$ channel. In the micrograph, the drain and source are labeled as T1 and T5; and T2-T4 are inner electrodes used for four-terminal and Hall effect measurements.

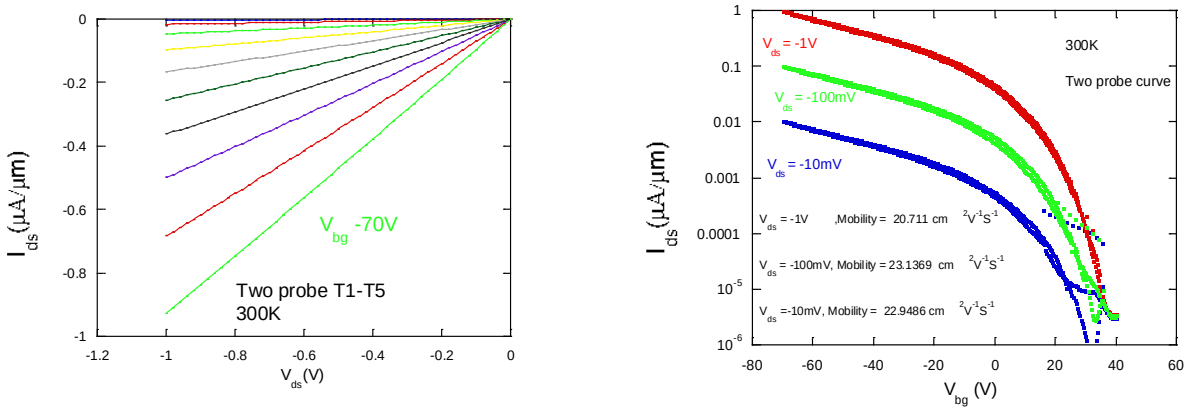


Figure 5.5:(a) The output curves at 300K for the Two probe field effect mobility for T_{67} electrode pair**.(b)** Two probe transfer curve for different bias voltages at 300K.

Figure 5.5 shows the output and transfer characteristics of the $Nb_{0.0005}W_{0.9995}Se_2$ device in Figure 5.4. measured at room temperature. The output curves are linear for a wide range of back gate voltages from 20V to -70V, indicating near Ohmic contacts. In contrast to our 0.5% Nb doped WSe_2 devices which display weak gate dependence, our 0.05% Nb doped WSe_2 devices show a significantly higher ON/OFF ratio of 10^6 for V_{ds} = -1V. Two-probe field-effect mobility in our 0.05% Nb doped WSe_2 devices falls the range of ~ 20 - 23 $cm^2V^{-1}S^{-1}$ at 300K , which is also substantially higher than that in 0.5% Nb doped WSe_2 devices.

5.3.2 Transmission line measurements (TLM) for $Nb_{0.0005}$ $W_{0.9995}Se_2$ samples.

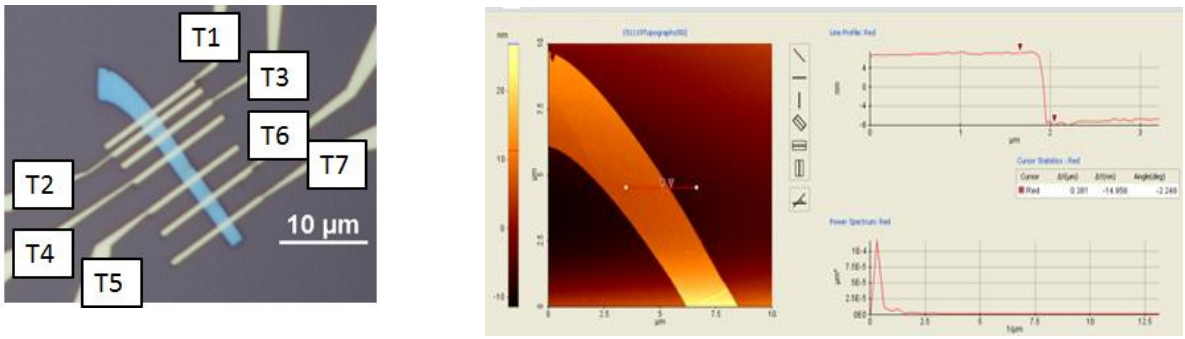


Figure 5.6: (a) Optical micrograph of a device structure for TLM measurement consisting of a ~ 15nm thick $Nb_{0.0005}$ $W_{0.9995}Se_2$ with Ti/Au metal contacts. **(b)A**FM image of the $Nb_{0.0005}$ $W_{0.9995}Se_2$sample in (a).

To quantify the contact resistance in our$Nb_{0.0005}$ $W_{0.9995}Se_2$ device, transmission line method was used with Ti/Au metal electrodes at room temperature. Figure 5.6 (a) shows an optical micrograph of the device structure that was used to calculate the metal/P- doped WSe2 contact resistance R_{MC},where the channel length is defined as the spacing between adjacent Ti/Au metal electrodes. The total resistance measured between any adjacent pair of electrodes is the sum of contact resistance R_{MC} and channel res

istance. By plotting the total resistance (multiplied by the channel width) as a function of channel length, both contact resistance and channel resistance can be separately determined for a uniform channel with consistent contacts.

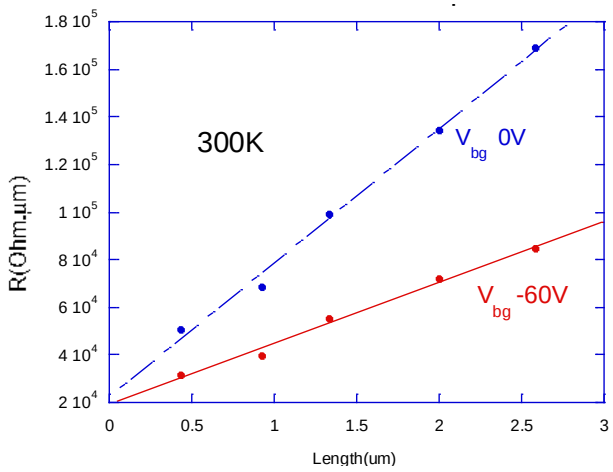


Figure 5.6: Normalized total resistance as a function of channel length measured at room temperature.

Figure 5.6 shows the normalized total resistance as a function of channel length for the device measured at room temperature. From the intercept of the linear fit to the total resistance, we extract the contact resistance $R_{\mathrm{MC}} \sim 11\ \mathrm{k}\Omega\mu m$ for room temperature. This contact resistance value is higher with respect to what we have observed for $Nb_{0.005}W_{0.995}Se_2$ ($\sim 0.2\mathrm{K}\Omega\mu m$). This difference can be attributed to the dependence of Schottky barrier thickness on the doping level: higher hoping concentration leads to thinner Schottky barriers.

5.3.3. Hall Effect measurements for $Nb_{0.0005}$ $W_{0.9995}Se_2$ samples

To accurately determine the mobility,we performed Hall-effect measurements on $\mathbf{Nb_{0.0005}}$ $\mathbf{W_{0.9995}Se_2}$devices.The transverse Hall resistancedefined as $R_{xy} = \frac{V_{xy}}{I_{ds}}$ was measured at different

magnetic fields between -2T to 2Tfor different gate voltages.Extracted values of R_{xy} were plot against magnetic field B as shown in figure 5.8.The Hall coefficient R_H was calculated using the equation:

$$R_H = \frac{dR_{xy}}{dB}.$$

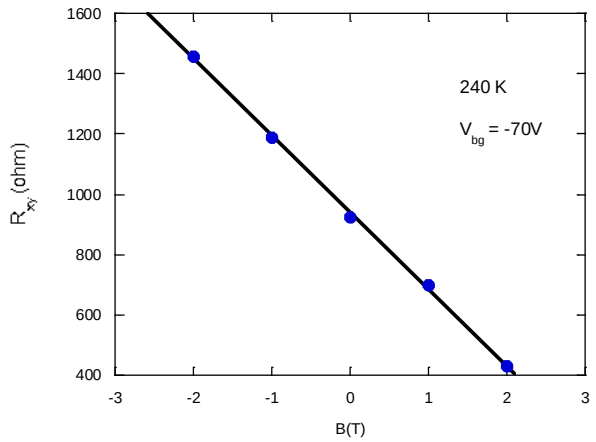


Figure 5.8:R_{xy} Vs B(T) was plot to calculate the R_H value from the slope at 240K for V_{bg} = -70V.Similar graphs were plot for V_{bg} ranging from -50V to -70 V and at temperatures between 300K to 180K.

From$R_{H,}$we can calculate the carrier density$n$ by using the expression:

$n = \frac{1}{(eR_H)}$, where e is the charge of an electron.Finally the Hall mobility $\mu_H$is calculated using four probe conductivity and carrier density as $\sigma = (ne)\mu_H$, where σ is the four probe conductivity.

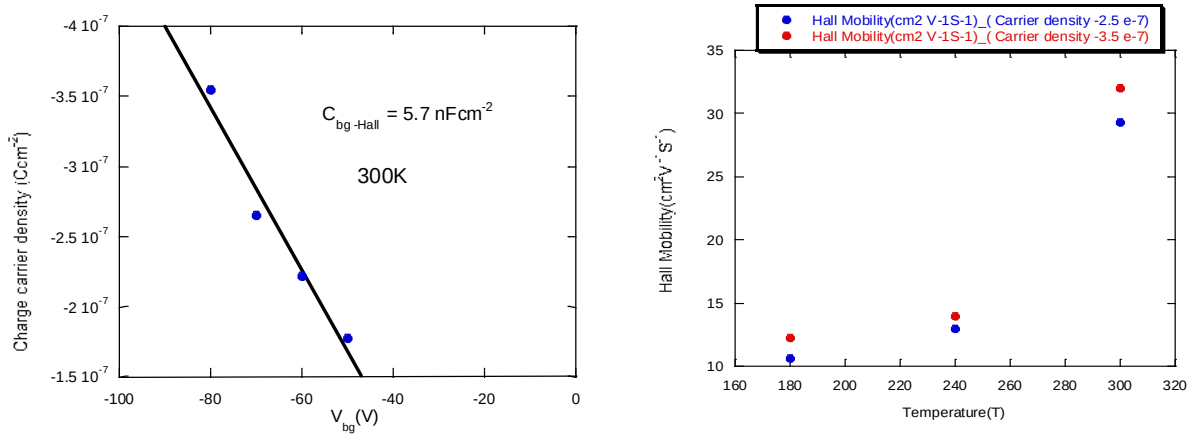


Figure 5.9:(a) Carrier density extracted from Hall effect measurement as a function of back gate voltage at 300 K to determine the back gate capacitance.**(b)**Temperature dependence of Hall mobility for two different carrier concentrations.

Figure 5.9 (a) shows the carrier (Hole) density determined by Hall measurement as a function of back gatevoltage at 300 K. The slope of the gate dependence of hole density yields a back gate capacitance of $C_{bg\text{-}Hall}$ = 5.7 nFcm^{-2}.The temperature dependence of hole mobility for hole concentrations of 2.5 e-7 and 3.5 e-7 (correspond to V_{bg} = -70V and -80V respectively) are shown in Figure 5.9 (b).With decreasing temperature the mobility is decreasing , indicating that the carrier transport scattering is dominated by ionized impurities introduced by dopants. The calculated two probe field effect mobility values (22-24 cm^{2}V^{-1}S^{-1}) are consistent with the obtained Hall mobility value, indicating that contact resistance does not limit the device performance.

5.4) Fabrication of 2D/2D contacted WSe_2 FETs for lightly doped channel.

The metal contacted $Nb_{0.0005}W_{0.9995}Se_2$ FETs showhighly transparent low resistance contacts, but the mobility is rather low due to the charged impurity scattering introduced by dopants. In order to improve the mobility, WSe_2FETs with lower channel doping concentration

is necessary. However, if we further lower the channel doping level, it becomes a major challenge to achieve highly transparent metal contacts. To further investigate how the channel doping effect the transport properties, new contact engineering approaches are needed. Here we report fabrication of 2D/2D contacted FETs with degenerately doped WSe_2 ($Nb_{0.0005}W_{0.9995}Se_2$) as electrodes and 0.01% doped WSe_2 ($Nb_{0.0001}$ $W_{0.9999}Se_2$) as channel material

Figure 5.10 shows an optical micrograph of a two probe 2D/2D contacted WSe_2 FET with 0.01% Nbdoped channel. To provide high quality atomically smooth dielectric surface with reduced interface traps and charge impurity scattering, h-BN is used as the bottom dielectric. In order to protect the channel from the residues that could beintroduced from the dry transfer method and standard e-beam lithography process, the channel is passivated by top h-BN piece. The length of the channel is defined by the width of the h-BN on top of the WSe_2 channel. .

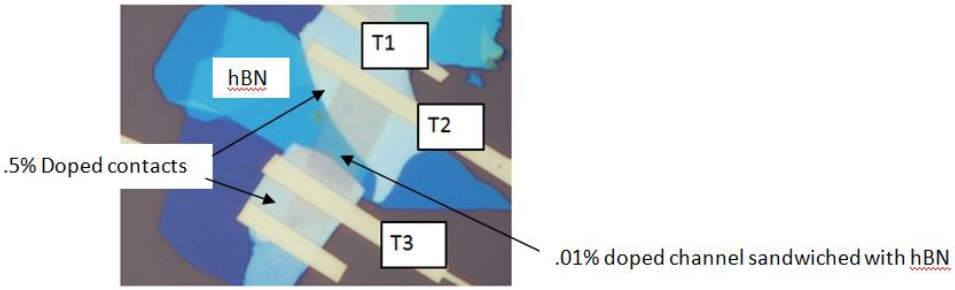
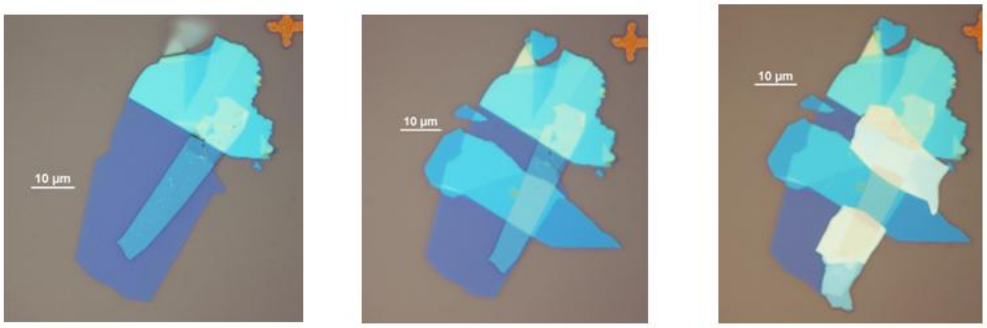


Figure 5.10: Optical micrograph of 2D/2D contacted device.

Thin h-BN crystals (10 - 40 nm thick) were produced from bulk h-BN crystals by a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrate covered with a 270 - 290 nm-thick thermal oxide layer. Atomically thin flakes of slightly doped TMDs were exfoliated from bulk crystals onto a PDMS stamp. Using a home-built precision transfer stage, undoped few-layer TMD flakes used as the channel were

subsequently transferred onto selected thin h-BN crystals on the SiO_2/Si substrate. To passivate the TMD channel, a second thin h-BN crystal is exfoliated to a PDMS stamp and subsequently transferred onto the few-layer WSe_2 flake to cover its middle section while exposing its two ends for electrical contacts.

Thin flakes of degenerately doped TMDs were exfoliated onto PDMS stamps and transferred to the two exposed ends of the TMD channel as drain/source contacts. To improve the interface quality between the h-BN and TMD channel as well as between the doped TMD drain/source contacts and TMD channel, a mild annealing step was carried out after each transfer step at 250^{o}C for 30 minutes in a vacuum chamber purged by 10% H_2 and 90 Ar. The dimensions (e.g. the sample thickness) and the surface quality (e.g. the cleanness and smoothness) of the h-BN substrate and TMD channel were characterized by Park Systems atomic force microscopy (AFM) in the non-contact mode after each annealing step. Metal electrodes, consisting of 5 nm of Ti covered by 50 nm of Au, were fabricated to electrically wire up the degenerately doped TMD drain/source electrodes using standard electron beam lithography (EBL) and electron beam deposition.



Channel transferred on to hBN

Top hBN transferred

After doped contacts transferred.

Figure 5.11: The step by step transfer process to fabricate the 2D/2D contactedWSe_2 FET.

(a)

(b)

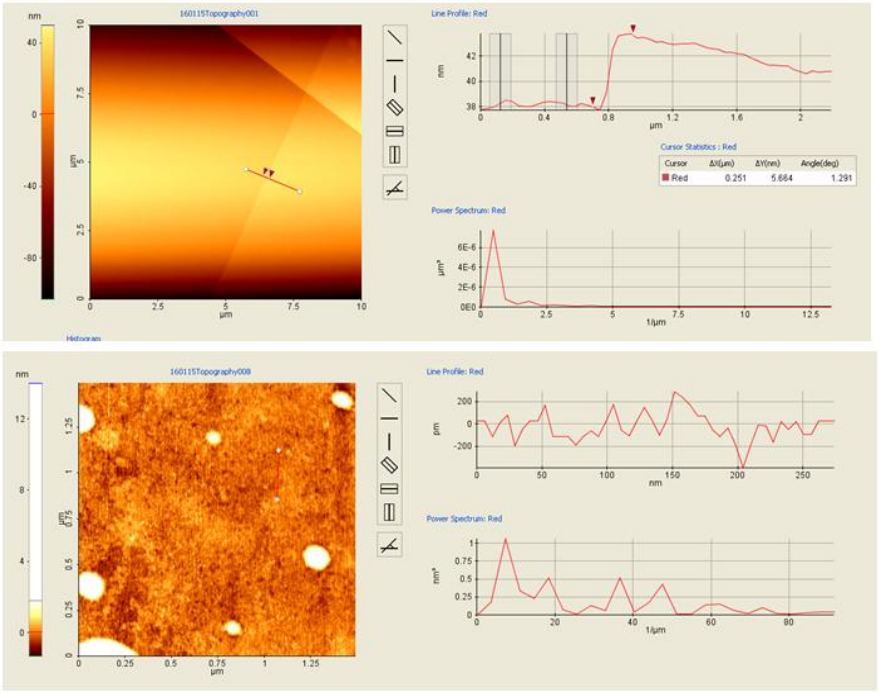


Figure 5.12: The AFM scanned images of the .01% Nb doped WSe_2 samples**.(a)**The AFM image with the scale bar that represents the thickness of the sample which is around 5.6 nm in this case**.(b)** shows the 1.5 X 1.5 um^2 close analysis of the channel. The roughness of the channel can be estimated by the "Line profile red", graph which is in-between -200pm to 200pm.This means sample is pretty clean. The observed white spots represent the bubbles happen to be in the interface between bottom h-BN dielectric and the $Nb_{0.0001}$ $W_{0.9991}Se_2$ channel.

The $Nb_{0.005}$ $W_{0.995}Se_2$ samples were used to exfoliate on to the PDMS patches. The appropriate samples were used to cover the contact area with dry transfer method. The thickness range for these contact electrodes are around 15-30 nm is used to make sure

that both contacts are homogeneously and equally doped. After each transfer step the samples were annealed at 250^0C for 30 minutes. It's important to point out that with the annealing, sometimes the transferred components may shift. As a precaution we heat the fabricating device at 80^0C for 5 minutes before annealing. Once the fabrication is done we used standard electron beam lithography and metal deposition method to form electrodes.

5.3.2.C) Stable 2D/2D contacted .01% doped WSe_2 channel for excellent performance

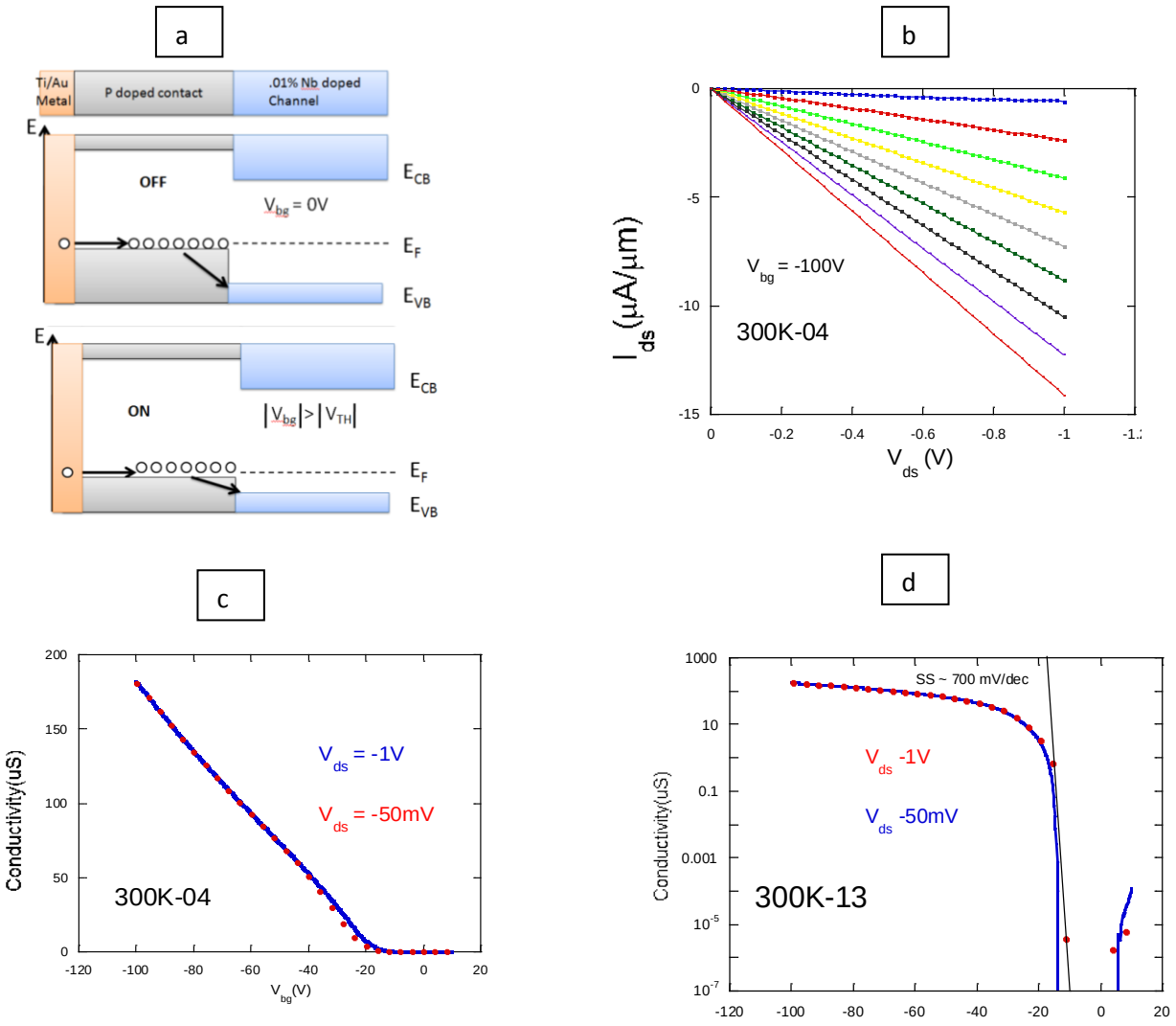


Figure 5.13 : The transport properties of .5% Nb doped contacted (two probe) WSe_2 FET with .01% channel doping.**(a)**The schematic band diagramme to explain how 2D/2D contacts work. **(b)**I_{ds} Vs V_{bg} at 300K for fixed V_{bg} from -20V to -100V. **(c)** The linear version of the coductivity transfer curves of the device at 300K for both V_{ds} = -50V and -1V. **(d)** The logarithmi version of the same transfer curves.

Figure 5.13 (a) shows the schematic digaramme which explains the operation of low resistance 2D/2D junctions. When the highly Nb doped electrodes are at contact with slightlydoped WSe_2 channel, the system is at equilibrium. So the band diagrams are formed such a way that the Fermi levels are aligned. This leads to a relatively larger band offset between Valance band maximums (Conduction band minimums) between contact and channel materials. For highly p doped ($Nb_{0.005}$ $W_{0.995}Se_2$) contact electrodes, the Fermi level is inside the valance band. But for slightly dope channel, the Fermi level is around at the middle of the band gap but little bit lean in to the valance band maximum. This position leads to existence of an energy band offset at the junction. When the negative back gate voltage is applied , the Fermi level of the channel shifts towards to the valance band maximum forming smaller band offset in between slightly doped channel and degenerately doped contacts . Due to the fact that the interlayer interaction between2D TMDs and the junctions are weaker, the back gate voltage is higher enough to tune the Fermi level of channel.[39, 40] This interesting principal is used to achieve low resistance, tunable, Ohmic contacts for TMD based FETs. A typical 2D/2D contacted TMD device shows no significant amount of free carriers in the valance band of the channel below the threshold voltage($|V_{bg}| < |V_{TH}|$).This corresponds to the OFF state of the device. When the V_{bg} is larger than V_{TH} ($|V_{bg}| > |V_{TH}|$), the device will be ON state since the band off set becomes

smaller at channel contact region and the carrier injection from contact to channel is significant which leads to low contact resistance.

Figure 5.13 (b-d) represent the transport and output properties of 2D/2D contacted 0.01% channel doped WSe_2 ($Nb_{0.0001}$ $W_{0.9991}Se_2$)FET with h-BN dielectric and encapsulation. This device channel is 5.6 nm thick and contacted with degenerately p-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$).This device shows superior p- channel behavior with exceeding 10^9 ON/OFF ratio and 700mV/dec sub threshold swing at 300K with V_{ds} = -1V.The sub threshold swing can be improved further by using top h-BN gating[101] and the range of V_{ds} can be further reduced by high- κ dielectric gating.[102]According to Figure 5.13 (b) the output characteristics were measured for the device in the V_{bg} range from -20V to -100V. According to the linear plot of the transfer curve, the threshold voltage (V_{TH}) at 300K for this device is close to -20V.Taking this into account the output curves were measured from -20V to -100V. Figure 5.13 (c) shows the conductivity transfer curves at room temperature for both V_{ds} = -1V and V_{ds} = -50mV.Both curves overlap perfectly indicating that even at low bias the contacts are already improved. The same graph was plot in logarithmic scale.

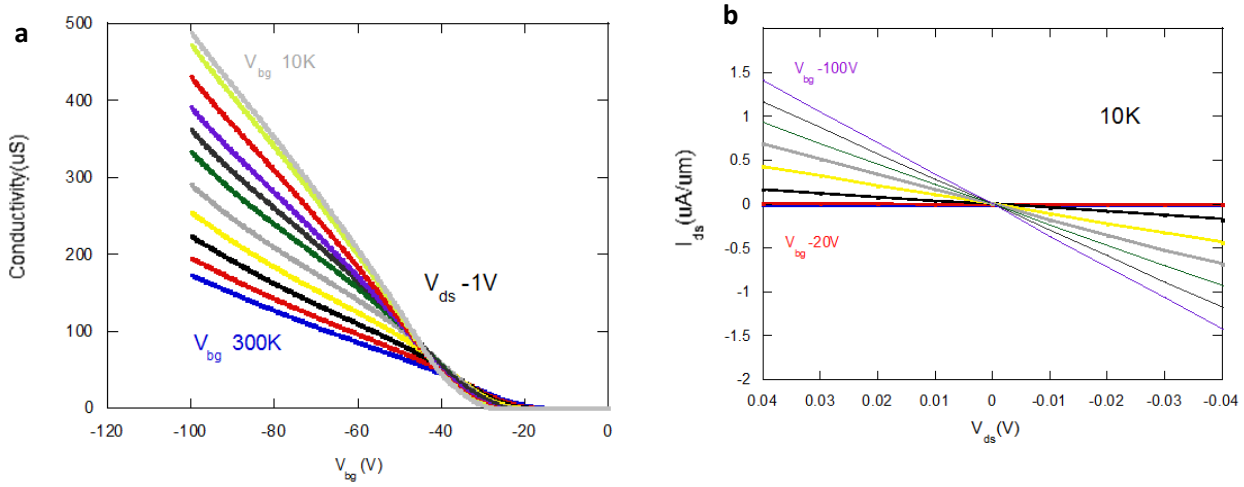


Figure 5.14: The observed intrinsic transfer properties of 2D/2D contacted slightly doped WSe_2 FETs **(a)** The temperature dependence of two probe conductivity at V_{ds} = -1V **(b)** The output characteristic for the range of V_{ds} = -0.04V to 0.04V.

The successfully achieved low resistance 2D/2D contacts, open up the possibility to further investigate the intrinsic channel properties. Figure 5.14 (a) shows the temperature dependence of two probe conductivity of the same device. The conductivity is defined as $\sigma = \frac{I_{ds}}{V_{ds}} \times \frac{L}{W}$where **L** is the length of the channel and **W** is the width. At higher V_{bg} ranges when the temperature increases the conductivity decreases indicating the channel transport is predominantly limited by intrinsic phonon limited behavior (metallic region). However for lower V_{bg} range the device shows insulating behavior,where the conductivity increases with increasing temperature. According to the output characteristic curves measured at 10K (Figure 5.14 (b), the curves remain linear for all the V_{bg} values , indicating that even at low temperaturesthe 2D/2D contacts are barrier free. This is also reflected in the ON state conductivity as it increases by nearly 3 times as the temperature is dropped from 300K to 10K.

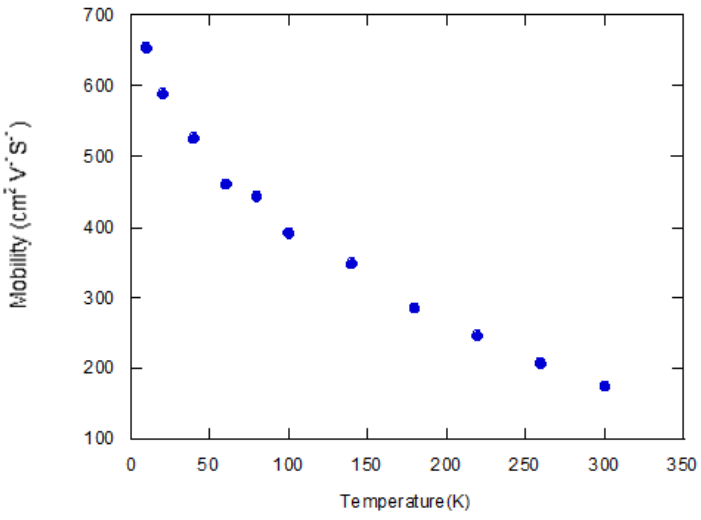


Figure 5.14: The two terminal field effect hole mobility as a function of temperature.

The linear regions of the conductivity curves were used to extract the two probe hole mobility for each temperature. The expression $\mu_{FE} = \left(\frac{1}{C_{bg}}\right) \times (\frac{d\sigma}{dv_{bg}})$ was used to extract the two probe mobility, where C_{bg} is the back gate capacitance, σ is the conductivity and V_{bg} is the back gate voltage. C_{bg} is taken as the geometric capacitance of the device where contribution coming from 290 nm SiO_2 plus the thickness of the h-BN bottom dielectric. The value of the calculated geometric capacitance is consistent with the calculated capacitance with Hall bar measurements. As the temperature dropped to 10K from room temperature, the mobility increased from 175 $cm^2V^{-1}S^{-1}$ to 654 $cm^2V^{-1}S^{-1}$.This trend of temperature dependence of the mobility clearly indicates that the hole transport is largely limited by intrinsic phonons.

Conclusions

We have systematically studied the electrical transport properties of FETs consisting of WSe_2 channels with different Nb dopant concentrations. To construct FETs for 0.5% and 0.05% Nb doped channel materials, metal electrodes were used. Forrelatively low doped (0.01% Nbdoped) channels, a novel low resistance 2D/2D contact engineering method was used. For higher doping channels, it is relatively easy to make low resistance transparent contacts with metal electrodes. However higher channel doping reduces the mobility due to increased dopant ion scattering. Metal electrodes can make low resistance Ohmic contacts for 0.5% Nb doped WSe_2 channel. However, the low mobility and weak gate dependence of 0.5% Nb doped WSe_2 severely its application as a FET channel material. On the other hand, 0.5% Nb doped $WSe_2$is suitable as the drain and source contacts for *p*-type WSe_2 FETs. The transport characteristics of 0.05% Nb doped WSe_2 demonstrate better gate dependence and higher mobility than 0.5% doped

channel. Even higher mobility and better performance are achieved inWSe_2 channels with low Nb concentration (0.01% Nb doped WSe_2). Due to the low channel doping level of 0.01% Nb doped WSe_2, anovel 2D/2D contact engineering technique is employed to achieve low resistance contacts. As the temperature drops form room temperature to 10K, the mobility increases from 175 $cm^2V^{-1}S^{-1}$ to 654 $cm^2V^{-1}S^{-1}$.This trend of temperature dependence of the mobility clearly indicates that the hole transport is largely limited by intrinsic phonons.This device shows superior p- channel behavior with high ON/OFF ratio of$10^9$and a substhreshold swing of 700mV/decat 300K andV_{ds} = -1V.

CHAPTER 6: SUMMARY AND FUTURE WORK

The focus of this work is to improve the performance of TMD based FETs by contact engineering to open up its potential for applications in next generation nano electronics. TMDs got attraction due to finite band gap, chemical and thermal stability, optical properties, flexibility and transparency. When these TMD materials were used to fabricate devices, there's a barrier formed at metal/semiconductor interface due to the energy mismatch. This hinders device performances as well as ability to observe intrinsic physics phenomena . The first attempts of developing contacts were done by using different metal contacts with different work function to form lower Schootky barrier height at metal - semiconductor interface. Metals with lower work function were used to achieve lower Schootky barrier and higher carrier injection for n channel MoS_2FETs.Ti can be used as the metal contact to achieve lower Schootky barrier height. However generally there will be a tunneling barrier at metal- semiconductor interface . In this study, Ionic liquid gating (DEME-TFSI) was used to eletro-statically doped and achieve highly transparent tunneling contacts. The high capacitance introduced by thin electric double layer, causes strong band bending at metal- semiconductor interface which eventually leads to better device performance through higher tunneling efficiency. The mobility for IL gated MoS_2 FET is high as 60 $cm^2V^{-1}s^{-1}$ at 250K in contrast to 5 $cm^2V^{-1}s^{-1}$, what we observed with conventional Si back gate configuration. This is a clear indication that the contacts were dramatically improved with IL gating. The performance enhancement also reflected with 10^7 high current ON/OFF ratio, near ideal sub threshold swing of 50 mV/decade at 250K.The IL gated two probe data is in a good agreement with the true channel measurements. The temperature dependence of IL gated

data follows the relationship $\mu \sim T^{-\gamma}$ where $\gamma \approx 1$ indicating that the carrier transport is predominantly limited by phonons.

In order to take the contact engineering to the next level, we tried to achieve low resistance Ohmic contacts by using graphene as a work function tunable electrodes. Using appropriate doping, the Fermi level of graphene was able to tune towards the conduction band minimum (for n channel) or valance band maximum (for p channel) of the 2D semiconductor to lower the Schottky barrier height. As mentioned earlier, efforts to achieve lower Schottky barrier were carried out using different work function metals. But this have limitations due to the Fermi level pinning. Hence using graphene electrodes standouts as an attractive approach especially this method can be used to achieve both n and p channel behavior simultaneously for the same device. We fabricated graphene contacted MoS_2 FETs using h-BN as a bottom gate dielectric and top passivation layer. Both ionic liquid and more air stable Benzyl Viologen were used to dope the graphene electrodes. The room temperature mobility for graphene contacted n channel Mos_2 is as high as $50cm^2V^{-1}S^{-1}$. At low temperature regime the un-doped device does not show the phonon limited behavior, mainly due to the non ideal contacts. So both IL gating and BV doping were used to dope the Fermi level towards the conduction band minimum and achieve low resistance Ohmic contacts. We successfully observed phonon limited behavior with these two doping methods separately, which reflects the importance of doping to achieve better contacts. In order to understand the intrinsic transport properties and the scattering mechanism, four probe graphene contacted devices were fabricated. Moreover the four probe measurements were measured using different doping methods. We obtained almost identical data for the four

probe measurements with and without doping, which indicates that using doping to improve contacts, doesn't affect the intrinsic transport properties.

When it comes to the real world applications, we need more permanent, air-stable Ohmic contacts. To overcome this challenge we used doped 2D contacts as electrodes for 2D semiconductors. In this particular study we used $Nb_{0.005}$ $W_{0.995}Se_2$ (.5% Nb doped WSe2) as contact material and $Nb_{0.0001}$ $W_{0.9991}Se_2$ (.01% Nb doped WSe2) as channel material. This method can be used for wide range of 2D materials. In order to provide atomically smooth surface , and reduce long range and short range disorder, interface traps and to protect the channel, these devices were fabricated on h-BN dielectric layer and passivated by another piece of h-BN. For this study we achieved room temperature p channel mobility for slightly doped WSe_2 of 175 $cm^2V^{-1}S^{-1}$ which increases up to 654 $cm^2V^{-1}S^{-1}$ at cryogenic temperature. This method successfully demonstrate the intrinsic channel behavior with 10^9 ON/OFF ratio and 100 mV/Dec subthreshold swing. The slightly doped feature of the channel offers lower threshold voltage, still preserving the high carrier mobility.

The mobility of WSe_2 FETs with different channel doping was studied using three different Nb doping levels,(.01% , .05% and .5%.). Metal electrodes are good enough to make good contacts for the channels with .5% and .05% doping levels. Higher doping levels make the Schootky barrier thinner and make highly transparent contacts. The .5% Nb doping channel doesn't show any gate dependency. However it shows higher ON current with low resistance even at cryogenic temperature, indicating it's potential for contact electrodes. .05% .On the other hand .05% Nb doped channel demonstrates clear gate dependency, near ideal sub threshold swing, 10^6 ON/OFF rato. However due to the impurity scattering introduced by dopants, It's

room temperature mobility is in the range of 20- 22 $cm^2V^{-1}S^{-1}$.Considering all the facts, .01% Nb doped channel can be considered as a better option for the device performance.

As future work, I'm eager to understand the performance enhancement by using the modulation doping method, on TMD based FETs.This method is expected to use by combining highly doped and non doped TMD materials as a heterostruture.The charge carriers are spatially separated by the dopant material so the scattering of carriers are expected to be low.Another interesting way to enhance the performance is by using cut patterns in TMD/ metal junction.Designed patterns on sample area of MoS2 will increase the serface area that overlaps with the metal electrodes.This will increase the charge injection from metal to channel which ultimately results in low contact resistance.

Isolation of graphene opens up the possibility to explore 2D materials. Currently, 2D material research going well beyond the graphene studies. Growing and stacking of 2D materials with different stockings variety of homo or hetero structures of atomically thick layers open up a new direction of science that can lead to fascinating technological breakthrough.[103]The thickness dependant properties of 2D materials becoming so exciting and it's expected to offer unlimited research and technological opportunities.[103] Already understood properties of 2D materials have contributed to new frontiers of science such as spin and valley-tronics.[104] As Richard P. Feynman inspired generations to explore the layered materials during his lecture "There's plenty of room at the bottom" emphasizing that we can control the properties of materials if we can arrange the atoms the way we want them.

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ABSTRACT

OPTIMIZATION OF TRANSITION METAL DICHALCOGENIDES(TMDS) BASED FIELD EFFECT TRANSISTORS(FETS) VIA CONTACT ENGINEERING

by

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Layered transition Metal Dichalcogenides (TMDs) have demonstrated a wide range of remarkable properties for applications in next generation nano-electronics. These systems have demonstrated many "graphene-like" properties including a relatively high carrier mobility, mechanical flexibility, chemical and thermal stability, and moreover offer the significant advantage of a substantial band gap. However, fabricating a high performance Field Effect Transistors (FETs) is challenging for these TMDs mainly due to the formation of significant Schootky barrier height at metal/TMD interface in most cases. The main goal of this study is to use novel contact engineering approaches to achieve highly transparent tunneling contacts by thinning the Schottky barrier width or low resistance Ohmic contacts by making the Schootky barrier height smaller.

The first approach is to use Ionic Liquid (IL) gating for metal contacted MoS_2 FETs which make highly transparent tunneling contacts due to the strong band banding at metal/MoS2 interface. The substantially reduced contact resistance in ionic-liquid-gated bilayer and few-layer MoS_2 FETs results in an ambipolar behavior with high ON/OFF ratios, a near-ideal subthreshold

swing, and significantly improved field-effect mobility. Remarkably, the mobility of a 3-nm-thick MoS_2 FET with ionic-liquid-gating was found to increase from ~ 100 $cm^2V^{-1}s^{-1}$ to ~ 220 $cm^2V^{-1}s^{-1}$ as the temperature decreased from 180 K to 77 K. This finding is in quantitative agreement with the true channel mobility measured by four-terminal measurement, suggesting that the mobility is predominantly limited by phonon-scattering. In order to make the Schootky barrier height smaller and achieve low resistance Ohmic contact, work function tunable electrodes (graphene) were used with MoS_2 channel. Both electrostatic (IL) and surface charge transfer (Benzyl Viologen-B.V) dopants were used to tune the work function of graphene electrodes. With both doping methods the graphene contacted MoS_2 device demonstrates phonon limited behavior. On the other hand the same device without doping, mobility remains pretty much the same value for a wide range of temperature. Furthermore four probe garphene contacted devices with hBN passivation demonstrate that the doping used to improve the contacts don't affect the intrinsic transport properties of MoS_2 devices.

Finally 2D/2D contact engineering method was utilized as more attractive contact engineering strategy since it provides more air and thermal stable doping for both channel and contacts. With this method room temperature p channel mobility for .01% Nb doped WSe_2 of 175 $cm^2V^{-1}S^{-1}$ which increases up to 654 $cm^2V^{-1}S^{-1}$ at cryogenic temperature. This method successfully demonstrates the intrinsic channel behavior with 10^9 ON/OFF ratio and 100 mV/Dec subthreshold swing. The performance limitation of WSe_2 FETs with their channel doping level was also studied.

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