Calibration of pipeline ADC with pruned Volterra kernels

F. Centurelli, P. Monsurrò✉, F. Rosato, D. Ruscio and A. Trifiletti

A Volterra model is used to calibrate a pipeline ADC simulated in Cadence Virtuoso using the STMicroelectronics CMOS 45 nm process. The ADC was designed to work at 50 MSps, but it is simulated at up to 125 MSps, proving that calibration using a Volterra model can significantly increase sampling frequency. Equivalent number of bits (ENOB) improves by 1–2.5 bits (6–15 dB) with 37–101 model parameters. The complexity of the calibration algorithm is reduced using different lengths for each Volterra kernels and performing iterative pruning. System identification is performed by least squares techniques with a set of sinusoids at different frequencies spanning the whole Nyquist band. A comparison with simplified Volterra models proposed in the literature shows better performance for the pruned Volterra model with comparable complexity, improving linearity by as much as 1.5 bits more than the other techniques.

Introduction: Non-linear calibration of pipeline ADCs enables better linearity and higher sampling frequency, correcting errors due to incomplete settling, slew-rate limitations, switches' and amplifiers' non-linearity, and so on. Calibration using Volterra models with iterative pruning, presented in [1] for a sample and hold (SHA) stage, can be extended to pipeline ADCs, and its performance advantage increases with the sampling frequency of the ADC. This approach achieves better linearity with comparable complexity than other simplified Volterra models found in the literature.

Volterra models [2] are meant for weakly non-linear effects. For this reason ADC front-end stages, such as SHAs [1, 3, 4], can be more accurately represented with Volterra models, as they do not contain comparators, which produce heavily non-linear behaviour. More complex models can be expected to be required in ADCs.

Model complexity is a limiting factor in the applicability of Volterra models. An a posteriori approach to reduce the computational complexity of Volterra models was applied in [1] to a SHA stage. For each kernel order, a specific memory length was chosen, and an iterative pruning technique was then used to further reduce complexity.

The literature on ADC calibration usually employs a different approach. Volterra kernels used for generic ADCs are based on a priori hypotheses on the structure of the kernel [4–6] to reduce the number of parameters. We show that these approaches may be less effective, and sometimes ineffective, for the calibration of high-speed pipeline ADCs.

Pipeline ADCs: Pipeline ADCs [7] are composed of several cascaded stages, called MDACs (multiplying DACs). In this Letter, 1.5-bit MDAC stages are used [7]. Radix-based calibration [8] has been used to correct errors in pipeline ADCs such as finite gain and capacitor mismatch [7].

Only the output of the pipeline ADC (after conventional calibration) is used in our non-linear calibration technique. This makes this technique suitable for calibrating off-the-shelf components, as it does not require modifications in the ADC hardware [5].

Volterra models: A Volterra model is composed of kernels of order o and length L. Each kernel is, with output $y_{o,L(o)}(n)$, input $x(n-i_1)$, and model coefficients $h^o_{i_1,i_2,\ldots,i_o}$

$$y_{o,L(o)}(n) = \sum_{i_1=0}^{L}\sum_{i_2=i_1}^{L}\cdots\sum_{i_o=i_{o-1}}^{L} h^o_{i_1,i_2,\ldots,i_o}\Psi_{i_1,i_2,\ldots,i_o}$$
$$\Psi_{i_1,i_2,\ldots,i_o} = x(n-i_1)x(n-i_2)\ldots x(n-i_o) \quad (1)$$

The Volterra model is the sum of the Volterra kernels in an order set O

$$y(n) = \sum_{o\epsilon O} y_{o,L(o)}(n) \quad (2)$$

To reduce model complexity, as in [1], the length of each kernel falls with the kernel order; besides, even-order kernels are neglected or made shorter because of the fully-differential architecture; finally, iterative pruning is applied to minimise complexity.

Reduced-complexity Volterra kernels: Due to the large number of parameters, several a priori approaches have been proposed in the literature, which use only a subset of the Volterra terms [3–6].

In [6], a very compact model is used, as it is a second-order model of mixed products of the input and its derivative, approximated as a central difference. This model can be extended to higher orders.

In [4], a simplified Volterra model was obtained by forcing $h^o_{i_1,i_2,\ldots,i_o} = 0$ for $i_2, i_3, \ldots, i_o \neq 0$ in (1). This model is also used in [9], though in the frequency domain, as described in Subsection III.A in that paper.

In [5], two models are used, called memory polynomial (MP) [10] and modified general memory polynomial [11].

The MP model is the cascade of a memoryless distortion and a linear filter, and is a linear model. The MGMP is the cascade of a linear filter and a memoryless distortion, is non-linear, and has been identified using non-linear optimisation techniques.

A posteriori model simplification: Simulations show that the length required for a given accuracy falls with the order of the kernel, so that short lags can be used for high-order kernels. Besides, even-order distortions are mostly negligible. Furthermore, pruning is used [1]: starting from a model with M parameters, M different models with $M-1$ parameters are evaluated, and the least important parameter is removed. The procedure is repeated as long as performance is satisfactory.

Identification of our proposed model: As in [1, 5], a set of sinusoidal tones spread throughout the Nyquist band is used. Thirty frequencies have been simulated, separated by $f_S/64$ steps. Of these, 22 frequencies have been used for model estimation, and 8 for out-of-sample validation [1], to verify that the model is accurate also for signals not included in the calibration set. Each sinusoidal tone has 64 points.

Simulation results: The simulated ADC has a SHA stage and 16 1.5-bit MDAC stages [7]. The amplifier is a two-stage Miller-compensated operational transconductance amplifier (OTA) with a telescopic cascode as first stage. Reference voltages are buffered, with one buffer per stage. Each stage has a common-mode feedback (CMFB) with resistive-partitioning and a diode-loaded differential pair. All the switches are transmission gates. The reference voltage is 1 V_{pp} differential. The integrated circuit was simulated in the CMOS 45 nm STMicroelectronic process, with 1.2 V power supply. The power dissipation of the ADC is 30 mW. The clock frequency was originally 50 MSps, but it has been pushed up to 125 MSps, thanks to digital calibration. Power consumption does not change appreciably with the clock frequency.

The ADC's signal-to-noise-and-distortion-ratio has been defined as that of the tone from DC to 80% of the Nyquist frequency with the highest distortion. All the 30 frequencies are considered: if the model overfits the data, out-of-sample tones have lower SNDR.

Figs. 1 and 2 show results for kernels described as $\{L_1, L_3, L_5, \ldots, L_{19}\}$ (only odd-order kernels are included [1]). The nominal resolution of the pipeline is the number of MDAC stages plus 1.

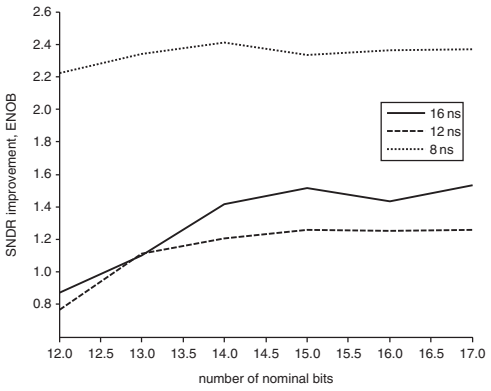

Fig. 1 *ENOB improvement against nominal ADC resolution and sampling period, starting with lag structure {30, 4, 2, 2, 1, 1, 1, 0, 0, 0} for odd orders from 1 to 19. Number of parameters is 162 without pruning*

The Volterra model has been used to simulate both the improvement in the SHA stage alone (assuming an ideal ADC) and of the whole ADC.

The ADC has about 9 bits of ENOB before calibration and close to 11.5 after. The SHA's ENOB is 10.5 bits and reaches 14 bits after calibration.

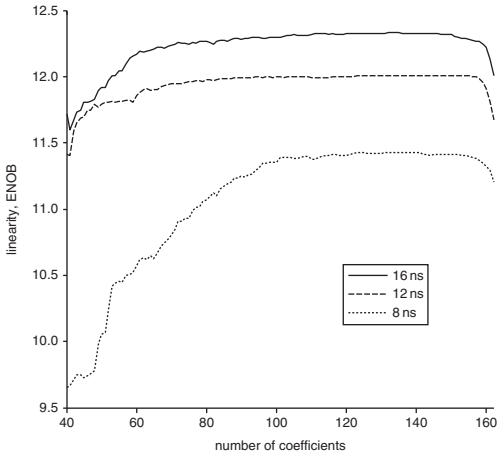

Fig. 2 *ENOB against pruning and sampling period, starting with lag structure {30, 4, 2, 2, 1, 1, 1, 0, 0, 0} for odd kernels from orders 1 to 19*

A memoryless polynomial model with odd-order kernels from 3 to 19 has been simulated: it improves linearity by 0.5 bit at 16 and 12 ns of clock frequency, but it has no effect at 8 ns (125 MSps).

Pruning improves linearity, initially, and reduces model complexity by a factor of about 2.

The models in [4, 6], and in [5, 10, 11] have been used to calibrate our 8 ns sampling time dataset. Table 1 reports the best results we have found for each algorithm. The model [6] is simple but not effective. The MP model in [5] has limited effectiveness (about 0.5 bit peak improvement), with a low parameter count. The MGMP model is marginally better, but more complex. The model in [4] is more effective, yielding a maximum improvement of about 1.2 bits with 205 coefficients, and about 0.9 bit with 21 coefficients. ENOB improvement saturates at 1.2. Our pruned Volterra model achieves performance improvements larger than 1.2 bits, up to 2.5 bits, with a cost from about 40–101 parameters.

Table 1: Linearity improvement and complexity for various models

Reference	Max order	Length	Complexity	ΔENOB
[6]	3–19	–	–	0
[4]	5	3	21	+0.9
	9	20	205	+1.2
[5] (MP)	5	2	6	+0.5
[5] (MGMP)	9	4	20	+0.4
	11	5	30	+0.7
	see Fig. 1		53	+1.5
	see Fig. 1		72	+2.0
	see Fig. 1		101	+2.5

Conclusion: Starting from a Volterra model with odd-order kernels, and lengths dependent on the kernel order (shorter high-order kernels and longer low-order kernels), we have applied the iterative pruning technique to a switched capacitor pipeline ADC.

The ADC was designed to work at 50 MSps, but was simulated at 66.7, 83.3, and 125 MSps to determine the effectiveness of the calibration technique in correcting for heavily non-linear incomplete signal settling.

We have then compared our calibration technique, using our 125 MSps dataset, with others reported in the literature. Our approach is shown to be more effective, reaching higher linearity with comparable complexity.

Pipeline ADCs, as opposed to SHA front-end stages, are heavily non-linear because their input–output characteristic depends on the sub-ADCs inside the MDACs (two comparators in the case of 1.5-bit stages) [12]. Volterra models are thus less effective for the ADC as a whole and larger models are required to achieve a given linearity improvement. Despite this, a performance improvement between 6 and 15 dB is possible, with models from 37 to 101 coefficients. Even-order distortions are usually lower than odd-order ones in fully-differential structures, and in [1] a few additional even-order terms were sufficient to correct them.

It is possible to enhance performance for pipeline ADCs driven at much higher sampling frequencies than the nominal one, as the Volterra model can correct for the effects of the non-linear dynamics of the circuits. The performance improvement is in fact particularly significant for the largest simulated sampling frequency of 125 MSps.

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