PI and Fuzzy Control Strategies for High Voltage Output DC-DC Boost Power Converter – Hardware Implementation and Analysis

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***Abstract*–This paper presents the control strategies by Proportional-Integral (P-I) and Fuzzy Logic (FL) for a DC-DC boost power converter for high output voltage configuration. Standard DC-DC converters are traditionally used for high voltage direct current (HVDC) power transmission systems. But, lack its performances in terms of efficiency, reduced transfer gain and increased cost with sensor units. Moreover, the internal self-parasitic components reduce the output voltage and efficiency of classical high voltage converters (HVC). This investigation focused on extra high-voltage (EHV) DC-DC boost power converter with inbuilt voltage-lift technique and overcome the aforementioned deficiencies. Further, the control strategy is adapted based on proportional-integral (P-I) and fuzzy logic, closed-loop controller to regulate the outputs and ensure the performances. Complete hardware prototype of EHV converter is realized and experimental tasks are set out with digital signal processor (DSP) TMS320F2812 under different perturbation conditions. Observed set of results is provided and shown good conformity with developed hypothetical predictions.**

***Index Terms*–DC-DC boost converter, proportional-integral (P-I) controller, fuzzy controller, voltage-lift technology, HVDC power converter.**

I. Introduction

In transportation systems, both electric vehicles (EVs) and hybrid electric vehicles (HEVs), DC-DC boost power converters (BPC's) find widely employed [1-4]. Moreover, the recent transmission system is shifting towards high voltage direct current (HVDC) systems and classical DC-DC BPC plays vital role in the generation and DC link enhancing capabilities [1-3]. In EVs applications, input power is supplied by 42V battery banks and is boosted to around 300V during start-up by DC-DC converter [2]. But the output performances are suffering, due to limited power transfer ratio (k) by the internal parasitic effects of switching (IGBT/MOSFET) devices and also due to passive components that contributes circuit configuration. Moreover, the output performances also restrict by digital controller in application and gate driving circuits due to their parasitic effect by nature. Numerous, topologies addressed and focused to meet the HV requirements, but suffers with aforementioned limitations in the outputs [1], [4-13].

Investigations are focused with transformer-less DC-DC boost resonant converter for higher output voltages, includes four semiconductor devices to shape the full-wave output [4-5]. However, the topology restricts the switching frequency up to 10 kHz for limiting the switching losses and to increase efficiency. Furthermore, the converter cascaded structures of six MOSFETs are proposed for high output voltages and which comparatively require complex control algorithm [6-8]. On the other hand, the transformer based configuration are investigated and proposed to obtain high-voltage gain, but with an increased number of switches [9-11] But, the structure is bulky and requires highly expensive devices. Also, the increased switching devices make the control strategy furthermore complex leads to limit the efficiency and power transfer capabilities [6-11]. Motivated by the above facts, this paper investigates the DC-DC converter with integrated voltage-lift technique and owing to its simpler control P-I and fuzzy logic scheme with the higher transfer gain on output [12-16]. The voltage-lift technique provides a staircase geometrical progression arrangement to increment the output voltage. Extra HV (EHV) DC-DC boost power converter (BPC) reconfigured from the classical buck converter with voltage-lift by the inclusion of additional few passive (inductor/capacitor) components. Advantages of the EHV power converter add the below [12-16]:

- By increasing output transfer-gain (k) ratio.
- By simple control algorithm with wide range of operation.
- By reducing output ripple levels.
- By increasing power density and efficiency.
- By the one sensor requirement (voltage feedback) for controlling strategies of P-I and fuzzy logic/

The prototype version of hardware EHV DC-DC BPC is realized with digital signal processor (DSP) TMS320F2812 platform. This investigation, study in this paper focused on the simple control strategy of P-I and fuzzy logic for comparative performances under different perturbation conditions. The

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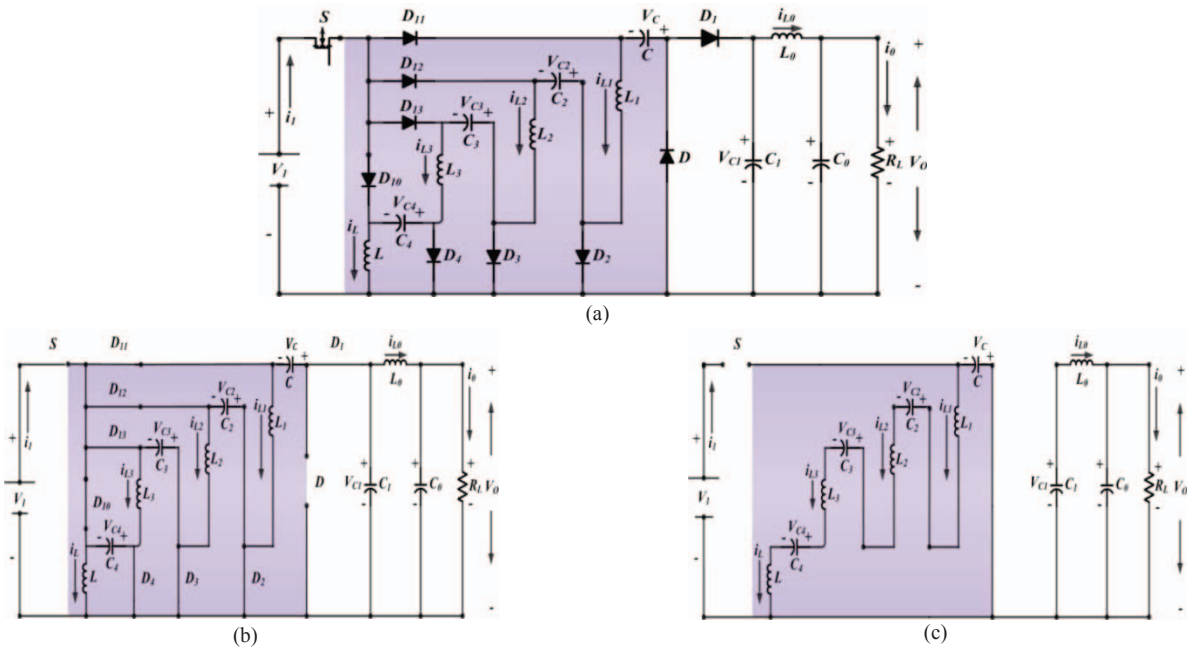


Fig. 1. (a) Schematic circuit of extra high voltage (HV) DC-DC boost power converter configuration; (b) Equivalent circuit when switch ON-state; (c) Equivalent circuit when switch OFF-state

TMS320F2812 processor performs the algorithm of P-I and fuzzy logic, and PWM generation for *n*-channel MOSFET. Set of observed experimental results are provided and shown close conformity with the analytical predictions.

This paper is organized as follows as the EHV boost power circuit is illustrated in section II with the mode of operation (ON and OFF) states. Design and implementation of P-I and fuzzy logic controller are elaborated in section III. Experimental verification results are provided in section IV. Finally, concludes this research paper work.

II. EHV DC-DC Power Circuit and Theoretical Analysis

The EHV DC-DC BPC circuit is shown in Fig. 1(a) [12-14]. The load voltage (V_O), load current (i_O), the supply voltage (V_1), supply current of the power circuit (i_1) are described by the same Fig. 1(a). In detail, power circuit consist of a *N*-channel MOSFET as static switch *S*, and diodes (*D, D1,..., D13*). The voltage-lift circuit is configured by inclusion of additional capacitors (*C, C1,..., C4*) and inductors (*L, L0,..., L3*). To be noted, the lift in gain is actually obtained by the capacitors (C_2, C_3, C_4), where the capacitor voltage V_c is built-up by four times (transfer gain ratio) of the battery input voltage V_S (V_{CO}=V_{C1}). For continuous conduction mode, assumed that all components are ideal, capacitors are large enough. In detail, when the switch *S* is turned ON, circuit configuration as described with voltages and currents direction by Fig. 1(b). The instantaneous input current (i_1) equal to sum of all capacitor and inductor currents, except i_{CO} and i_{C1}. The load current (i_O) flows depending to the sum of the battery voltage V_1 and the capacitor voltage V_C. Whereas, the capacitors C_2, C_3, and C_4 are charged by the input voltage and all inductor currents increased leads to first interval of investigation. The equivalent circuit when instant switch *S* is turned OFF is described along with voltages and currents direction by Fig. 1(c). The instantaneous input current (i_1) equals to zero. The voltage-lift (L_1, L_2, L_3 and L), inductor store the energy, whereas the C_2, C_3 and C_4 capacitor discharge the stored energy. Corresponding directions of discharge the capacitor C are described by Fig. 1(c). The load current i_{L0} flows through the through the inductor and decreases the current to second interval of investigation. Now, the steady–state average inductor voltage is written as [12-14]:

$$V_{CO} = V_O \tag{1}$$

Voltages are given as below when switch S during ON state:

$$V_{C2} = V_{C3} = V_{C4} = V_1 \tag{2}$$

Also:

$$V_O = V_{C1} = V_C + V_1 \tag{3}$$

Now, the voltages across the inductor L is expressed as:

$$kTV_1 = (1\text{-}k)\ TV_{L\text{-}OFF} \tag{4}$$

$$V_{L\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \tag{5}$$

To be noted, the inductor current I_L will increase when the switch S is turned ON and will decrease when switch *S is* turned OFF. Further, the voltages across inductors (L_1, L_2, L_3) are calculated as:

$$V_{L1\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \tag{6}$$

$$V_{L2\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \tag{7}$$

$$V_{L3\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \tag{8}$$

By Fig. 1(c) the analytical determination of the capacitor voltage V_C and output voltage V_O are written as:

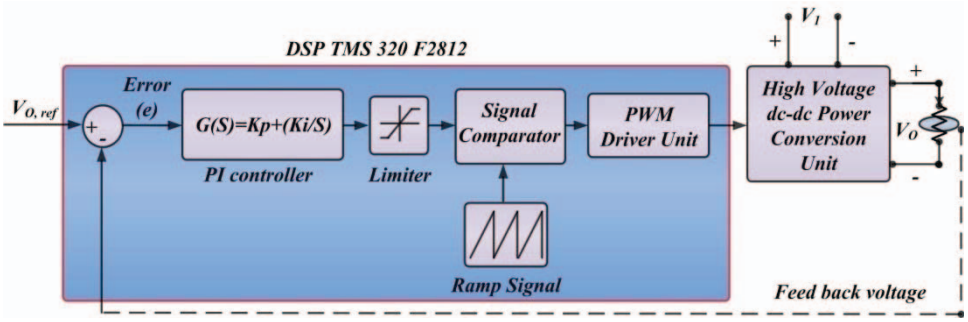


Fig. 3. Schematic of simple P-I control strategy with one sensing unit for DC-DC BPC under test for perturbation conditions.

$$V_C = V_{C\text{-}OFF} = V_{L\text{-}OFF} + V_{L1\text{-}OFF} + V_{L2\text{-}OFF} + V_{L3\text{-}OFF} + V_{C2} + V_{C3} + V_{C4} \quad (9)$$

$$V_C = 4k/(1-k)\ V_1 + 3V_1 \quad (10)$$

$$V_O = V_C + V_1 \quad (11)$$

$$V_O = [4/(1-k)]\ V_1 \quad (12)$$

Therefore, the gain transfer ratio of output current and voltage are predicted as:

$$i_O = [(1-k)/4]\ i_1, \quad (13)$$

$$M_O = 4/(1-k). \quad (14)$$

The average voltages and currents are now represented as:

$$V_C = [(3+k)/(1-k)]\ V_1, \quad (15)$$

$$V_{C1} = V_O, \quad (16)$$

$$V_{C2} = V_{C3} = V_{C4} = V_1. \quad (17)$$

$$i_{LO} = i_O, \quad (18)$$

$$i_L = [k/(1-k)]\ i_O, \quad (19)$$

$$i_{L1} = i_{L2} = i_{L3} = i_L + i_{LO} = [1/(1-k)] i_O \quad (20)$$

A comparative illustration between EHV DC-DC BPC and classical BPC are given in Table I with respect to output transfer gain ratio *k*. Correspondingly Fig. 2 proves the effectiveness by showing output generated voltages versus duty ratio. The investigated DC-DC BPC (red bar) output voltage varies in the range of 44.44V to 400V, whereas the classic DC-DC BPC (blue bar) varies in the range of 1.11V to 90V. To be noted, output transfer gain (duty ratio) k = 0.1 to 0.9 variation is set with parameters taken from Table II. Hence, it could be confirmed that the converter produced high output voltage due to the inclusion of additional passive (L, C) components and proven by Eq. 12.

TABLE I. COMPARATIVE PERFORMANCE EMPHASIS THE INVESTIGATED WITH CLASSICAL DC-DC BPC.

Converter Type	Output Voltage (V_0) (Volts)	Output Current (i_0) (Amps)
Classical Converter	$V_0 = [k/(1-k)]\ V_1$	$i_0 = [(1-k)/k]\ i_1$
Proposed Converter	$V_0 = [4/(1-k)]\ V_1$	$i_0 = [(1-k)/4]\ i_1$

III. CONTROL STRATEGIES BASED ON PI AND FUZZY LOGIC

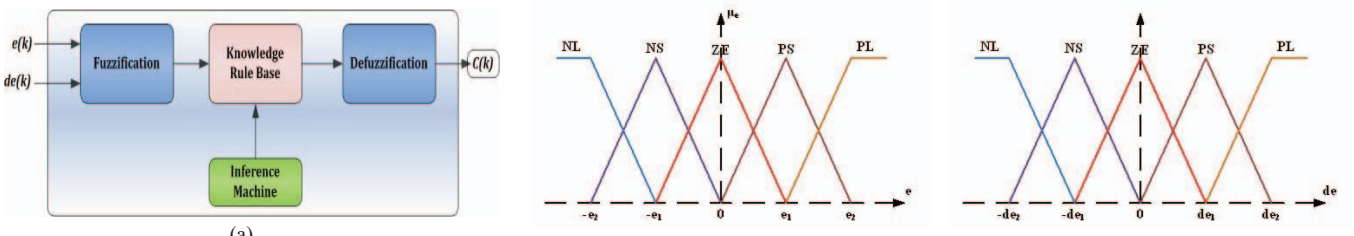
TABLE II. SIMULATION PARAMETERS TAKEN FOR INVESTIGATION.

Parameter		Value
Input Voltage	(V_1)	10 V
Inductance	(L)	100µH
Capacitance	(C)	5µF
Load Resistance	(R)	44 ohms
Duty Ratio	(k)	2/3
Switching	(F_{SW})	50 KHz
Digital Processor	**DSP**	TMS 320F2812
***N*-channel MOSFET**	**(IRFPC60)**	V_{DSS}= 600V, $R_{DS(ON)}$= 0.40Ω, I_D=16A

A classic P-I controller algorithm is adapted for EHV DC-DC BPC and shown by Fig. 3. It is notably that control scheme consists of one voltage sensor feedback. Further, compared with the set voltage $V_{O,\ ref}$ reference to calculate the error between the reference and actual DC bus voltage. Furthermore, the error signal now applied to the P-I regulator to compensate the error. The manipulated signal obtained from the P-I defined as the set duty ratio k and compared with high frequency ramp-signal for the purposes of generating controlled pulse-width modulated (PWM) signal to the static S switch. To be noted, the parameters (P-proportional gain, I-integral gain) are tuned according to the condition illustrated in the reference work [12-15].

A schematic block diagram of generalized rule based fuzzy logic controller (FLC) is elaborated by Fig. 4(a), where *e(k)* denotes the input error and *de(k)* denotes the rate of change in the input variables. The FLC block is composed of fuzzification interface, fuzzy rules, and inference and de-fuzzification mechanism. The FLC has two inputs where one is error signal *e(k)* and other is change in error signal *de(k)*, and the output *c(k)* which represents the control component to generate the switching signal for n-channel MOSFET switch.

First process, the crisp variables *e(k)* and *de(k)* are converted to fuzzy variables such as *E(k)* and *dE(k)* using the triangular membership functions and shown by Fig. 4(b) and Fig. 4(c). Each universe of discourse divided into five fuzzy sets: NL (negative large), NS (negative small), ZE (zero), PS (positive small) and PL (positive large). Further, each fuzzy variable is a member of the subsets with a degree of membership varying between 0 (non-member) and 1 (full-member) [17-20]. A second process, the fuzzy variables *E(k)* and *dE(k)* are operated by inference engine and that executes a set of control 5×5 rules and given by Table III. These rules are based on the dynamic of the error signal behavior, resulting in



(a) (b) (c)

Fig. 4. (a) Fuzzy logic rule based system generalized structure. Membership function of the fuzzy logic controller, (b) membership function of error (*e*), (c) membership function of change-in-error (*de*).

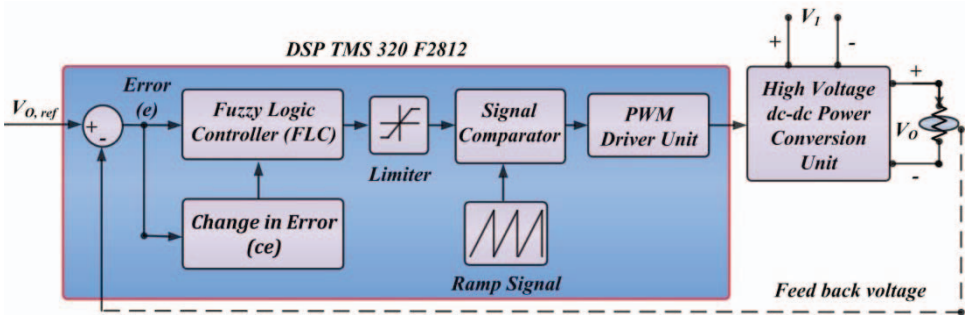


Fig. 5. Schematic of fuzzy control strategy with one sensing unit for DC-DC BPC under test for perturbation conditions.

symmetrical matrix. Generalized rule-based design with 2-D phase plane and expressed as below:

Rule: *If x is A and y is B then z is C.*

The different inference algorithm is available to space the fuzzy set values for the output fuzzy variable *c(k)*. During this investigation, the max-min inference is adapted, membership degree equal to the maximum of the product of *E* and the *dE* membership degree. Furthermore, the output variables from the inference engine are converted into a crisp value in the de-fuzzification stage. Several de-fuzzification algorithms are available and this work, the centroid de-fuzzification algorithm is implemented. In which the crisp values are calculated as the center of gravity of the membership function. The definition of the spread of each partition, or conversely the width and symmetry of the membership functions, is generally a compromise between dynamic and steady state accuracy. Equally, spaced partitions and consequently symmetrical triangles are reasonable choices [17-19].

TABLE III. MATRIX FORMULATION (5X5) FOR FUZZY LOGIC RULES.

e(k) / *de(k)*	NL	NS	ZE	PS	PL
NL	NL	NL	NL	NS	ZE
NS	NL	NL	NS	ZE	PS
ZE	NL	NS	ZE	PS	PL
PS	NS	ZE	PS	PL	PL
PL	ZE	PS	PL	PL	PL

A complete control scheme based on FLC for the EHV DC-DC BPC is illustrated by Fig. 5. Experimental test is executed in both variable load/line regulation conditions using dsp processor with resistive load. The obtained results are compared with developed theoretical background and discussed in detail in the next section.

II. PROTOTYPE HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

A prototype hardware module of the EHV DC-DC BPC is realized using (DSP) TMS 320F2812 processor and parameters are taken from Table II. The control strategies of P-I and fuzzy logic algorithm are executed with the DSP and the event manager unit of PWM generates the controlled pulse signals to n-channel MOSFET. The inductance and capacitance values of the power circuit are designed to the criteria of 5% output ripple factor as per IEEE standards [12-15]. Fig. 6(a) and Fig. 6 (b) depicts the P-I control strategy, experimental behaviors of output voltage and current at the rated conditions (set output voltage 120V, load resistance 44Ω and duty ratio k = 2/3). It is noticed that the output voltage settles at 119.8V with 1.0833% peak overshoot, 200mv steady state value and 1 Sec settling time. Hence, closely matches the hypothesis given by Eq. 12 in k = 2/3. The output current 2.722A with 1.0833% peak overshoot and 1 Sec settling time is observed and correspondingly shown close conformity with the hypothesis given by Eq. 13. Fig. 6(c) and Fig. 6 (d) depicts the fuzzy logic control strategy, experimental behaviors of output voltage and current at the rated conditions (set output voltage 120V, load resistance 44Ω and duty ratio k = 2/3). It is noticed that the output voltage settles at 119.925V with 1.016% peak overshoot and 0.4 Sec settling time. Hence, closely meets the hypothesis given by Eq. 12 in k = 2/3. The output current 2.7255A is observed with 1.016% peak overshoot and 0.4 Sec settling time is observed and correspondingly shown close conformity with the hypothesis given by Eq. 13. Fig. 7(a) and Fig. 7 (b) emphasize the P-I control strategy, experimental behaviors of output voltage and current obtained under line and load regulatory conditions. It could be noticed that the output voltage and current are stabilized with 1 Sec and peak overshoot 1.125%, while the battery voltage source undershoot a perturbation of 10V to 9V.

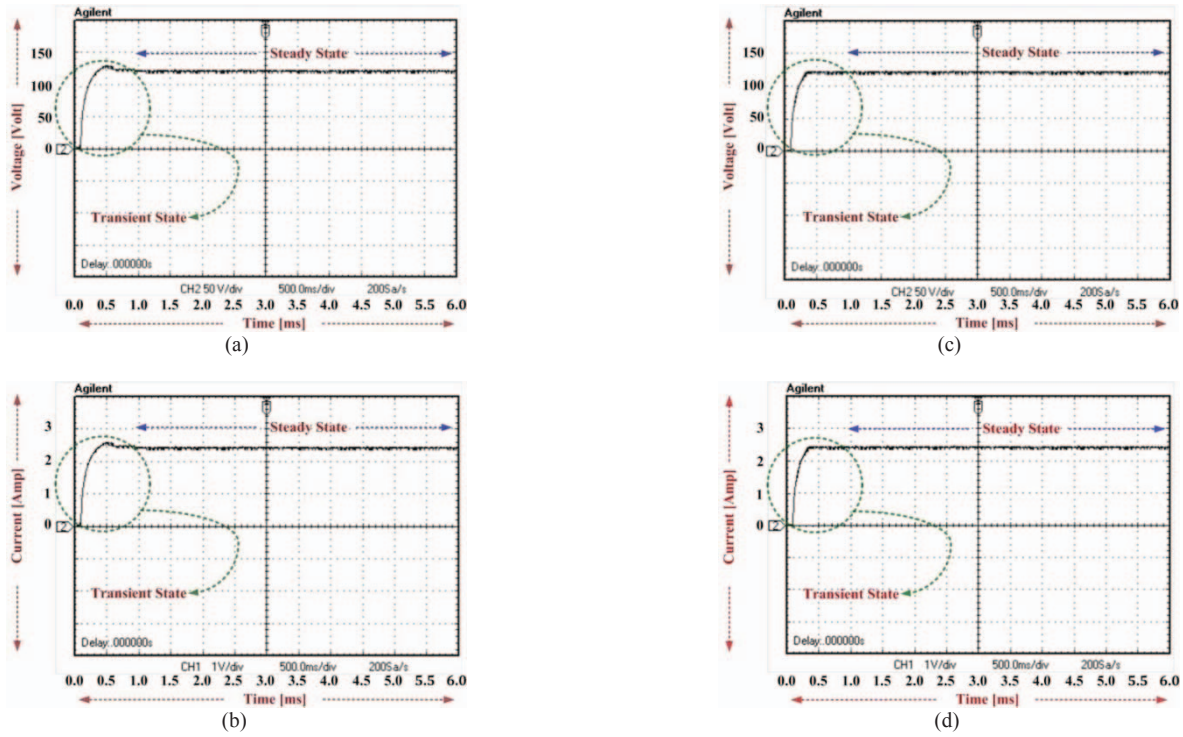


Fig. 6. Experimental behavior of P-I and fuzzy controller strategies adapted for EHV BPCin transient, line/load perturbation & steady-state conditions. P-I: (a) output voltage, (b) output current. Fuzzy: (c) output voltage, (d) output current. [50v/div, 2A/div].

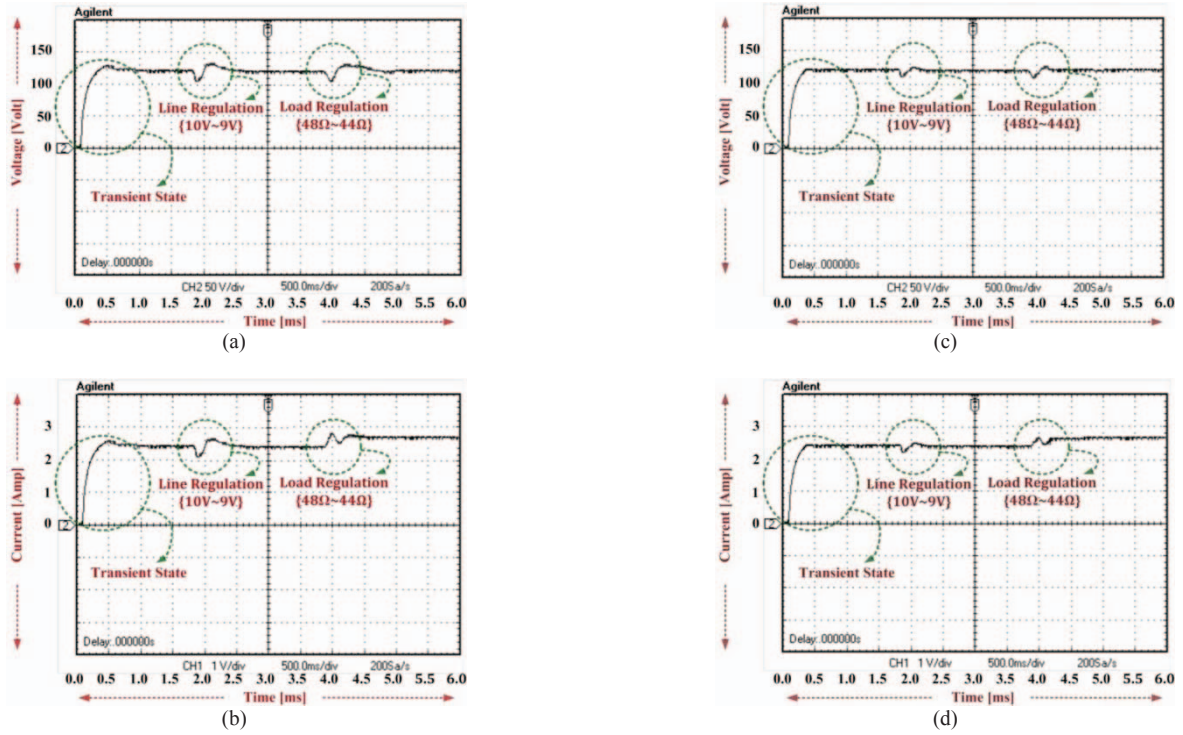


Fig. 7. Experimental behavior of P-I and fuzzy controller strategies adapted for EHV BPCin transient, line/load perturbation & steady-state conditions. P-I: (a) output voltage, (b) output current. Fuzzy: (c) output voltage, (d) output current. [50v/div, 2A/div].

Furthermore, the load resistance varies from 48Ω to 44Ω, but the output voltage retains 119.8V and output current 2.722A. During the load regulation, it is also observed 1.125% peak overshoot and 1.2 Sec as the settling time. To be noted the

output voltage and current results shown close conformity with the hypothesis given by Eq. 12 and Eq. 13. Fig. 7(c) and Fig. 7(d) emphasizes the fuzzy logic control strategy, experimental behaviors of output voltage and current obtained under line and load regulatory conditions. It could be noticed that the output voltage and current are stabilized with 0.28 Sec and peak overshoot 1.0416%, while the battery voltage source undershoot a perturbation of 10V to 9V. Furthermore, the load resistance varies from 48Ω to 44Ω, but the output voltage retains 119.925V and output current 2.7255A. During the load regulation, it is also observed 1.0666% peak overshoot and 0.25 Sec as the settling time. To be noted the output voltage and current results shown close conformity with the hypothesis given by Eq. 12 and Eq. 13. Experimental performance criteria are summarized and given in the Table IV. It is confirmed that the control strategy by fuzzy logic shown minimal peak overshoot and quick settling time with lesser steady error in comparisons to P-I strategy. Moreover, practically it is verified that generated outputs losses in the range of Milli-amplitude and practically appreciable.

TABLE IV. PERFORMANCE COMPARISON BETWEEN P-I AND FUZZY LOGIC CONTROLLER.

Performance Parameters	P-I	Fuzzy Logic
Peak over-shoot (M_p)	1.0833%	1.016%
Settling time (t_s)	1 Sec	0.4 Sec
Steady state error (*ess*)	200mv	75mv
Overshoot in line variations	1.125%	1.0416%
Undershoot in line variations	1.15%	1.0833%
Overshoot in load variations	1.125%	1.0666%
Undershoot in load variations	1.15%	1.0833%
Settling time in line variations	1 Sec	0.28 Sec

V. CONCLUSIONS

This article presented the simple control strategy based on P-I and Fuzzy Logic for an EHV DC-DC boost power converter. Investigated power circuit is derived from the standard buck DC-DC converter with the inclusion of voltage-lift techniques to overcome parasitic effects and to generate higher output voltage reduced ripples (voltage/current). The complete prototype model is implemented using (DSP) TMS 320F2812 processor with resistive load. Observed experimental results are provided in this paper. The fuzzy logic control strategy, shown better performances in different designed perturbation conditions, when compared to standard P-I strategy. Furthermore, the experimental results shown good agreement with theoretical background and shown suitable for high-voltage applications.

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