Single-Phase Seven-Level Stack Multicell Converter Using Level Shifting SPWM Technique

Sanjeevikumar Padmanaban
Research and Development
Ohm Technologies, Chennai, India..
sanjeevi_12@yahoo.co.in

Pierluigi Siano
Dept. of Industrial Engineering
University of Salerno, Salerno, Italy.
psiano@unisa.it

Ahmet H. Ertas
Dept. of Biomedical Engineering, Faculty of
Engineering, Karabuk Univesity, Kurbuk, Turkey.
ahertas@karabuk.edu.tr

Rajasekar Selvamuthukumaran
Technology Department, Power Grid Corporation of India Limited,
Gurgaon, India.
rajasekar6387@gmail.com

Pandav Kiran Maroti
Dept. of Electrical & Electronics Engg.,
Marathwada Institute of Technology,Aurangabad, India.
kiranpandav88@yahoo.co.in

Abstract— This paper presents a single-phase seven-level stack multicell converter (SMC) which provides a viable solution for multilevel converter. Conventional cascaded multilevel inverter (MLI) removes the drawbacks of clamping diodes and clamping capacitors topologies. However, in a cascaded MLI number of voltage source and power switches increases as the number of level increases. The main advantage of single-phase SMC converter is only two DC sources are needed for any number of levels. Level shifting SPWM technique has been incorporated to achieve gate pulses, in which carrier wave of 20kHz is compared with 50Hz sinusoidal reference wave at a modulation index of 1 and 0.9. Total harmonic distortion (THD) for SMC converter is achieved at 1.55% and 5.26% with and without filter respectively. The seven-level SMC topology is simulated in MATLAB/SIMULINK and simulation results are provided to verify the performance.

Keywords—Multilevel Inverter (MLI); Stacked Multicell converter (SMC); SPWM Technique; Modulation Index; Total Harmonic Distortion (THD).

I. INTRODUCTION

In recent year, DC-AC multilevel converter topologies provide a feasible solution for the medium and high voltage applications in the power industries [1-2]. Conventional H-bridge two level inverter is incapable to produce waveform closer to sinusoidal and therefore, large harmonic content present in the output. It is also not suited for high power applications due to high voltage stress across switches. Consequently, to remove the above drawbacks conventional H-bridge inverter is replaced by a multilevel inverter (MLI) [3]. The MLI is employed to obtain nearly sinusoidal output waveform and also have the capability to work with voltage in the range of kilovolts to megavolts. Hence, MLI gained popularity in the field of High power.

Conventional multilevel inverter (MLI) topologies include three types, namely diode clamped MLI, flying capacitor MLI and cascaded MLI topologies [4-5]. Total harmonic distortion is reduced as number of level increases. In diode clamped MLI, the number of switches and diodes are increasing as number of level increases [5]. In [6], diode clamped MLI with reduce number of clamping diode is discussed. The drawback of diode clamped MLI is overcome by flying capacitor MLI. However, the number storage capacitors and switches are

increasing as the number of levels is increasing. In [7], flying capacitor MLI with reduced number of clamping capacitors is discussed. The conventional cascaded MLI is introduced to overcome the drawback of diode clamped MLI and flying capacitor MLI [1-4]. Conventional MLI required the least number of power devices compared to diode clamped and flying capacitor MLI. Thus modularized circuit layout and packaging is possible, but, in cascaded MLI separate DC sources and power devices are increasing as the number of level increases. Further, the drawback of the large number of switches is overcome by modifying cascaded MLI discussed in [8-11]. The asymmetrical multilevel inverter provides a suitable solution in order to achieve a large number of levels with less number of supplies. The main drawback of asymmetrical MLI is that voltage stress across power devices is unequal [12-14]. The drawback of above discussed MLI topologies are overcome by SMC topology [15-16].

In this paper single-phase SMC converter is present with level shifting SPWM technique. The SMC topology is simulated for seven-levels in MATLAB/SIMULINK and simulation results are provided to verify the performance.

II. PX2 STACK MULTICELL CONVERTER

A stack multicell converter based on the basic commutation cell (See Fig.1) and classified as a multilevel converter. A commutation cell consists of two devices which operating in complementary states. The topology of PX2 stack multicell converter (SMC) is designed by a P number of cell (column) and 2 number of stack (rows). The arrangement of PX2 SMC is shown in Fig.2. Each cell (column) of PX2 SMC is made up of by two basic commutation cells. Therefore, a $2P$ number of basic commutation cell is needed to design PX2 SMC. Single-phase SMC requires only two voltage sources which are connected to 1st cell and intermediate capacitors are used as a voltage source connected between two adjacent cells. $2P$-2 number of capacitors and $4P$ number of power switches is required to design PX2 stack multicell converter.

Switches S_1 to S_P and S_{P+1} to S_{2P} are used to generate positive and negative level respectively. PX2 SMC is capable to generate a 2P+1 number of levels. The voltage across it

intermediate capacitor (i [2, 4 … 2P-2]) is equal to Eq. 1 as below:

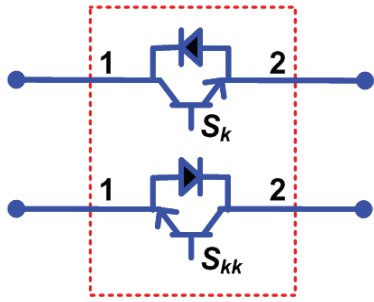$$V_{C_i} = V_{C_{i-1}} = \frac{(2P - i)V_{in}}{4P} \tag{1}$$
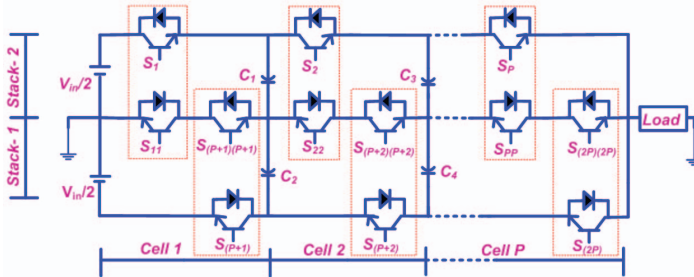

Fig. 1. Basic Commutation Cell.

Fig. 2. PX2 Stack Multicell Converter.

III. PRINCIPAL OF OPERATION

In this section, operation of 7 level (3X2) SMC is briefly described. The circuit diagram of seven-level SMC is shown in Fig.3. The topology of seven-level SMC is made by 3 number of cell (column) and 2 number of stack (row). Proposed SMC needs 2 voltage sources, 6 commutation cells (12 power switches), 4 capacitors as per design. The voltage across capacitor C_1 and C_2 is Vin/3 in cell-1. The voltage across capacitor C_3 and C_4 is Vin/6 in cell-2. Switch pair S_1 and S_{11} operate in complementary states. Similarly, other pairs (S_2, S_{22}), (S_3, S_{33}), (S_4, S_{44}), (S_5, S_{55}) and (S_6, S_{66}) are operated in the same manner. Switches S_1, S_2 and S_3 are used to generate three positive levels. Switches S_4, S_5 and S_6 are used to generate three negative levels. Vin/6, Vin/3, Vin/2, 0, -Vin/6, -Vin/3 and -Vin/2 output voltage levels are obtained from seven-level (3X2) SMC. The possible switch combination of each level is given in TABLE-I. '1' and '0' is indicates switch position i.e. on and off respectively. There are three possible combinations of the switches to obtain voltage level Vin/6, Vin/3, -Vin/6 and -Vin/3.

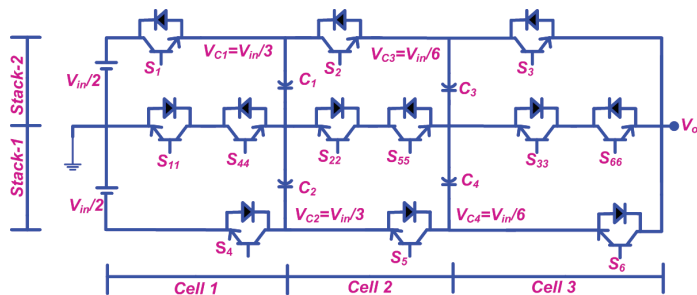Fig. 3. Seven-level (3X2) Stack multicell converter.

Highest positive (Vin/2) level is generated when all upper switches (S_1 to S_3) and all lower switches (S_4 to S_5) are turn

ON and turn OFF respectively. Similarly the highest negative level (-Vin/2) is generated when all upper switches (S_1 to S_3) and all lower switches (S_4 to S_6) are turned OFF and turn ON respectively. Vin/3 voltage level is generated by a combination of any two switches from upper stack (S_1 to S_3) are turning ON and all lower switches (S_4 to S_6) are turning OFF. Similarly the voltage level (-Vin/3) is generated by a combination of any two switches from a lower stack (S_4 to S_6) are turned ON and all upper switches (S_1 to S_3) are turning OFF. Vin/6 voltage level is generated when any one switch from upper stack (S_1 to S_3) is turned ON and all lower switches (S_4 to S_6) are turning OFF.

TABLE I. POSSIBLE SWITCH COMBINATION OF 3X2 SMC

| Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6
Vin/2	1	1	1	0	0	0
Vin/3	0	1	1	0	0	0
	1	1	0	0	0	0
	1	0	1	0	0	0
Vin/6	0	0	1	0	0	0
	0	1	0	0	0	0
	1	0	0	0	0	0
0	0	0	0	0	0	0
-Vin/6	0	0	0	0	0	1
	0	0	0	0	1	0
	0	0	0	1	0	0
-Vin/3	0	0	0	0	1	1
	0	0	0	1	1	0
	0	0	0	1	0	1
-Vin/2	0	0	0	1	1	1

Similarly the voltage level (-Vin/3) is generated when any one switch from lower stack (S_4 to S_6) is turn ON and all upper switches (S_1 to S_3) are turn OFF. zero level is obtained when all upper and lower (S_1-S_6) switches are turn OFF. Current direction for positive levels, including zero level, negative level is shown in the Fig.4 (a)-(d) and Fig. 5(a)-(c) respectively.
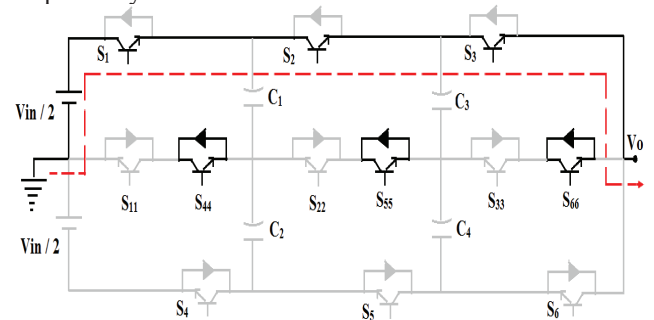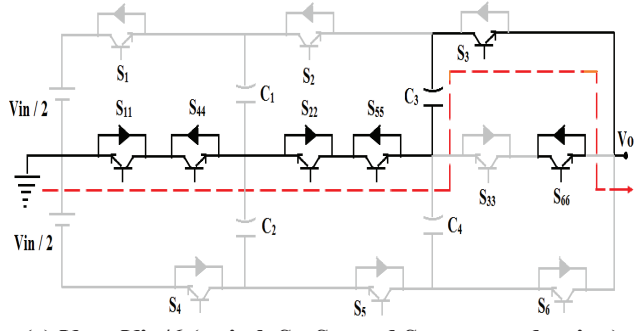

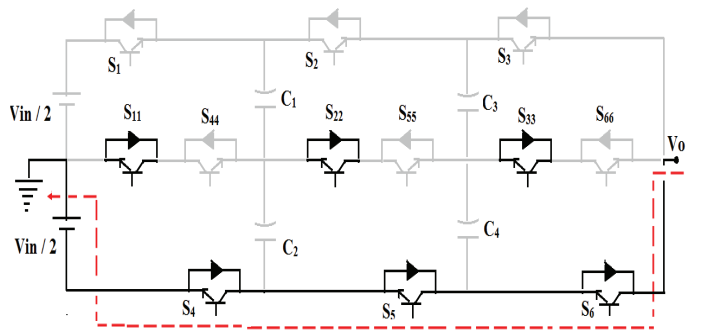
(a) Vo = Vin/2 (switch S_1, S_2, S_3 are conducting)
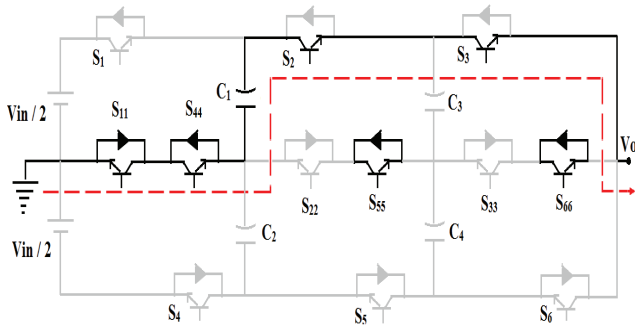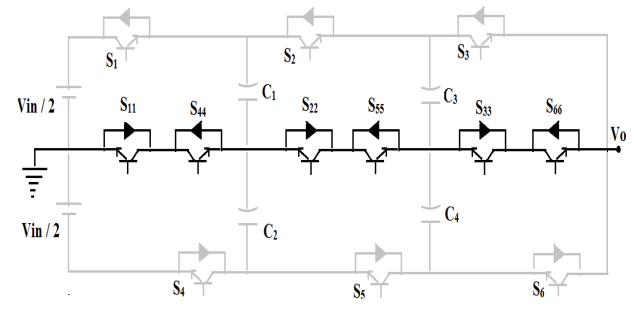
(b) Vo = Vin/3 (switch S₂, S₃ and S₄₄ are conducting)
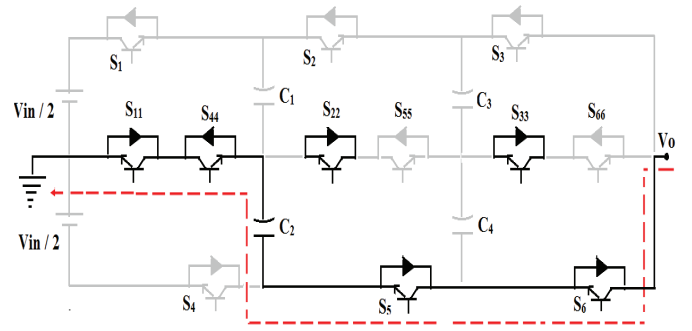
(b) Vo = -Vin/3 (switch S₅, S₆ and S₁₁ are conducting)

(c) Vo = Vin/6 (switch S₃, S₄₄ and S₅₅ are conducting)

(c) Vo = -Vin/2 (switch S₄, S₅ and S₆ are conducting)

Fig. 5 (a)-(c). Current directions for negative level.

(d)Vo =0 (all upper and lower switches are turned OFF)

Fig.4. (a)-(d). Current directions for positive level.
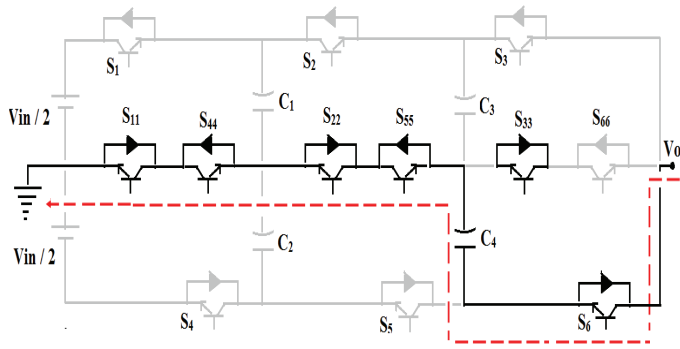
(a) Vo = -Vin/6 (switch S₆, S₁₁, S₂₂ are conducting)

IV. SIMULATION RESULTS

A SMC is simulated in MATLAB/SIMULINK for 3 Cell (column) and 2 stacks (row) i.e. 3X2 SMC. 3X2 SMC generates seven-levels output; three positive levels, one zero level and three negative levels. Level shifting SPWM technique has been incorporated to achieve gate pulses in which carrier wave of 20kHz is compared with 50Hz sinusoidal wave reference at modulation index of 1 and 0.9. 3X2 SMC converter is designed for 10V and 9V output voltages. Level shifting SPWM technique with modulation index 1.0 and 0.9 is used to generate driving pulses for switches (see Fig.6 and Fig.10 respectively). The generated PWM driving pulses when modulation index is 1.0 are shown in Fig.6. The 10V output voltage of 3X2 SMC before and after filter is shown in Fig.7 and Fig.8 respectively. Phase current after filter for 10V is shown in Fig.9. The generated driving pulses when modulation index is 0.9 are shown in Fig.10. The 9V output voltage of 3X2 SMC before and after filter is shown in Fig.11. and Fig.12. respectively. Phase current after filter for 9V is shown in Fig.13. The total harmonics distortion (THD) frequency response of output voltage is before and after filter is shown in Fig.14 and Fig.15 respectively. Total harmonics distortion (THD) harmonic order response of output voltage is before and after filter is shown in Fig.16 and Fig.17 respectively. It is observed that fundamental voltage of 9.994V with THD 5.26% is obtained before filter. Also, it is observed that fundamental voltage of 9.99V with THD 1.54% is obtained after filter.
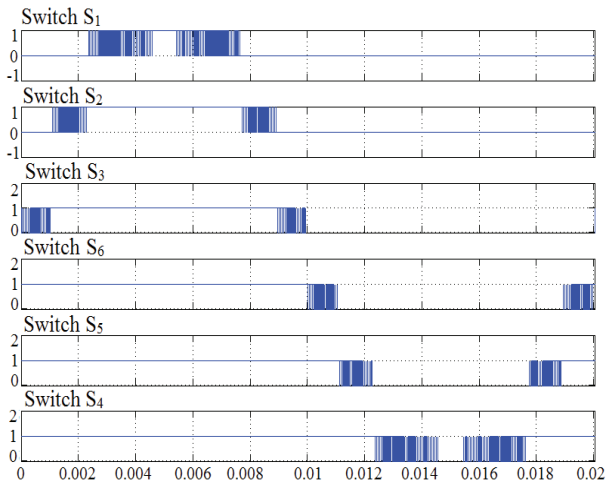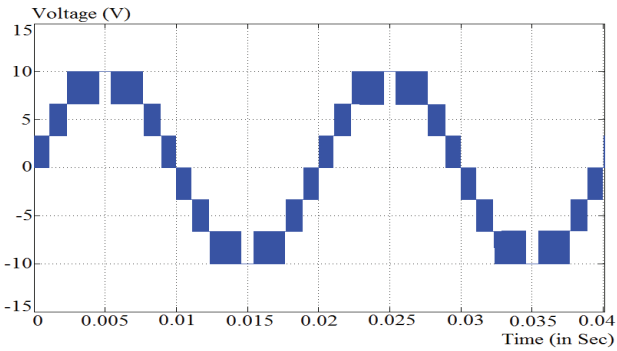
Fig.6. PWM Driving Pulses [10volt output].
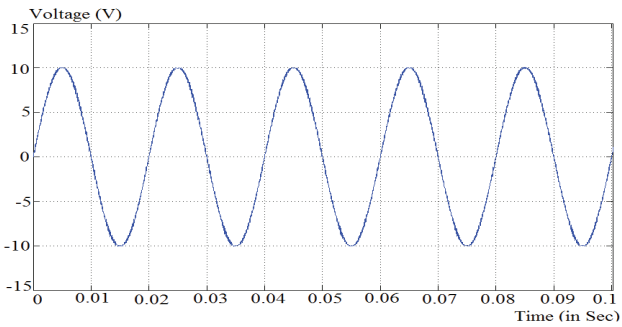

Fig.10. PWM Driving Pulses [9volt output].

Fig.7. Phase Voltage before filter [10volt output].
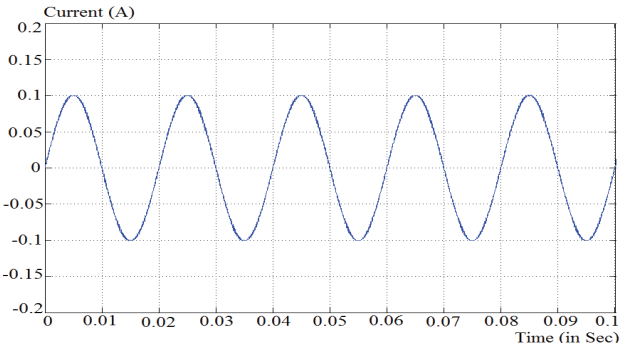

Fig.11. Phase Voltage before filter [9volt output].

Fig..8. Phase Voltage after filter [10volt output].

Fig.12. Phase Voltage after filter [9volt output].
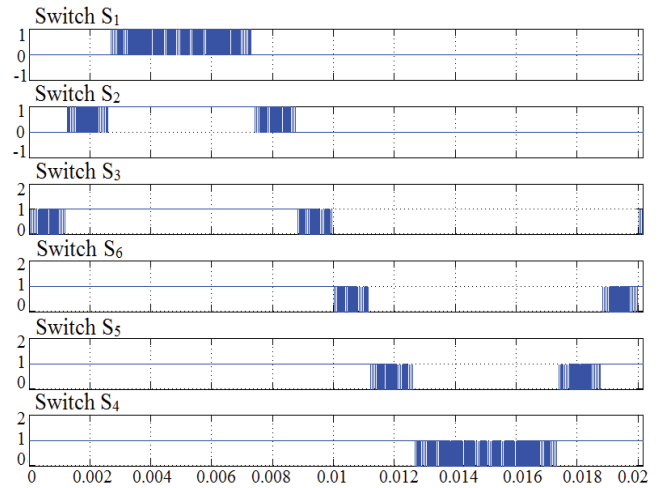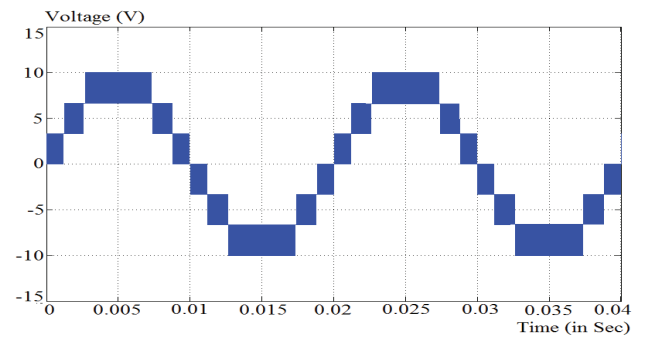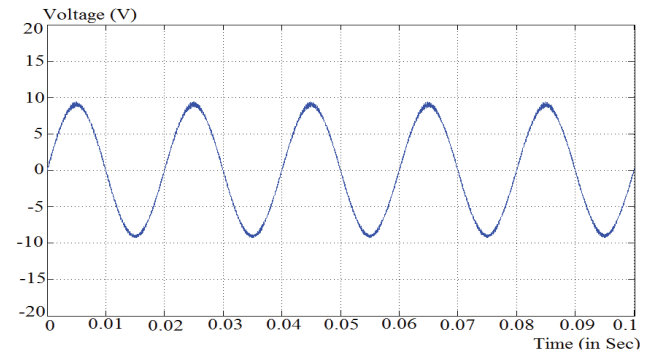

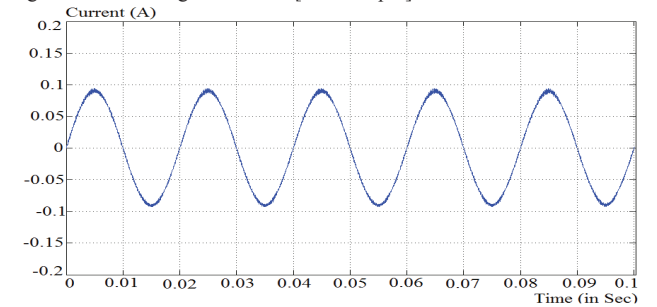Fig.9. Phase Current after filter [10volt output].

Fig.13. Phase Current after filter [9volt output].

V.   CONCLUSION

This paper presents a stack multicell converter SMC which is alternative for multilevel Inverters. Only two DC sources are needed to design SMC for any number of levels. SMC topology removes the drawbacks of conventional multilevel inverter (MLI) such as large number of clamping diodes,

clamping capacitor and sources. Working principle of seven-level (3X2) SMC is discussed and simulation results are provided to verify the performance of converter. Level shifted SPWM technique is incorporated to generate gate pulses for switches. Total harmonic distortion (THD) of seven-level (3X2) SMC before and after filter is achieved 5.26% and 1.55%. Hardware implantation of the 3X2 SMC topology is in progress.

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