A Three-phase Digital Current Controller with Improved Performance Indices

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***Abstract*—Performance of conventional digital current controllers is constrained by transport delays within the feedback acquisition chain, as well as by delays inherent to the pulse width modulation. In this paper, we introduce a novel current controller which provides a very high closed-loop bandwidth, improves the robustness and disturbance rejection, and eliminates the noise and sampling errors in the feedback path. In order to achieve these goals, we suppress the transport delays by introducing an improved execution schedule of the control interrupt and by inserting a cascaded multiplier of differential character. With the novel gain setting rule, the closed loop bandwidth reaches 17% of the sampling frequency, disturbance rejection capability is doubled, the step response has a negligible overshoot, and the robustness is characterized by the vector margin of 0.65. Experimental verification is performed using an experimental setup with a three-phase inverter, digital controller, and a permanent magnet synchronous motor.**

***Index Terms*—Ac motor drives, High-performance control, Signal acquisition, Delay lines, Control design**

I. Introduction

DIGITAL current controllers are used in inner control loops of electrical drives [1] and grid-connected power converters, and their characteristics have considerable impact on the overall performance [2], [3]. Desirable features of current controllers [4] include a high closed loop bandwidth in tracking of the current references, and also the capability to suppress the impact of the voltage disturbances on the controlled current.

Most contemporary current controllers include proportional, integral and axis-decoupling actions, and they operate in the synchronous reference frame [4], [5], [6]. Well established parameter setting procedures [3], [5], [7] contribute to a fast step response with the closed loop bandwidth f_{BW} up to 10% of the sampling frequency f_S. By reducing the crossover frequency from 9.3% to 4% of the sampling frequency, the gain setting of [4] achieves the step response with no overshoot.

The closed loop bandwidth of high-performance current controllers is limited by transport delays [3], [6] which include computation delays, digital sampling delays and PWM-process delays. A number of important contributions [3], [4], [8] deal with the current controller in *s*-domain, where the transport delays are modeled by Pade rational approximation, while the *s*-domain controllers and/or integrators are replaced by Tustin approximation. In the frequency range of the desired bandwidth, the *s*-domain models of discrete-time processes are less accurate, while Pade approximation introduces the right half-plane zeros and a false non-minimum phase modes. The PI controller of [5] applies the internal-model-control (IMC) concept in *z*-domain with exact model of transport delays and discrete-time phenomena, and it provides complete decoupling even at very high fundamental frequencies f_e. With the gain of $k = 0.25 \cdot f_S$, the closed loop bandwidth reaches $f_{BW} = 0.1 \cdot f_S$ even at very large f_e/f_S ratios. Fast response is also available with dead-beat and predictive controllers [9], but their sensitivity to parameter changes reduces their practical use.

The sampling at the center of the voltage pulses [5] is widely used in an attempt to acquire the current feedback at instants when the PWM-related ripple crosses zero. The zero-crossing instants are shifted by the lockout time, by gating delays and also by the phase shift of the anti-aliasing filters, thus introducing the sampling errors [10], [11]. The errors are further increased by the switching-excited oscillations caused by the power cable parasitic inductances and capacitances [12]. An error-free measurement that overcomes the above listed problems can be obtained by using the oversampling technique and calculating the average of the output current over the past PWM period [11]. This averaging over one PWM period increases the transport delays from $1.5/f_S$ up to $2.5/f_S$ and further constrains the closed loop performance.

In this paper, we adopt the error-free feedback acquisition approach of [11], and we propose the control enhancements which reduce the impact of delays and result in the closed loop bandwidth that outperforms the similar contemporary solutions. The two essential modifications include a novel approach to scheduling of the control interrupt routines, suited to reduce the overall transport delays, and the introduction of a series connected differential multiplier. Operability of the novel interrupt scheduling is thoroughly examined by a series of experimental runs. We also develop a novel gain-setting procedure with an optimization criterion that considers the closed loop bandwidth and disturbance rejection, while maintaining the required robustness against the parameter variations.

In Section II, the conventional digital current controller is revisited first, including the standard interrupt scheduling and feedback averaging over one PWM period. The relevant pulse transfer functions are summarized next, both for the conventional controller and for the controller enhanced by the addition of a differential multiplier, on the basis of [11].

In Section III, the new interrupt schedule is introduced as

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the means of reducing the overall transport delay within the system. The schedule proposed in subsection III.A arranges the data acquisition, pulse width modulation and calculation processes and reduces delays by T_S - Δt_{EXE}, where T_S is the sampling period while Δt_{EXE} is the calculation delay. It should be noted that the idea of this modified scheduling has been floated for the first time by the authors in [13]. However, the concept was applied only to the simplest PI current controller with no decoupling, with the load transfer function W_{OBJ} derived in the stationary reference frame, and with the experimental waveforms representing the stationary frame currents. The validity of the key hypothesis ($\Delta t_{EXE}/T_S << 1$) was not tested at all. In contrast to [13], a synchronous reference frame current controller with IMC designed decoupling is considered here and the validity of the key hypothesis of the new scheduling is thoroughly verified later on in the paper by experiments. The change of the delay affects the pulse transfer function of the load, as well as the closed loop transfer and disturbance transfer functions. In subsection III.B, the relevant transfer functions are derived for the controller with the new schedule and without the differential compensator. In subsection III.C, the improved scheduling is used in conjunction with the enhanced controller, which uses the differential multiplier.

A novel parameter setting procedure is introduced in Section IV, suited to achieve a quick response, high disturbance rejection and an adequate robustness. Simulation comparison of the developed controllers is given in Section V, with experimental verification provided in Section VI. Conclusions are given in Section VII.

II. Standard Interrupt Routine Scheduling and Transfer Functions

A. Classical Interrupt Routine Scheduling

The voltage actuator of digital current controllers is the three-phase inverter, which outputs the train of pulse-width-modulated (PWM) voltage pulses u_A, u_B, and u_C. The position of commutation instants ①-④ (Fig. 1) coincides with the intersection of the PWM carrier and the voltage commands u_{n-2} ... u_{n+1}. There are two commutations in each PWM period (T_{PWM}). Each commutation affects the average voltage within the ongoing sampling period $T_S = T_{PWM}/2$. The control interrupts are triggered both by the zero count and by the period count of the PWM carrier, and they execute twice in each PWM period.

In Fig. 1, the voltage reference u_{n+1} is calculated within the control interrupt triggered at $(n+1)\cdot T_S$. The value of u_{n+1} is loaded into the pulse-width registers of the PWM peripheral unit at $(n+2)\cdot T_S$, and it affects the commutation ④ and the average output voltage between $(n+2)\cdot T_S$ and $(n+3)\cdot T_S$. The interrupt $(n+1)$ uses the feedback sample i^F_{n+1}, obtained by the averaging over one PWM period [11], representing the average output current in the interval $[(n-1)\cdot T_S \ldots (n+1)\cdot T_S]$. Thus, the consequential transport delay corresponds to $2.5\cdot T_S$, and it restrains the closed loop bandwidth of the digital current controller. In order to reduce the impact of the delays, it is possible to reschedule the control interrupt, as discussed in Section III.

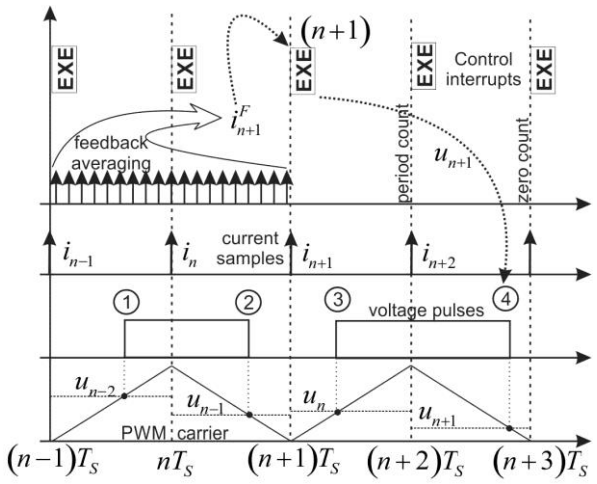

Fig. 1. The sequence of control actions in a conventional digital current controller. Computation is performed in control interrupts (EXE). Each $T_S = T_{PWM}/2$, the averaging over one PWM period provides the feedback sample (i^F_{n+1}), used to calculate a new voltage command (u_{n+1}).

The closed loop transfer function $W_{SS}(z)$ and the disturbance transfer function $Y(z)$ are derived next for the conventional schedule of Fig. 1. The functions $W_{SS}(z)$ and $Y(z)$ are formulated first for the controller without the differential multiplier (subsection II.B), and then for the controller that includes the multiplier (subsection II.C). The subsequent developments are based on results published in [5] and [11]. Therefore, some considerations are shortened or omitted.

B. The Load and Closed Loop Transfer Functions

The PWM inverter voltages u_A, u_B, and u_C are fed to the three phase load. The per-phase load can be represented by the series connection of a resistance R, inductance L, and the electromotive force e. The load currents i_A, i_B, and i_C can be transformed into the stationary α-β frame, along with the voltages and electromotive forces. Adopting the complex vector notation [14]-[15], the current vector in α-β frame can be defined as $i^s = i_\alpha + \mathrm{j}i_\beta$. Considering the schedule of Fig. 1, the load current is described by the difference equation

$$i^s_{n+3} = i^s_{n+2}\exp(-\beta) + \frac{1-\exp(-\beta)}{R}\left(u^s_{n+1} - e^s_{n+2}\right), \qquad (1)$$

where $\beta = R\cdot T_S/L$, R and L are the load parameters, i^s_{n+2} and i^s_{n+3} are the current samples, while e^s_{n+2} represents the average value of the electromotive force from $(n+2)\cdot T_S$ to $(n+3)\cdot T_S$. Due to $L/R >> T_S$, the gain $(1-\exp^{-\beta})/R$ is very close to T_S/L.

In the d-q frame, the complex vectors of currents and voltages are $i^e = i_d + \mathrm{j}i_q$ and $u^e = u_d + \mathrm{j}u_q$. The vectors in α-β frame are obtained by multiplying the d-q frame vectors by $\exp(\mathrm{j}\theta)$, where θ is the position of the d-q frame ($i^s_n = i^e_n\exp(\mathrm{j}\theta_n)$). The change of the d-q frame speed ω within a single sampling period T_S is negligible. Therefore, the position θ_{n+1} is close to $\omega T_S + \theta_n$. The d-q frame equivalent e^e_{n+2} of the electromotive force average over the interval $[(n+2)T_S \ldots (n+3)T_S]$ is obtained as $e^s_{n+2}\cdot\exp(-\mathrm{j}(\theta_{n+2}+\theta_{n+3})/2)$. By transforming (1) into the d-q frame, by dividing the result by $\exp(\mathrm{j}\theta_{n+2})$, and then transforming the difference equation into z

domain, relation between the complex vectors $i^e(z)$ and $u^e(z)$ of currents and voltages becomes

$$i^e(z)\cdot z^3\cdot\exp(j\omega T_S)=i^e(z)\cdot z^2\cdot\exp(-\beta)+ \quad (2)$$
$$+\frac{T_S}{L}\left(u^e(z)\cdot z\cdot\exp(-j\omega T_S)-e^e(z)\cdot z^2\cdot\exp(j\omega T_S/2)\right).$$

The pulse transfer of the load $W^{S1}_{OBJ}(z)$ is calculated from (2) as the ratio $i^e(z)/u^e(z)$, obtained with $e^e(z) = 0$,

$$W^{S1}_{OBJ}(z)=\frac{T_S/L}{z\cdot\exp(j\omega T_S)\left[z\cdot\exp(j\omega T_S)-\exp(-\beta)\right]}. \quad (3)$$

The block diagram of the digital current controller is shown in Fig. 2. The transfer function $W_{FB}(z)$ represents the feedback subsystem with averaging over one PWM period, introduced in [11] and illustrated in Fig. 1. The feedback sample i^F_{n+1} can be approximated by $(i_{n+1} + 2i_n + i_{n-1})/4$. Thus, the transfer function in the feedback path becomes

$$W_{FB}(z)=i^F(z)/i^e(z)=\left(z^2+2\cdot z+1\right)/\left(4z^2\right). \quad (4)$$

The current controller $W_{REG}(z)$ in Fig. 2 is obtained by applying the IMC concept [5], where the inverse model of the load W_{OBJ} is multiplied by an integrator $\alpha\cdot z/(z\text{-}1)$. In order to obtain a causal controller for the schedule of Fig. 1, it is necessary to divide the result $\alpha\cdot z/(z\text{-}1)/(W_{OBJ})$ by z^2,

$$W^{S1}_{REG}=\frac{\alpha L\cdot\exp(j\omega_e T_S)\left[z\cdot\exp(j\omega_e T_S)-\exp(-\beta)\right]}{T_S(z-1)}. \quad (5)$$

Corresponding closed loop transfer function $W^{S1}_{SS}(z)$, where $f_1(z)$ is the characteristic polynomial, is given with:

$$W^{S1}_{SS}=\left.\frac{i^e(z)}{i^*(z)}\right|_{e^e=0}=\frac{4\alpha z^2}{4z^4-4z^3+\alpha z^2+2\alpha z+\alpha}=\frac{4\alpha z^2}{f_1(z)}. \quad (6)$$

Disturbance transfer function $Y^{S1}(z)$ is obtained next as:

$$Y^{S1}=\left.\frac{i^e(z)}{-e^e(z)}\right|_{i^*=0}=\frac{4T_S\cdot z^3(z-1)\cdot\exp(j\omega T_S/2)/L}{\left[z\cdot\exp(j\omega T_S)-\exp(-\beta)\right]\cdot f_1(z)}. \quad (7)$$

C. Conventional Schedule with Differential Multiplier

The impact of transport delays can be reduced by introducing a series-connected differential multiplier $W_{DIF}(z) = 1 + d\cdot(1\text{-}z^{-1})$ [11], thus resulting in an enhanced controller,

$$W^{S1}_{REGD}(z)=W^{S1}_{REG}(z)\cdot W_{DIF}(z). \quad (8)$$

The closed loop transfer function of the system in Fig. 2, obtained with the current controller schedule of Fig. 1 and with the controller transfer function of (8), is given with:

$$W^{S1}_{SSD}=\frac{W^{S1}_{REGD}(z)\cdot W^{S1}_{OBJ}(z)}{1+W^{S1}_{REGD}(z)\cdot W^{S1}_{OBJ}(z)\cdot W_{FB}(z)}= \quad (9)$$
$$=\frac{4\alpha(1+d)z^3-4\alpha dz^2}{4z^5-4z^4+\alpha(1+d)z^3+\alpha(2+d)z^2+\alpha(1-d)z-\alpha d}.$$

Corresponding disturbance transfer function $Y_D{}^{S1}(z)$ is given with ($f_2(z)$ represents denominator of (9)):

$$Y^{S1}_D=\frac{T_S}{L}\cdot\frac{4z^4(z-1)\cdot\exp(j\omega T_S/2)}{\left[z\cdot\exp(j\omega T_S)-\exp(-\beta)\right]}\cdot\frac{1}{f_2(z)}. \quad (10)$$

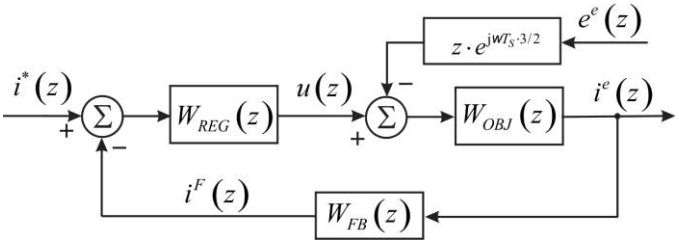

Fig. 2. The block diagram of the digital current controller in the *d*-*q* frame.

III. Improved Interrupt Scheduling and Corresponding Transfer functions

Rescheduling of [13], as mentioned already, applies to the PI controller with no decoupling and with the load transfer functions derived in the stationary reference frame. Experimental results were also obtained with current control located in the stationary frame. In contrast to this, in subsection III.A we describe the new interrupt schedule and then apply it to the synchronous frame IMC structure. The same transfer functions as in subsection II.B are derived next for the modified scheduling in subsection III.B. In subsection III.C, the improved scheduling is used in conjunction with the enhanced controller, which uses the differential multiplier. A parameter setting procedure for the rescheduled IMC structure, which considers both the disturbance rejection capability and the reference tracking, will be further developed in Section IV. The procedure also relies on the hypothesis that the execution time Δt_{EXE} is negligible when compared to the sampling time. With the gain settings of Section IV, the controller of III.C performs with unparalleled closed loop bandwidth and disturbance rejection, as will be proved by experiments in Section VI.

A. Improved Interrupt Routine Scheduling

In Fig. 3, the scheduling is improved by triggering the control interrupts Δt_{EXE} before the corresponding zero/period counts of the PWM carrier. In this way, the interrupt triggered at $[(n+1)\cdot T_S - \Delta t_{EXE}]$ calculates the voltage command u_{n+1} which gets loaded into the PWM peripheral unit at $(n+1)\cdot T_S$. As a result, u_{n+1} controls the commutation ③ and sets the average voltage on the interval $[(n+1)\cdot T_S \ldots (n+2)\cdot T_S]$, thus reducing the transport delay by T_S. The time shift Δt_{EXE} has to be sufficient for the control interrupt to complete before the loading instant $(n+1)\cdot T_S$ of PWM registers. Thus, the value of Δt_{EXE} has to be slightly larger than the worst-case execution time of the current control tasks.

In Fig. 3, the same interrupt event uses the feedback i^F_{n+1}, obtained by oversampling and averaging consecutive current samples acquired on the interval that extends from $[(n\text{-}1)\cdot T_S - \Delta t_{EXE}]$ to $[(n+1)\cdot T_S - \Delta t_{EXE}]$. Related train of samples is shown in the upper left part of Fig. 3. Compared to the corresponding feedback sample in Fig. 1, the feedback sample i^F_{n+1} in Fig. 3 gets delayed by Δt_{EXE}. Proposed reduction of the transport delay relies on the crucial assumption that the feedback delay Δt_{EXE} does not have any meaningful impact on the closed loop dynamics, and therefore can be neglected. This assumption is thoroughly tested in subsection VI.A for the range of time shifts Δt_{EXE} that include and exceed most typical execution times of current control tasks on typical DSP controllers.

The schedule proposed in Fig. 3 affects both the closed-loop transfer function $W_{SS}(z)$ and the disturbance transfer function $Y(z)$. The transfer functions obtained with the new schedule are derived next for the controller without the differential multiplier (subsection III.B), and for the controller that includes the multiplier (subsection III.C).

B. The Load and Closed Loop Transfer Functions

In schedule of Fig. 3, the application of the voltage commands takes place one sampling period earlier than in Fig. 1. This affects the transfer function of the load, which becomes

$$W_{OBJ}^{S2}(z)=\left.\frac{i^e(z)}{u^e(z)}\right|_{e^e=0}=\frac{T_S/L}{z\cdot\exp(j\omega T_S)-\exp(-\beta)}. \quad (11)$$

The current controller W^{S2}_{REG}, suitable for the load transfer function of (11), is obtained by applying the IMC concept [5]. The IMC design $\alpha\cdot z/(z\text{-}1)/(W_{OBJ})$ is obtained with W_{OBJ} of (11), and it has to be divided by z in order to meet the causality requirement. The resulting current controller W^{S2}_{REG} is

$$W_{REG}^{S2}=\frac{\alpha}{(z-1)W_{OBJ}^{S2}}=\frac{\alpha L}{T_S}\frac{z\cdot\exp(j\omega T_S)-\exp(-\beta)}{z-1}. \quad (12)$$

Corresponding closed loop transfer function W^{S2}_{SS} is

$$W_{SS}^{S2}=\left.\frac{i^e(z)}{i^*(z)}\right|_{e^e=0}=\frac{4\alpha z^2}{4z^3+(\alpha-4)z^2+2\alpha z+\alpha}=\frac{4\alpha z^2}{f_3(z)}, \quad (13)$$

where $f_3(z)$ is the characteristic polynomial. Disturbance transfer function $Y^{S2}(z)$, obtained with W^{S2}_{REG} (12) and with W^{S2}_{OBJ} of (11) is calculated from the block diagram of Fig. 2,

$$Y^{S2}=\left.\frac{i^e(z)}{-e^e(z)}\right|_{i^*=0}=\frac{4T_S\cdot z^2(z-1)\cdot\exp(j\omega T_S/2)/L}{\left[z\cdot\exp(j\omega T_S)-\exp(-\beta)\right]\cdot f_3(z)}. \quad (14)$$

C. Improved Schedule with Differential Multiplier

The current controller of (12) can be enhanced by adding a series connected differential multiplier $W_{DIF}(z) = 1+ d\cdot(1\text{-}z^{-1})$ [11], thus resulting in an enhanced controller, obtained by multiplying the transfer function W^{S2}_{REG} of (12) by W_{DIF},

$$W_{REGD}^{S2}=\frac{\alpha L}{T_S}\frac{\left[(d+1)z-d\right]\left(z\cdot\exp(j\omega T_S)-\exp(-\beta)\right)}{z(z-1)}. \quad (15)$$

The closed loop transfer function W^{S2}_{SSD} of the system in Fig. 2, obtained with the current controller schedule of Fig. 3, and with the controller transfer function of (15) is

$$W_{SSD}^{S2}(z)=\frac{W_{REGD}^{S2}(z)\cdot W_{OBJ}^{S2}(z)}{1+W_{REGD}^{S2}(z)\cdot W_{OBJ}^{S2}(z)\cdot W_{FB}(z)}= \quad (16)$$

$$=\frac{4\alpha(1+d)z^3-4\alpha dz^2}{4z^4+\left[\alpha(1+d)-4\right]z^3+\alpha(2+d)z^2+\alpha(1-d)z-\alpha d}.$$

Corresponding disturbance transfer function $Y_D^{S2}(z)$ is obtained as $-i^e(z)/e^e(z)$, calculated under the assumption that the reference current i^* is equal to zero. It is given with ($f_4(z)$ represents denominator of W^{S2}_{SSD} in (16)):

$$Y_D^{S2}(z)=\frac{4\cdot T_S\cdot z^3(z-1)\cdot\exp(j\omega T_S/2)/L}{z\cdot\exp(j\omega T_S)-\exp(-\beta)}\frac{1}{f_4(z)}. \quad (17)$$

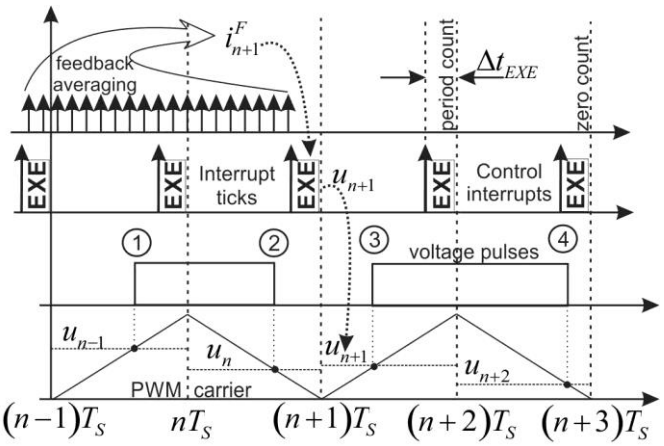

Fig. 3. Modified schedule of control actions for digital current controllers. Control interrupts are triggered Δt_{EXE} before each zero-count and period-count of the PWM carrier. Compared to Fig. 1, delay in applying the new voltage command (u_{n+1}) is reduced by T_S.

Four different controllers and four sets of relevant transfer functions (W_{SS}, Y) have been derived in subsections II.B, II.C, III.B, and III.C. It is of interest to find the optimum gains for each set, and to compare the resulting performances. The criteria for the optimum gain set include the closed loop bandwidth, the robustness and the disturbance rejection capability.

IV. The Optimum Setting of The Feedback Gains

Digital current controller is expected to track the input reference i^* quickly with the least possible error, and to suppress the impact of the voltage disturbances on the output current. Digital current controllers designed in II.B and III.B have a single gain parameter α, while the controllers designed in II.C and III.C have a pair of gains, d and α. In all of the four closed loop transfer functions W_{SS}, both α and d are relative numbers. Differential gain d appears in the compensator function $W_{DIF}(z) = 1+ d\cdot(1\text{-}z^{-1})$, where its role is relative and unrelated to the application-specific parameters. The gain α originates in the IMC concept, where the design goal is the open loop transfer function $\alpha\cdot z/(z\text{-}1)$. An IMC-designed controller cancels out dependence on the application-specific parameters and yields a single, generic parameter α, unrelated to the application. Closed loop transfer functions - such as the one in (16) - are the same for any application, and depend on α and d parameters only. Hence their optimum values do not change with the actual parameter values in an application (please note however, that the practical implementation of the controllers given with (5), (12), (15) of course does require the sampling period T_s, the load inductance L and the parameter β (i.e., the load resistance)). For each of the four controllers, it is necessary to find the optimum gain α (or d and α) setting(s) which improve both the step response and the disturbance rejection.

A. Criterion Function

The speed of the step response is characterized by the settling time t_{01} [4], defined by the instant when the output error subsides below 1%. The input-step response is obtained from the closed loop transfer functions in (6), (9), (13), and

(16). The settling time is expressed as a multiple of the sampling periods, $t_{01} = N_{01} \cdot T_S$.

Disturbance rejection capability can be characterized by IE_1, which is the integral of the current error $|\Delta i^e|$ caused by the unit step change of the voltage disturbance e^e [4]. Response to the voltage disturbance is obtained from the admittances $Y(z)$ in (7), (10), (14), and (17). In order to avoid impact of the application specific parameters on the optimum relative gains α and d, the factors T_S/L are removed from $Y(z)$ expressions, while the speed ω is set to zero. Thus, the value of IE_1 is obtained by (i) deriving the pulse-train of the unit-step-response for each transfer function $(L/T_S) \cdot Y(z)$, and then (ii) finding the sum of absolute values of the pulse-train samples. The criterion function Q is calculated by assigning the same weight to N_{01} and IE_1 performance metrics, as

$$Q = N_{01} + \frac{IE_1}{100} \quad . \tag{18}$$

Selection of the same weights for two components of (18) is justified because the two terms in (18) are always of the same order of magnitude and of similar values for any well-tuned controller response.

Finding the optimum gains by analytical means would be difficult, since the relevant transfer functions include up to five closed loop poles (9), while the calculation of the criterion Q includes some nonlinear operations. Instead, the optimum gains α for the controllers of II.B and III.B are found by performing a numerical search for the optimum along the axis α. For the controllers of II.C and III.C, the optimum pair of gains (α, d) is found by searching the α-d plane.

B. Optimisation Constraints

In addition to meeting the performance requirements of (18), the current controller is also required to be robust against the parameter changes, and to perform without any significant overshoot. The robustness of the controller (which here relates to the capability of the system to maintain the response quality and/or stability in the presence of parameter changes, i.e. variations in R and L) can be quantified by the vector margin VM [5]. The values of VM lower than 0.5 are usually associated with elevated sensitivity to parameter changes and with consequential oscillatory response. Therefore, the parameter search excludes any solution where the vector margin falls below 0.6, and it also excludes solutions where the overshoot exceeds 2%.

C. The Search Results

The search for the optimum gains is performed for the four controller structures described in II.B, II.C, III.B, and III.C. In the first two cases (Case 1 and Case 2 further on), the current controller uses conventional schedule of Fig. 1. The latter two cases (Case 3 and Case 4) have the novel schedule of Fig. 3. In cases 2 and 4, the controller structure is enhanced by adding the series differential multiplier W_{DIF}. The search results are summarized in Table I. They include the optimum gain settings which meet the constraints of IV.B while minimizing the criterion (18). The Table also includes the corresponding closed loop bandwidth, the vector margin, the overshoot, and the integral of the current error (IE_1) caused by the unit-step voltage disturbance and calculated as described in IV.A.

For the four optimum gain settings of Table I, the ratio between the factor N_{01} and the factor (IE_1/100) in (18) is equal to 1.34, 1.04, 1.377 and 1.08, respectively. The difference in values stems from the fact that the optimum gains are found by searching for the best value of Q in (18), rather than considering the individual terms of (18). This proves that the proposed composition of the criterion function attributes a similar weight to the input step response and to the disturbance rejection. The optimum gains (α, d) are generic, and they do not change with the application parameters, as already explained in the beginning of Section IV. Thus, there is no need to repeat the search in other applications.

The following conclusions are drawn from Table I:

- By adding the multiplier W_{DIF}, the bandwidth f_{BW}(-3dB) is increased more than twice, and the factor IE_1 is reduced by 30% (Case 2 vs. Case 1, Case 4 vs. Case 3);
- By introducing the new interrupt schedule, the bandwidth f_{BW}(-3dB) is increased 1.5 times, and the factor IE_1 decreased by 36% (Case 3 vs. Case 1, Case 4 vs. Case 2);
- Introduction of the new schedule increases the vector margin by 3% in Case 3, and by 7% in Case 4;
- When both the new schedule and the multiplier W_{DIF} are used, the bandwidth f_{BW}(-3dB) is increased 3.14 times and the factor IE_1 reduced 2.2 times (Case 4 vs. Case 1).

The best results are obtained in Case 4, where the bandwidth f_{BW}(-3dB) reaches 17.6% of the sampling frequency (35.2% of the switching frequency), keeping at the same time the vector margin at VM = 0.655, and maintaining stability even with the inductance L enlarged or reduced 3.5 times.

V. Simulation Results

The closed loop step response and the disturbance rejection of the four digital current controllers are tested by means of computer simulation. The simulation is based on the assumption that Δt_{EXE} in Fig. 3 is considerably smaller than the sampling interval T_S, and it is therefore negligible ($\Delta t_{EXE} = 0$).

Simulated step responses of the four current controllers are given in Fig. 4. The responses are mutually shifted for an easy comparison. The responses obtained with conventional schedule (Fig. 1) have the rise time some 50% larger than the responses obtained with the new schedule (Fig. 3). The rise time is nearly halved when using the multiplier W_{DIF}.

Disturbance rejection capability of the four current controllers is explored by simulating the unit-step response of the pulse-transfer-functions $(L/T_S) \cdot Y(z)$, given in (7), (10), (14), and (17). Corresponding traces are given in Fig. 5. They represent the response of the scaled current error to the step change of the electromotive force by 1 V. In order to obtain the actual peak of the current error, the reading from Fig. 5 has to be multiplied by (T_S/L) and by the amplitude of the voltage disturbance. The response obtained with the Case 4 has the current peaks reduced more than two times.

These performance improvements come as the result of the new scheduling, the use of W_{DIF} multiplier, and the improved parameter setting procedure. It is of interest to compare the bandwidth f_{BW}(-3dB) obtained with Case 2 of Table I with the corresponding bandwidth obtained in [11] (please see Table

VI). The latter uses the same controller structure, but with a different gain setting. With the gain setting proposed here, the ratio between the bandwidth f_{BW}(-3dB) and the sampling frequency f_S is increased by 11%.

VI. Experimental Verification

The experimental verification is performed with the setup comprising a three-phase permanent magnet (PM) synchronous motor, an industrial PWM-controlled IGBT inverter [16], and a DSP controlled platform. The experimental rig is illustrated in Fig. 6 and full setup data are given in [11]. The switching frequency used in the experiments is set to 10 kHz. The current controller with conventional schedule has been thoroughly tested in [11], both in its original form [5] and with the multiplier W_{DIF}. Therefore, the experimental runs described in this section are focused on the two current controllers with the new schedule, described in III.B and III.C, and denoted as Case 3 and Case 4 in Table I.

The experimental verification has the following goals:

- To explore the impact of Δt_{EXE} on the dynamic performances of the controllers with the new schedule, and to establish viable limit for the ratio $\Delta t_{EXE}/T_S$;
- To compare simulated and experimental step responses;
- To compare simulated and experimental responses to the voltage disturbance; and
- To check the performance of the current controller in operation with elevated fundamental frequencies.
- To verify the robustness to parameter uncertainties.

The subsequent experimental waveforms comprise the current response in the *d-q* frame, and they represent the feedback signal i^F in Fig. 2. The samples of i^F are logged into the internal RAM, written off-line on an SD card (Fig. 6, (c)), and plotted in the subsequent figures. The samples of i^F are spaced by T_S = 50μs. The signal i^F is obtained by averaging the actual current i^e over one PWM period. The process is modeled in (4). Therefore, i^F waveforms are slightly different from the actual *d-q* current i^e. The actual noise-free samples i_n, taken at instants $n \cdot T_S$, are not available. The feedback transfer function W_{FB} of (4) is taken into account when generating the reference Trace 1 in Figs. 7 and 8, as well as in simulated traces of Fig. 10.

A. The Impact of The Time Shift Δt_{EXE}

The crucial hypothesis introduced with the new scheduling is that delay Δt_{EXE} of the feedback signal i^F_{n+1} in Fig. 3 does not have any meaningful effect on the dynamic behavior. This hypothesis is experimentally tested and verified by performing the step response test and varying Δt_{EXE} over a wide range. With conventional controllers such as the DSC TMS320F28335, the current control tasks complete in less than 4 μs. During the test runs, Δt_{EXE} is varied from 2.4 μs up to 12 μs.

Corresponding step responses of the *q*-axis current are given in Fig. 7 for the controller of III.B (Case 3), and in Fig. 8 for the controller of III.C (Case 4). The measurements were repeated for Δt_{EXE} set to 2.4μs, 4μs, 8μs, and 12μs. In Figs. 7 and 8, the reference Trace 1 is obtained by simulation, and it corresponds to $\Delta t_{EXE} = 0$ (i.e. it is obtained with the simulation code which includes the crucial hypothesis). The remaining traces are obtained from the experimental setup. Trace 2 with Δt_{EXE} = 2.4μs was obtained with time-optimized code that includes some assembler sequences and excludes the unnecessary routines. Trace 3 is obtained with Δt_{EXE}= 4μs, and with the full-featured interrupt routine. In traces 4 and 5, the

TABLE I
The Optimum Gains and Corresponding Closed Loop Performances

Case	Gain α	Gain d	f_{BW}(-45°)	f_{BW}(-3dB)	VM	Over-shoot	IE_1
1	0.172	×	0.026 f_S	0.056 f_S	0.686	.0098	817
2	0.244	0.735	0.041 f_S	0.116 f_S	0.612	.0081	577
3	0.277	×	0.048 f_S	0.087 f_S	0.711	.0096	508
4	0.380	0.444	0.080 f_S	0.176 f_S	0.655	.0067	370

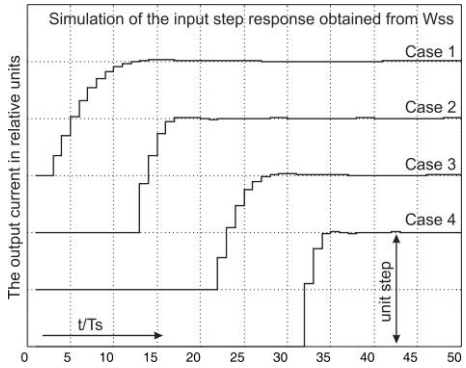

Fig. 4. Simulated step responses of the four digital current controllers. Conventional schedule is used in cases 1 and 2, while the new schedule is used in cases 3 and 4. In cases 2 and 4, the controller is enhanced by the differential action.

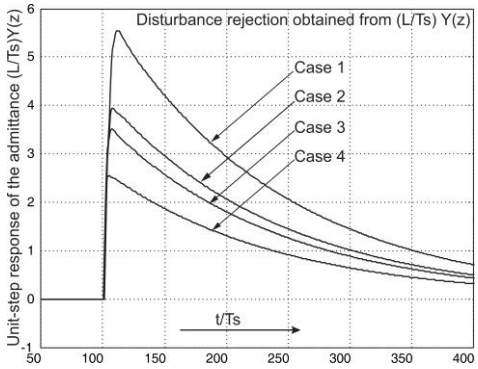

Fig. 5. The step response of the admittance transfer function $(L/T_S)\cdot Y(z)$ obtained at zero speed and with the unit voltage disturbance (1 V).

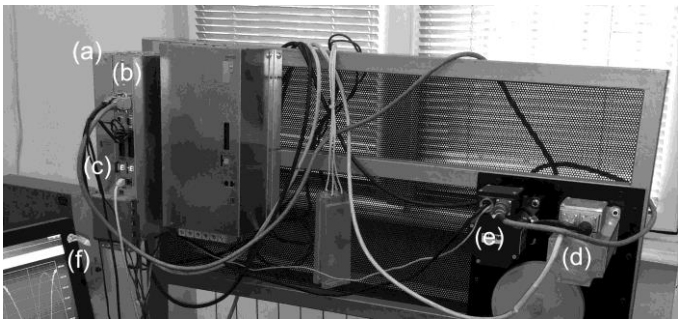

Fig. 6. Experimental setup with two permanent magnet synchronous motors: (a) Main power supply unit providing the dc-bus voltage E_{DC}; (b) Two 3-phase IGBT inverters with control circuits [16]; (c) SD-card slot used for data logging; (d) The motor under the test; (e) The motor used as the load; (f) PC-based GUI connected over the EtherCat link.

value of Δt_{EXE} is deliberately increased first to 8μs, and then to 12μs.

Compared to the reference Trace 1, traces 2 and 3 in Figs. 7 and 8 are practically unaffected by Δt_{EXE}. The step response is noticeably changed in Trace 5 of Fig. 7, where Δt_{EXE} exceeds $0.2 \cdot T_S$. Similarly, the response significantly deteriorates in Fig. 8 for Traces 4 and 5, where Δt_{EXE} equals 8μs and 12μs, respectively. With only a minor difference between reference Trace 1 and experimental Trace 3, we conclude that the time shift Δt_{EXE} of $0.08 \cdot T_S$ does not have any meaningful impact on the closed loop dynamics. This corroborates the assumption introduced in III.A and Fig. 3.

B. The Step Response at the Rated Speed

The step response of the *q*-axis current is tested at the rotor speed of 628 rad/s, with f_e= 300Hz, and with the back-electromotive force close to the rated voltage. The traces 1 and 2 of Fig. 9 correspond to the controller of III.B (Case 3), while the traces 3 and 4 correspond to the controller of III.C (Case 4). Time axis covers $400T_S$ = 20ms. At instants of *q*-axis current transients, *d*-axis currents remain unchanged, thus proving the decoupling capability of both controllers. The i_q traces of Fig. 9 are redrawn in Fig. 10, focusing on the rise time of the step response. Along with the experimental traces, Fig. 10 also includes the simulation traces used as a reference. Similarity between the traces obtained by simulation, with Δt_{EXE} = 0, and the experimental traces obtained with Δt_{EXE} =4μs confirms the hypothesis $\Delta t_{EXE} << T_S$, introduced in III.A and tested in VI.A.

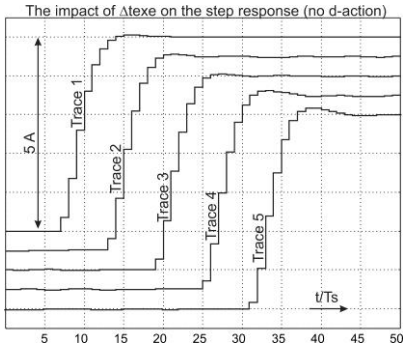

Fig. 7. Step responses of the *q*-axis current obtained with the current controller of III.B (Case 3 in Table I). Trace 1 is the result of simulation, and it serves for the reference. For the experimental traces 2-5, the time shift Δt_{EXE} of the execution of the control interrupt is set to 2.4μs, 4μs, 8μs, and 12μs.

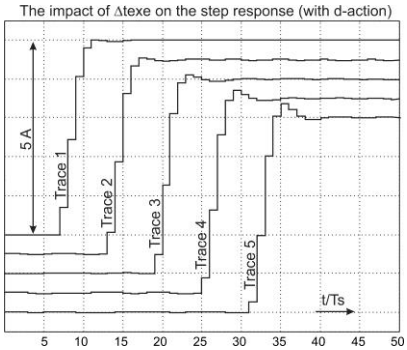

Fig. 8. Step responses of the *q*-axis current obtained with the current controller of III.C (Case 4 in Table I). Trace 1 is the result of simulation, and it serves for the reference. For the experimental traces 2-5, the time shift Δt_{EXE} of the execution of the control interrupt is set to 2.4μs, 4μs, 8μs, and 12μs.

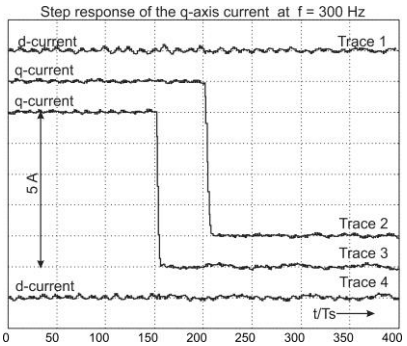

Fig. 9. Step response of the i_q at the fundamental frequency of f_e = 300Hz. The traces 1 and 2 correspond to the controller of III.B (Case 3) while the traces 3 and 4 correspond to the controller of III.C (Case 4).

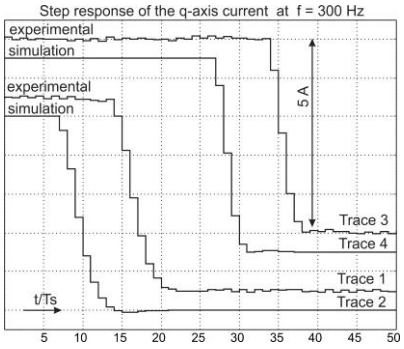

Fig. 10. Comparison of the simulated traces 2 and 4 and the experimental step responses given with traces 1 and 3. The experimental traces 1 and 3 are obtained by scaling and redrawing the traces 2 and 3 of Fig. 9.

C. Disturbance Rejection Capability

The capability to suppress the voltage disturbance e^e of Fig. 2 is tested in the operating conditions that correspond to simulations given in Fig. 5. The actual change of the back-electromotive force e^e could not be initiated. It is therefore emulated by the abrupt change of the *q*-axis voltage command [4] by $E_{DC}/4$. Corresponding experimental traces are shown in Fig. 11, along with the traces predicted by simulation. The difference between the experimental results and simulated traces is lower than 2%. This confirms the conclusions drawn in IV.C from Table I, which claim that the controllers with the multiplier W_{DIF} have an improvement of 30% in disturbance rejection, while the new schedule contributes to a further improvement of 36%. Compared to the performances obtained with Case 1, simultaneous use of both W_{DIF} and the new schedule (Case 4) improves disturbance rejection by approximately two times.

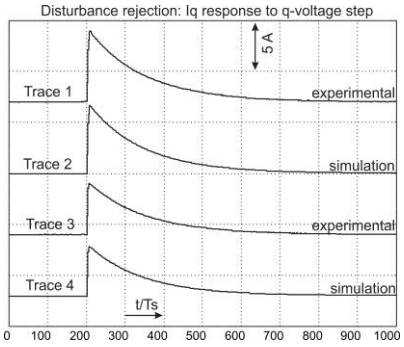

Fig. 11. Simulated and experimental traces that illustrate disturbance rejection. Traces 1 and 2 are obtained with the current controller of III.B, while the traces 3 and 4 correspond to the current controller of III.C.

D. Operation with Very High Fundamental Frequencies

The capability to maintain decoupled operation with very high fundamental frequencies f_e is proved in Figs. 12 and 13. Comparable current controllers maintain their performance even with f_e/f_S= 0.083 [5]. Therefore, the step response is tested with f_e/f_S = 0.071 in Fig. 12, and with f_e/f_S = 0.1 in Fig. 13. Corresponding motor speeds were not achievable and the inverter is therefore connected to a suitable passive load with three chokes. The step response of the *q*-axis current in Figs. 12 and 13 demonstrates the capability of the proposed controllers to provide decoupled operation even at very high f_e/f_S ratios.

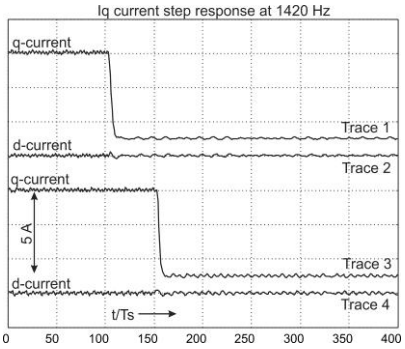

Fig. 12. Step response of the i_q at the fundamental frequency of f_e= 0.071·f_S. The three phase inverter is loaded with three star-connected inductances. Traces 1 and 2 are obtained with the controller of III.B. Traces 3 and 4 are obtained with the controller of III.C.

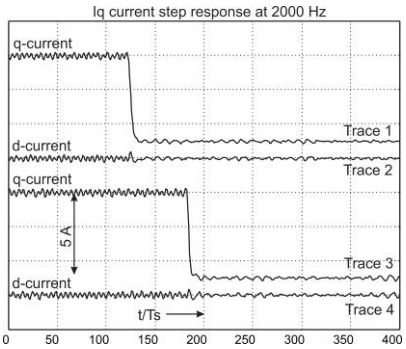

Fig. 13. Step response of the current controller at the fundamental frequency of f_e= 0.1·f_S. The three phase inverter is loaded with the three star-connected inductances. The two uppermost traces are obtained with the current controller of III.B. The bottom two traces correspond to the current controller of III.C.

E. Robustness to Parameter Uncertainties

With the gain settings of Table I, the vector margin VM exceeds 0.6. For Case 3 and Case 4, stability limit is reached with the parameter mismatch of 4.8 and 3.4 times, respectively. The step responses obtained with a large mismatch are poorly damped and of little use. Therefore, we performed an experimental investigation of the step response changes obtained with parameter changes that could be encountered in a practical application.

The load resistance affects the pulse transfer functions by altering the factor $\exp(-\beta) = \exp(-R \cdot T_S/L)$. The factor remains close to 1 for all the reasonable fluctuations of the load resistance. Significant changes of the step response are observed only in cases where the load resistance changes by more than 10 times. The impact of the load inductance is considerably more emphasized, as it changes the closed loop gain. In electrical drives, the load inductance varies due to magnetic saturation within the stator and rotor magnetic circuits, and these variations can exceed 20%.

In Figs. 14 and 15 we studied the impact of the load inductance changes from 60% up to 150% of the nominal value. The step responses are given for the Case 3 (Fig. 14) and for the Case 4 (Fig. 15). The experimental results demonstrate the robustness of the proposed control structure and the parameter setting procedure with respect to the parameter variation effects.

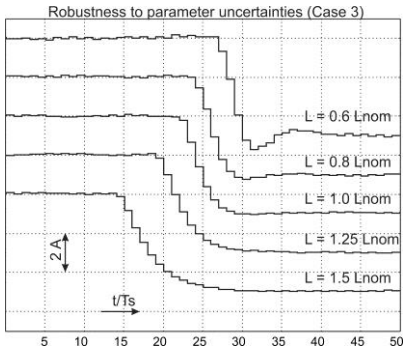

Fig. 14. Step response of the i_q at the fundamental frequency of f_e = 300Hz. The test is carried out for the Case 3. The ratio between the actual motor inductance and the design parameter L_{nom} is varied from 0.6 up to 1.5.

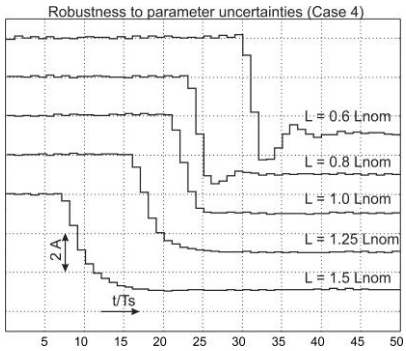

Fig. 15. Step response of the i_q at the fundamental frequency of f_e = 300Hz. The test is carried out for the Case 4. The ratio between the actual motor inductance and the design parameter L_{nom} is varied from 0.6 up to 1.5.

VII. CONCLUSION

In this paper, we considered a digital current controller with the PWM inverter as the voltage actuator, and with the ripple and noise suppression of the feedback signal obtained by introducing the 'averaging over one PWM period technique' into the feedback chain. The closed loop performance is limited by the PWM process delays, computation delays and the feedback acquisition delays. In order to suppress the impact of transport delays, we introduced an improved scheduling of the control interrupt, along with the insertion of a series differential compensator.

The crucial hypothesis of the improved interrupt scheduling has been verified by a series of experimental runs, proving that the use of conventional digital signal controllers with the novel scheduling reduces the transport delays by one sampling period.

A novel gain setting procedure is proposed, suited to provide an optimum step response, disturbance rejection and robustness. The optimum gains are generic in nature, and they do not change with the application-specific parameters. With

the optimum setting, digital current controller performs with the closed loop bandwidth exceeding 17% of the sampling frequency (34% of the switching frequency). Disturbance rejection is doubled, the step response has a negligible overshoot, while the vector margin of 0.65 ensures stability even with the load inductance reduced or enlarged 3.5 times.

The current controller has been verified on an experimental setup with a three-phase inverter, digital controller, and a synchronous permanent magnet motor. The experimental results confirm the analytical findings and simulation results. Decoupling of *d*-axis and *q*-axis transients is maintained even with very large fundamental frequencies, up to 10 % of the sampling frequency. The paper comprises analytical considerations, implementation details, an optimum parameter setting procedure, and a comprehensive description of experimental results.

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