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Photovoltaic Generators Interfacing a DC Micro-Grid: Design Considerations for a Double-Stage Boost Power Converter System

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Abstract: A photovoltaic generator (PVG) is usually connected to a DC micro-grid via a multi-stage-step-up power converter to improve system modularity, minimise shading effects and boost PVG voltage. Under varying operating conditions, the nonlinear characteristics of a PVG may affect performance of the entire PVG system. Further, if these issues are not properly taken into account at the design stage, significant changes in system dynamics may risk stability of the system. Therefore, it is important to understand interactions between a PVG and the rest of the system. A clear understanding of these interactions can help to set system design recommendations and guidelines. In particular, this paper explores the effects of a nonlinear PVG source interfacing a double-stage conventional boost converter connected to a DC bus. It addresses the impact of these effects on the design of both the power circuit and the control loops. Finally, this paper provides system design recommendations to ensure stability under varying operating conditions.

1. Introduction

Burning fossil fuels has been identified as a primary cause of global warming which has led to a number of environmental and socio-economic problems. To address these issues, governments around the world have set targets in generating electricity from clean resources such as wind, solar, geothermal, hydroelectric and fuel cells. Among these resources, over the last few years the installed capacity of solar PV generators have experienced huge growth due to their improved efficiency and reduced cost per watt [1]. These improvements make solar energy one of the most promising renewable sources in electricity generation. Of note is that the main challenges in connecting distributed generators (DGs) to the main grid are: synchronization, harmonics, voltage rise, circulating current and instability caused mainly by an increased number of connected DGs. That being the case, an AC micro-grid has been proposed as a new paradigm for connecting DGs to the main power network [2, 3] and significant work has been made to improve their performance [4, 5]. However, power quality is still an ongoing issue in AC micro-grids, especially for very sensitive power loads. The author in [6] proposed a DC micro-grid as a possible configuration to meet the needs of customers' power quality, since when DC micro-grids have received more attention in the research community. Many studies have been devoted to DC micro-grids where they have been recognized not only for providing high power quality but also for many other advantages such as a smaller system, higher efficiency and a simple control structure [6].

This paper focuses on the generation side of the DC micro-grid, and in particular when using the PVG as a primary DG. The standardization of the DC micro-grid goes towards adopting 380-400 V as the nominal voltage for the main DC bus where all DG sources are connected to it. Low PVG voltage (30-48V) can be boosted by one of three ways: I) connecting many PVG modules in series; II) connecting PVG modules in parallel through single-stage high-step-up converter type; III) connecting PVG modules in parallel through a double-stage step-up converter. These different system configurations for interfacing a PVG system to a DC micro-grid are discussed in Section 2 below.

Conventionally, PVG converters are chosen based on 70% of the rated power of the PVG system. The rationale behind the downsizing of the converter is to reduce its cost. However, this approach results

in reduced efficiency of energy harvesting at the high solar irradiances. In this case, the design procedure for optimal selection of converter parameters (i.e. inductance L and capacitance C) is based on considering only 70% of the nominal power of the PVG under the maximum current ripple condition [7, 8]. In [8] for the boost converter design a duty cycle of 0.5 is selected, because the maximum current ripple condition occurs when the output voltage is twice the input voltage. This conventional design procedure does not report on the limitation of the output voltage due to the maximum power point tracking (MPPT) controller, or the effect of different weather conditions on choosing optimal values for L and C . The authors in [9] has considered the MPPT limitation and the effect of weather conditions on choosing the converter parameters, but the analysis is restricted only to stand-alone applications (i.e. resistive load at the output). In grid-connected mode applications, the PVG system is connected to a regulated DC bus which implies a fixed level of voltage at the output to be considered for converter design. Moreover, connecting a PVG to a DC micro-grid requires a high conversion ratio which has to be taken into account when designing the power-stage. The design considerations of PV-interfaced power converters when connected to a DC micro-grid are not well documented in the literature, and therefore discussed in this paper.

For PVG systems interfacing a DC micro-grid, the literature focuses on improving MPP tracking algorithms [10], proposing new topologies to increase system efficiency or to reduce the cost [11], suggesting different controllers arrangements to ensure high performance at both grid-connected and islanded modes [12] and highlighting stability issues that occur in DC micro-grids due to constant power loads. However, the interactions between the non-linear PVG sources and the rest of the system, which may affect the system performance and stability, are not well documented. A clear understanding of these interactions can help to set system design recommendations and guidelines for the PVG power-stage interfacing a DC micro-grid, and for this reason these issues are investigated in this paper.

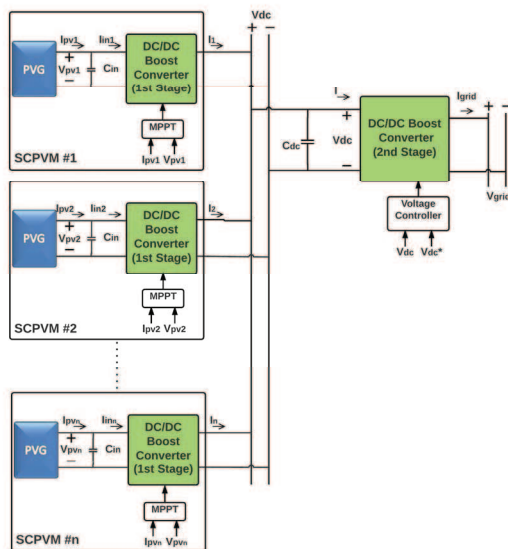
2. System Configuration

It is generally agreed that a future DC system should be formed as multiple buses with different voltage levels. The main bus with most of DGs connected to it, is suggested as having a regulated voltage level in the range of 380-400V, since this voltage level can meet the industry standard for consumer electronics with the power factor correction circuit at the input [12, 13]. Also, this voltage level offers good efficiency when supplying high-demanding loads (e.g. hybrid electric vehicle chargers, washing machines) [12]. The PVG low voltage output (around 30-48V) is usually connected to the high voltage DC bus (~400V). The most common configuration connects multiple PVG modules in series to a centralized MPPT power converter [1]. The main disadvantage of this configuration is very sensitive to mismatching phenomena which increase the system losses. Also, the centralized MPPT may induce increased power losses resulting in poor overall system efficiency. To overcome the drawbacks of mismatching and MPPT low efficiency, nowadays an alternative PVG system structure called Distributed MPPT (DMPPT) is widely adopted [10]. It is based on dedicating an MPPT DC/DC converter for each PVG module. In the rest of this paper, a PVG module with its dedicated MPPT converter will be referred to as a Self-Controlled Photovoltaic Module (SCPVM). A series connection of multiple SCPVMs can be directly connected to the DC micro-grid. The drawback of this configuration is that under a mismatching condition there is difficulty in achieving the desired output voltage of some SCPVMs. This is because voltage across each SCPVM depends on the ratio of its output power with respect to the total output power of the whole string [10]. To solve this problem an advanced and more complex control structure is necessary, or a parallel configuration adopted instead.

In the parallel configuration, the SCPVMs are connected in parallel to the main DC bus. The main disadvantage of this topology is the requirements set on a DC/DC converter to fulfil two contrasting requirements: a high-step-up voltage conversion ratio (about 10-15) and a high conversion efficiency [10]. That being the case, a significant number of research papers have been focused on achieving these requirements for a single-stage-power conversion system, with different solutions proposed in [11]. Another approach to boost the voltage is by using a double-stage-power conversion [11]. In this configuration, the conventional boost converter can be used for each stage. Choosing between the

single-stage and the double-stage power conversion is normally based on its capability to provide high-step-up voltage, high efficiency, low cost, simplicity, high MPPT efficiency and high MPP tracking speed. The single-stage conversion topology is superior in its efficiency but the dynamic performance of the MPPT with the new proposed single-stage topologies has not been proven so far. However, in the case of double-stage based on using conventional boost converter, a high MPPT efficiency has been proven [10] and achieving high tracking speed is easy due to the simple structure of the boost converter.

The parallel configuration with double-stage boost converter is adopted in this paper as it offers advantages in boosting the voltage, minimizing shading effects, improving system modularity, improving MPPT performance and efficiency, and providing the same voltage level at the output of each SCPVM under mismatching conditions. The full system configuration is shown in Figure 1. The system consists of many SCPVMs connected in parallel. Each SCPVM consists of a DC/DC boost converter, a PV generator (i.e. PVG NU-E240) and a MPPT digital controller. In this paper, the controllers' implementation is based on the assumption that the DC micro-grid is in grid-connected mode or in islanded mode where the storage system is large enough to allow MPP tracking all the time. The first-stage converter's controller is responsible for MPP tracking (i.e. direct duty cycle perturbation and observation P&O method is adopted) and the second-stage converter's controller controls the DC-link voltage V_{dc} . The DC micro-grid voltage ($V_{grid}=400V$) is controlled either by the bidirectional AC/DC inverter which connects the DC micro-grid to the main AC network, or by the storage system converter. The second stage DC/DC converter is responsible for boosting the V_{dc} voltage to the DC micro-grid voltage ($V_{grid}=400V$).



The technical specifications of the PVG

NU-E240 (J5)	
Quantity and wiring cells in series	60
Maximum Power	240 Wp
Open Circuit Voltage	37.3 V
Short Circuit Current	8.63 A
Standard Operation Condition	25 °C
Voltage Maximum Power (V_{MPP})	30.2 V
Current Maximum Power (I_{MPP})	7.95 A

Figure 1: System Configuration, PVG interfaced DC micro-grid

The data and the simulation results in this paper are obtained from a simplified system; the case when the system has only one SCPVM. However, the system can be scaled up for a higher power rating simply by increasing the number of parallel SCPVMs, and increasing the power rating of the second stage converter. The first-stage converter of the SCPVM does not need to be re-designed if identical PVG panels are used.

3. Design Considerations of double-stage DC-DC Boost Converter

There are two key points to be considered when designing the first-stage converter, namely the limitation on the output voltage to ensure the MPPT is functioning under all weather conditions and the effect of changes in weather conditions and output voltage on the converter parameters.

The first-stage boost DC/DC converter is controlled by an MPPT algorithm to track the maximum power available, and to adjust the duty cycle of the converter accordingly. The required duty cycle

(D_{MPP}) for the boost converter to obtain the maximum power from the PV array can be found from the basic boost voltage gain equation in [14].

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \quad (1)$$

If the system operates at MPP, the PVG voltage will be $V_{in} = V_{mpp}^{STC}$ and if the output voltage is regulated, then the output voltage V_{out} will be constant. Assuming a converter efficiency of 100% (*i. e.* $P_{in} = P_{mpp} = P_{out}$), the duty cycle is given by:

$$D_{mpp} = 1 - \frac{V_{mpp}^{STC}}{V_{out}} \quad (2)$$

Under different solar irradiation and constant temperature conditions, V_{mpp} changes very slightly and can be assumed to be constant (equal to V_{mpp}^{STC}). This means that both the input voltage and the output voltage of the boost converter are constant, thus the duty cycle will not change as the irradiation changes. This makes the design of the converter easier. The situation will be different if the effect of changing the cell temperature is included because V_{mpp} will not be constant in this case. Figure 2(a) shows the required duty cycle for the highest and lowest irradiation to achieve the maximum power

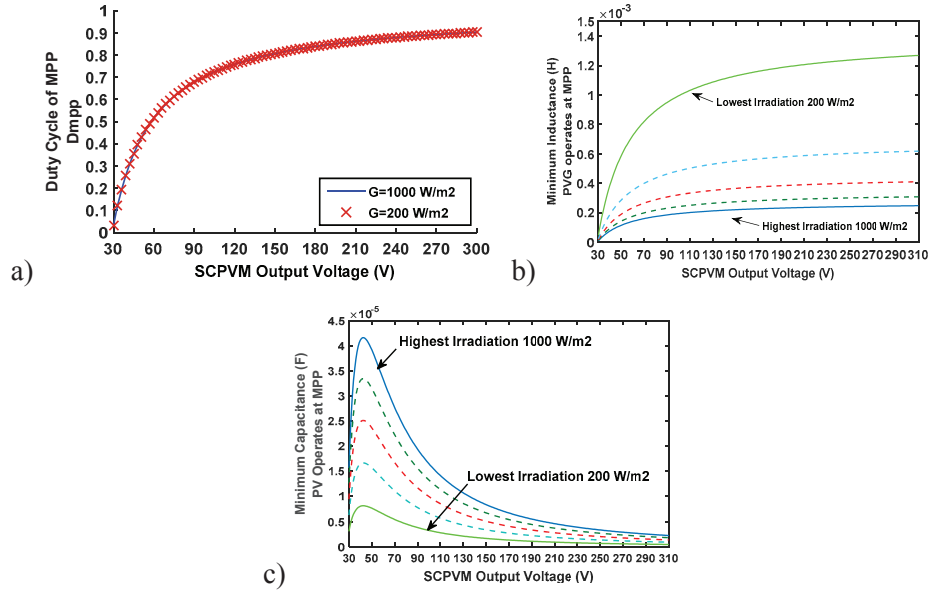


Figure 2: Effect of SCPVM voltage and solar irradiation (1000 W/m²-200 W/m²) on the first stage converter design: (a) Duty cycle (b) Inductance size for 13% current ripple (c) Capacitance size for 1% voltage ripple.

point for a given constant output voltage. It shows that the duty cycle is the same for different irradiation conditions and it hits its maximum defined limit of $D_{max} = 0.9$ at 290V. Therefore, for the tested system under constant temperature conditions, the output voltage limit is given by:

$$V_{mpp}^{STC} < V_{out} < \frac{V_{mpp}^{STC}}{1-D_{max}} \quad (3)$$

and

$$29 V < V_{out} < 290 V \quad (4)$$

First-stage converter design and its parameters (*i. e.* inductance L and capacitance C) selection will be analysed considering the output voltage range in (4). The minimum inductance L_{min} of the first stage converter can be found from the following equation [14]:

$$L_{min} = \frac{V_{in} \cdot D_{MPP}}{\Delta I_{p-p} \cdot f_{sw}} \quad (5)$$

In general, the current ripple ΔI_{p-p} in (5) can be selected based on the minimum current ripple requirement for the highest PV input current (i.e. the highest irradiation) or for the lowest input current (i.e. the lowest irradiation). Figure 2(b) shows the effect of changing the solar irradiation and SCPVM output voltage on L_{min} . Low solar irradiation conditions present the worse-case design requirement. However, other factors have to be considered such as the inductance core size, power production, and its effect on the speed of the MPPT controller in deciding which operating point to use for the design. If L is designed based on the highest irradiation, the result is smaller inductance than for the lowest irradiation as shown in Figure 2(b). In this case the core size will be smaller [15] and the MPP tracking is faster [10]. However, two key drawbacks can be identified. First, at lower solar irradiation the current ripple amplitude accounts for the higher percentage of the total current and thus the power production of the PV panel will be lower than in the case if the higher inductance were used [15]. Second, under the conditions of low input current (i.e. low solar irradiation) the converter might operate in discontinuous conduction mode (DCM). If L is designed based on the lowest irradiation the higher inductance is needed and more power will be extracted at the low irradiation levels [15]. However, for this case the core size has to be designed for the highest current to avoid magnetic saturation.

The inductance is one of the factors that affects the MPPT sampling rate. A smaller inductance will result in the faster MPPT for the same input capacitance [10]. Aiming for the faster MPPT and small inductance core, high irradiation is used for designing L . DCM can be avoided by opting for the current ripple to be less than twice the minimum current at the lowest irradiation.

The capacitance can be found from equation (6) [14]. The effect of the irradiation level and the SCPVM output voltage on the capacitance size is shown in Figure 2(c) for peak to peak voltage ripple requirements v_r of 1%. The highest irradiation level presents the worst case scenario.

$$C_{min} = \frac{I_{out} D_{MPP}}{v_r \cdot f_{sw}} \quad (6)$$

Figure 2(c) shows that increasing the output voltage will reduce the required capacitance; however, this will increase the duty cycle which affects the inductor copper losses and the semiconductor conduction losses [14]. Also, going back to the inductance design, increasing the output voltage will increase the inductance size. Another point that has to be considered when choosing the capacitance is the chosen PVG configuration. As example, in case of series connection of SCPVM, the voltage across each SCPVM will vary randomly due to the non-uniform solar irradiation [10]. Therefore, in order to meet the minimum voltage ripple requirement the worst case operating condition has to be considered in the design of C_{dc} . This limitation is not applied in the case of parallel connections which give more flexibility in choosing C_{dc} depending on the regulated DC-link voltage.

The proposed double-stage boost converter requires a conversion ratio to be not less than 14 to boost the voltage from 29V to 400V. Splitting this conversion ratio between the two converter stages will guarantee better performance and avoid that one of the converters operating at a very high conversion ratio. The converter of the SCPVM has been designed with a conversion ratio of 3.5 and output voltage of 100V. Therefore, the inductance (L_1) and the capacitance (C_{dc}) are chosen as 200 μ H and 41 μ F, respectively. The second-stage converter is designed for a conversion ratio of 4 and its parameters (L_2 & C_o) are selected so that the peak-peak output voltage (V_{grid}) ripple is less than 1.5V and the peak-peak current ripple is 20% of the input current, in the case when the SCPVM operates under the highest solar irradiation.

4. The Effect of PVG on the Controller Performance

The controller structure of the system operating at MPP mode is shown in Figure 3(a). MPPT's parameters (sampling period T_{mpp} and the amplitude of the duty-cycle perturbation Δd) has been optimized based on [16]. A PID controller (7) is used for controlling the dc-link voltage.

$$G_c(s) = \frac{K_v \left(1 + \frac{s}{\omega_{z1}}\right) \left(1 + \frac{s}{\omega_{z2}}\right)}{s \left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (7)$$

The controller is designed by considering an ideal current source at the input of the second-stage converter as shown in Figure 3(b). The transfer function of the duty-cycle-to-dc-link voltage $G_{v_{dc}d_2}$ of the second-stage is:

$$G_{v_{dc}d_2}(s) = \frac{\tilde{v}_{dc}}{\tilde{d}_2} = -\frac{V_{grid}}{L_2 C_{dc}} \frac{1+r_{C_{dc}} C_{dc} s}{s^2 + \frac{r_{l_2} + r_{C_{dc}}}{L_2} s + \frac{1}{L_2 C_{dc}}} \quad (8)$$

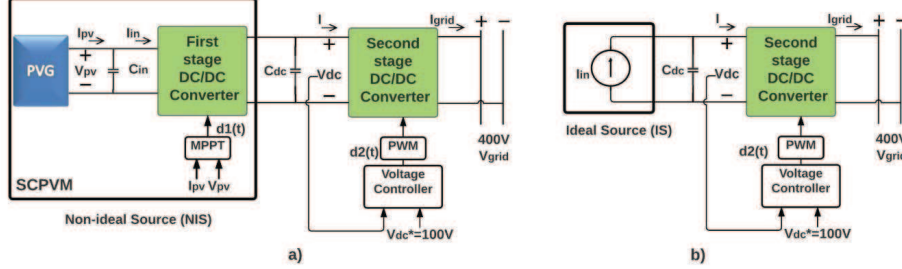


Figure 3: Controller structure of the simplified system. (a) non-ideal source configuration, (b) ideal source configuration.

A switching model of the double-stage boost converter connected to a 400V grid is implemented in MATLAB Simulink. The PVG NU-E240 is modelled using the single diode model. The simulation parameters for the P&O controller and the first-stage and second-stage converters are listed in Table I. The designed PID controller is shown in (9). The cut-off frequency ω_c is tuned to 118k rad/s which gives a phase margin of $PM \cong 66^\circ$ and a gain margin of $GM = 105\text{dB}$.

$$G_c(s) = \frac{-197}{s} \frac{\left(1 + \frac{s}{1904}\right) \left(1 + \frac{s}{5338.6}\right)}{\left(1 + \frac{s}{2e+07}\right) \left(1 + \frac{s}{3.142e+05}\right)} \quad (9)$$

Table I: Simulation Parameters

Parameter	First-stage converter							P&O		Second-stage conv.			
	C_{in}	r_{cin}	L_1	r_{l1}	C_{dc}	r_{cdc}	f_{sw}	T_{mpp}	Δd	L_2	C_o	r_{co}	f_{sw2}
Value	1.5	8	200	6.4	41	1.2	100	60	0.02	1.5	4	12	100
Unit	μF	$\text{m}\Omega$	μH	$\text{m}\Omega$	μF	$\text{m}\Omega$	kHz	μs	-	mH	μF	$\text{m}\Omega$	kHz

Figure 4 shows the analytical and simulation results for the control loop $T = G_c(s) \cdot G_{v_{dc}d_2}(s) \cdot G_{PWM}(s)$ for the system with ideal-source IS (Figure 3(b)) and with non-ideal source NIS (i.e. with SCPVM) under the conditions of solar irradiation changes. The figure shows that with the NIS as an input, the system is well damped at high solar irradiation, while the cut-off frequency and the PM are not affected.

Figure 5 shows the effect of the NIS when the PVG operating regions (i.e. constant voltage CV, constant current CC and MPP as shown in Figure 6) vary. It can be noted that the phase of the system is greatly affected at the low and medium frequencies. However, the phase is the same for all regions at high frequencies.

As seen in Figure 4 and 5 the high cut-off frequency has ensured the same system performance (the same phase and gain margins) under different operating conditions. However, this cut-off frequency is very high and might not be reasonable for real practical applications with higher power ratings. The switching frequency of the second-stage is chosen to be 100 kHz which allows very high cut-off frequency, though normally lower switching frequency is preferable to avoid high switching losses.

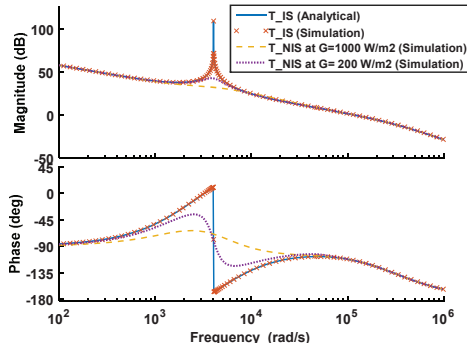


Figure 4: Effect of non-ideal source on the control loop. T_{IS} is the control loop gain with ideal current source. T_{NIS} is the control loop gain with non-ideal source. $C_{dc}=41\mu F$, $V_{dc}=100V$, $V_{grid}=400V$, and $K_v=197$. SCPVM operates at MPP.

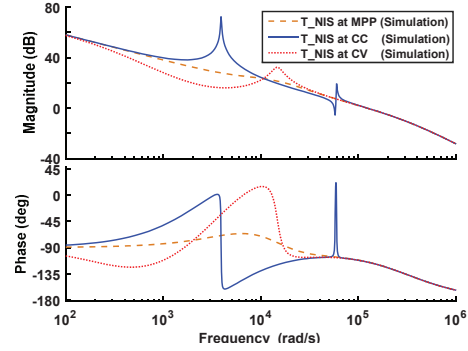


Figure 5: Effect of non-ideal source on the control loop when operating region changes. T_{NIS} is the control loop with non-ideal source. $C_{dc}=41\mu F$, $V_{dc}=100V$, $V_{grid}=400V$, $K_v=197$ and $G=1000 W/m^2$.

For these reasons ω_c is decreased by reducing the voltage gain K_v . Then the effect of the NIS source on the control loop gain at different operating regions is again examined. The control loop gain results after reducing ω_c to 12.7k rad/s are depicted in Figure 7. It shows that the system cut-off frequency and PM are affected as the operating region changes. In this paper the area of particular interest is the MPP region. It can be observed that in MPP mode, the system PM improves as K_v decreases which in return enhances system stability. The PM of the system in MPP mode has been measured from simulations for three different values of K_v as listed in Table II.

Table II: Simulation results for the phase margin PM as ω_c reduced. The system operates at MPP mode and C_{dc} is 41 μF .

K_v	ω_c (k.rad/se)	PM
197	118	66°
15	12.7	103°
6	2.6	106°

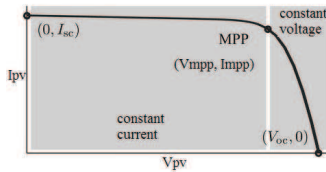


Figure 6: The three operating regions of PVG

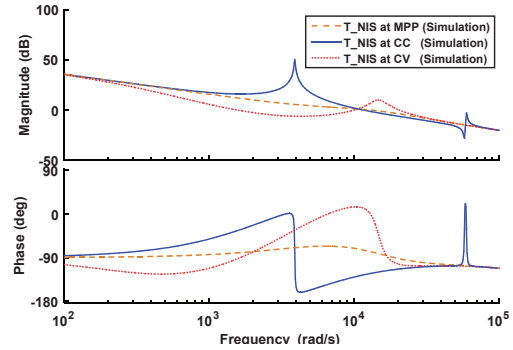


Figure 7: Effect of non-ideal source on the control loop gain when ω_c is reduced. $C_{dc}=41\mu F$, $V_{dc}=100V$, $V_{grid}=400V$ and $K_v=15$. At MPP ($V_{pv}=29V$), CV ($V_{pv}=35V$), and CC ($V_{pv}=19V$).

5. The Minimum DC-link Capacitance

Figure 8 shows the DC-link and grid currents for two different values of C_{dc} (i.e. for 70 μF and 20 μF). From the results it can be observed that the harmonic currents injected into the DC link were increased as the size of C_{dc} was reduced. These harmonics are produced from the increased interactions between the two converters as the DC-link capacitance is reduced and under these conditions the P&O duty cycle perturbations of the SCPVM are seen as disturbances by the second-stage. In addition, Figure 9 shows the effect of different irradiation levels on the harmonic currents injected into the DC link.

Based on the above discussion, at specific values of C_{dc} , K_v and DC-link current the high-order harmonics might occur in the DC-link and that can cause chaotic behaviour and even loss of system stability. The critical values of C_{dc} for different K_v and irradiation values for the double-stage boost converter in MPP mode were identified from the simulations. Firstly, for different solar irradiances (G) and under specific voltage gain (K_v) the dc link capacitance C_{dc} is reduced in small steps until the system became unstable (at critical value $C_{dc_min_G}$). For this critical capacitance value the cut-off frequency of the control loop, $\omega_{c_unstable_G}$, was measured from the simulation. Of note is that the value of $C_{dc_min_G}$ changes as K_v changes. The minimum $C_{dc_min_G}$, for different irradiation and voltage gain levels, to ensure stable operation of the system was found to be defined by (10) which can be derived from the control loop gain T shown in Figure 10 and the steps provided in Appendix A.

$$C_{dc_min_G} = \frac{V_m K_v K_G}{L_2 \omega_{z1} \omega_{z2} \omega_{c_unstable_G}} \quad (10)$$

where K_v is the dc gain of the voltage controller, K_G is the dc gain of $G_{v_{dc}d_2}$, $\omega_{c_unstable_G}$ is the cut-off frequency where the system becomes unstable at irradiation G , L_2 is the inductance of the second stage, ω_{z1} and ω_{z2} are the PID controller's zeros. The minimum required DC-link capacitance C_{dc} at MPP of a input-voltage-mode-controlled double-stage boost converter is depicted in Figure 11.

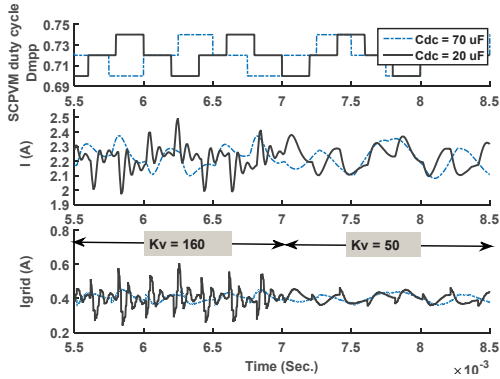


Figure 8: The effect of C_{dc} and K_v on the system behaviour: $G=1000 \text{ W/m}^2$, $C_{dc}=20\mu\text{F}$ and $70\mu\text{F}$, $V_{dc}^*=100 \text{ V}$, $V_{grid}=400\text{V}$, $T_{mpp}=0.2\text{ms}$, and K_v is changing from 160 to 50 at $t=7\text{ms}$

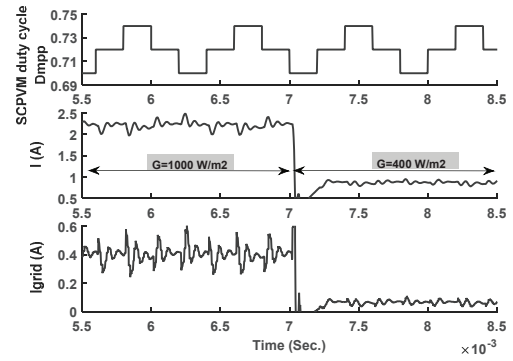


Figure 9: The effect of G on the system behaviour: G changes from 1000 to 400 W/m^2 at $t=7\text{ms}$, $C_{dc}=20 \mu\text{F}$, $V_{dc}^*=100 \text{ V}$, $V_{grid}=400\text{V}$, $T_{mpp}=0.2\text{ms}$, and $K_v=160$.

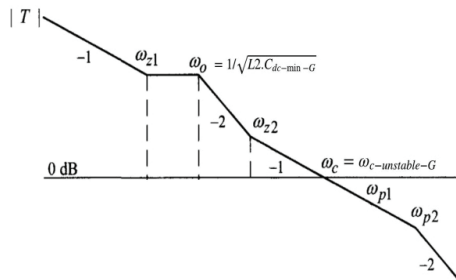


Figure 10: Asymptotic plot of the control loop gain magnitude.

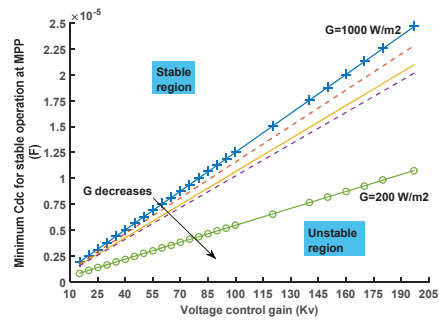


Figure 11: Stable operating regions of the double-stage boost converter

The unstable case, when SCPVM operates at MPP and insufficient value of C_{dc} (e.g. $20\mu\text{F}$) is used with high solar irradiation (1000 W/m^2) and $K_v=197$, is shown in Figure 12 and Figure 13. In Figure 12 it can be seen that after reducing K_v from 197 to 150 at $t=7\text{ms}$, the system stabilises. Figure 13 shows the effect on stability due to changes in irradiation; the system becomes stable by reducing the irradiation from 1000 W/m^2 to 400 W/m^2 .

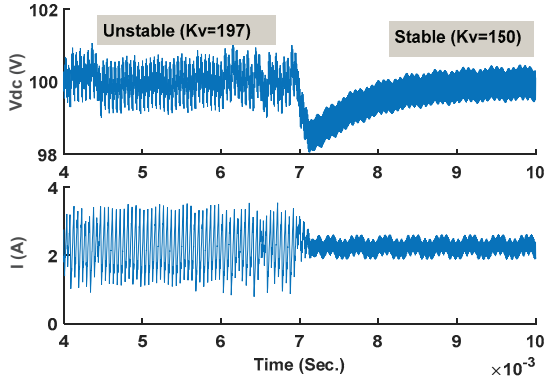


Figure 12: Stabilising the system by reducing K_v from 197 to 150 under the same solar irradiation. ($H_G=1000W/m^2$, $V_{dc}=100V$, $C_{dc}=20 \mu F$)

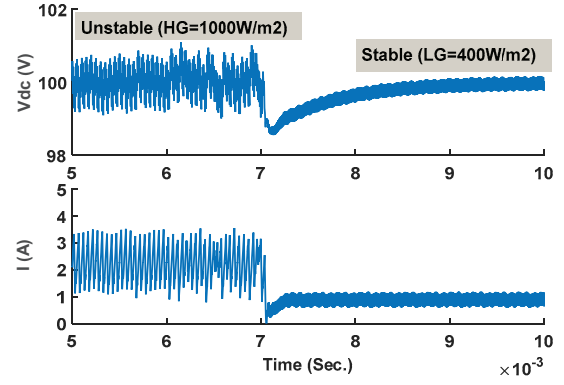


Figure 13: Effect of solar irradiation changes from $H_G=1000W/m^2$ to $L_G=400W/m^2$, $V_{dc}=100V$, $C_{dc}=20\mu F$, $K_v=197$

6. Conclusions

The design considerations of the double-stage boost converter for connecting a PVG to a DC micro-grid have been discussed. The available range of the DC-link voltage for successful tracking of MPP has been identified. The effect of that voltage range on the first-stage converter parameters under different weather condition is analysed. The converter parameters are chosen based on the highest solar irradiation condition to ensure high performance of the MPPT, small inductance core size and the required DC-link voltage ripple under different weather conditions.

Regarding the controller design, designers have to bear in mind that when operating at low or medium system bandwidth the cut-off frequency and PM are affected by the non-linear PVG source as the operating region changes due to weather conditions or load variations.

Minimizing the DC-link capacitance is preferable for system reliability, however it was shown in this paper that insufficient dc-link capacitance can lead to chaotic behaviour and even loss of system stability. To avoid this problem the minimum dc-link capacitance for stable operation of the double-stage boost-converter was identified under different solar irradiation levels and with different voltage gain of the second-stage converter.

Appendix A

The control loop gain (T) is

$$T = G_c(s) \cdot G_{v_{dc}d_2}(s) \cdot G_{PWM}(s) \quad (A1)$$

$G_{PWM}(s) = \frac{1}{V_m}$. Defining $K_G = -V_{grid}$ equation (A1) gives (A2):

$$T = \frac{K_v K_G}{V_m} \cdot \frac{1 + r_{C_{dc}} C_{dc} s}{L_2 C_{dc} s^2 + C_{dc}(r_{L_2} + r_{C_{dc}})s + 1} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (A2)$$

The resonance frequency ω_o at $\omega_{c_unstable_G}$ is $\frac{1}{\sqrt{L_2 C_{dc_min_G}}}$. From Figure 11 and equation (A2), the following relation is derived:

$$20 \log\left(\frac{K_v K_G / V_m}{\omega_{z1}}\right) - 40 \log\left(\frac{\omega_{z2}}{1/\sqrt{L_2 C_{dc_min_G}}}\right) - 20 \log\left(\frac{\omega_{c_unstable_G}}{\omega_{z2}}\right) = 0 \text{ dB} \quad (A3)$$

Solving and re-arranging equation (A3) for $C_{dc_min_G}$ gives:

$$C_{dc_min_G} = \frac{V_m K_v K_G}{L_2 \omega_{z1} \omega_{z2} \omega_{c_unstable_G}} \quad (A4)$$

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