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Self-Synchronized Universal Droop Controller

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ABSTRACT In this paper, a self-synchronization mechanism is embedded into the universal droop controller (UDC), which is applicable to inverters having an impedance angle between $-\pi/2$ rad and $\pi/2$ rad, to form a self-synchronized UDC (SUDC). Both the voltage loop and the frequency loop of the UDC are modified to facilitate the standalone and grid-connected operation of inverters. Importantly, the dedicated phase-locked-loop that is often needed for grid-connected or parallel-operated converters is removed. The inverter is able to achieve synchronization before and after connection without the need of a dedicated synchronization unit. Since the original structure of the UDC is kept in the SUDC, the properties of the UDC, such as accurate power sharing and tight output voltage regulation, are well maintained. Extensive experimental results are presented to demonstrate the performance of the proposed SUDC for a grid-connected single-phase inverter.

INDEX TERMS Grid-connected inverters, universal droop controller (UDC), phase-locked-loop, self-synchronization, smart grid integration, parallel operation.

I. INTRODUCTION

Due to global warming and environmental crisis, renewable energy systems in smart grids, e.g., wind, solar and tidal power, have been extensively studied during the last few decades [1]–[3]. When the amount of such renewable energy exceeds a certain level, it is inevitable that they will be required to take part in the regulation of system frequency and voltage in smart grids. This means numerous power inverters will be connected to the power grid, which are practically operated in parallel. For such applications, droop control is widely considered as a key technique to regulate the power flow between renewable energy sources and power grid [1], [2], [4]–[10], due to its simple structure and the independence from external communication.

Grid-connected inverters can be operated in the islanded and grid-connected modes. In the islanded mode, the main control objective is to achieve accurate load sharing among inverters and voltage regulation. Sharing linear and non-linear loads equally has been extensively investigated [11]–[16] and high accuracy of equal sharing can be achieved. In order to achieve accurate proportional sharing, it was required that the inverters in parallel operation should have the same per-unit output impedance, which is difficult to be satisfied in practice. This problem is solved in [17] with a robust droop controller to achieve accurate proportional sharing without the need of having the same per-unit output impedances for all the inverters. In addition, the load voltage drop due to the load effect and the droop effect is significantly reduced. However, inverters can have different types of output impedance, which requires changing the form of the droop controller. Recently, the requirement on the same type of output impedance for droop control is removed in [18], where it is mathematically proven and experimentally validated that the robust droop controller proposed in [17] originally for R-inverters can actually be applied to all practical inverters having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad, without the need of knowing the type or value of the impedance. In other words, it is a universal droop controller (UDC) [18].

When an inverter is operated in the grid-connected mode, the main objective is to regulate the power flow between the inverter and the grid. There are two different modes: the set mode to send the desired amount of real power and reactive power to the grid and the droop mode to change the real/reactive power exchanged with the grid according to the grid frequency/voltage. In this paper, the set mode is denoted as the P-mode for the real power and the Q-mode for the reactive power; the droop mode is denoted as the P_D-mode for the real power and the Q_D-mode for the reactive power. For grid-connected inverters, it is expected that all the four operations can be achieved so that the inverters can fully take part in the regulation of grid voltage and frequency under different scenarios.

Grid-connected inverters often require a dedicated synchronization unit to synchronize with the grid [5]–[7], [14], [15]. The difference between the output voltage and the grid voltage should be small enough in order to avoid high inrush current when connecting the inverter to the grid. Phase-locked-loops (PLLs) are normally used for this purpose. However, it is well known that PLLs are highly non-linear, which inevitably complicates systems [19] or even causes instability [20]. When there are many PLLs in a system, they tend to compete with each other as well. Recently, it has been shown that the synchronization can be achieved without using PLLs for the first time in [19]. Instead of using a dedicated synchronization unit, like a PLL, the controller for synchronverters [19], [21], which are inverters that mimic synchronous generators, is equipped with a built-in self-synchronization mechanism to achieve synchronization. Another example is [22], where a universal integrated synchronization method is implemented so that the output voltage can be synchronized with the grid without using a dedicated synchronization unit. Very recently, it has been shown that the droop controller and the enhanced phase-locked loops structurally resemble each other [23], [24]. This provides the theoretical explanation why the dedicated synchronization unit could be removed.

In this paper, this line of research has been further advanced. A self-synchronized universal droop controller (SUDC) is proposed for grid-connected inverters to achieve PLL-less grid-connected operation for droop controllers, via embedding the self-synchronization strategy proposed in [19] into the universal droop controller proposed in [18]. The dedicated synchronization unit normally needed in the droop controller is removed, which simplifies the system structure and reduces the burden of tuning the parameters. More importantly, the original structure of the UDC is well maintained so that accurate proportional power sharing and tight voltage regulation can be achieved, for inverters having an output impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad. All the four modes, i.e., P- and Q-mode, P- and Q_D-mode, P_D- and Q-mode, P_D- and Q_D-mode, can be achieved without any problem. Since the proposed SUDC is the same as the original UDC in the islanded mode, the main focus of this paper is put on the grid-connected mode. Readers interested in the performance of the SUDC in the islanded mode can refer to [17] and [18]. A lot of experiments are presented to verify the effectiveness of the proposed SUDC. Note that although some of the ideas in [18], [19], and [24] played an important role in forming the proposed controller, it is different from any of the controllers in [18], [19], and [24] and is worth special attention.

The rest of this paper is organized as follows. The original UDC in the islanded mode is first reviewed in Section II. The SUDC is proposed in Section III, with detailed discussions about the operation modes. In Section IV, the SUDC for both R-inverters and L-inverters are experimentally validated. Finally, conclusions are made in Section V.

II. OVERVIEW OF THE UNIVERSAL DROOP CONTROLLER (UDC)

The form of droop controllers normally changes with the type of the impedance [1], [18]. Here, the universal droop controller that is applicable to any inverters having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad is reviewed.

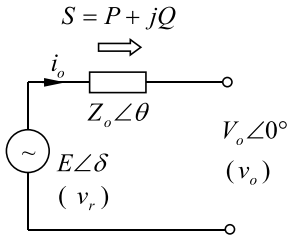


FIGURE 1. A single-phase inverter model.

The model of a single-phase inverter is shown in Figure 1, where E is the RMS value of the reference voltage v_r and V_o is the RMS value of the output/terminal voltage v_o. The real and reactive power transferred from the inverter source v_r to the terminal v_o are

$$P = (\frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o})\cos\theta + \frac{EV_o}{Z_o}\sin\delta\sin\theta \quad (1)$$

$$Q = (\frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o})\sin\theta - \frac{EV_o}{Z_o}\sin\delta\cos\theta. \quad (2)$$

Here, δ is the phase difference between the voltage v_r and the terminal voltage v_o. Assume the output impedance is dominantly resistive for the moment. When it is purely resistive, i.e., $\theta = 0$, and assume that δ is small, there are

$$P \approx \frac{E - V_o}{Z_o}V_o, \quad \text{and} \quad Q \approx -\frac{EV_o}{Z_o}\delta. \quad (3)$$

Hence,

$$P \sim E \quad \text{and} \quad Q \sim -\delta \quad (4)$$

where $\sim$ means "positive correlation". As a result, the droop control principle is formulated as

$$E = E^* - nP \quad (5)$$

$$\omega = \omega^* + mQ \quad (6)$$

where E^* is the rated RMS value of the output voltage v_o, ω^* is the rated system frequency, and n and m are the droop coefficients. This is used as the basic rules to construct conventional droop controllers [1], [17]. However, the conventional droop controller is sensitive to numerical errors, noises, disturbances, component mismatches and parameter shifts etc [17]. In order to address this problem, the robust droop controller proposed in [17], as shown in Figure 2, changes the droop control strategy to

$$\dot{E} = K_e(E^* - V_o) - nP \quad (7)$$

$$\omega = \omega^* + mQ \quad (8)$$

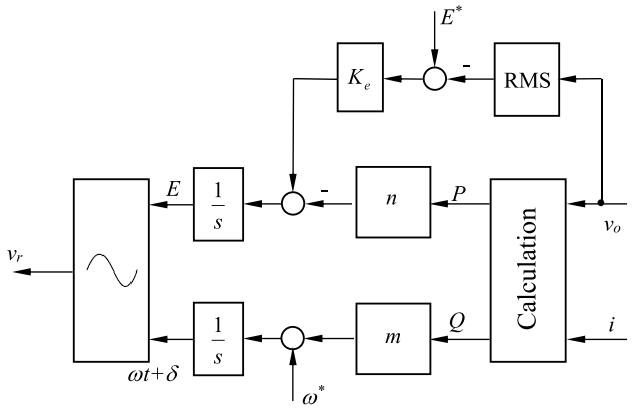


FIGURE 2. The robust droop controller that is universal for inverters having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad [17], [18].

where K_e is an amplifying coefficient. This is a dynamic implementation of (5) with an integrator. In the steady state, there is

$$nP = K_e(E^* - V_o). \tag{9}$$

As long as K_e is the same for all inverters, there is

$$nP = \text{constant}, \tag{10}$$

which guarantees the accurate proportional sharing of real power among the inverters in parallel operation. Moreover, the parallel-operated inverters have the same frequency as long as the system is stable, and thus the accurate proportional sharing of reactive power is guaranteed as well [17]. According to (9), the output voltage magnitude is

$$V_o = E^* - \frac{nP}{K_e E^*}E^*, \tag{11}$$

where $\frac{nP}{K_e E^*}$ is the voltage drop ratio. If a large K_e is chosen, the voltage magnitude could be maintained within the desired range to achieve tight voltage regulation.

Actually, (1-2) can be rewritten as

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o} \\ -\frac{EV_o}{Z_o}\sin\delta \end{bmatrix}.$$

The eigenvalues of $\begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}$ are $\cos\theta \pm j\sin\theta$, of which the real part $\cos\theta$ is positive for any output impedance with $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$. Hence, the relationship (4) holds for $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$. This means the robust droop controller discussed above is universal and can be applied to any inverters having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad. More details can be found in [18] and [25].

III. EQUIPPING THE UDC WITH A SELF-SYNCHRONIZATION MECHANISM

In order to synchronize the output voltage of inverters with the grid voltage, a droop controller, including the UDC, often needs a dedicated synchronization unit like a PLL. However, it is well known that the parameters of PLLs are usually difficult and time-consuming to tune. According to [23] and [24], a droop controller is intrinsically a PLL so it is possible to adopt the "hidden" synchronization mechanism in the UDC to achieve synchronization without a dedicated synchronization unit. This is the purpose of this paper and will be shown in this section. The resulting UDC is called the self-synchronized UDC (SUDC). It is expected that the SUDC could automatically synchronize the output voltage with the grid voltage by itself so that the inverter can be smoothly connected to the grid without noticeable inrush currents. After the inverter is connected to the grid, the SUDC should accurately regulate real and reactive power between the inverter and the grid.

A. DESCRIPTION OF THE CONTROLLER

The proposed SUDC is shown in Figure 3. Compared to the UDC shown in Figure 2, several major changes are made: 1) because the original UDC is designed to operate under the droop mode only, in order to operate the SUDC in the set mode and to facilitate the self-synchronization process, summation blocks are added after the power calculation block to compare the measured real power P and reactive power Q with the power references P_{set} and Q_{set}, respectively. This is equivalent to setting the rated operational point of the inverter at $P = P_{set}$ and $Q = Q_{set}$ when $V_o = E^*$ and $\omega = \omega^*$; 2) A virtual current i_s is generated via passing the voltage error $v_o - v_g$ through a virtual impedance $Ls + R$, which consists of a virtual inductance L in series with a resistance R; 3) A Switch S_c is added so that the current sent to the controller can be switched between the virtual current i_s and the grid current i_g; 4) A Switch S_P is added to enable or disable the addition of the term $K_e(E^* - V_o)$ from the controller; 5) An integrator is added to regulate $Q_{set} - Q$ to zero, with the reset function to enable or disable it via turning the Switch S_Q ON or OFF. The operation modes of the controller are summarized in Table 1, which will be discussed in detail later.

TABLE 1. Operation modes of the SUDC.

Mode	Switch S_C	Switch S_P	Switch S_Q
Self-synchronization mode	s	OFF	OFF
P-mode, Q-mode	g	OFF	OFF
P_D-mode, Q-mode	g	ON	OFF
P-mode, Q_D-mode	g	OFF	ON
P_D-mode, Q_D-mode	g	ON	ON

As can be seen from Figure 3, the controller can be described as

$$\dot{E} = V_d + n(P_{set} - P) \tag{12}$$

$$\omega = \omega^* + \omega_d - m(Q_{set} - Q) \tag{13}$$

with

$$V_d = \begin{cases} 0, & (S_P = \text{OFF}) \\ K_e(E^* - V_o), & (S_P = \text{ON}) \end{cases}$$

$$\omega_d = \begin{cases} \frac{mK}{s}(Q - Q_{set}), & (S_Q = \text{OFF}) \\ 0, & (S_Q = \text{ON}) \end{cases}$$

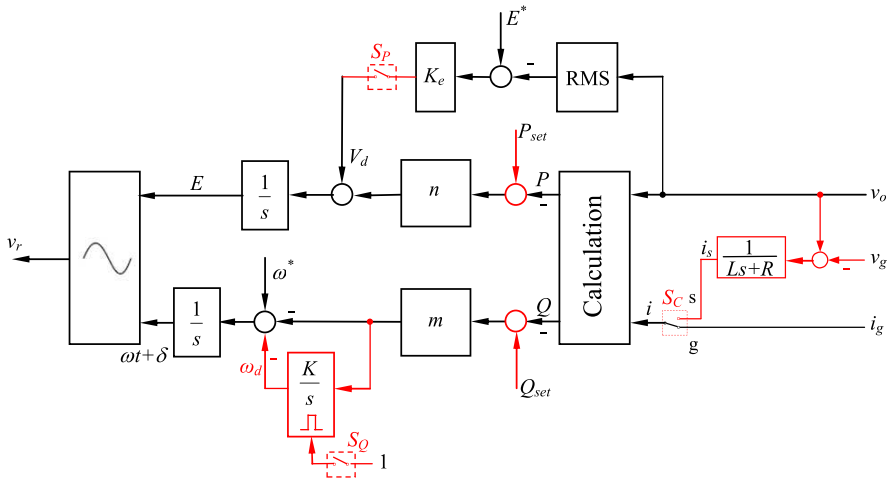


FIGURE 3. The proposed self-synchronized universal droop controller (SUDC).

where K is a positive gain. When the Switch S_P is turned OFF, the addition of the term $K_e(E^* - V_o)$ is disabled; when the Switch S_P is turned ON, the addition of the term $K_e(E^* - V_o)$ is enabled. Moreover, when the Switch S_Q is turned ON, the reset function of the integrator $\frac{K}{s}$ is enabled; when the Switch S_Q is turned OFF, the reset function is disabled and the integrator is added into the controller.

The real power P and reactive power Q are calculated from v_o and i. Note that a low-pass filter or a hold filter should be adopted to filter out the ripples in P and Q so that P and Q only contain the DC components. The current i can be switched between the grid current i_g and the virtual current

$$i_s = \frac{v_o - v_g}{Ls + R}. \tag{14}$$

When the Switch S_C is set at Position s, the virtual current i_s is sent to the power calculation block; when the Switch S_C is set at Position g, the grid current i_g is sent instead.

The parameters L and R can be chosen smaller than the inductance and resistance of the filter inductor to speed up the synchronization process. In order to filter out the effect of the harmonics on the synchronization, the ratio $\frac{L}{R}$ can be chosen larger than the fundamental system period. More details about selecting these parameters can be found in [19].

B. SELF-SYNCHRONIZATION MODE

Before the inverter is connected to the grid, the terminal voltage v_o should be synchronized with the grid voltage v_g, which means $V_o = V_g$ and $\omega = \omega_g$. According to (12) and (13), when S_P is OFF and S_Q is OFF, at the steady state, the real power P and the reactive power Q sent to the grid are controlled to be around their reference values P_{set} and Q_{set}, respectively, which are set at zero in the self-synchronization mode. However, both P and Q are always zero before the inverter is connected to the grid. In order to force the SUDC to start synchronizing with the grid, a virtual impedance $Ls + R$ is introduced to generate a virtual current i_s described by (14) according to the voltage difference $v_o - v_g$. For this purpose, the Switch S_C is set at Position s to route i_s for power calculation. In this mode, the SUDC becomes

$$\dot{E} = n(P_{set} - P) \tag{15}$$

$$\omega = \omega^* + \frac{mK}{s}(Q - Q_{set}) - m(Q_{set} - Q) \tag{16}$$

with

$$i = i_s. \tag{17}$$

Under this condition, if P_{set} and Q_{set} are both set at zero, then, at the steady state, when the current carried by the virtual impedance is regulated to zero, the terminal voltage $v_o = v_g$. In other words, v_o is synchronized with the grid voltage v_g. In order to enable this mode, both the Switch S_P and the Switch S_Q should be turned OFF with the Switch S_C set at Position s. After the synchronization is achieved, the relay in the inverter can be turned ON to connect the inverter to the grid. At the same time, the Switch S_C should be turned to Position g so that the real grid current i_g can be fed into the SUDC for the power calculation.

C. SET MODE (P-MODE AND Q-MODE)

After the inverter is connected to the grid, the Switch S_C is at Position g and the real grid current i_g is fed into the SUDC for the power calculation. When S_P is OFF, there is

$$\dot{E} = n(P_{set} - P). \tag{18}$$

The voltage magnitude E settles down at a constant value in the steady state, which results in

$$P = P_{set}. \tag{19}$$

The desired real power P_{set} is sent to the grid. Similarly, when Switch S_C is at Position g and S_Q is turned OFF, there is

$$\omega = \omega^* + \frac{mK}{s}(Q - Q_{set}) - m(Q_{set} - Q) \tag{20}$$

and the frequency settles down at a certain value in the steady state, which results in

$$Q = Q_{set}. \tag{21}$$

The desired reactive power Q_{set} is sent to the grid.

This mode is called the set mode, and the set mode for the real power is called the P-mode and the set mode for the reactive power is called the Q-mode.

D. DROOP MODE (P_D-MODE AND Q_D-MODE)

When the Switch S_C is at Position g and the Switch S_P is ON, there is

$$\dot{E} = n(P_{set} - P) + K_e(E^* - V_o) \tag{22}$$

and the voltage magnitude settles down at a constant value in the steady state, which results in

$$P = P_{set} + \frac{K_e}{n}(E^* - V_o). \tag{23}$$

This is the droop function of the real power with respect to the voltage. Similarly, when Switch S_C is at Position g and S_Q is ON, there is

$$\omega = \omega^* - m(Q_{set} - Q)$$

and the frequency settles down at a certain value, which results in

$$Q = Q_{set} + \frac{\omega - \omega^*}{m}. \tag{24}$$

This is the droop function of the reactive power with respect to the frequency. As can be seen from (23) and (24), the actual real power and reactive power sent to the grid are changed automatically according to the grid voltage V_o and the grid frequency ω, respectively.

The main purpose of this paper is to equip the UDC with the self-synchronization mechanism, as described above. Other aspects of the controller, e.g. stability analysis, are covered in [17] and [18].

IV. EXPERIMENTAL VALIDATION

In order to verify the proposed SUDC, intensive experiments were conducted on a single-phase grid-connected inverter. Here, the results from two cases with the inverter operated as an R-inverter and an L-inverter are presented. The virtual resistor used for the R-inverter is 4 Ω. The inverter has an LCL filter to filter out the high-frequency components in the output voltage and the grid current. The parameters of the system are summarized in Table 2. The control circuit of the system was constructed based on TMS320F28335 DSP, with the sampling frequency of 4 kHz. A DC power supply Agilent N8944A was used to provide the DC-bus voltage at 200 V.

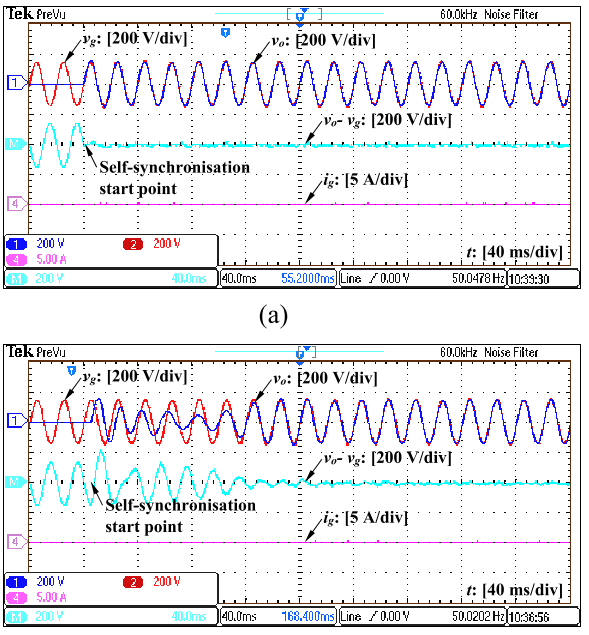
The droop coefficients are set in such a way that 100% increase of real power P results in 10% decrease of voltage E and 100% increase of reactive power Q results in 1% increase of the frequency f. Then, the droop coefficients can be calculated as $n = \frac{0.1K_eE^*}{S}$ and $m = \frac{0.01\omega^*}{S}$ according to [17], where S is the rated apparent power of the inverter.

TABLE 2. Parameters of the inverter.

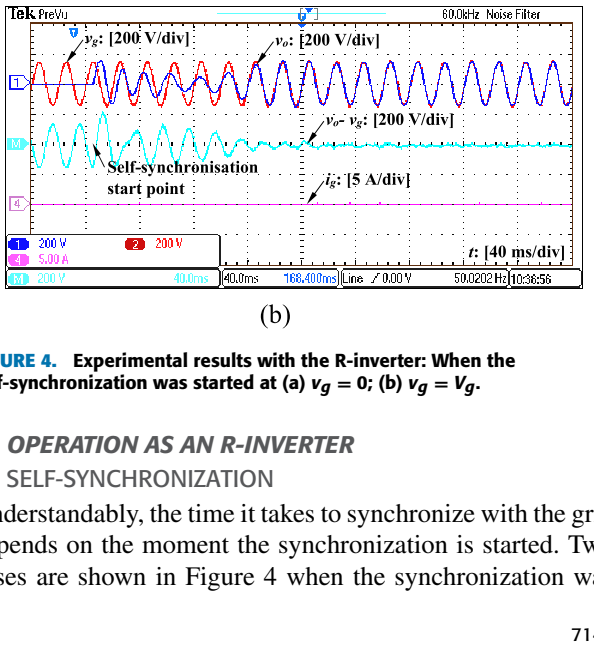
Parameters	Values
Grid voltage (RMS)	110 V
Line frequency f	50 Hz
Switching frequency f_s	19 kHz
DC-bus voltage V_{DC}	200 V
Rated apparent power S	300 VA
Inductance L_s	2.2 mH
Resistance R_s	0.2 Ω
Inductance L_g	2.2 mH
Resistance R_g	0.2 Ω
Capacitance C	10 μF

The experiments were conducted according to the following sequence of actions:

1) starting the self-synchronization mode (S_C: Position s; S_P: OFF; and S_Q: OFF) with $P_{set} = 0$ W, $Q_{set} = 0$ Var at $t = 0$ s;
2) turning the relay ON and switching S_C to the Position g at $t = 3$ s;
3) applying $P_{set} = 150$ W at $t = 6$ s;
4) applying $Q_{set} = 150$ Var at $t = 9$ s;
5) switching S_P ON to enable the P_D-mode at $t = 12$ s;
6) switching S_Q ON to enable the Q_D-mode at $t = 15$ s;
7) stopping data acquisition at about $t = 18$ s.



(a)



(b)

FIGURE 4. Experimental results with the R-inverter: When the self-synchronization was started at (a) $v_g = 0$; (b) $v_g = V_g$.

A. OPERATION AS AN R-INVERTER

1) SELF-SYNCHRONIZATION

Understandably, the time it takes to synchronize with the grid depends on the moment the synchronization is started. Two cases are shown in Figure 4 when the synchronization was

started at $v_g = 0$ and $v_g = V_g$. For the case with $v_g = 0$, the voltage difference between the output voltage and the grid voltage, i.e., $v_o - v_g$, quickly became very small as shown in Figure 4(a). It took less than one cycle for the whole self-synchronization process. For the case with $v_g = V_g$, as shown in Figure 4(b), it took about 6 cycles for the synchronization.

2) CONNECTION TO THE GRID

After the synchronization process is finished, the inverter is ready to be connected to the grid. At $t = 3$ s, the relay was turned ON and S_C was turned to Position g, which shifted the current used for calculating P and Q from the virtual current i_s to the real grid current i_g. As shown in Figure 5, the connection was seamless and the grid current i_g was well maintained around zero without any spikes, as expected, because $P_{set} = 0$ and $Q_{set} = 0$.

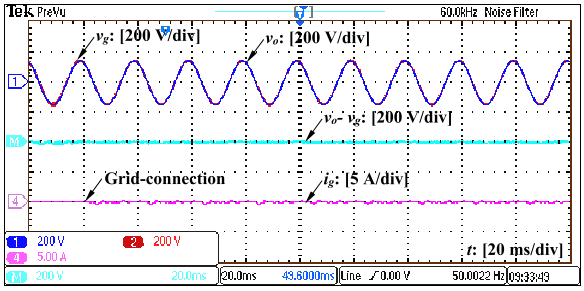


FIGURE 5. Experimental results with the R-inverter: Connection to the grid.

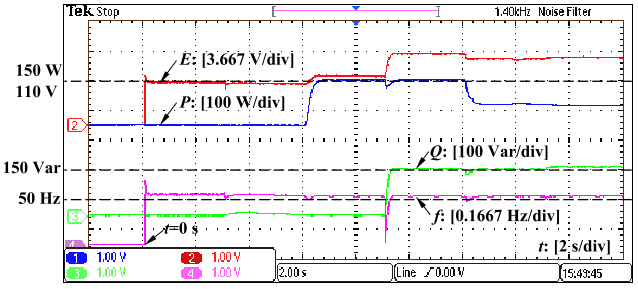


FIGURE 6. Experimental results with the R-inverter: Performance during the whole experimental process.

3) REGULATION OF REAL AND REACTIVE POWER

The real power, reactive power, frequency and voltage during the whole process are shown in Figure 6. After the self-synchronization was enabled at $t = 0$ s, both the real power and the reactive power were controlled around zero. When the inverter was connected to the grid at 3 s, there was not much transient and both the real and reactive power were maintained around zero. After that, the system responded quickly to the step changes of the real and reactive power demands at $t = 6$ s and $t = 9$ s, respectively, without any static error. After the P_D-mode was enabled at $t = 12$ s, the voltage E was 112.93 V, which is about 2.67% higher than the nominal value 110 V. In this case, according to the given droop coefficients, i.e., 10% increase of E results in 100% decrease of P, the real power is expected to drop by $\frac{2.67\%}{10\%} \times 300\,\text{W} \approx 80\,\text{W}$. Indeed, as shown in Figure 6, the real power P dropped by about 80 W from 150 W to 70 W. On the other hand, the reactive power increased after the Q_D-mode was enabled at $t = 15$ s, because the frequency f was 50.03 Hz, which is 0.06% higher than the nominal value. According to the droop coefficients, i.e., 1% increase of f results in 100% increase of Q, the reactive power is expected to increase by $\frac{0.06\%}{1\%} \times 300\,\text{Var} \approx 20\,\text{Var}$. As shown in Figure 6, the reactive power indeed increased by 20 Var from 150 Var to 170 Var.

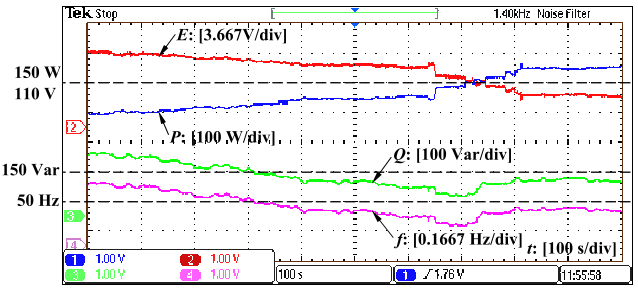


FIGURE 7. Experimental results with the R-inverter: Regulation of system frequency and voltage in the droop mode.

In order to test the regulation of the real power P and reactive power Q with respect to the variations of E and f, the inverter was kept running continuously in the P_D-mode and the Q_D-mode. The results are shown in Figure 7. The real power P is symmetrical to the changing voltage E and the reactive power Q follows the trend of the frequency f very well. It is worthy highlighting that this was achieved without a dedicated synchronization unit and the inverter kept in synchronization with the grid all the time, even when the frequency and voltage changed.

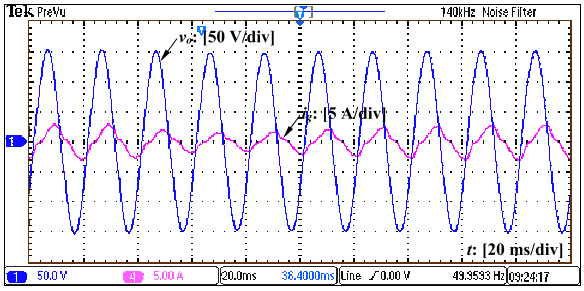
4) CHANGE OF THE DC-BUS VOLTAGE V_{DC}

In order to further test the robustness of the system, the DC-bus voltage V_{DC} was changed from 200 V to 180 V and then from 180 V to 200 V when the system was operated in the P-mode and Q-mode with $P_{set} = 150$ W and $Q_{set} = 150$ Var. When the V_{DC} was suddenly dropped from 200 V to 180 V, as shown in Figure 8, the grid current i_g dropped because of the lowered V_{DC}. But it only took about 5 cycles for the grid current i_g to recover in order to maintain the real power and reactive power sent to the grid at the reference values. When V_{DC} was suddenly increased from 180 V to 200 V, the grid current increased and it took about 5 cycles for the grid current to recover to its value before the voltage change.

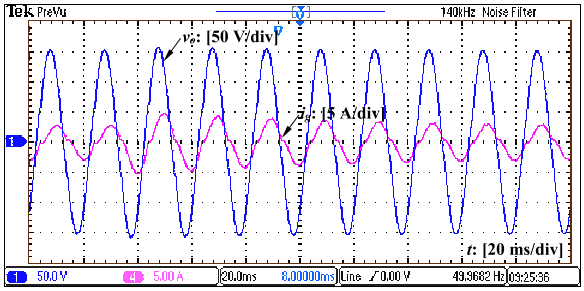
B. OPERATION AS AN L-INVERTER

1) SELF-SYNCHRONIZATION

Again, two cases with $v_g = 0$ and $v_g = V_g$ when the synchronization was started are considered here, with the

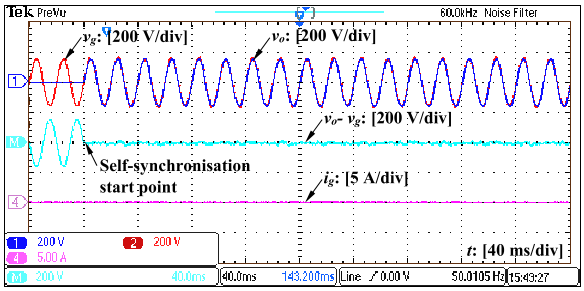


(a)

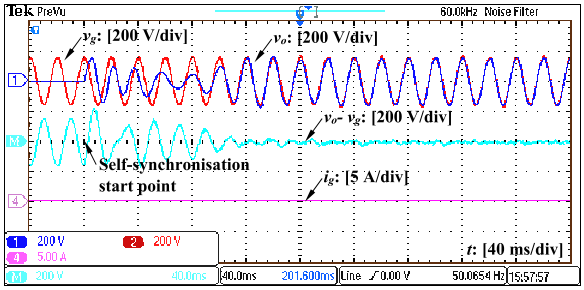


(b)

FIGURE 8. Experimental results with the R-inverter: Change of the DC-bus voltage V_{DC} (a) from 200 V to 180 V and (b) from 180 V to 200 V.



(a)



(b)

FIGURE 9. Experimental results with the L-inverter: When the self-synchronization was started at (a) $v_g = 0$; (b) $v_g = V_g$.

results shown in Figure 9. When $v_g = 0$, it took less than one cycle to synchronize with the grid. When $v_g = V_g$, it took about 6 cycles to synchronize.

2) CONNECTION TO THE GRID

At $t = 3$ s, the relay was turned ON and the S_C in the controller was turned to Position g to connect the inverter

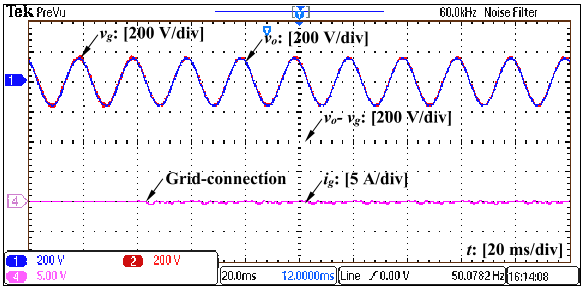


FIGURE 10. Experimental results with the L-inverter: Connection to the grid.

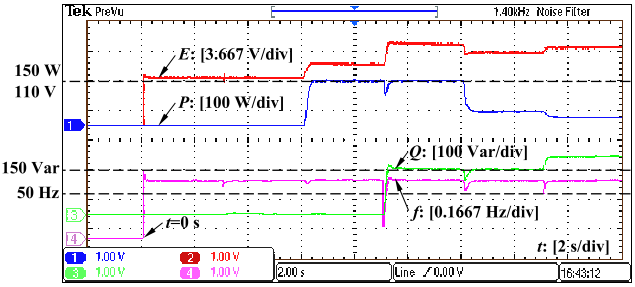


FIGURE 11. Experimental results with the L-inverter: Performance during the whole experimental process.

to the grid. As shown in Figure 10, the grid current i_g was smoothly maintained at around zero without any noticeable spikes.

3) REGULATION OF REAL AND REACTIVE POWER

The real power, reactive power, frequency and voltage during the whole process are shown in Figure 11. After the self-synchronization was enabled at $t = 0$ s, both the real power and the reactive power were controlled around zero. At $t = 3$ s, the inverter was connected to the grid without much transient, and both the real and reactive power were maintained around zero. At $t = 6$ s and $t = 9$ s, the inverter quickly responded to the real and reactive power demands, respectively. After the P_D-mode was enabled at $t = 12$ s, the voltage E was 114.4 V, which is about 4% higher than the nominal value 110 V. In this case, according to the given droop coefficients, i.e., 10% increase of the E results in 100% decrease of the P, the real power is expected to drop by $\frac{4\%}{10\%} \times 300\,\text{W} \approx 120\,\text{W}$. Indeed, as shown in Figure 11, the real power P dropped by about 120 W from 150 W to 30 W. On the other hand, the reactive power increased after the Q_D-mode was enabled at $t = 15$ s, because f is about 50.0667 Hz, which is 0.133% higher than the nominal value. According to the droop coefficients, i.e., 1% increase of f results in 100% increase of Q, the reactive power is expected to increase by $\frac{0.133\%}{1\%} \times 300\,\text{Var} \approx 40\,\text{Var}$. As shown in Figure 11, the reactive power indeed increased by 40 Var from 150 Var to 190 Var.

In order to test the regulation of P and Q with respect to the variations of E and f, the inverter was kept running

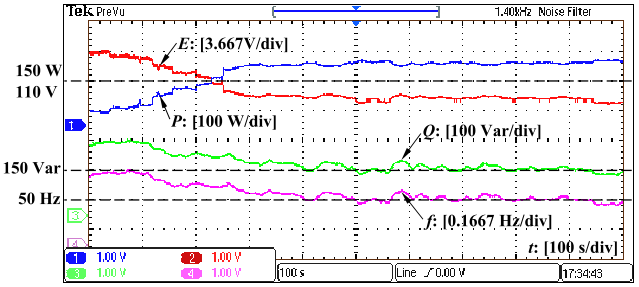
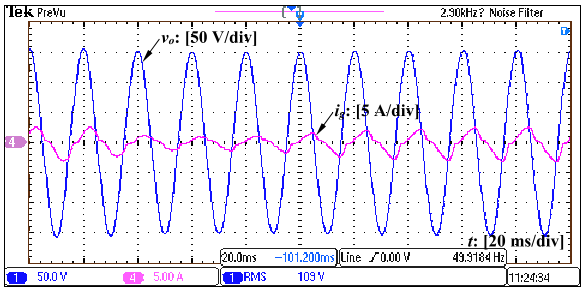
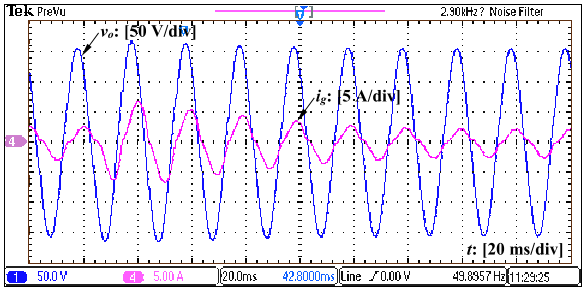


FIGURE 12. Experimental results with the L-inverter: Regulation of system frequency and voltage in the droop mode.



(a)



(b)

FIGURE 13. Experimental results with the L-inverter: Change of the DC-bus voltage V_{DC} (a) from 200 V to 180 V and (b) from 180 V to 200 V.

continuously in the droop mode (P_D- and Q_D-mode). The results are shown in Figure 12. The real power P is symmetrical to the varying voltage E and the reactive power Q closely follows the trend of the varying frequency f. Note again that this was achieved without a dedicated synchronization unit and the inverter kept in synchronization with the grid all the time, even when the frequency and voltage changed.

4) CHANGE OF THE DC-BUS VOLTAGE

In order to further test the robustness of the system, the DC-bus voltage V_{DC} was changed from 200 V to 180 V and then from 180 V to 200 V when the system was operated in the P-mode and Q-mode with $P_{set} = 150$ W and $Q_{set} = 150$ Var. The results are shown in Figure 13. The performance of the L-inverter during the change of the V_{DC} is very similar to that of the R-inverter. In both cases, it took about 5 cycles to recover.

V. CONCLUSIONS

In this paper, a self-synchronized universal droop controller has been proposed for inverters. With the proposed SUDC, no PLL is required, which reduces the complexity and computational burden of the controller. The output voltage of inverters can be synchronized with the grid before and after the connection by itself. Additionally, the proposed SUDC can be easily configured to operate in the set mode (P- and Q-mode) and the droop mode (P_D- and Q_D-mode). As a result, the inverters equipped with the SUDC can fully take part in the regulation of the grid voltage and frequency, which is important for large-scale renewable energy systems connected to the grid. Experimental results have validated the system performance in different operational modes.

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