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Modelling, Analysis and Experimental Validation of Clock Drift Effects in Low-Inertia Power Systems

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***Abstract*—Clock drift in digital controllers is of great relevance in many applications. Since almost all real clocks exhibit drifts, this applies in particular to networks composed of several individual units, each of which being operated with its individual clock. In the present work, we demonstrate via extensive experiments on a microgrid in the megawatt-range that clock drifts may impair frequency synchronisation in low-inertia power systems. The experiments also show that—in the absence of a common clock—the standard model of an inverter as an ideal voltage source does not capture this phenomenon. As a consequence, we derive a suitably modified model of an inverter-interfaced unit that incorporates the phenomenon of clock drifts. By using the derived model, we investigate the effects of clock drifts on the performance of droop-controlled grid-forming inverters with regard to frequency synchronisation and active power sharing. The modelling and analysis is validated via extensive experiments on a microgrid in the megawatt-range.**

***Index Terms*—Smart grid applications, low-inertia power systems, microgrids, grid-forming inverters, droop control, power sharing.**

I. Introduction

A. Motivation

WORLDWIDE, the use of renewable energies has increased significantly over the past years. This development is driven by political as well as environmental goals and facilitated by technological advances. Though the transition to a low-carbon future is desirable, it has tremendous implications for the operation of future power systems. The present paper is mainly concerned with the consequences for a particular, yet elementary, operational task in AC power systems, namely frequency control.

Maintaining the frequency within a certain range is one of the most important criteria to guarantee operational performance in power systems [1]–[3]. A main reason for this is that the frequency is an indicator of the active power balance between generation and demand. Also, the overall power system is designed to work satisfactorily around a nominal frequency. Therefore, if the frequency deviates beyond a certain threshold from its nominal value, protection devices may be activated that disconnect generation units and loads, in order to drive the system back into its desired frequency range [1].

Current frequency control mechanisms are dictated by the dynamics of power generation plants interconnected to the system via rotating generators [2]. In particular, the rotational inertia of large generators, supported by directly interfaced motors, provides a natural fast-reacting energy storage that helps to balance sudden changes in load or generation [3]. Yet, opposed to conventional units, most renewable power sources and storage devices, such as batteries or flywheels, are interfaced to the power grid via power electronic devices, in particular AC inverters [1], [4]. Hence, replacing conventional synchronous generator (SG)-interfaced units by renewable inverter-interfaced units results in a reduced system inertia. Consequently, systems with a large number of inverter interfaced units are often termed *low-inertia power systems*.

Clearly, in low-inertia power systems, current frequency control strategies need to be revisited and adjusted to the new system characteristics [1], [3]. In particular, frequency control has to be supported by inverter-interfaced generation units [3]. However, many proposed solutions for bulk power systems still assume the existence of a common grid frequency to which the inverter can synchronise [3], [5]. Yet, this requires the presence of a sufficient number of grid-forming units in the network that provide this frequency. Hence, an underlying assumption of the approaches discussed, e.g., in [3], [5] is that—following the traditional paradigm—a sufficient number of conventional SG-interfaced power plants can be employed for this purpose. However, due to the increasing penetration of inverter-interfaced generation and storage units, not only *grid-supporting*, but also *grid-forming* capabilities have to be provided sooner than later by inverter-interfaced sources [6], [7].

The fact that grid-forming capabilities have to be pro-

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vided by inverter-interfaced units is already very common in microgrids (MGs). A MG is a locally controllable subset of a larger electrical network that gathers and coordinates several distributed generation (DG) units, storage devices and loads. Amongst the key drivers for MGs is the fact that most renewable power units are relatively small-sized in terms of their generation power and, therefore, often connected to the power system at medium and low voltage levels. By taking local control actions within the MG, the operational burden on the transmission system can be reduced. At the same time, grid resiliency can be increased, as the MG can ensure reliable power supply to local loads during faults in the main utility grid [8]. Due to these and other features, MGs have been identified as a promising approach to integrate large shares of renewable generation units and are foreseen to be essential components of future smart grids [8]–[11].

B. About the paper

The development of suitable models of grid-forming inverter-interfaced units is a fundamental prerequisite for the provision, design and analysis of practical frequency control schemes for such plants. Thus far, inverters operated in grid-forming mode are commonly represented as ideal AC voltage sources in MG analysis and control design [4], [6], [7], [12]–[16]. Though this may appear a reasonable assumption, it neglects the important fact that in most real-world applications each inverter is operated with its own processor. It is well-known that the clocks used to generate the time signals of the individual processors differ from each other due to clock drifts [17], [18]. Moreover, it has been argued in [12], [19], [20] that apart from sensor uncertainties, the presence of clock drifts is the main reason why inverters operated with fixed electrical frequency cannot operate in parallel—unless the network possesses a very accurate clock synchronisation system, which is rarely the case in practice [20].

Motivated by these claims, the present paper is devoted to the analytical and experimental investigation of clock drift effects on the parallel operation of multiple inverter-interfaced grid-forming units. To this end, at first we demonstrate experimentally on a MG in the megawatt (MW)-range that clock drifts may indeed impair frequency synchronisation in low-inertia networks and that the standard model of a grid-forming inverter as an ideal voltage source does not capture this behaviour. As a consequence of these observations, we derive an improved model of a grid-forming inverter with unknown constant clock drift. Thereby, we also extend the previous work [21] by providing an extensive experimental motivation and validation of the derived inverter model with inaccurate clock. As discussed above, the provision of practically feasible control concepts for inverters is essential for the operation of future power systems and, hence, a very active area of research [20], [22]. However, the successful achievement of this task heavily relies on the development of suitable inverter models that capture the plant's behaviour with sufficient accuracy, which is the topic addressed in the present paper.

We then provide an exemplary application of the derived model by analytically investigating the performance of the droop control laws proposed in [23] under explicit consideration of clock drifts. Our analysis focuses on characterising the electrical synchronisation frequency and quantifying the impact of clock drifts on the active power sharing accuracy. The droop control laws given in [23] are decentralised and derived heuristically under the assumption of a dominantly inductive network. For such scenario, they are (by far) the most commonly used ones. However, despite many positive features, the droop controls in [23] also have several drawbacks, such as load-dependent frequency and amplitude deviations or sensitivity to line impedance characteristics [20], [24], [25]. As a consequence of this, the development of alternative control schemes with improved performance is a timely and relevant research area [20], [22] and several modified droop controls or alternative control schemes for inverters have been proposed [26]–[28], including adaptive [29] and ultimate droop [25], as well as virtual synchronous machines [24], [30]. A key feature common to most of these strategies is their decentralised nature, obviating the need for communications or a common clock. We refer the reader to [20], [22], [31] for a comprehensive overview of such control strategies.

Both the model derivation as well as the subsequent analysis are validated via an extensive experimental case study in a real MG. The employed experimental setup consists of two grid-forming 500 kW inverters and one 1 MW grid-feeding inverter unit that is used to mimic load and renewable infeed. In accordance with the analysis in this paper, each inverter is operated with its own processor and their clocks are *not* synchronised. In addition to the power range, this also significantly distinguishes our experimental setup to the one used in [32], where all inverters are operated via a joint digital processor.

In summary, our main contributions are as follows.

- To demonstrate experimentally that the standard model of a grid-forming inverter as an ideal voltage source does not capture the phenomenon of clock drifts.
- As a consequence of the former, to derive and experimentally validate an improved model of a grid-forming inverter incorporating the clock drift phenomenon.
- By using the derived model, to investigate the effect of clock drifts on the parallel operation of multiple droop-controlled grid-forming inverters in the absence of a common clock.
- To provide an extensive experimental validation and demonstration of the analytic claims and the proposed model.

The remainder of the paper is structured as follows. In Section II, we review the standard model of a grid-forming inverter, outline its shortcomings with regards to the consideration of clock drifts and illustrate this discussion via experimental results. Motivated by these findings, we provide a model of a grid-forming inverter incorporating the phenomenon of clock drifts in Section III. The impact of clock drifts on the performance of multiple droop-controlled inverters is investigated in Section IV. The experimental validation is conducted in Section V. The paper is concluded with a summary and outlook in Section VI.

II. The effect of clock drifts in low-inertia power systems: problem statement and experimental illustration

This section further motivates the need for considering the effect of clock drifts in the parallel operation of multiple grid-forming inverters.

A. Model of grid-forming inverter as ideal voltage source

We consider a power system with $n \geq 2$ nodes and denote the set of network nodes by $\mathcal{N} := \{1, \dots, n\}$. For the purposes of the present paper and to ease presentation, we assume that all generation units are inverter-interfaced.

Under the (implicit) assumption of ideal clocks, the inverter-interfaced DG unit operated in grid-forming mode and connected at the i-th node, $i \in \mathcal{N}$, is typically modelled as an ideal AC voltage source, the frequency and amplitude of which can be specified by the designer[1] [6], [14], [33], i.e.,

$$\begin{aligned} \dot{\delta}_i &= \omega_i = u_i^{\delta}, \\ \tau_i \dot{P}_i^m &= -P_i^m + P_i, \\ V_i &= u_i^V, \\ \tau_i \dot{Q}_i^m &= -Q_i^m + Q_i, \end{aligned} \tag{II.1}$$

where $\delta_i \in \mathbb{R}$ is the phase angle of the voltage at the i-th node, $\omega_i \in \mathbb{R}$ its frequency, $V_i \in \mathbb{R}_{\geq 0}$ its amplitude and $u_i^{\delta} \in \mathbb{R}$ and $u_i^V \in \mathbb{R}_{\geq 0}$ are controls. Furthermore, it is usually assumed that the active and reactive power outputs $P_i \in \mathbb{R}$ and $Q_i \in \mathbb{R}$ are measured and passed through filters with time constant $\tau_i \in \mathbb{R}_{>0}$ [34]. The measured powers are denoted by $P_i^m \in \mathbb{R}$ and $Q_i^m \in \mathbb{R}$.

In the experimental setup, the active and reactive powers P_k and Q_k are calculated in real-time based on the *instantaneous* power theory for 3-phase 3-wire systems, see [33], [35]. This is implemented as follows. Denote the three-phase voltage and current at the k-th inverter, $k \in \{1, 2\}$, by $v_k^{abc} \in \mathbb{R}^3$, respectively $i_k^{abc} \in \mathbb{R}^3$. Furthermore, in the present case the inverters are connected to a 3-phase 3-wire system on the low voltage side of the transformers, see Section V for a detailed description of the experimental setup. Thus, the abc-voltage and -current can equivalently be represented in $\alpha\beta$-coordinates, i.e., $(v_k^{\alpha}, v_k^{\beta})^T$, $(i_k^{\alpha}, i_k^{\beta})^T$ [35]. Then, the instantaneous active and reactive power flows P_k, respectively Q_k, are given by [35]

$$\begin{aligned} P_k &= i_k^{\alpha} v_k^{\alpha} + i_k^{\beta} v_k^{\beta}, \\ Q_k &= i_k^{\alpha} v_k^{\beta} - i_k^{\beta} v_k^{\alpha}. \end{aligned} \tag{II.2}$$

For the analysis in Section IV, we make the standard assumption that the power lines of the network can be represented by algebraic equations (see [33]). Then, the active and reactive power flows for a balanced system are given by [2]

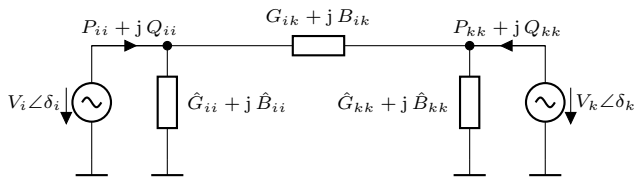

Fig. 1. Single line equivalent circuit for active and reactive power flow.

$$\begin{aligned} P_i &= G_{ii} V_i^2 - \sum_{\substack{k=1 \\ k \neq i}}^{n} \left(G_{ik} \cos(\delta_{ik}) + B_{ik} \sin(\delta_{ik}) \right) V_i V_k, \\ Q_i &= |B_{ii}| V_i^2 - \sum_{\substack{k=1 \\ k \neq i}}^{n} \left(G_{ik} \sin(\delta_{ik}) - B_{ik} \cos(\delta_{ik}) \right) V_i V_k, \end{aligned} \tag{II.3}$$

where $\delta_{ik} = \delta_i - \delta_k$, $G_{ik} \in \mathbb{R}_{\geq 0}$ is the conductance, $B_{ik} \in \mathbb{R}$ the susceptance between nodes i and k and

$$G_{ii} = \hat{G}_{ii} + \sum_{\substack{k=1 \\ k \neq i}}^{n} G_{ik}, \quad B_{ii} = \hat{B}_{ii} + \sum_{\substack{k=1 \\ k \neq i}}^{n} B_{ik},$$

where $\hat{G}_{ii} \in \mathbb{R}_{\geq 0}$ and $\hat{B}_{ii} \in \mathbb{R}$ denote the shunt conductance, respectively shunt susceptance, at the i-th node, representing, e.g., a load (see Fig. 1). Note that $G_{ik} = B_{ik} = 0$ if nodes i and k are not connected via a power line. In a synchronised state, the expressions (II.2) reduce to (II.3), see [33].

B. Problem statement

In a practical setup, the dynamics (II.1) together with the controllers generating the signals u_i^{δ} and u_i^V are implemented on a processor by means of numerical integration. After each integration step, the generated values of the angle δ_i and the voltage amplitude V_i are passed to the internal controllers of the inverter at the i-th node. These internal controls then ensure that the inverter provides the desired sinusoidal voltage at its terminals [12].

The sampling interval used to perform this numerical integration at each unit in the network stems from the internal clock of the processor of that same unit. Following standard terminology and to avoid confusions with the electrical frequency, we denote the frequency at which the processor is running by clock rate. Usually, the clock rate is determined by some sort of resonator, e.g., a crystal oscillator. Almost all resonators suffer from precision inaccuracies [17], [36]. As a consequence, the clocks of different units in the network are not synchronised per se. In particular, this implies that the numerical integration required to implement (II.1) is carried out with different time signals at the individual inverter control units in the network.

Unfortunately, this fact is not captured by the model (II.1). On the contrary, consider a generic MG and suppose (for simplicity) that only inverter-interfaced units are responsible for frequency control. Then the model (II.1) insinuates that frequency synchronisation can, e.g., be achieved by setting

$$u_i^{\delta} = \omega^d,$$

[1] A fundamental underlying assumption for the model (II.1) is that whenever the grid-forming inverter connects a fluctuating renewable generation source, e.g., a photovoltaic plant, to the network, it is equipped with some sort of storage (e.g. a battery). Thus, it can increase and decrease its power output within a certain range, see [33].

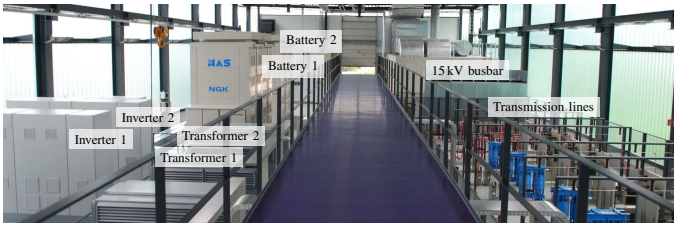

Fig. 2. Technology center of Younicos AG in Berlin with NaS Batteries, 500 kW inverters, transformers, transmission lines and 15 kV busbar.

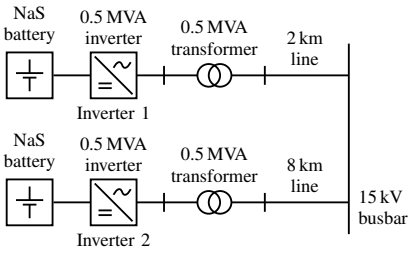

Fig. 3. Single line diagram of the employed test set-up.

where $\omega^d \in \mathbb{R}_{>0}$ is the desired synchronisation frequency. From (II.1), clearly then the $\delta_{ik}(t)$, are constant for all $t \geq 0$. However, the phenomenon of clock drifts detailed above does impair practical feasibility of such a control strategy, as demonstrated by the experimental results in the next section.

C. Experimental illustration

The impact of clock drifts on system performance in terms of frequency stability and frequency synchronisation is illustrated via experimental results. The experiments have been conducted in the real MW-range MG of Younicos AG in Berlin, Germany (see Fig. 2).

Two grid-forming inverters shown in Fig. 3 from the manufacturer IDT, Switzerland, with a nominal voltage of 600 V and power of 0.5 MVA have been used in the test (see also Fig. 2 left). On the DC side, each inverter is connected to a sodium sulfur (NaS) battery from NGK Insulators, LTD, Japan, with a nominal power of 0.5 MW, and a capacity of 3.6 MWh. The AC side of each inverter is controlled by a dSPACE® DS1005 and a DC5202 AC motor module. We remark that the dSPACE® controllers of the inverters are *not* connected via communication lines with each other and that their clocks are *not* synchronised. On the AC side, the inverters are connected via Y-Δ transformers to 15 kV transmission lines with lengths of 2 km and 8 km, respectively. These transmission lines are implemented by a π-equivalent circuit with real capacitors, inductances, and resistors (see Fig. 2, right). Both lines are connected to a 15 kV busbar.

In the experiment, at first inverter 1 is started with a desired fixed frequency of $u_1^\delta = 2\pi 50\,\frac{1}{\mathrm{s}}$ and voltage amplitude of $u_1^V = 600\,\mathrm{V}$ (RMS) as shown in Fig. 4. Recall that inverters don't exhibit a natural coupling between frequency and active power. Hence, for the mere purpose of frequency control a constant value of $u_1^\delta = 2\pi 50\,\frac{1}{\mathrm{s}}$ can be directly applied to the system (II.1) in a feed-forward manner without the need for additional (feedback) controllers. After the grid is energised, inverter 2 is synchronised to the network. The employed synchronisation module is similar to the standard modules used with conventional SGs (see [37]). That is, the synchronisation module measures the frequency and voltage amplitude of the AC waveform at the low voltage side of the transformer (i.e., the point of connection to the grid) and then adjusts the setpoints ω_i^d and V_i^d for the frequency, respectively the voltage magnitude, in order to minimise the error between both AC waveforms. Once the error is below a certain threshold, the switch of inverter 2 is closed. This happens at time $t = 2\,\mathrm{s}$. As can be seen in Fig. 4, the frequency measured by an "imc NEMO I" device at the 15 kV busbar remains within the limits of $50\,\mathrm{Hz} \pm 1\,\%$ determined by the industrial standard DIN EN 50160 [38] during this period. Also, the active power flows between both units are (almost) zero and constant.

At time $t = 10\,\mathrm{s}$, the synchronisation module of inverter 2 is disabled and the frequency of both inverters is set to $u_1^\delta = u_2^\delta = 2\pi 50\,\frac{1}{\mathrm{s}}$, see the upper plot in Fig. 4. That plot also shows that the electrical frequency measured at the 15 kV busbar does not coincide with $u_1^\delta = u_2^\delta = 2\pi 50\,\frac{1}{\mathrm{s}}$. It can be seen in Fig. 4 that the instantaneous active power measurements P_1^m and P_2^m start to diverge in opposite directions as the synchronization module is disabled. As the voltage amplitudes remain constant, this divergence must originate from a continuously growing angle difference $|\delta_{12}|$, see also (II.3). Furthermore, as $u_1^\delta = u_2^\delta = 2\pi 50\,\frac{1}{\mathrm{s}}$, the only explanation of the observed continuous growth of $|\delta_{12}|$ are the drifts of the internal clocks of the dSPACE® units. The power values continue to grow until they reach the nominal power of the inverters at time $t = 89\,\mathrm{s}$, where inverter 2 is turned off to prevent damage of the units. We remark that the elapsed time between a perfectly synchronised network state and the generator outage amounts

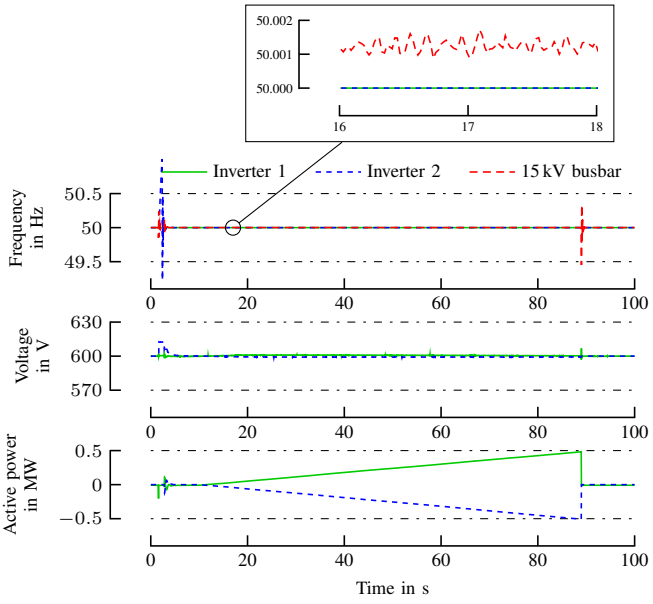

Fig. 4. Inverters running in parallel without droop control at a fixed and equal frequency input $u_1^\delta = u_2^\delta = \omega^d$.

merely to $80\,\mathrm{s}$ (see Fig. 4).

Clearly, the experiment demonstrates that the model (II.1) does lead to wrong predictions of the behaviour of a practical low-inertia power system with parallel grid-forming inverters. Consequently, the phenomenon of clock drifts has to be taken into account when modelling such units.

In addition, the experiment confirms the observation made in [12], [19], [20] that, if several inverters in parallel are to be operated with a constant uniform frequency control signal $u_i^\delta = \omega^d$, $i = 1, \dots, n$, a clock synchronisation mechanism is required in order to maintain constant angle differences. See [20] for a discussion on possible solutions for this.

III. Model of an inverter with inaccurate clock

We now derive a model that adds the effect of an inaccurate processor clock to (II.1). For an illustration of the influence of clock inaccuracy on the numerical integration of (II.1), consider the well-known Euler method, e.g., [39] as an exemplary numerical integration method[2]. Let $x \in \mathbb{R}^n$, $f : \mathbb{R} \times \mathbb{R}^n \to \mathbb{R}^n$ and consider the ordinary differential equation

$$\dot{x}(t) = f(x(t)), \quad x(t_0) = x_0.$$

Fix an initial time $t_0 \in \mathbb{R}$ and an integration step size $h \in \mathbb{R}_{>0}$. Let $k \in \mathbb{N}$ be the k-th integration step. Then

$$t(k) = t_0 + kh \tag{III.1}$$

and the integration step of the Euler method from $t(k)$ to $t(k+1) = t(k) + h$ is given by [39]

$$x(t(k+1)) = x(t(k)) + hf(x(t(k))). \tag{III.2}$$

Recall that at each inverter the integration (III.2) is carried out using the time signal provided by the local clock. As outlined in Section II, almost all real clocks exhibit a certain (though often small) inaccuracy. In data-sheets, this clock drift is usually specified relative to the nominal clock rate [36]. To see how such a clock drift affects the time signal provided by a processor clock, denote an exemplary nominal clock rate by $f_c \in \mathbb{R}_{>0}$ and its relative drift by $\mu \in \mathbb{R}$. Typically, $|\mu| \leq 10^{-5}$ [36]. Then, the actual clock cycle $\Delta t_c \in \mathbb{R}_{>0}$ with respect to the nominal clock cycle without drifts $\Delta \bar{t}_c = {}^1/_{f_c}$ of the processor is

$$\Delta t_c = \frac{1}{f_c(1+\mu)} = \frac{1}{1+\mu}\Delta \bar{t}_c. \tag{III.3}$$

Note that both the step size h in (III.1) and the time signal provided by the processor (given, e.g., by (III.1)) are multiples of the clock cycle Δt_c in (III.3). For the subsequent model derivation, it is convenient to introduce a *virtual* global network time which we denote by $t \in \mathbb{R}$ with initial time $t_0 \in \mathbb{R}$, as well as a step size $h \in \mathbb{R}_{>0}$ in *virtual* global time. We emphasize that this global time is a *virtual* quantity used in the model derivation and does *not* imply the existence of a common clock that is accessible by all inverters. Furthermore, we denote by $t_i \in \mathbb{R}$ the local time of the clock of the i-th inverter, by $t_{i_0} \in \mathbb{R}$ its initial time and by $h_i \in \mathbb{R}_{>0}$ its step size, as well as the relative drift of the clock of the i-th inverter by $\mu_i \in \mathbb{R}$. Due to the good short-term accuracy of many resonators (see Section II), we assume in the following that μ_i is an unknown constant parameter satisfying $|\mu_i| \ll 1$. Furthermore, we account for a possible constant local clock offset $\bar{\zeta}_i \in \mathbb{R}$. Without loss of generality, it is convenient to write $\bar{\zeta}_i$ as $\bar{\zeta}_i = t_0/(1+\mu_i) + \zeta_i$, $\zeta_i \in \mathbb{R}$. Hence, with (III.3), t_{i_0} and h_i can be expressed as

$$t_{i_0} = t_0 + \bar{\zeta}_i = t_0\Big(\frac{1}{1+\mu_i}\Big) + \zeta_i, \quad h_i = h\Big(\frac{1}{1+\mu_i}\Big).$$

Then

$$t_i(k) = t_{i_0} + kh_i = t(k)\Big(\frac{1}{1+\mu_i}\Big) + \zeta_i,$$

with $t(k)$ given in (III.1). It follows that, for sufficiently fast sampling times, the clock drift of the processor of the i-th inverter can formally be included in the continuous-time model (II.1) by an appropriate time-scaling, i.e.,

$$t_i = \Big(\frac{1}{1+\mu_i}\Big)t + \zeta_i. \tag{III.4}$$

Note that the clock model (III.4) is identical to that used to investigate clock synchronisation, e.g., in [18]. Furthermore,

$$\frac{d(\cdot)}{dt_i} = (1+\mu_i)\frac{d(\cdot)}{dt}. \tag{III.5}$$

Suppose the time derivatives in (II.1) are expressed with respect to the local time t_i of the i-th inverter. Inserting (III.5) in (II.1) yields

$$\begin{aligned} (1+\mu_i)\dot{\delta}_i &= (1+\mu_i)\omega_i = u_i^\delta, \\ (1+\mu_i)\tau_i \dot{P}_i^m &= -P_i^m + P_i, \\ V_i &= u_i^V, \\ (1+\mu_i)\tau_i \dot{Q}_i^m &= -Q_i^m + Q_i, \end{aligned} \tag{III.6}$$

where the time derivatives are now expressed with respect to the nominal time t. Furthermore, without loss of generality, the local clock offset ζ_i can be included in the initial conditions of the system (III.6).

We note that it follows from the discussion in Section II-B that usually the clock drifts μ_i of different inverter-interfaced units in the network also differ from each other, i.e., $\mu_i \neq \mu_k$, $i \in \mathcal{N}$, $k \in \mathcal{N}$, $i \neq k$. Hence, by using the model (III.6) instead of (II.1) it is straight-forward to see that setting

$$u_i^\delta = u_k^\delta = \omega^d$$

leads to growing phase angle differences over time. More precisely, from (III.6) we have that

$$\delta_i(t) - \delta_i(0) = \int_0^t \dot{\delta}_i d\tau = \int_0^t \tfrac{1}{1+\mu_i}\omega^d d\tau = \tfrac{1}{1+\mu_i}\omega^d t \tag{III.7}$$

and, hence, the absolute phase angle difference between nodes i and k is given by

$$|\delta_{ik}(t)| = \left|\delta_{ik}(0) + \left(\tfrac{1}{1+\mu_i} - \tfrac{1}{1+\mu_k}\right)\omega^d t\right|, \tag{III.8}$$

which clearly tends to infinity for $t \to \infty$ and $\mu_i \neq \mu_k$. Consequently, by recalling the power flow equations (II.3), we conclude that, unlike the standard model (II.1), employing

[2]Our analysis and model derivation apply equivalently to other numerical integration methods, at the cost of a more complex notation.

the model (III.6) permits to draw the correct conclusion that several grid-forming inverters operated in parallel with constant uniform frequency control signals exhibit large power flows. This observation is in accordance with the experimental results in Section II-C and demonstrates the practical validity of the model (III.6) compared to the the standard model (II.1), which neglects the effect of clock drifts.

Based on the above derivations, the difference in the relative clock drifts of inverter 1 and inverter 2 in our experimental setup in Section II-C have been computed. With the power flows (II.3), the grid impedances, and the measurements in Fig. 4, the relative clock drift between the inverters amounts to $0.0028\,\frac{\text{rad}}{\text{s}}$. In terms of (III.3) this can be expressed as an inaccuracy of $|\mu_1 - \mu_2| = 9.0996 \cdot 10^{-6}$.

IV. Impact of clock drifts on the performance of droop-controlled MGs

In addition to sensitivity with respect to clock drifts, the operation of parallel grid-forming inverters with fixed constant frequencies (and voltage amplitudes) exhibits two further main disadvantages. First, the network operator looses all controllability over the current and power flows in the network (unless the internal clocks are synchronised by an additional signal [20]). Hence, the control objective of power sharing can, in general, not be achieved. Second, such an operation may lead to very high uncontrolled current flows in the network.

A widely-employed control scheme to address both aforementioned problems is droop control, e.g., [20], [23]. There exists a large variety of control schemes for inverters named droop control. Amongst those, the most commonly employed frequency and voltage droop controls are [20]

$$\begin{aligned} u_i^\delta &= \omega^d - k_{P_i}(P_i^m - P_i^d), \\ u_i^V &= V_i^d - k_{Q_i}(Q_i^m - Q_i^d), \end{aligned} \tag{IV.1}$$

where $k_{P_i} \in \mathbb{R}_{>0}$ and $k_{Q_i} \in \mathbb{R}_{>0}$ are the droop gains, $\omega^d \in \mathbb{R}_{>0}$ and $V_i^d \in \mathbb{R}_>$ setpoints for frequency and voltage amplitude and $P_i^d \in \mathbb{R}$ and $Q_i^d \in \mathbb{R}$ the reference setpoint for the active and reactive power. For an in-depth discussion and motivation of the control (IV.1) see [13], [14], [23].

Combining (III.6) with (IV.1) yields the closed-loop model of the inverter at the i-th node

$$\begin{aligned} (1+\mu_i)\dot{\delta}_i &= (1+\mu_i)\omega_i \\ &= \omega^d - k_{P_i}(P_i^m - P_i^d), \\ (1+\mu_i)\tau_i \dot{P}_i^m &= -P_i^m + P_i, \\ V_i &= V_i^d - k_{Q_i}(Q_i^m - Q_i^d), \\ (1+\mu_i)\tau_i \dot{Q}_i^m &= -Q_i^m + Q_i. \end{aligned} \tag{IV.2}$$

In the following, we use the model (IV.2) to analyse the effect of clock drifts on the performance of parallel droop-controlled inverters. This analysis is carried out for the example of a MG. More precisely, we consider an inverter-based droop-controlled MG formed by n inverters modelled by (IV.2) with power flows given by (II.3). Compared to previous work on analysis of droop-controlled MGs, e.g., [13], [15], we explicitly consider the effect of clock drifts in the analysis. In particular, we characterise the electrical synchronisation frequency and investigate the impact on the active power sharing accuracy under droop control[3].

For the analysis, it is convenient to introduce the *internal* frequencies of the inverters

$$\bar{\omega}_i := (1+\mu_i)\omega_i, \quad i \in \mathcal{N}. \tag{IV.3}$$

The qualifier *internal* is motivated by the fact that the signal $\bar{\omega}_i$ is the *internal* frequency control signal generated by the processor of the i-th unit. We employ this notation to distinguish the internal control signal $\bar{\omega}_i$ from the actual electrical frequency ω_i. Clearly, in the case of ideal clocks, i.e., $\mu_i = 0$, the internal and the electrical frequencies are identical, i.e., $\bar{\omega}_i = \omega_i$.

For the analysis in this section, we assume that the system (IV.2), (II.3), $i \in \mathcal{N}$, possesses a synchronised motion, i.e., a synchronised operating point,

$$\text{col}(\delta_i^s, P_i^{m,s}, V_i^s, Q_i^{m,s}),\ i \in \mathcal{N}, \tag{IV.4}$$

where $P_i^{m,s}$, $Q_i^{m,s}$ and V_i^s, V_k^s as well as all $\delta_i^s - \delta_k^s$ are constant for all pairs (i,k) for $i \in \mathcal{N}$, $k \in \mathcal{N}$, $i \neq k$ and all $t \geq 0$.

A. Synchronisation frequency in droop-controlled MGs under consideration of clock drifts

Along any synchronised motion, it is possible to further characterise the *internal* frequencies $\bar{\omega}^s = \text{col}(\bar{\omega}_i^s) \in \mathbb{R}^n$, as well as the electrical synchronisation frequencies $\omega^s = \text{col}(\omega_i^s) \in \mathbb{R}^{n_g}$ as follows. For the presentation of the result it is convenient to introduce the synchronised active power network losses due to line and shunt conductances given by

$$P_{\text{loss}} = \sum_{i=1}^{n} \Big(G_{ii}(V_i^s)^2 - \sum_{\substack{k=1 \\ k\neq i}}^{n} G_{ik} V_i^s V_k^s \cos(\delta_{ik}^s) \Big). \tag{IV.5}$$

The proof of the lemma below is given in Appendix A.

Lemma 4.1: The vector of internal frequencies $\bar{\omega}^s$ of any synchronised motion (IV.4) of the system (IV.2), (II.3), $i \in \mathcal{N}$, is given by

$$\bar{\omega}^s = \big(I_n + \text{diag}(\mu_i)\big)\underline{1}_n \omega^N, \tag{IV.6}$$

where $\underline{1}_n$ is the vector with all ones and the real constant ω^N is given by

$$\omega^N = \Big(\omega^d \sum_{i=1}^{n} \tfrac{1}{k_{P_i}} - P_{\text{loss}} + \sum_{i=1}^{n} P_i^d\Big)\Big(\sum_{i=1}^{n} \tfrac{1+\mu_i}{k_{P_i}}\Big)^{-1}. \tag{IV.7}$$

Here, ω^N denotes the *electrical* synchronisation frequency of the MG, which, of course, is identical at all nodes in the network. Furthermore, for $\mu_i = 0$, $i \in \mathcal{N}$, i.e., for ideal clocks, all internal frequencies $\bar{\omega}_i^s$ become identical to the electrical frequency ω^N and (IV.7) reduces to the usual expression of the synchronisation frequency in a MG, see [15]. Thus, under the presence of clock drifts, the *internal* synchronised frequencies of the inverters are scaled with respect to the

[3]We merely focus on purely inverter-based networks to simplify notation and exposition. The analysis and interpretation of the effect of clock drifts on network performance is extendable in a straight-forward manner to networks with mixed generation pool but at the cost of a more involved notation, see [14].

electrical synchronisation frequency ω^N by $1/(1+\mu_i)$ for $i \in \mathcal{N}$. It can be seen from (IV.7) that, as in conventional power systems and also in the presence of clock drifts, the synchronisation frequency is an indicator for the active power balance in the network.

Remark 4.2: See [21] for a proof that stability of *lossless* (i.e. $G_{ik} = 0$ for all pairs (i,k) for $i,k \in \mathcal{N}$ and $i \neq k$) droop-controlled inverter-based MGs is robust to constant unknown clock drifts.

B. Power sharing in droop-controlled MGs under consideration of clock drifts

This section is dedicated to the analysis of the performance of the frequency droop control (IV.1) with regard to active power sharing under the consideration of clock drifts. Recall that power sharing is an important performance criterion in the operation of power systems. For our analysis, we employ the following definition of power sharing.

Definition 4.3: Let $\chi_i \in \mathbb{R}_{>0}$ denote weighting factors and P_i^s the steady-state active power flow, $i \in \mathcal{N}$. Then, two inverters at nodes i and k are said to share their active powers proportionally according to χ_i and χ_k, if $P_i^s/\chi_i = P_k^s/\chi_k$.

For droop-controlled inverters with ideal clocks, it has been shown in [13], [15] that the objective of active power sharing is achieved along a synchronised motion if the parameters of the frequency droop controllers are chosen such that

$$k_{P_i}\chi_i = k_{P_k}\chi_k \text{ and } k_{P_i}P_i^d = k_{P_k}P_k^d. \tag{IV.8}$$

The result below quantifies the largest ratio of weighted power outputs P_i^s/χ_i introduced by the clock drifts μ_i if the parameters k_{P_i} and P_i^d are chosen according to (IV.8). We restrict the statement to units with positive active power outputs, but the statement for negative active power outputs follows accordingly. The proof of the lemma is given in [21].

Lemma 4.4: Consider the system (IV.2), (II.3), $i \in \mathcal{N}$. Let $\hat{n} \subseteq \mathcal{N}$. Fix χ_i and select the parameters k_{P_i} and P_i^d according to (IV.8), $i \in \hat{n}$. Then the largest ratio of weighted power outputs P_i^s/χ_i, $i \in \hat{n}$, satisfying $\text{sign}(P_i^s) = \text{sign}(P_k^s) = 1$, is given by

$$\frac{\max_{i\in\hat{n}}\left(P_i^s/\chi_i\right)}{\min_{k\in\hat{n}}\left(P_k^s/\chi_k\right)} = \frac{-\min_{i\in\hat{n}}(\mu_i)\omega^N + c}{-\max_{k\in\hat{n}}(\mu_k)\omega^N + c} \tag{IV.9}$$

with $c = k_{P_i}P_i^d + \omega^d - \omega^N$, $i \in \hat{n}$ and ω^N defined in (IV.7).

Condition (IV.9) reveals that the presence of unknown clock drifts has a deteriorating effect on the active power sharing accuracy. Yet, since in general $|\mu_i| \ll 1$, (IV.9) also shows that the introduced error in power sharing is negligible in most practical scenarios. Therefore, the selection criterion (IV.8) still seems appropriate in the presence of clock drifts. This observation is confirmed experimentally in the next section.

V. Experimental validation

We provide experimental results obtained in the real MW-range MG of Younicos AG in Berlin (see Fig. 2), Germany. These validate the analysis of Section IV. To perform the tests, the setup in Fig. 3 from Section II-C, consisting of two grid-forming inverters, is extended by a 4 km line that connects

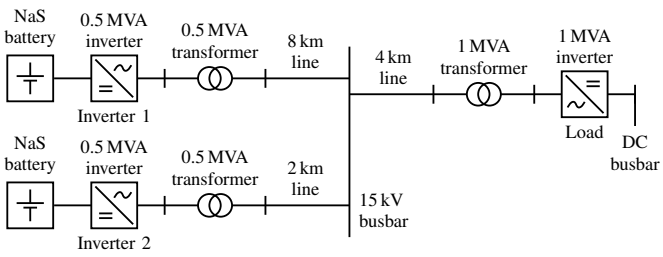

Fig. 5. Single line diagram of the employed test set-up.

a 1 MW grid-feeding inverter to the MG, see Fig. 5. The qualifier "grid-feeding" means that the additional third inverter is controlled in such a way that it consumes or delivers a prespecified amount of active and reactive power [12], [33]. Furthermore, this inverter is synchronised to the grid via a phase lock loop, see [40]. Even though, the inverter is denoted as a load in Fig. 5, it can also act as a source providing power to the grid. More precisely, the power that this inverter provides or consumes can be set between -1 MW and 1 MW and is provided on the DC side by a 1 kV busbar. A 1 MVA transformer connects the grid-feeding inverter to the 15 kV transmission line. The frequency at the medium voltage busbar is again measured with an "imc NEMO I" device.

Compared to Section II-C, now both grid-forming inverters are operated with the droop control laws given in (IV.1). As in Section II-C, the power for each grid-forming inverter is provided by NaS batteries. On the AC side, the inverters are still connected to the 15 kV busbar by transformers as well as 2 km, and 8 km lines, respectively.

With the outlined system configuration, we have performed a large variety of tests with different load conditions, droop gains and power setpoints to validate the analysis of Section IV. A representative scenario is described in detail in the following. The employed parameters for the filter time constants τ_1, τ_2 in (II.1), integration step size h in (III.1), and droop control in (IV.2) of the chosen scenario are given in Table I. The Euler method as described in (III.2) has been used to implement the integration. For both grid-forming inverters, we have chosen $P_1^d = P_2^d = 0\,\text{kW}$. This implies that for $P_1^m = P_2^m = 0\,\text{kW}$, we have that $u_1^\delta = u_2^\delta = \omega^d = 2\pi 50\frac{1}{\text{s}}$, i.e., the inverters operate at nominal frequency at no load, see (IV.1). The experimental results are displayed in Fig. 6.

At the beginning of the experiment both grid-forming units (inverter 1 and inverter 2 in Fig. 5) are synchronised and running in parallel at no load. This can be seen from Fig. 6, as the active power injections of both grid-forming units are zero. At time $t = 5\,\text{s}$, the grid-feeding inverter is started with a

TABLE I
TEST PARAMETERS FOR THE GRID-FORMING INVERTERS

Parameter	Value	Parameter	Value
h	166.67 ms	τ_1, τ_2	0.2 s
ω^d	$2\pi 50\,\frac{1}{\text{s}}$	V_1^d, V_2^d	600 V
k_{P_1}, k_{P_2}	$0.5\,\frac{\text{Hz}}{\text{MW}}$	k_{Q_1}, k_{Q_2}	$33.3\,\frac{\text{V}}{\text{MVAr}}$
P_1^d, P_2^d	0 kW	Q_1^d, Q_2^d	0 kVAr

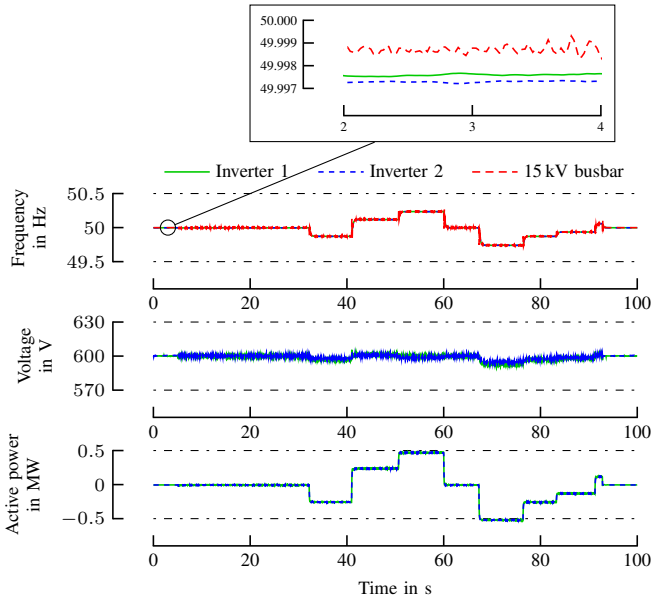

Fig. 6. Experimental results demonstrating that droop control mitigates the effect of clock drifts and can achieve a uniform electrical frequency in a low-inertia power system, while ensuring a desired active power sharing. The displayed frequencies of inverter 1 and 2 are their respective internal frequencies $\bar{\omega}_1 = 2\pi\bar{f}_1$ and $\bar{\omega}_2 = 2\pi\bar{f}_2$.

power setpoint of 0 MW. Due to the hysteresis current control of this unit, the waveform of the voltage amplitudes of the grid-forming inverters show some additive noise. From time $t = 32\,\mathrm{s}$ to $t = 93\,\mathrm{s}$, several changes of power setpoints within the specification of the grid-feeding inverter are performed (see Fig. 6). Thereby, the grid-feeding inverter operates either as a load (then $P_1 > 0, P_2 > 0$) or as a generator (then $P_1 < 0, P_2 < 0$). The internal frequencies of the inverters and also the electrical frequency measured at the 15 kV busbar change with the power consumed or supplied by the grid-feeding inverter. This is a direct consequence of the frequency droop control (IV.1) and also in accordance with the results in Section IV. Due to the choice of $k_{P_1} = k_{P_2} = 0.5\,\frac{\mathrm{Hz}}{\mathrm{MW}}$, the electrical network frequency, measured at the 15 kV busbar, changes from approximately 50.25 Hz, when the batteries are being charged, to 49.75 Hz, when the batteries are being discharged. Hence, the electrical network frequency remains within the limits defined in standard DIN EN 50160 [38].

Furthermore, the frequency plot in Fig. 6 shows that the internal frequencies of the inverters $\bar{\omega}_1 = 2\pi\bar{f}_1$, and $\bar{\omega}_2 = 2\pi\bar{f}_2$, see (IV.3), differ from each other in a synchronised state. Yet, they are close to each other. This validates Lemma 4.1, which states that the internal synchronised frequencies $\bar{\omega}_1^s$ and $\bar{\omega}_2^s$ are scaled by a factor $1/(1+\mu_i)$ with respect to the electrical synchronisation frequency ω^N and where μ_i denotes the relative clock drift.

With regard to active power sharing, we observe that, as $k_{P_1} = k_{P_2}$, both grid-forming inverters share the power demand, respectively injection, by the grid-feeding inverter equally. Hence, the experiment also validates the analysis in Section IV-B by showing that clock drifts have a negligible impact on the active power sharing accuracy. Finally, the voltage droop control (IV.1) modifies the voltage amplitudes of the grid-forming inverters, whenever there is a change in reactive power of the grid-feeding inverter. In summary, the experiments also confirm the result in Section IV that droop control mitigates the effect of clock drifts and achieves a synchronised electrical frequency in the network.

VI. Conclusion

It has been demonstrated via experimental results of a MG in the MW-range that—if not taken appropriately into account—clock drifts can have drastic impacts on the performance of low-inertia power systems including large power flows and even outages of generation units caused by triggering of protection devices. Hence, in the absence of a common clock or a highly accurate clock synchronisation mechanism—both of which are unlikely to be present in real-world power applications—the phenomenon of clock drifts deserves special attention in the control design and analysis of grid-forming inverters to ensure the practicality of any control or operation scheme. However, our experiments show that the standard model representing a grid-forming inverter as an ideal controllable voltage source does *not* capture the influence of clock drifts and, hence, is *not* a practically valid model.

Motivated by these observations, we have derived and experimentally validated a suitably modified inverter model incorporating clock drifts. By using this model, we have shown that, due to clock drifts, the *internal* frequency control signals generated by the digital controls used to operate the inverters differ from the *electrical* frequency of the AC waveform provided by the inverters at their terminals.

Furthermore, by means of the improved inverter model we have given explicit expressions for the *electrical* frequency, as well as for the *internal* synchronisation frequencies of the inverters in a droop-controlled microgrid. Our analysis also reveals that the power sharing performance under droop control is deteriorated by clock drifts. Yet, these effects are minor and, as our experiments demonstrate, negligible in practice. Hence, our analysis and experiments demonstrate that the well-known droop control represents a useful decentralised control strategy to compensate the effects of clock drifts and to achieve a synchronous *electrical* frequency in the network.

Future work will address the analysis, both analytical and experimental, of the effect of clock drifts on secondary frequency control schemes and the design of alternative primary and secondary control schemes for low-inertia power systems. Furthermore, we plan to extend the experimental investigations to different controller settings, as well as load configurations.

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APPENDIX

A. Proof of Lemma 4.1

To prove Lemma 4.1, we recall that a synchronised motion of the system (IV.2), (II.3), $i \in \mathcal{N}$, is characterised by constant voltage amplitudes V_i^s, as well as constant angle differences δ_{ik}^s for all $t \geq 0$. Hence, $\dot{\delta}_{ik}^s = 0,\ \forall t \geq 0$, which implies that $\omega_i^s = \omega_k^s =: \omega^N$. Moreover, it follows from (IV.2) that $P_i^{m,s} = P_i^s$, and, thus with (IV.3),

$$\bar{\omega}_i^s = (1+\mu_i)\omega^N = \omega^d - k_{P_i}(P_i^s - P_i^d),$$

which by using (II.3), summing over all $\bar{\omega}_i^s$ and rearranging terms yields (IV.7).

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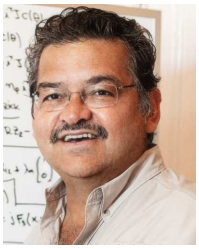

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