Impact of Quantum Confinement on Transport and the Electrostatic Driven Performance of Silicon Nanowire Transistors at the Scaling Limit

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***Abstract*—In this work we investigate the impact of quantum mechanical effects on the device performance of n-type silicon nanowire transistors (NWT) for possible future CMOS applications at the scaling limit. For the purpose of this paper, we created Si NWTs with two channel crystallographic orientations <110> and <100> and six different cross-section profiles. In the first part, we study the impact of quantum corrections on the gate capacitance and mobile charge in the channel. The mobile charge to gate capacitance ratio, which is an indicator of the intrinsic performance of the NWTs, is also investigated. The influence of the rotating of the NWTs cross-sectional geometry by 90º on charge distribution in the channel is also studied. We compare the correlation between the charge profile in the channel and cross-sectional dimension for circular transistor with four different cross-sections diameters: 5nm, 6nm, 7nm and 8nm. In the second part of this paper, we expand the computational study by including different gate lengths for some of the Si NWTs. As a result, we establish a correlation between the mobile charge distribution in the channel and the gate capacitance, drain-induced barrier lowering (DIBL) and the subthreshold slope (SS). All calculations are based on a quantum mechanical description of the mobile charge distribution in the channel. This description is based on the solution of the Schrödinger equation in NWT cross sections along the current path, which is mandatory for nanowires with such ultra-scale dimensions.**

***Index Terms*— CMOS, electrostatics, nanowire transistors, performance, quantum effects, TCAD.**

I. INTRODUCTION

The gate-all-around (GAA) silicon nanowire transistors (NWT) have the potential to extend Moore's law beyond the 7nm mark [1-3]. One of the major reasons being that the GAA design provides the best electrostatic integrity in comparison to all other transistors architectures and therefore the best gate control over the channel [4-7]. However, in such ultra-scaled GAA NWT, the quantum mechanical effects play a significant role and they must be considered in order to obtain accurate device performance results [8-10]. For example, the quantum confinement effects lead to quantum threshold voltage shifts, simultaneously reducing the gate-to-channel capacitance and the available charge for transport in the channel [11-13]. The reduced gate-to-channel capacitance also has a negative effect on the electrostatic integrity. The impact of the above effects increases with the reduction of the characteristic confined dimensions and therefore it will play a critical role in simulation-based research and design of NWT-based CMOS technology at the scaling limits.

Moreover, the improvement in electrostatics can lead to much shorter effective channel length which can increase the density of integration. Also, in conventional transistors minimising the interaction between the source and drain is critical for the improvement of the short-channel effects. The short channel-effects can be characterized by the drain-induced barrier lowering (DIBL), sub-threshold (SS) slope and the threshold voltage roll-off [14-16]. These effects create technical and scientific challenges, which can be tackled by a careful device design consideration [2, 17].

Overall, in this paper, taking into account the quantum confinement effects, we provide a comprehensive overview of the performance of numerous GAA NWTs as a function of cross-section shape and area, channel length, crystallographic orientation and different gate materials. The ultimate goal is to establish the strengths and weaknesses of such devices and determine the best design configuration and parameters for a specific application.

The next section describes the template transistors, where the methodology is revealed in Section III. The major results and analysis on the impact of quantum confinement on gate capacitance, charge and short channel effects are presented in Sections IV and V. Section V concludes the paper.

II. SIMULATED NANOWIRE TRANSISTOR

The simulated NWTs considered in this subsection of the paper have four different cross-sections: cylindrical, elliptical, square and rectangular, which are schematically presented in Fig. 1. The elliptical and rectangular NWTs have two different heights and widths of the wires but more importantly all devices have an identical cross-section area of 4π nm^2. The precise cross-sectional dimensions for all six wires are shown in Table 1. Two channel crystallographic orientations on (001) wafer are considered: <110> and <100>. Table 2 reveals the

design parameters for all devices. All NWTs simulated in this paper have effective oxide thickness of 0.8nm, gate length between 6-14 nm, spacer thickness of 5nm, source/drain doping peak of $2x10^{20}$ cm^{-3} and channel doping of 10^{15} cm^{-3}.

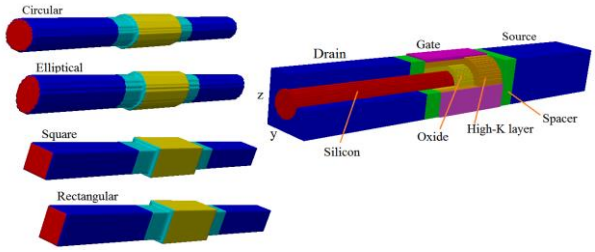

Fig. 1 3D schematic view of the circular NWT (right) and different cross-sectional shapes (left).

	Y(nm)	Z(nm)	Y/Z	Area (nm^2)
Circular	4	4	1	4π
Elliptical 1	3.45	4.64	0.74	4π
Elliptical 2	3.34	4.8	0.69	4π
Square	3.54	3.54	1	4π
Rectangular 1	3.06	4.13	0.74	4π
Rectangular 2	2.95	4.25	0.69	4π

Table 1 Physical dimensions of simulated devices.

T_{oxide} (nm)	0.8
Gate length (nm)	6-14
Spacer thickness (nm)	5.0
S/D peak doping (cm^{-3})	$2\text{-}10^{20}$
Channel doping (cm^{-3})	10^{15}
Substrate orientation	001
Nanowire orientation	<110> & <100>

Table 2 Parameters of the simulated devices

III. Simulation Methodology

The simulations in this work are based on the Poisson-Schrödinger (PS) quantum correction technology achieved in the drift-diffusion (DD) model 'atomistic simulator' GARAND [18]. The PS approach is coupled with the DD solution in stages to allow a computationally efficient manner of combining the impact of quantum confinement and carrier transport. To achieve this the DD simulation is carried out until convergence, then the quasi-Fermi level from the converged DD solution is used as a fixed reference within the Poisson-Schrödinger model to transfer the current transport behaviour. The PS solution is than iterated until convergence to obtain a quantum mechanical (QM) solution of the charge density.

Next the QM charge density from the Poisson-Schrödinger solution is used to obtain a fixed 'quantum correction' term. The GARAND DD loop is carried out again, using the 'quantum correction', until convergence is obtained. More specifically in our case the quantum corrections in the DD modules are introduced by solving the 2D Schrödinger equation. The 2D solutions of the Schrödinger equation are obtained in each cross-section along the gate length of the simulated transistor. The 2D Schrödinger equation is solved in an effective mass approximation [19-25]. The charge distribution obtained from the solutions of the 2D Schrödinger equation is used to calibrate the effective quantum-corrected potential in DD module.

In the inner PS loop the 2D charge distribution for each cross-section solution is combined to constitute the 3D solution of the charge density of the device. This 3D charge density is then used in the Poisson solver to obtain the updated potential. The updated potential is used as a driving potential in the solution of the current-continuity equation, keeping the charge distribution in the NWT cross-section identical to the charge distribution obtained from the solution of the Schrödinger equation. The simulations are finished when the current converges. The Hamiltonian used in the discretization of the Schrödinger equation is the effective-mass Hamiltonian that folds the full crystal interaction into the electron effective masses. The effective masses correspond to their bulk values for (100) and (110) crystal orientation in Si. As a caveat, the effective masses do not scale with the device sizes in our simulations. This may be an issue for severe confinement regimes, as shown in [26], and deserve further investigations by means of first-principles simulations. In this work, the following three carrier mobility models have been used; Masetti concentration dependent mobility model, The Lombardi perpendicular field dependent model, and Caughey-Thomas, field dependent mobility model.

Moreover, we would like point out that the investigation of the tunnelling effects in such ultra-scaled nanowire transistors is beyond the scope of this work. Our main area of interest is the charge distribution profile in the cross section of the circular, elliptical, square and rectangular nanowires. For this reason, we believe that the calibrated density gradient effective masses in the cross section are scientifically justified and robust.

IV. Nanowire's Gate Capacitance and Charge

A. Simulated nanowire transistors with an identical cross-section area

Based on the methodology described in Section II we are able to obtain device characteristics, such as charge carrier distribution in the 3D volume of the device. For example, the 2D charge distribution (cut perpendicular to the channel transport direction) for all NWTs discussed in this subsection is presented in Fig. 2. From the figure it is clear that the quantum simulations capture the well-known volume inversion effects [21].

More importantly, Fig. 2 reveal the fact that the 2D charge distribution profile for the <100> and <110> NWTs is different. This is well-pronounced especially for the circular and square devices. For example, in the <100> circular NWT the charge distribution is of an almost perfect circular shape, which corresponds to the complete symmetrical cross-section shape of the wire. However, in the <110> transistor, even though the device has the perfect circular symmetry, the shape of the charge distribution in this 2D plane is closer to an ellipse. The explanation is related to the fact that the effective masses along the cross-section of the wire in the <110> channel directions are different and this difference leads to an anisotropic charge distribution. Moreover, all transistors with the <100> channel

orientation have more charge in the channel in comparison to the <110> transistors. This is also valid for the case when the <110> wire is rotated by 90º, which is presented in the third column in Fig. 2.

The 2D charge distribution is constructed from the probability distribution given by the quantum eigenvectors (wavefunctions) and the occupation density obtained from the Fermi level and eigenvalues (subband energies). The wavefunctions in the two-fold (Δ2) and four-fold (Δ4) degenerate valleys in the cross-section of the circular nanowire are presented in Fig. 3.

In order to evaluate the potential performance of the discussed transistors, we calculated the mobile charge (Q_M) and the gate capacitance (C_G) as a function of the shape of the NWT. The simulated gate capacitance is Quasi-static capacitances The mobile charge in the channel per-unit length QM at particular gate voltage VG is directly proportional to the NWT gate capacitance per-unit length $C_G=\partial Q/\partial V$, and the $Q_M=C_G$ (V_G-V_T). Where V_T is the threshold voltage, and ($V_G - V_T$) is the gate overdrive. For example, Table 3 compares the mobile charge Q_M at V_G=0.60V for the <110> wires. For a meaningful comparison, the Q_M (V_G) curves are aligned by modifying the gate work function. The following important conclusions can be obtained from Table 3. The quantum charge at V_G=0 QM is $0.193580x10^{01}$ (the curves of integrated charge of circular cross section NW is considered as reference).

Firstly, the circular and the two elliptical NTWs have ~9% more mobile charge in the channel in comparison to the square and rectangular devices. Also, the mobile charge is insignificantly affected by the Y/Z ratio. Secondly, the gate capacitance increases with decreasing of the Y/Z ratio. Thirdly, overall all devices with circular shape have lower gate capacitance in comparison to the squared wires.

Also Table 3 reveals interesting information about the Q_M/C_G ratio, again, the circular and elliptical devices show better characteristics in comparison to the square and rectangular wires.

Table 4 presents values for the Q_M, C_G and Q_M/C_G ratio for the wires with the same cross-section as in Table 3 but when the <100> channel orientation is considered. Comparing the results presented in Table 3 and Table 4 the following main conclusions can be established.

Firstly, all wires with the <100> channel direction have more charge in the channel in comparison to the <110> wires. Therefore, changing the crystal orientation of the silicon channel leads to an increase of the mobile charge in the channel. As a consequence, the gate capacitance increases as well which results in improving of the electrostatic control in the transistor. Secondly, the circular and elliptical NWTs discussed in Table 4 have around ~20 % more charge in comparison to the same devices in Table 3. More importantly, for the <100> channel direction, the charge in the circular, Elliptical 1 and Elliptical 2 cases is almost identical. Thirdly, all devices in Table 4 have bigger values for the Q_M/C_G ratio in comparison to the NWTs reported in Table 3, which means that the 'intrinsic' performance of those nanowires is better.

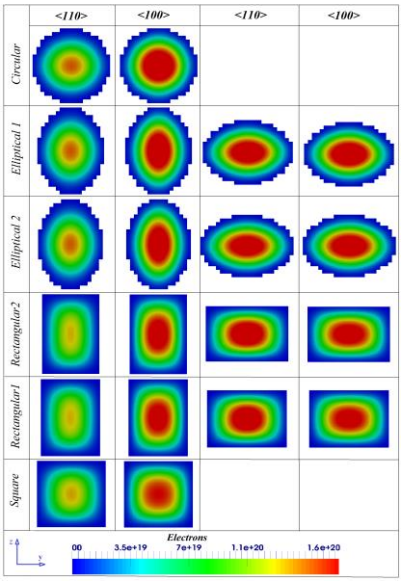

Fig. 2 Different NWT cross-sections simulated in this paper. Comparison of the charge distribution in the nanowire cross-section obtained from the Poisson-Schrödinger simulations at Vg=0.60V.

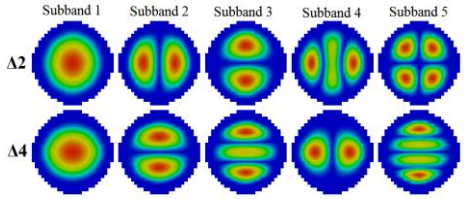

Fig. 3 Wavefunctions in the two-fold and four-fold degenerate valleys in the 2D cross-section of a circular Si NWT (VG=0.60V).

	Q_M ($\times 10^6$/cm)	C_G (10^{-11}F/cm)	Q_M/C_G (10^{17}/F)
Circular	*5.80413*	*1.473629*	*3.938664345*
Elliptical 1	*5.8225*	*1.481912*	*3.929045719*
Elliptical 2	*5.8641*	*1.510259*	*3.882843936*
Square	*5.5937*	*1.810817*	*3.089047651*
Rectangular1	*5.7271*	*1.826929*	*3.134823521*
Rectangular2	*5.7678*	*1.829183*	*3.153211024*

Table 3 Q_M(V_G=0.60V), C_G (V_G=0.60V) and Q_M/C_G ratio at identical Q_M (V_G=0.0V) for NWTs at L_G=14nm. With crystallographic channel orientation <**110**>.

	Q_M ($\times 10^6$/cm)	C_G (10^{-11}F/cm)	Q_M/C_G (10^{17}/F)
Circular	8.84131	1.71893	5.143496245
Elliptical 1	8.85225	1.720764	5.144371919
Elliptical 2	8.89878	1.728156	5.149292078
Square	8.01986	1.710817	4.687736912
Rectangular1	8.60415	1.81754	4.733953586
Rectangular2	8.83076	1.845104	4.786050000

Table 4 Q_M(V_G=0.60V), C_G (V_G=0.60V) and Q_M/C_G ratio at identical Q_M (G_V=0V) for NWTs at L_G=14nm. With crystallographic channel orientation <**100**>.

	Q_M ($\times 10^6$/cm)	C_G (10^{-11}F/cm)	Q_M/C_G (10^{17}/F)
*crystallographic orientation <**110**>*			
Elliptical 1	8.4769	1.643003	5.159394109
Elliptical 2	8.5981	1.713704	5.017260857
*crystallographic orientation <**100**>*			
Elliptical 1	8.85803	1.720764	5.147730892
Elliptical 2	8.93109	1.730152	5.162026227

Table 5 Q_M(V_G=0.60V), C_G (V_G=0.60V) and Q_M/C_G ratio at identical Q_M (V_G=0V) for NWTs at L_G=14nm. Those are the wires in the 3rd and 4th column in Fig. 3 where the the structure is rotated by **90º** for both the <**110**> and <**100**> crystallographic orientations.

In summary, similarly to the wires with the <110> channel orientation, the circular, elliptical 1 and elliptical 2 NWTs with the <100> orientation have better characteristics than the square and rectangular transistors. Moreover, all transistors with the <100> channel direction have more mobile charge in the channel and higher gate capacitance in comparison to the <110> wires.

Table 5 presents data for only two types of NWTs – Elliptical 1 and Elliptical 2. Those wires are shown in the 3rd and 4th columns on Fig. 2. Comparing Elliptical 1 and Elliptical 2 with <110> channel direction from Table 3 and Table 5 (top), reveal that rotating the wires by 90º increases the amount of charge in the channel by around 30%. This is most likely due to the fact that the anisotropic spatial confinement induced by the elliptical shape compensates the (opposite) electrostatic confinement induced by the different quantum masses along the cross-sectional diameters, offering, therefore, a more uniform charge distribution that is more effectively controlled by the wrapped-around gate. Thus leading to more capacitance and, as a result, a 'faster' wire. Also, comparing Elliptical 1 and Elliptical 2 with <100> channel direction Table 4 and Table 5, show that this time the rotation of the NWT by 90^0 does not affect the charge, gate capacitance and the Q_M/C_G ratio.

B. Nanowire with a different area of the cross-section

In our recent publication [27], we reported results for the NWTs with the <110> crystal orientation and similar cross sectional shapes as discussed above but with the 10 times bigger cross sectional area – 14 π (44 nm^2). In this subsection we expand the already published study by comparing not only the wires with the <110> crystal orientation but also with the <100> channel direction. More importantly, in this work we establish a link between the cross-sectional area and the 2D charge profile. For the purpose of this comparison we simulated wires with a circular cross-section and diameter of exactly 5nm, 6nm, 7nm and 8nm. It should be noted that the source and drain regions are removed in order to show the intrinsic charge distribution without the effect of the source and drain capacitances.

Fig. 4 reveals the 2D charge distribution in the middle of the channel for the NWTs with four diameters and two channel directions. The first important difference between the <100> and <110> wires is the observed isotropic charge distribution in the <100> case. This is consistent with the results presented in the section above. Again, the symmetry in the charge is based on the fact that the electron effective masses along the main principal axes (y and z) are the same. However, in the <110> case the electron effective masses are different and this leads to an anisotropic charge distribution. In Fig. 4 this effect is clearly visible and very well pronounced in the NWTs with the 7 and 8nm diameter.

Fig. 5 shows charge distribution of the same NWTs as in Fig. 4 but from a 1D perspective. Here we present the cut-lines along the y and z direction of the device. The <100> devices have identical values of electron effective masses and, as a result, the curves representing the charge distribution along the principal axes are identical. However, for the <110> wires the effective masses are different in the y and z direction. This

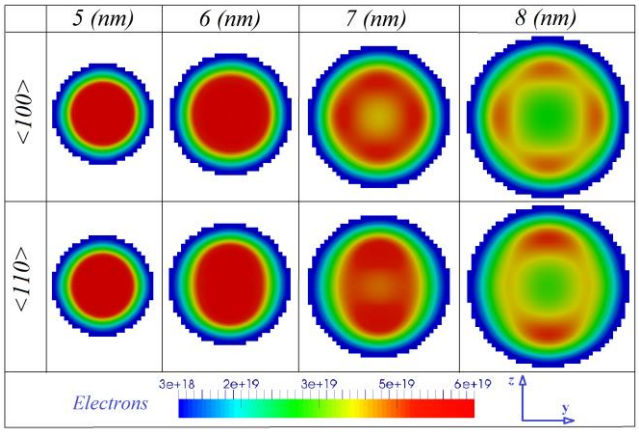

Fig. 4 2D charge distributions obtained for the circular cross-section NWT of 4nm, 5nm, 6nm, 7nm and 8nm for both <**100**> and <**110**> channel.

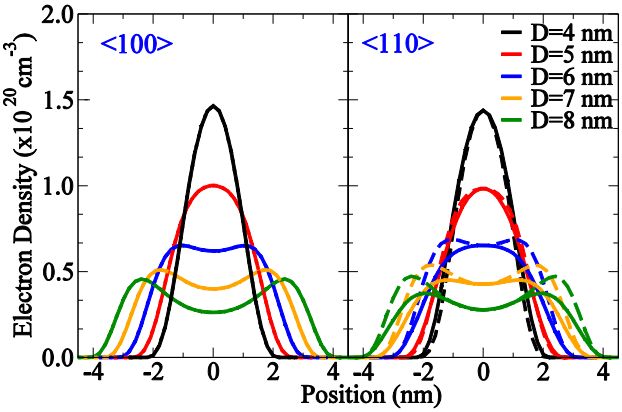

Fig. 5 1D charge distributions for the circular cross-section NWT of 4nm, 5nm, 6nm, 7nm and 8nm for both the <**100**> and <**110**> devices. The dashed line represents the plot over line of the charge along the 'height' of the wire (z direction) and the solid line is a line along the 'width' (y direction). For <**100**> wires the solid and dashed lines overlapped and this is the reason that only the solid one is visible.

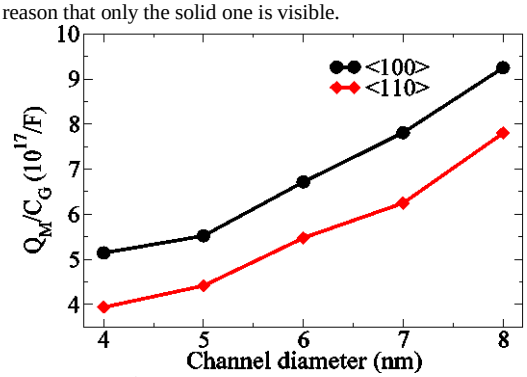

Fig. 6 Dependence of the Q_M/C_G ratio on the circular cross-section NWTs of 4nm, 5nm, 6nm, 7nm and 8nm for both the 100 and 110 devices.

explains two lines (dashed and solid) for each case in Fig. 5. Also, for the wires with the smallest cross-sections (4nm and 5nm) the charge distribution has almost perfect bell shape for both the <100> and <110> wires. With the increase of the cross-sectional area the charge distribution starts to deviate from this bell shape and gradually forms curves with two peaks close to the surface of the oxide. Moreover, these two peaks move further away from each other to create a clearly visible double humped distribution. The height of these peaks depends on the value of the election effective masses and confinement.

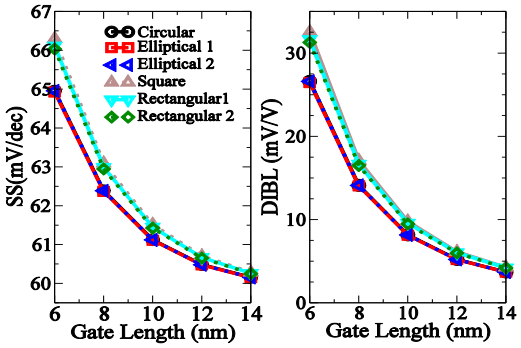

Fig. 7 Impact of the gate length on the SS (left) and DIBL (right) for all NWTs with different cross-sections. Channel orientation <**110**>.

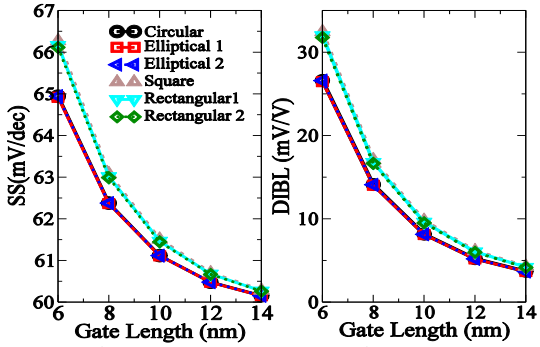

Fig. 8 Impact of the gate length on the SS (left) and DIBL (right) for all NWTs with different cross-sections. Channel orientation <**100**>.

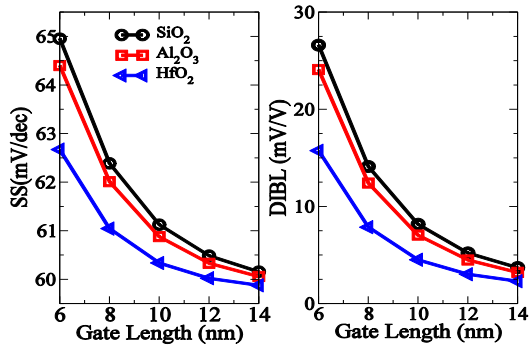

Fig. 9 The impact of three gate materials on the SS (left) and DIBL (right) for the circular nanowire with the <**110**> channel direction.

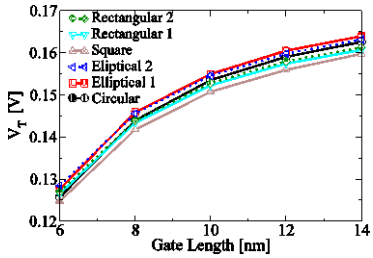

Fig. 10 Impact of the gate length on the V_T for all NWTs with different cross-sections. Channel orientation <110>.

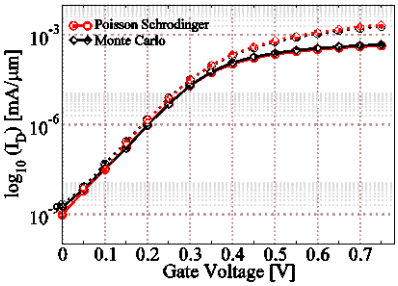

Fig 11 I_D-V_G curves of elliptical cross-section (eleptical2) NW with L_G=14nm. Dashed lines are at V_D=0.7V and solid lines V_D=0.05V. compare both MC and PS simulation results.

This specific charge distribution, based on the quantum nature of elections in the NWTs, could have a significant impact on the device reliability.

Moreover, Fig. 6 shows the mobile charge (Q_M) vs gate capacitance (C_G) for the <110> and <100> the same circular NWTs. Consistent with the data presented in the previous section, the NWTs with the <100> wire have a higher value of the QM/CG ratio in comparison to the <110> case, which can lead to a 'faster' device. Also value of the QM/CG ratio decreases with shrinking the 2D cross-section of the wire.

V. Impact of Q_M Effects on the SS and DIBL

The impact of the gate length on the drain-induced barrier lowering (DIBL), defined as $\Delta V_T/\Delta V_D$, and sub-threshold slope (SS) is illustrated in Fig. 7 and Fig. 8. There is a relatively little difference in the electrostatic integrity between the NWTs with different cross-sections and the two channel directions, all NWTs have equal cross-sectional area of 4π nm^2. However, all circular-shaped devices perform slightly better in comparison to other devices. It is important to emphasize the fact that the SS performance, even at the 6nm gate length, is comparable to the corresponding figures achieved by the 22nm and 14nm FinFET CMOS technologies however the DIBL performance is better. Moreover, the SS for the 14nm channel length is close to the theoretical limit of ~60 mV/dec at room temperature. Additionally, all NWTs demonstrate excellent electrostatics even at ultra-short gate length of 6nm. However, the two elliptical wires and the circular device again perform better in comparison to all other NWTs.

Fig. 9 compares the dependence of the SS and DIBL on the channel length for the circular wire with three oxide materials; SiO_2, Al_2O_3 and HfO_2, where the dielectric constant value increases in the same order. The high-K layer (Al_2O_3 and HfO_2,) has the 0.8nm physical thicknesses and the interfacial SiO_2 layer is of 0.3nm. From Fig. 13 it is clear that the devices with a hafnium dioxide used as the high-K gate layer material, which has the smallest equivalent oxide thickness (EOT), show the best values in terms of the SS and DIBL characteristics. Fig. 10 Impact of the gate length on the V_T for all NWTs with different cross-sections. Channel orientation <110>. Fig 11 I_D-V_G curves of elliptical cross-section (Eleptical2) NW with L_G=14nm compare both MC and PS simulation results [28].

Fig. 12 (left) illustrates the dependence of (I_{on}/I_{off}) on the channel length for the <110> NWTs with six different cross-sections, where I_{off} is the leakage current and I_{on} is the drive current at low drain voltage V_D=0.05V and gate voltage V_G=0.60V. Also Fig. 13 (right) compares the (I_{on}/I_{off}) for the circular nanowire wire with three oxide materials – SiO_2, Al_2O_3 and HfO_2. The calculated values of I_{on}/I_{off} curves are consistent with conclusions obtained for the mobile charge (Q_M) and gate capacitance (C_G) presented in Table 3. Indeed, the circular and elliptical NWTs show better performance than the square and rectangular wires.

Moreover, the nanowire with HfO_2 as a gate material shows the highest I_{on}/I_{off} ration in comparison to the two devices with

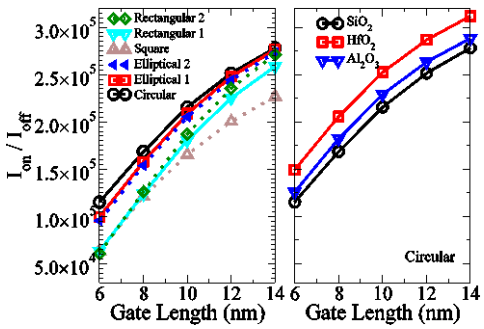

Fig. 12 The impact of the six cross-section shapes on I_{on}/I_{off} with the crystallographic **orientation <110>** (left). The impact of the various gate oxide materials on I_{on}/I_{off} only in circular NWTs (right).

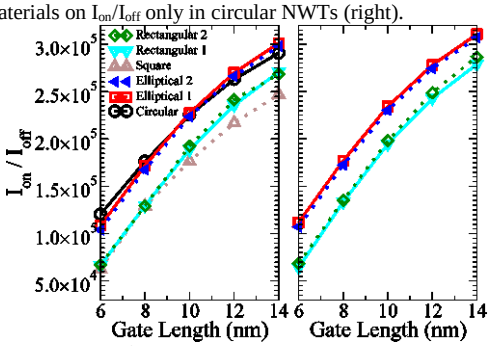

Fig. 13 The impact of the six cross-section shapes on I_{on}/I_{off} with the crystallographic **orientation <100>** (left). The impact of rotating the elliptical and rectangular nanowire by 90° with crystallographic **orientation <110>** (right).

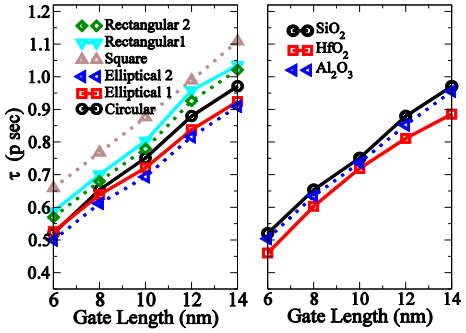

Fig. 14 The impact of the six cross-section shapes on intrinsic delay (τ) with the crystallographic orientation <**110**> (left). The impact of the various gate oxide materials on intrinsic delay (τ) only in circular NWTs (right).

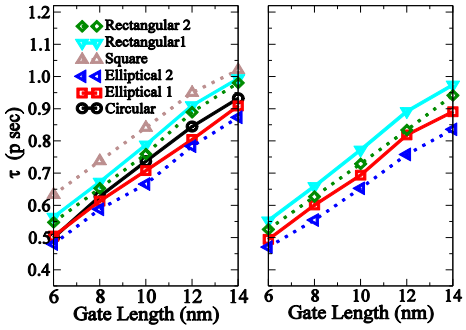

Fig. 15 The impact of the six cross-section shapes on intrinsic delay (τ) with the crystallographic orientation <**100**> (left). The impact of rotating the elliptical and rectangular nanowire by 90° with crystallographic orientation <**110**> (right).

SiO_2 and Al_2O_3 as the high-K gate layer material. This can be explained in the following way. The 'natural channel length' parameter λ_N in equation 3 is an effective way to determine the electrostatic requirements to the best possible short-channel control, where L_{eff} 6× is longer than λ_N

$$\lambda_N = \sqrt{\frac{2\varepsilon_{Si}t_{Si}^2 ln\left(1+\frac{2t_{ox}}{t_{Si}}\right)+\varepsilon_{ox}t_{Si}^2}{16\varepsilon_{ox}}} \qquad (1)$$

Where ε_{ox} is the electrical permittivity of the gate dielectric and ε_{Si} is the electrical permittivity of the channel [28-33]. The natural length is proportional to $t_{si}\times t_{ox}$ and the oxide material (high-*k* gate dielectric). Hence, wrapping the silicon channel in the high-K oxide material improves the gate capacitance and gives a better I_{on}/I_{off} ratio.

Fig. 13 reveals the impact of channel length on the (I_{on}/I_{off}) for the <100> NWTs with six different cross-sections. The right hand side of Fig. 11 shows data for the <110> wires which are rotated by 90°. For the <110> NWTs, rotation by 90° gives a slightly better I_{on}/I_{off} ratio in comparison to the <110> wire presented in Fig. 13, which has a positive effect on the device performance. Similarly, to the discussion in the previous section, the elliptical and circular devices show better performance in comparison to the square and rectangular ones.

Fig. 14 presents of evaluating the NWTs' speed in terms of intrinsic delay $\tau = C_G(V_{DD}/I_{eff})$ [34, 36], where C_G is the total gate capacitance, $I_{eff}=(I_H+I_L)/2$ is the effective current where I_H=Id(Vg=Vdd, Vd=Vdd/2) and I_L=Id(Vg=Vdd/2, Vd=Vdd), V_{dd}=0.7V, In all case the leakage current is I_{off}=0.1μA/μm. The evaluation of the intrinsic delay agrees with the conclusions derived from I_{ON}/I_{OFF} in Fig 12 and Fig 13. Elliptical wires, Elliptical 1 and Elliptical 2, show higher speed in comparison to all other devices. For example, Elliptical 2 wire with L_G = 6nm has 0.5ps delay and 0.93ps delay at L_G = 14 nm. On the opposite end is the Square nanowire which shows maximum delay of 0.68 ps and 1.12ps at L_G = 6 nm and L_G = 14 nm, respectively. Using high k oxide improves the performance as it is shown in Fig. 14 (right). Circular nanowire at L_G = 14nm, has τ = 0.87ps, 0.93ps, and 0.95ps for HfO_2, Al_2O_3, and SiO_2 respectively.

Fig 15 (left) shows the τ for all NWTs with <100> channel orientation various. In general all <100> have smaller intrinsic delay than <110>. For example, Elliptical 2 wire with L_G =14nm for <100> direction has τ = 0.87 ps while the value for the same wire but <110> is τ = 0.95 ps. Also similar to <110> wires the elliptical NWTs have better performance compare to rest. Also Fig. 15 (right) shows the effects of rotating the geometry of the nanowires with <100> channel orientation by 90°. The speed of all devices is slightly improved in comparison to the data presented in the same figure at the right hand side.

VI. CONCLUSION

In this paper we reported the quantum mechanical effects on the electrostatic performance of NWTs suitable for the beyond the 7-nm CMOS technology. Moreover, we revealed that the NWTs shape has an impact on the gate capacitance and the mobile charge in the channel. Additionally, we demonstrated that different gate oxide materials have an effect on the device characteristics, such as the sub-threshold slope and DIBL, and

that the thin effective oxide thickness could lead to an improvement of the device electrostatics. Moreover, we established a link between different gate materials and speed of the device in term of I_{on}/I_{off} and intrinsic delay (τ).

Overall, our work shows that the circular and elliptical wires, for both channel directions, have better device characteristics in terms of electrostatic driven performance and 'intrinsic' (Q_M/C_G) ratio in comparison to the square and rectangular ultra-scaled GAA NWTs. For example, we showed that the circular and elliptical wires have a more mobile charge (Q_M) in the channel and also a higher (Q_M/C_G) ratio in comparison to the square and rectangular devices. Also, our data revealed that the 2D charge profile and the amount of charge in the channel strongly depends on the channel direction. For example, all wires with the <100> channel have around ~20% more available mobile charge in comparison to the <110> cases. This can be crucial for establishing the strengths and weaknesses of such devices and determining the best design configuration and parameters for a specific application.

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