# Optimization of High Current Density Resonant Tunneling Diodes for Terahertz Emitters

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***Abstract*—We discuss the numerical simulation of high current density InGaAs/AlAs/InP resonant tunneling diodes with a view to their optimization for application as THz emitters. We introduce a figure of merit based upon the ratio of maximum extractable THz power and the electrical power developed in the chip. The aim being to develop high efficiency emitters as output power is presently limited by catastrophic failure. A description of the interplay of key parameters follows. We propose an optimized structure utilizing thin barriers paired with a comparatively wide quantum well.**

***Keywords—resonant tunneling diode, THz emitter.***

## I. Introduction

The ever increasing connectivity of the world is driving the need for wireless communication technologies, with the THz region attracting attention due to the possibility of high data rates with advantages in enhanced security and reduced network interference. Resonant tunneling diodes (RTDs) are high speed oscillators which have been coupled to antennae to realize effective room temperature emitters of THz radiation, demonstrating 1.92THz through harmonics[1]. The InGaAs/AlAs/InP material system is advantageous in terms of high electron mobility, suitable band-offsets, and offers low resistance contacts.

In this paper we explore the design of high performance RTDs using a 1D non-equilibrium Green's function simulator[2]. For this purpose, we propose a novel figure of merit related to the extraction efficiency of the radiated submillimetre wave emission power (Fig. 1). Previous studies have proposed using the peak current density, peak to valley current ratio (PVCR)[3], resonance linewidth[4] or a combination thereof, but we consider that these are not the ideal quantities when attempting to maximise the THz emission power from an RTD, as these are measures of the internal quantum efficiency of the device.

## II. RTD Modelling

The modelling package[2] approximates the solutions of the Schrödinger equation in a 1D crystal growth direction, taking into account the Fermi and Poisson distributions, effectively becoming a multibody electron-electron interaction calculator. The transmission matrix method is implemented for every applied bias to determine the quasi-bound superlattice well levels. The simulation does not fully accommodate the complex transport modes under thermally activated tunnelling and rough material interfaces. In this regard, the density matrix method has been proposed to overcome these limitations[5], however, we achieved a similar goal empirically matching the scattering potential (quantity in the Green's function introduced to take into account wave-packet perturbation).We have found that a 2-band $k{\cdot}p$ model is sufficient in most numerical simulation of our Type I RTD structures. The model successfully simulates the intrinsic hysteresis of structures described in the literature [6].

The MOVPE growth of the InGaAs/AlAs RTD on an InP substrate is described in [7]. The modelled structure consists of i) 20nm $In_{0.53}Ga_{.47}As$, $3{\cdot}10^{18}$ ii) 7 monolayer (MLs) $In_{0.53}Ga_{.47}As$ injector iii) 4MLs AlAs iv) 15 MLs $In_{0.8}Ga_{0.2}As$ (QW) v) 4MLs AlAs vi) 20nm $In_{0.53}Ga_{.47}As$ collector vii) 25nm $In_{0.53}Ga_{.47}As$, $3{\cdot}10^{18}$. This reference structure yields a peak current density of ~700kAcm$^{-2}$, used to generate a primary oscillation of 353GHz when coupled into a slot antenna. Fig. 1 shows representative I-V characteristic of these devices[7],

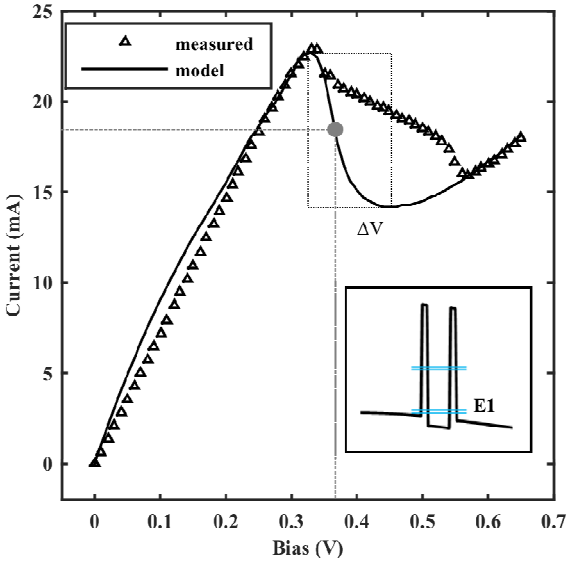
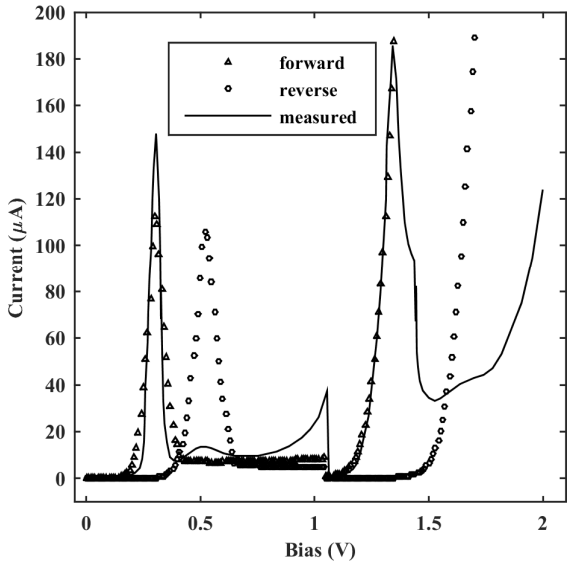
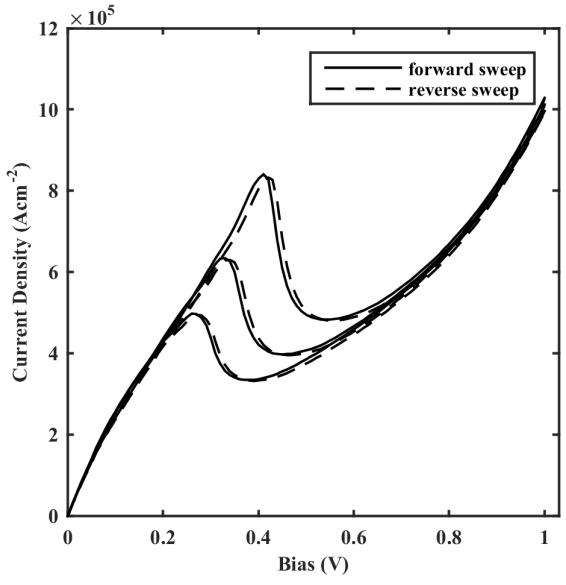



Fig. 1. Modelled and measured RTD I-V characteristic shown with electrical chip power (mid-point of negative differential conductance) and extractable power. (inset) Conduction band profile under bias, shown with 2 quasi-bound states.




(a)




(b)

Fig. 2. (a) Modelled forward and reverse voltage sweeps fit to data from [6], showing the intrinsic bistability of the device (b) Modelled forward and reverse voltage sweeps of our reference RTD design, with different QW widths.

together with the modelled fit which provides the baseline for this paper. Full Hartree potential calculations are employed in the area including the 2nm entry spacer, barriers, and quantum well (QW) layers. The rest of the model uses the bulk approximation to save computational time with minimal loss of minimum loss of fidelity.

## III. Nature of RTD resonance

One of the main issues in estimating the oscillator output power points back to the reported hysteretic region of measured I-V curves[8], [9]. However, the nature of this hysteresis can be either due to the intrinsic bistability of the device[6], [10], *i.e* quantum well charge accumulation and depletion due to quasi-bound level mis-alignment, or extrinsic, due to the external circuit and parasitic components such as contact resistance, inductance and line-loading effects [11]. An extensive modelling study has also been made to ascertain the effect of various design parameters on the hysteresis and plateau region[12] for memory applications.

We therefore investigated the nature of the intrinsic oscillation, and whether this comparatively slow charge-build-up and release is an issue in our designed structures. In this regard, we simulated an asymmetric barrier GaAs/AlGaAs device which shows strong intrinsic bistability [6]. Figure 2a plots our simulation results (ascending and descending voltage sweeps) in addition to experimental data extracted from [6] at 4K. The time averaged experimental data can be well explained by the superposition of the ascending and descending sweep simulations indicating how the simulator can be utilized to analyze the relative importance of intrinsic oscillation in RTDs. Simulations for our high current density structures is plotted in Fig 2b, which show limited difference between forward and reverse sweeps. The small differences are attributed to the difference in the undoped spacer layers of the structure. We confirm that oscillation is therefore dominated by the higher frequency extrinsic bistability in our structures.

## IV. Figure of merit

Our figure of merit is composed of two measures: the time-averaged electrical chip power ($P_{chip}$ = IV at the mid-point of the negative differential conductance (NDC)), and the extractable THz power, derived from the 3rd order polynomial approximation of the I-V plot, equation which can be re-written as a Van der Pol oscillator characteristic [13]

$$P_{THz} = 3/16\ \Delta I \Delta V \tag{1}$$

These values are highlighted schematically in Fig. 1. We therefore define our figure of merit (FOM) to be

$$FOM = P_{THz}/P_{chip} \tag{2}$$

Since $P_{chip} > P_{THz}$ , the ratio will be always subunitary and is a measure of the radiative extraction efficiency of the RTD. The simple 3rd order polynomial will not provide a satisfactory fit in this model, especially as the valley current is in practice a positive value. The modelled N-shaped I-V is spliced together using several asymptotes, the most important of which is the characteristic NDC region. Furthermore, the discrepancy seen in Fig. 1 can only be explained due to the contribution of parasitic circuit elements (both source and load-side), causing a current oscillation in the device, which is then time-averaged by the source-measuring unit.

## V. Results and discussion

Our investigation proceeds with varying the 3 key parameters of the RTD: the barrier width, QW width, and QW depth. In order to give an unambiguous calculation, all dimensions are expressed in monolayer (MLs).

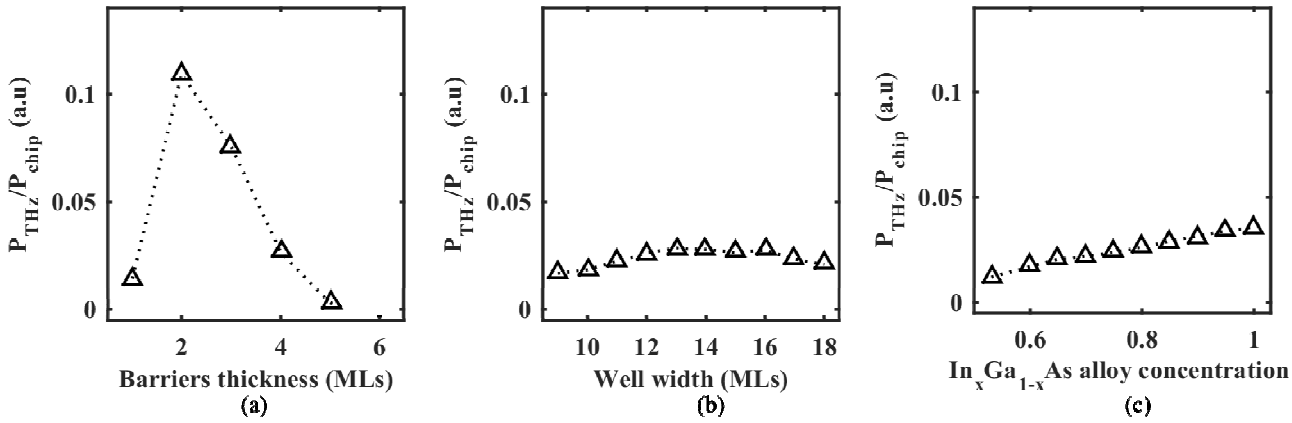



Fig. 3. The variation of our figure of merit shown against individual changes from the reference structure: (a) the width of the barriers in monolayers, (b) the QW width in monolayers (c) varying the depth of the QW through the composition of the ternary alloy

Changing the barrier width produces effects in line with previous publications[3], in that there is an exponential increase in peak current at the expense of PVCR; In most structures, there is an optimum occurring at around 3MLs. However, our figure of merit is maximised when the barriers are set to 2MLs thickness, due to the change in the NDC, something which conventional figures of merit neglect to take into account. At 1ML, the loss of confinement is pronounced as the non-linear behaviour is subdued, whereas our model could not predict the resonance at 6ML, which can be attributed to the lack of taking into account the changing strain conditions[14]. We mention that the maximum peak current density recorded in this case would reach values of 2.5MAcm$^{-2}$, requiring a device diameter <1μm and additional consideration for heat dissipation.

Increasing the QW width (Fig. 3b) brings the quasi-bound resonant levels closer to the conduction band potential limit, at the expense of an increased carrier dwell time[15], in effect trading off high power output with the cut-off frequency. Our reference structure with a 4ML barrier reaches an optimum at 13MLs.

Increasing the well depth is achieved by altering the indium composition in the InGaAs alloy. This has a two-fold effect however, in that the incorporation of further indium not only alters the band gap, but the lowered effective mass translates into a decrease in the available density of states, resulting in a lower peak current density. This however, also reduces the operational bias of the device, which in practice, we would expect to lead to longer life times and reduced noise. With that in mind, in most of our simulations, the addition of extra indium up to InAs has no negative effect (Fig. 3c), unless $E_1$ falls below the conduction band, which happens with a combination of thin well/high indium concentration.

Since the largest impact on our FOM was obtained with 2MLs barriers, the next iteration shown in Fig. 4 takes this value and compares different QW parameters, with an optimum reached at a QW thickness of 16ML, with an InAs alloy. The optimised structure in Fig. 5 exhibits lower biasing requirements, higher PVCR, and similar peak current compared to the reference design. We note that this model does not consider the practicalities of epitaxial growth. The present RTDs are partially strain balanced (4ML AlAs +3.54% strain, 15ML $In_{0.8}Ga_{0.2}As$ −1.85% strain). The proposed structure is therefore highly challenging in terms of high quality epitaxy. Future work will include strain balancing effects to determine an optimal structure which can be grown without significant strain relaxation. A 3ML barrier structure may be preferred in such a case due to the enhancement of strain balancing allowing a thicker, higher indium QW.

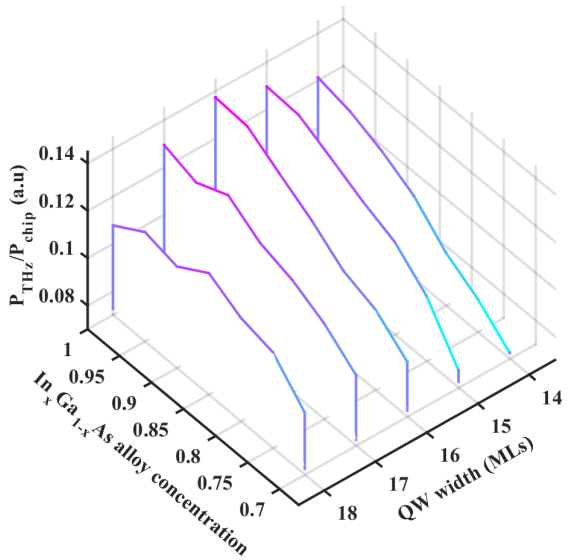



Fig. 4. The variation in the figure of merit using symmetric 2MLs AlAs barriers (color online)

## VI. Conclusion

We have shown a novel figure of merit based on measurements from our own fabricated RTDs that can be used as a design aid to maximize THz radiation output. We highlight the importance of the chip power and explain how the variation of certain epitaxial parameters affects the efficiency of the device. An optimal device is proposed by varying 3 essential geometrical parameters. The practicality of manufacturing this device is discussed.

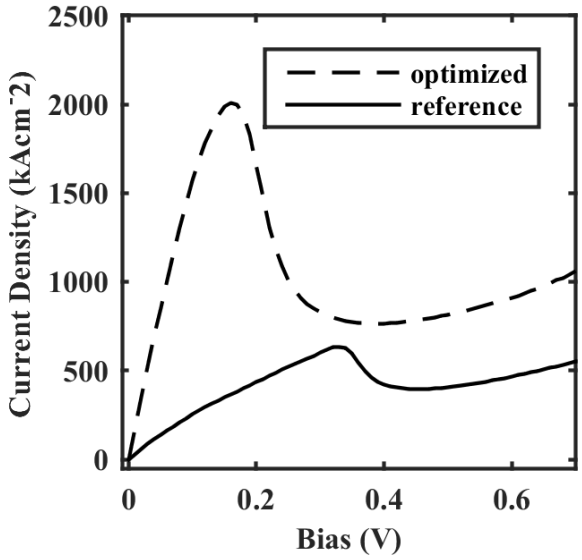



Fig. 5. Comparative I-V between current and proposed device

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