A Modular IGBT Based Current Flow Controller for Multi-terminal HVDC Grids

Hatem Yassin Mohamed Elhady Diab

A thesis submitted in partial fulfilment of the requirement of Staffordshire University for the degree of Doctor of Philosophy

August 2016

Acknowledgments

First of all, I am grateful to the Almighty God for establishing me to complete this thesis.

I would like to deeply thank my principle supervisor Professor Sarath Tennakoon for his valuable advice, excellent guidance and effective support. Also Dr Chris Gould my second supervisor is much thanked.

Special thanks to Professor Mostafa Marei, the external supervisor for his endless efforts and support throughout the project duration, his guidance is effectively reflected on the quality of the work produced.

I would like to acknowledge faculty staff members Dr. Soliman, Professor Claude, Professor Mansour and my colleagues Hesham, Hussein, Soheil, Samir and Monday for all their support.

My sincere thanks to Mr. Graham Preece and Mr. Dave Martin for their continuous technical support and fast response in all laboratories and logistic queries, thanks for doing your work with passion.

I would also like to acknowledge Arab Academy for Science and Technology for funding my PhD project.

I would like to express my gratitude to my lifetime friend, Mahmoud Al Wadie, for all his support and encouragement. I am really lucky to have you as a second brother, always present whenever I need you, I would have never gone that far without you by my side.

A heartfelt gratitude goes to engineer Ismail Taha, thank you for being my inspiration and I will never forget your precious advice.

Most importantly, I would like to thank my Family members; my mother, father, my brother Karim, my grandmother, Moshira, Tarek, Salma and Dodo for all the mental and physical support that they gave me, they all made my journey full of many unforgettable moments.

Last but not least, no words can describe how I feel towards my lovely wife Omnia, she gave away everything she had just to give me full support and worked day and night to make me feel comfortable; so I can complete my studies on the highest possible standards. May god bless her and my beloved son Mourad and keep them by my side as long as I live.

Abstract

Offshore wind turbines are preferred rather than onshore ones for their numerous advantages, such as land saving, higher wind speeds and higher power generation. However, AC power transmission would fail to deliver the generated power economically over distances longer than 80 kilometres using submarine cables. The more feasible option is to use High Voltage DC (HVDC) power transmission for offshore wind generation. Unlike AC transmission systems that have established power and current flow control methods, DC power transmission systems have only reliable power flow control techniques for point to point systems, which makes it one of the challenges preventing realisation of Multi Terminal HVDC grids (MT-HVDC) as cables may be subjected to higher currents causing overloading and thermal problems. Different HVDC power flow control schemes are suggested by controlling the AC/DC converters such as voltage droop control and voltage margin control. Other methods of power and current flow control based on the connection of new power electronic equipment to the grid have been also proposed.

This thesis presents operation and control of an IGBT based Current Flow Controller (CFC) for MT-HVDC grid applications. The CFC is studied in its preliminary two-port configuration and possible modes of operation and dynamic models are produced. An extended topology is proposed to allow the CFC to be connected to more than two cables at a time. Although the proposed extended CFC topology is simple in construction and gave acceptable results in most case studies, it has shown some drawbacks in certain case studies where controlled currents have significant differences in magnitudes. To resolve this problem, a generalized Modular CFC (MCFC) topology is proposed which allows each current to be controlled

independently and overcome the extended topology's drawback. Moreover, a reduced count switch count topology is proposed which reduces the MCFC cost by half in cases of unidirectional current flow control.

All proposed control strategies and topologies are validated using both computer simulation through MATLAB/SIMULINK and PSCAD/EMTDC software packages and experimental validation through Rapid Control Prototyping (RCP) with the aid of Opal RT real time simulator. Studies carried throughout this thesis show that the proposed MCFC may play an important role in current flow control applications in MT-HVDC grids due to its low cost, small footprint and accurate performance.

Table of Contents

List of Abbreviations

ANN	Artificial neural network
CCC	Capacitor commutated converter
CFC	Current flow controller
CNC	Computer numerical control
CSC	Current source converter
FACTS	Flexible alternating current transmission systems
FPGA	Field programmable gate array
GTO	Gate turn off
GUI	Graphical user interface
HCC	Hysteresis current control
HB	Hysteresis band
HVAC	High voltage AC
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
LCC	Line commutated converter
MCFC	Modular current flow controller
MMC	Modular multilevel converter
MTDC	Multi terminal direct current
NI-Crio	National instruments compact rio
PCB	Printed circuit board
PI	Proportional intergral
PID	Proportional integral derivative
PWM	Pulse-width modulation
RCP	Rapid control prototyping
SPWM	Sinusoidal pulse width modulation
VHDL	Very high -level design language
VSC	Voltage source converter
WECS	Wind energy conversion systems

List of Symbols

C	Capacitance
D	Diode
e	Error signal
f_s	Switching frequency
G	Neutral point
i_d	d-axis component current
i_{dc}	Steady state DC current
i_n	Current flowing in cable n
L	Inductance
P	Active power
P^*	Reference active power
P_{loss}	Power loss
P_{max}	Maximum active power
P_{min}	Minimum active power
R	Cable resistance
t_{off}	Turn off time
S	Power electronic switch
U	DC voltage
U^*	Reference DC voltage
U_T	Terminal voltage
V_a, V_b, V_c	Three phase voltages
V_c	Capacitor voltage
V_{dc}	Steady state DC voltage
V_o	Output voltage
V_n	Voltage at terminal n
X	Line impedance
ε	User defined threshold
δ	Power angle
ΔV	Potential difference between sending and receiving ends
ΔV_c	Voltage ripple
ρ_{DC}	Droop constant

Chapter

1

Introduction

1.1 Background

As more people continue to migrate from rural villages to big cities, the demand for new electrical power installations has increased rapidly in recent years [1]. Conventional fossil fuels such as coal, gas and oil are still the main sources of energy supply for electrical power generation. Although using these types of fuels results in producing the cheapest electricity, their high carbon emissions makes them the main contributor to environmental degradation that is clearly noticed in climate change problems [2]. Additionally, fossil fuels are not renewable and are expected to run out in the future [3]. Nuclear energy is considered to be another highly efficient, reliable and economically competitive energy source for electrical power generation [4]. However, nuclear energy has several political problems and long term environmental concerns, such as the catastrophic events of Ukrainian Chernobyl disaster in 1986 and Fukushima Daiichi nuclear disaster in Japan in 2011[5]. As a result, clean and renewable energy sources such as hydro, wind, solar and biomass became more attractive and several leading countries such as the United States and the United Kingdom have planned to increase the installed capacity of renewable energy resources dramatically over the upcoming few years. Some other countries such as Germany chose to abandon nuclear energy in favour of renewable energy [6].

In 2015, 28.9 GW of new power generating capacity was installed in the EU, 2.4 GW more than in 2014. Wind power was the energy technology with the highest installation rate in 2015: 12.8 GW as shown in Figure 1.1, accounting for 44% of all new installations. Solar PV came second with 8.5 GW (29% of 2015 installations) and coal came third with 4.7 GW (16%). Gas installed 1.9 GW (6.4 % of total installations), hydro 238.5 MW (0.8%), biomass 232.4 MW (0.8%), waste 118.5 MW, nuclear 100 MW, geothermal 4.3 MW and ocean 4.1 MW. Peat and fuel oil did not install any capacity in 2015. During 2015, Member States decommissioned 8 GW of coal capacity, 4.3 GW of gas, 3.3 GW of fuel oil, 1.8 GW of nuclear energy capacity, 518 MW of biomass and 281 MW of wind energy [7].

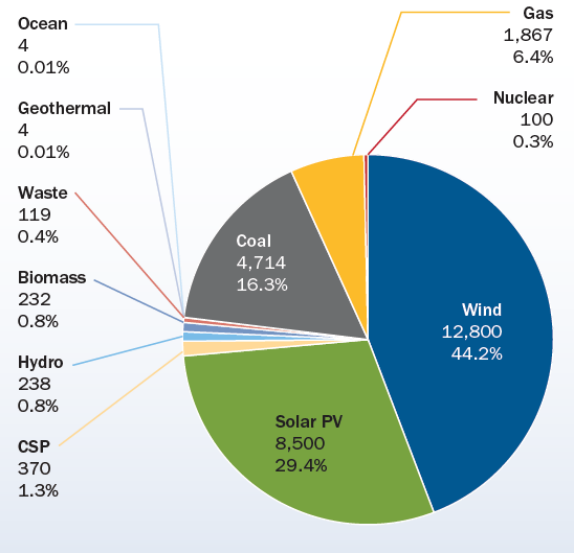


Figure 1.1 Share of new power capacity installations in EU in 2015. Total of 28.9 GW [7].

1.1.1 Current developments in wind energy

Wind energy has been utilized since early ages of ancient humans in 5000 BC when boats used wind to sail the river Nile. Also wind mills have converted the kinetic energy of wind into mechanical energy since 200 BC, where it was used for pumping water and grinding in china [8], [9]. In the early 1970s, wind energy started to gain interest for electrical power generation on a small scale as a result of the oil crisis. However, things changed in the 1990s and wind energy emerged as one of the leading sustainable energy resources [10].

Wind power generation gained more attention than other renewable energy resources as it is considered to have a low environmental impact [8], [10], [11]. The reasons can be summarized as follows:

- It offers a low cost alternative for fossil fuels.
- It does not consume any fuel or water and it does not produce any emissions.
- Has good lifetime expectancy of 20–25 years and breaks even its cost in three to six months of generation [7], [12], [13].
- It utilizes less land area per kilowatt-hour of power generation when compared to other resources.

- The wind energy conversion systems (WECS) have experienced a massive technological boost in recent years, increasing its efficiency and reliability.

In the 1990s, a single wind turbine was rated at a few kWs; now a single wind turbine can be rated up to 8 MW such as the Vestas V164 turbine introduced in 2014 [14]. Figure 1.2 shows the evolution of wind turbine diameter length and the power electronics from 1980 to 2018 [15].

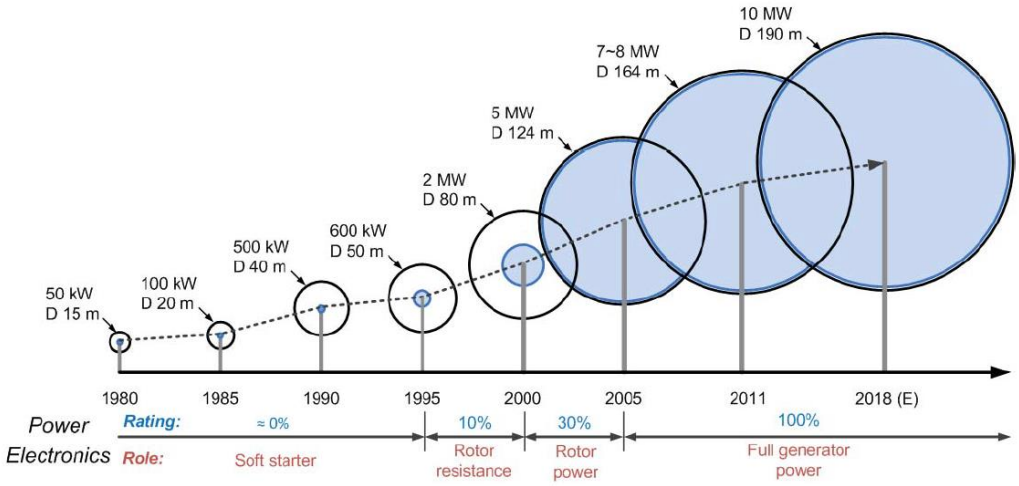


Figure 1.2 Evolution of wind turbine diameter length and it's power electronics *[15]*.

During 2015, 13.8 GW of wind power was installed across Europe, 5.4% more than in the previous year. 12.8 GW of it was in the European Union. Of the capacity installed in the EU, 9.7 GW was onshore and 3 GW was offshore. In 2015, the annual onshore market decreased in the EU by 7.8 %, and offshore installations more than doubled compared to 2014. Overall, EU wind energy annual installations increased by 6.3% compared to 2014 installations. Germany was the largest market in 2015 in terms of annual installations, installing 6 GW of new capacity; 38% of total capacity was installed in Germany. Poland came second with 1.2 GW, more than twice the annual installations in 2014 and one quarter of its national cumulative capacity at the end of 2015. France was third with 1.1 GW and the UK was fourth with 975 MW, 59% of which was offshore (572 MW). Almost half of the new capacity installed in 2015 came from the pioneering markets of Germany and Denmark. This

is mainly due to the stability of the regulatory frameworks in these countries, which gives investors visibility on cash flows of future projects and favours investments in wind energy. 47% of all new EU installations in 2015 took place in Germany and 73% occurred in the top four markets, a similar trend to the one seen in 2014. Offshore wind accounted for 24% of total EU wind power installations in 2015, double the share of annual additions in 2014. This confirms the growing relevance of the offshore wind industry in the development of wind energy in the EU [7]. Figure 1.3 shows the EU market shares for new wind energy capacities installed during 2015.

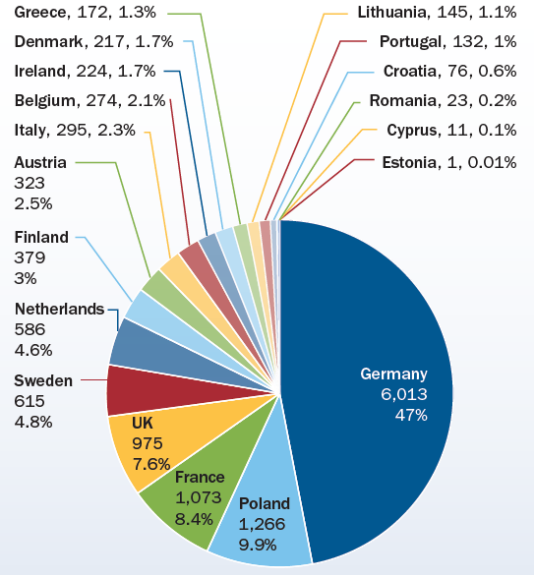


Figure 1.3 EU member state market share of new wind energy capacity installed during 2015 (MW), total 12.8 GW [7].

1.1.2 Offshore wind energy

As the wind technology emerged and the demand for more land use to install new wind farms increased, the idea of forming offshore wind generation platforms evolved [16]. In addition, offshore wind energy projects have one big advantage over the wind energy projects on land, namely more frequent and more powerful wind. Some recent studies have shown that offshore wind blow 40 percent more often than wind on land which means that in the future offshore wind farms can easily outpace

wind projects on land in terms of installed capacity [17]. However, the major disadvantage of offshore wind farms is high construction costs and complex logistics [16]. Structures in offshore wind energy projects need to be strong enough in order to withstand rough weather conditions; the cost of installing an offshore wind turbine was estimated to be double of that onshore per megawatt of capacity in 2010 [18]. Consequently, wind farms need to be large, or otherwise they are not economically viable. Figure 1.4 shows the global cumulative offshore wind capacity, where it can be noted that the United Kingdom is leading the charts by more than 5 GW of installed capacity, followed by Germany, Denmark, China, Belgium, Netherlands and Sweden [19].

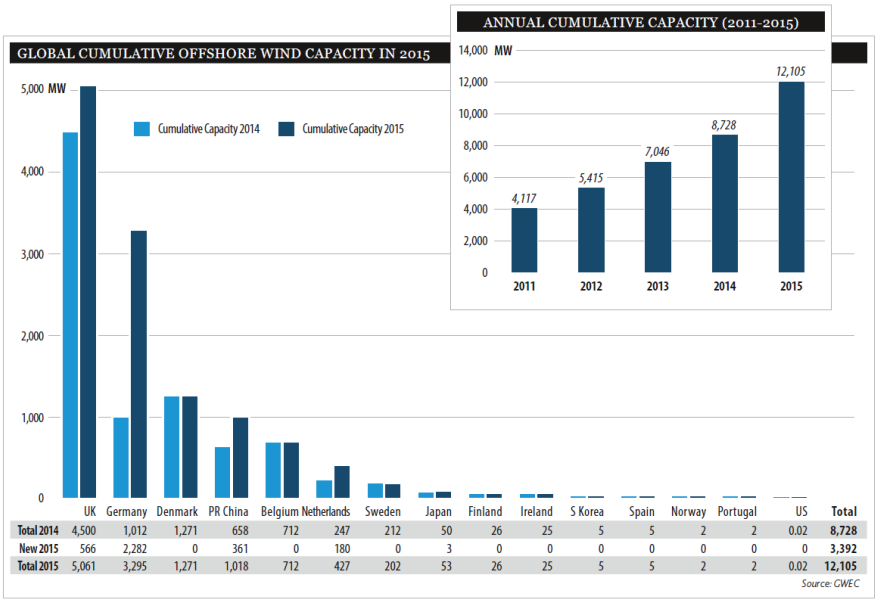


Figure 1.4 Global cumulative offshore wind capacity and annual cumulative capacity (2015) *[19]*.

1.2 Research Motivation

When offshore wind farms are built far into the sea, High Voltage Direct Current (HVDC) is the most viable way to transmit the generated power to shore [20]. However, almost all the available HVDC interconnections are point to point. Data presented in Figure 1.4, indicates that offshore wind energy farms are being installed extensively by European countries in the North Sea area. As a result, industry leaders

and research pioneers proposed the idea of interconnecting such farms with multi terminal HVDC (MT-HVDC) connections and forming the so called “European DC super grid” [21], [22] as shown in Figure 1.5.

Figure 1.5 Proposed European super grid *[21]*.

The collaboration between industry and researchers conducted a joint research group called “friends of the super grid” to work on practically realizing this idea. However, several challenges arose [23], [24] such as the following:

- Absence of reliable DC protection schemes and equipment that are needed to protect the system against Faults.
- The need of DC-DC high voltage transformer, to intertie connections with different voltage levels.
- Absence of power and current flow control methods. The control of the flowing current is important to prevent cables overloading and damage and to achieve dispatch orders.

This research project focuses on contributing to the MT-HVDC concept by offering a solution of precise current flow control in DC grids.

1.3 Research Aim and Objectives

This research studies an IGBT based Modular Current Flow Controller (MCFC) for application in MT-HVDC grids, with the aim of developing a feasible power electronic current control and limiting solution that can be implemented practically to prevent cables overloading and facilitate maintenance. To achieve this aim, the following objectives were set for this investigation:

- To perform a literature review to study AC/DC converter topologies, multi terminal HVDC grid configuration and available power and current flow control methods, especially methods proposed by industry.

- To investigate the available current flow controller (CFC) topology in order to develop all possible operating modes, mathematical model and appropriate control circuits.

- To achieve autonomous operation of the CFC by designing operating mode detection and change control unit, giving it the ability to operate continuously even under sudden load changes.

- To develop a generalized topology to be applied for large MTDC grids and a reduced switch count topology for unidirectional power flow applications.

- To validate all the developed operating modes, control strategies and topologies through both computer simulations and scaled down experimental prototyping.

1.4 Thesis Structure

This thesis consists of seven chapters as follows:

- Chapter 1: Introduces the thesis, includes a background on development of wind energy and multi terminal HVDC grids, research motivation and finally research aims and objectives.
- Chapter 2: Discusses current AC/DC converter topologies used in HVDC, MTDC grid configurations and challenges preventing their realisation.
- Chapter 3: Reviews existing current and power flow control methods through either the AC/DC converter control or applying addition equipment to the grid.
- Chapter 4: Presents the proposed current flow controller operating principle, modes of operation, mathematical model, control strategies, extended three-port topology and computer simulation results.
- Chapter 5: Presents the proposed modular generalized topology and reduced switches count topology of the CFC, and their validation through computer simulation.
- Chapter 6: Scaled down laboratory prototype details are demonstrated, and all proposed topologies and control schemes are validated experimentally.
- Chapter 7: Presents general conclusions, summary of contributions and recommendations for future research.

1.5 Publications

Journal papers:

- Diab, H.Y., Marei, M.I. and Tennakoon, S.B. “Operation and control of an insulated gate bipolar transistor-based current controlling device for power flow applications in multi-terminal high-voltage direct current grids”. *IET Power Electronics, 9(2), pp.305-315. 2016.*

- Diab, H.Y., Marei, M.I. , Tennakoon, S.B. and Abdelsalam M. "A Generalized Topology of a Modular Current Flow Controlling Device for Multi-terminal DC Grid Applications" a submitted *IEEE Transaction.*
- Diab, H.Y., Marei, M.I. and Tennakoon, S.B. "A Reduced Switches Count Topology of Current Flow Control Apparatus for MTDC Grids" *Journal of Power Electronics. Vol. 16, No. 5, 2016.*

Conference papers:

- Diab, H.Y., Tennakoon, S., Gould, C. and Marei, M.I. "An investigation of power flow control methods in multi terminal high voltage DC grids". *In Power Engineering Conference (UPEC), 2015 50th International Universities (pp. 1-5). IEEE. United Kingdom.*
- Diab, H.Y., Tennakoon, S., Gould, C. and Marei, M.I. "An IGBT based current flow controller for use in meshed HVDC grids" *The 5th International Conference on Renewable Power Generation – 2016, IET conference. United Kingdom.*
- Diab, H.Y., Abdelsalam, M., Tennakoon, S., Gould, C. and Marei, M.I. "Real Time Simulation of a Current Flow Controller for High Voltage DC Grids Applications" *In Power Engineering Conference (UPEC), 2016 51st International Universities. IEEE. Portugal.*
- Diab, H.Y., Tennakoon, S. and Abdelsalam, M. "A Current Flow Control Apparatus for Meshed Multi-Terminal DC Grids" *International Symposium on Electrical Apparatus and Technologies, SIELA 2016. IEEE. Bulgaria.*

Co-authored papers:

- Abdelsalam, M., Tennakoon, S. and Diab, H.Y. "An ADALINE Based Capacitor Voltage Estimation Algorithm for MMCs" *International*

Symposium on Electrical Apparatus and Technologies, SIELA 2016. IEEE. Bulgaria.

- Moussa, M., Abdelsalam, M. and Diab, H.Y. "Enhanced Approach for Modelling and Simulation of Modular Multilevel Converter Based Multiterminal DC Grids" *18th International Conference on Modelling & Simulation, UKSIM 2016, IEEE. United Kingdom.*
- Abdelsalam, M., Diab, H.Y., Tennakoon, S., Griffiths, A. and Marei, M.I. "Detection and Diagnosis of Sub-Module Faults for Modular Multilevel Converters" *In Power Engineering Conference (UPEC), 2016 51st International Universities. IEEE. Portugal.*

Chapter

2

Emergence of High Voltage DC and Multi terminal DC grids

2.1 Introduction

The modern configuration of electrical power generation, transmission and distribution systems has been changed significantly with the increased integration of advanced technologies and power electronics when compared with the conventional power system. In recent decades, new technologies such as smart grids (demand side management, bi-directional smart meters, etc.), Flexible AC Transmission Systems (FACTS) and new renewable power resources such as solar, wind, tidal and wave energy have been added gradually to the power system to enhance its functionality, reliability and continuity. Solar and wind energy, especially offshore, are considered to be the leading alternatives to conventional fossil fuel based systems in Europe generally and in the North Sea area in particular.

This chapter reviews the re-emergence of High Voltage Direct Current (HVDC) power transmission as a serious rival to High Voltage AC (HVAC) transmission and AC grid. Three AC/DC power converters topologies, Line Commutated Converters (LCC), Voltage Source Converters (VSC) and Modular Multilevel Converters (MMC) are reviewed as they form the core of any HVDC transmission network. The possible configurations that are available for forming multi-terminal DC grids are also discussed along with challenges that need to be overcome for the practical realisation of DC grids.

2.2 High Voltage DC Transmission

HVDC has been a power transmission option since early 1950s, where the world's first HVDC commercial transmission line was installed between Gotland and the Swedish mainland [25]–[27]. Since then, HVDC started to attract researchers and industry to investigate its feasibility and whether it can be a better substitute to conventional HVAC transmission. Until now, most European offshore wind farms are interconnected to the grids with HVAC [28], as each specific wind farm case in terms of network configuration and power rating play an important role in choosing the best solution. The main advantages that HVDC [28], [29] can offer when compared to HVAC can be summarized as follows:

- Ease of interconnecting two asynchronous grids, for example, the back to back HVDC link between Brazil and Argentina. By connecting two back to back AC/DC converters, AC power is converted to DC and then back to AC with the desired frequency, facilitating power exchange between 50Hz and 60Hz grids.
- Ease of active power control in point to point links.
- Lower power losses and cost over long distances of power transmission; in particular, in submarine transmission. This is the major factor that contributes toward HVDC to take over HVAC in offshore wind farm to grid connections. Figure 2.1 illustrates the cost against transmission distance for both overhead and submarine cable transmission. HVAC is more economical in shorter distances as the total cost is low when compared to the high cost of HVDC converter stations. Nevertheless, DC underwater cables rated to transfer an equal amount of power at lower costs than their three-wire AC rivals. On the other hand, transmitting power to long distances is more economical with HVDC as there are no reactive power compensators needed similar to when transporting via HVAC.As a result, HVDC is usually more economical when transmitting power using submarine cables for distances more than 70km [30].

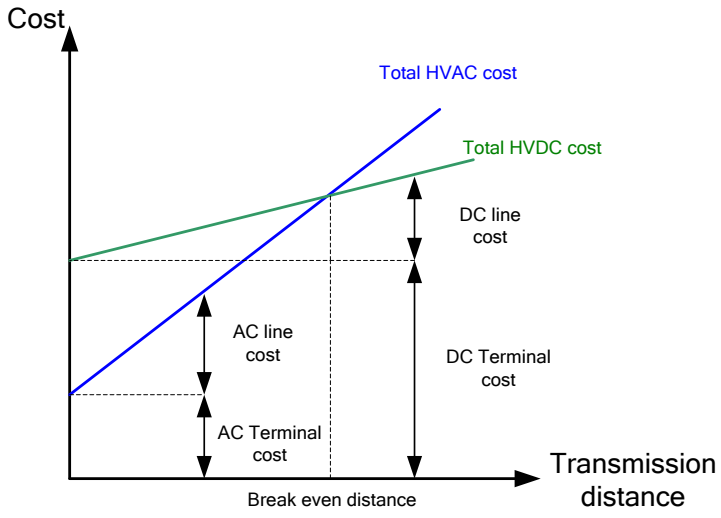


Figure 2.1: Power transmission cost versus distance with both HVDC and HVAC solutions.

The increase of more remote offshore wind farms as well as the desire for establishing international interconnections in the North Sea area [31]–[33] require long transmission networks and reliable power flow controllability. The large shunt capacitance of submarine cables affects HVAC connections causing stability problems and require large reactive power compensation equipment [28]. For these reasons, HVDC became the best available option for forming not only point to point connections, but also offshore multi terminal HVDC power transmission networks.

2.3 High Voltage DC Converter Stations

2.3.1 Line commutated current source converter

The most recognized and generally utilized in conventional HVDC power transmission is thyristor valve based three phase line commutated converter (LCC) or also known as 6 pulse Graetz bridge shown in Figure 2.2 [34]–[36]. LCC can transmit power in both directions where it can be operated in inverter or rectifier modes by changing the firing angle. If the firing angle is set to less than 90°, the converter is operated in rectification mode and transmits power from the AC side to the DC side. If the firing angle is set to a value between 90° and 180°, it can be operated as an inverter and power is transmitted from the DC side to the AC side. The high reliability, low cost technology and high power capability have put the LCC in a leading position when it comes to market share [37]. A widely used configuration of LCC is back to back HVDC transmission system shown in Figure 2.3. One major drawback of LCC based HVDC is that it suffers from low order harmonics which need to be treated through installing additional large passive filters. [38]. Despite the low cost and high efficiency of passive filters, they are still limited to specific frequencies. Moreover, they are affected by the system impedance [39] and consume large amount of reactive power due to the operation with AC current lagging the voltage[36], [40].

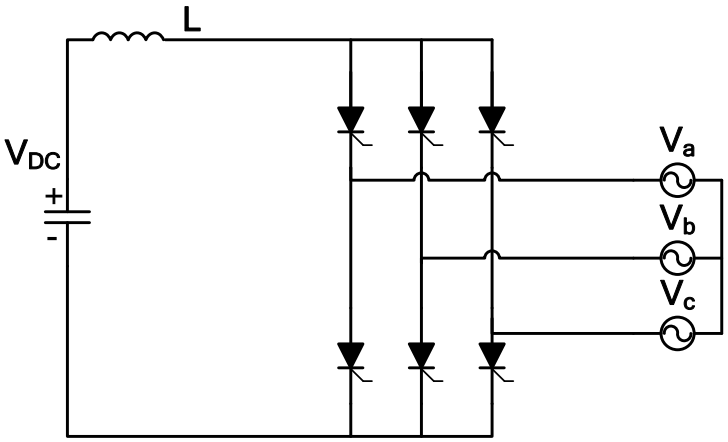


Figure 2.2: Three phase line commutated converter topology.

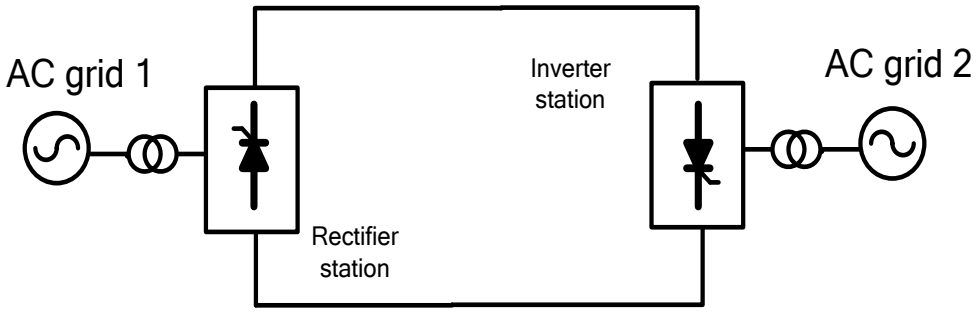


Figure 2.3: Back to back LCC based HVDC system.

To overcome these drawbacks, active filters have been proposed for LCC based HVDC systems as shown in Figure 2.4 as they are able to compensate the distorted current waveforms produced by the LCC [39], but on the other hand, more switching losses are introduced to the system as a result [34] and large footprints are lost. Also, a LCC needs to be connected to a strong AC grid to guarantee successful commutation otherwise operational problems may occur if connected to a weak system.

LCC HVDC converters are invariably 12 pulse as shown in Figure 2.5, where two 6 pulse LCC are displaced in phase by 30° [35], which leads to 12 pulse operation. The increased number of pulses eliminate all 6n±1 harmonics; 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics.

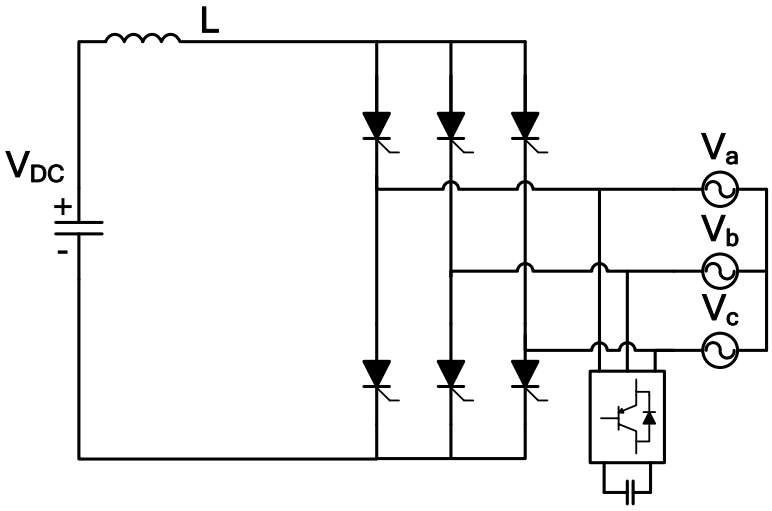


Figure 2.4: Active filter connected to LCC-HVDC system.

Another similar converter topology proposed is the Capacitor Commutated Converter (CCC) where series capacitors are connected between the converter and the AC grid (see Figure 2.6) allowing connection to weak AC grids, and overcoming LCC's commutation problem [41].

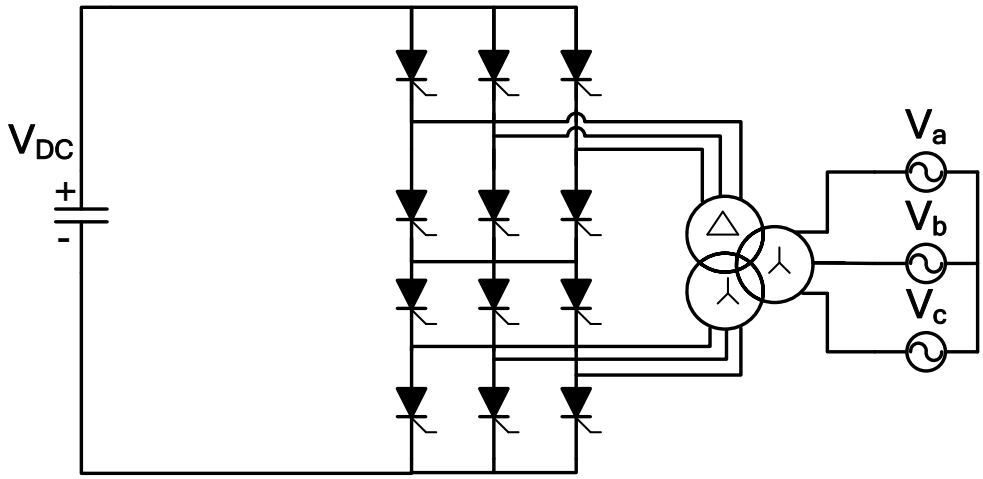


Figure 2.5: 12 pulse Line Commutated Converter circuit topology.

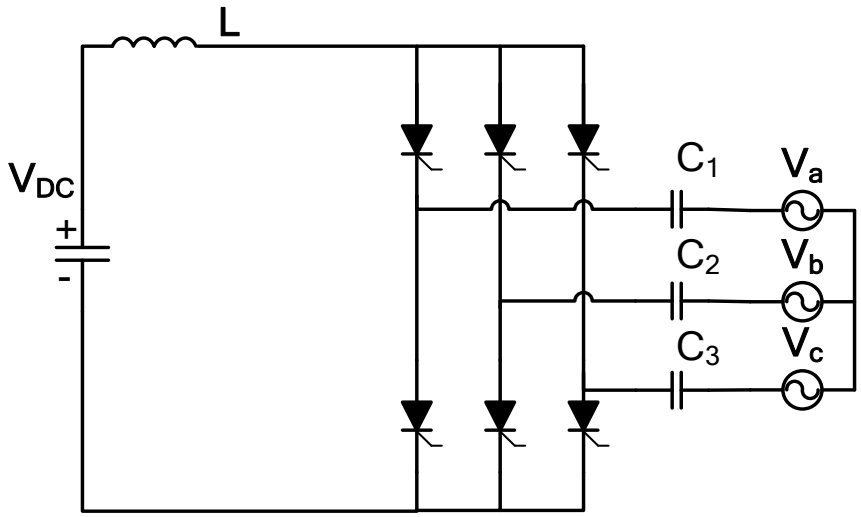


Figure 2.6: Circuit topology of Capacitor Commutated Converter (CCC).

2.3.2 Self-commutated voltage source converter

As its name implies, self-commutated Voltage Source Converters (VSC) use self-commutating switches such as Gate Turn Off Thyristors (GTO) or Insulated Gate Bipolar Transistors (IGBT), as shown in Figure 2.7 [42]. Switches can be switched on or off at any time by on/off gating signals, which is a great advantage in comparison with LCC's thyristor valves which can only be turned off by reducing the anode current below zero [42]. Anti-parallel diodes need to be connected with VSC's switches as IGBTs can only block voltage and permit current in one direction [43], and these diodes provide the ability to dissipate current in the other direction. VSCs give better waveforms as it can be operated in high frequencies, typically around 1 kHz, to get rid of low order harmonics [36]. Another important advantage of VSC technology is that it allows both active and reactive power control independently from each other and DC voltage level [40], allowing VSC converters to be installed at any point in the AC grid without the need of reactive power compensation as well [36].

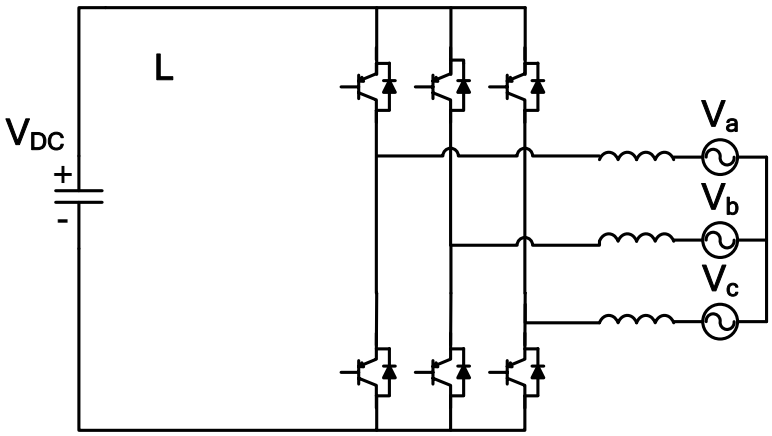


Figure 2.7: Three phase two level self-commutated – Voltage Source Converter (VSC).

One of the features that attracted researchers and industry leaders to the VSC technology is that it behaves as an amplitude and phase angle controlled voltage source [43], allowing the instant reversal of active power if needed, which gives VSC more potential to act in the converter role in futuristic MTDC grids when compared to LCC [42]. VSCs can also be connected in back to back configuration as shown in Figure 2.8. However, 2 - level VSC converters in its conventional form still need bulky DC link capacitors. VSCs also offer lower power capacities and higher switching losses when compared to LCC converters.

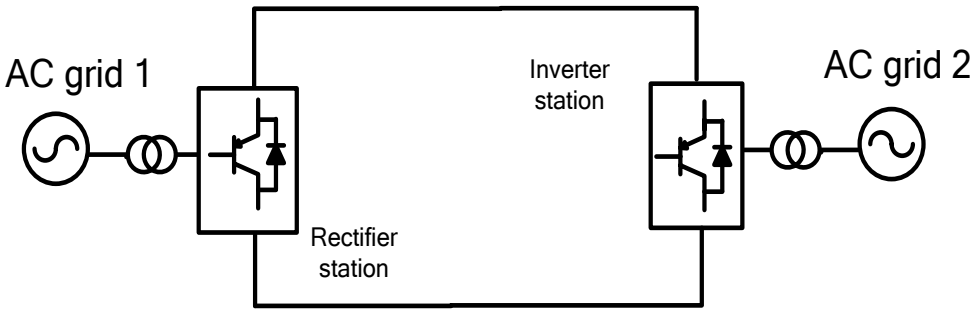


Figure 2.8: Back to back connection using VSC converters.

2.3.3 Multi-level converter topologies

Voltage source converters are thought to be the best choice for the future industry applications for HVDC transmission systems [44]. However, conventional topologies of two-level VSC still suffer from significant drawbacks such as poor performance in case of DC link faults [45], [46].

To make VSCs more feasible, several multi-level converter topologies have been introduced by researchers offering similar but upgraded operation to that of conventional VSC and providing features such as lower voltage stress on IGBT's, low dv/dt, and suppression of low order frequency harmonics and hence decreasing AC side filter footprint and cost [47], [48]. Diode clamped multilevel converter was first introduced in 1980 by [49] and afterwards extended to N levels topology in 1983 by [50]. Flying capacitor multilevel converter is another topology introduced in the early 1990s by [51], [52]. Both topologies suffered from DC link capacitors voltage imbalance, complexity with higher levels and vulnerability to the effect of system impedance [53]. Modular multi-level converters (MMC) emerged firstly in its half-bridge configuration in [54] and offered several advantages such as minimal conversion power losses when compared to other earlier VSC topologies, offer modular functionality to increase voltage level as desired, easy capacitors voltage balancing feature and higher system redundancy [55]. Unfortunately, half bridge MMCs suffer from AC inrush currents during DC link faults and are capable of operating in buck mode that does not provide active power to the AC grid when the DC link voltage decreases under the peak value of line AC voltage [55].

Full bridge MMC was introduced later on which offers similar advantages in addition to the ability of DC faults ride through and the voltage support capability to the AC grid during faults [56]. Also, H-bridge MMC cells can produce bipolar output voltage $+V_c$ or $-V_c$ which gives it another reason to be utilized in HVDC transmission and renewable energy interconnecting when compared to unipolar $+V_c$ output of half bridge MMCs.

Hybrid cascaded H-bridge multilevel converter was proposed as a special type of converter [57]. It offers multilevel output voltage waveform with less number of cells, but still has limited capabilities in interrupting DC faults and AC inrush current and the voltage stress on each switch is relatively high which in turn limits the application of such converter in HVDC transmission systems [58]. The next subsections discuss multilevel converters in more details.

2.3.3.1 Diode clamped multilevel converter

The topology of the diode clamped multilevel converter is formed of clamping diodes and series DC capacitors, each phase of n-level converter *(n-1)* capacitors are connected in series across the DC side and *2x(n-1)* switches are present along with *(n-1)x(n-2)* clamping diodes. This topology is capable of producing n levels of phase voltage in normal operation [59]. The single phase, three level diode clamped converter topology shown in Figure 2.9 consists of four IGBT switches (S_1, S_2, S_3 and S_4) each with its own anti parallel freewheeling diode (D_1, D_2, D_3 and D_4 respectively) allowing current flow capability in both directions. Each capacitor is subjected to voltage ½ V_{dc} and the neutral point *G* is set between both capacitors. These DC link capacitors are charged or discharged when current i_g flows into the neutral causing neutral-point voltage distortion [53].

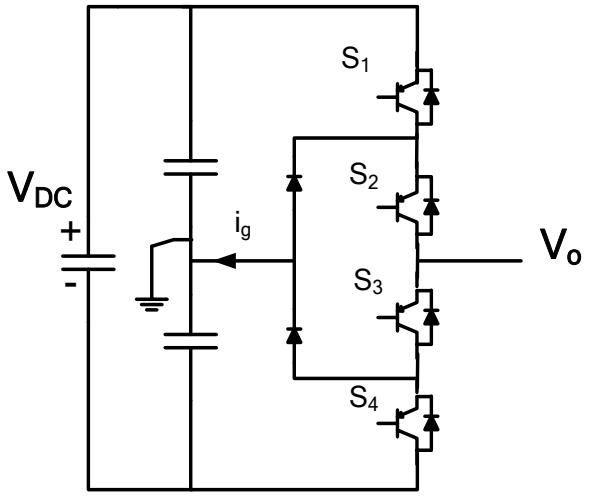


Figure 2.9: Single phase three-level diode clamped converter.

The output voltage of this converter V_o is produced by three switching stages. First, when switches S_1 and S_2 are on and S_3 and S_4 are off, the output is ½ V_{dc}. Second, when S_2 and S_3 are on and S_1 and S_4 are off, the output voltage is equal to zero. Finally, when S_3 and S_4 are the only switches that are on, the output voltage is -½ V_{dc}. The clamping diodes role is to clamp the voltage to ½ V_{dc} on each switch that is turned off [60]. The topology of the diode clamped converter is relatively complex making it difficult to be constructed in a high number of levels with high number of clamping diodes limiting its practical implementation in high voltage applications [61]. As the levels exceed three, DC link capacitors voltage become unbalanced and further circuits or capacitor voltage balancing techniques are required to solve this problem [62].

2.3.3.2 Flying capacitor multilevel converter

Another topology is the Flying capacitor multilevel converter, where the capacitors are combined with switches to produce different voltage levels by adding or subtracting the capacitor voltages [63]. The voltage stress on each IGBT is equivalent to the voltage rating of each capacitor; hence, for an n-level converter *(n-1)* DC link, capacitors are required as well as ½ *(n-1)x(n-2)* flying capacitor per phase. Figure 2.10 illustrates the circuit topology of a single phase three-level flying capacitor multilevel converter.

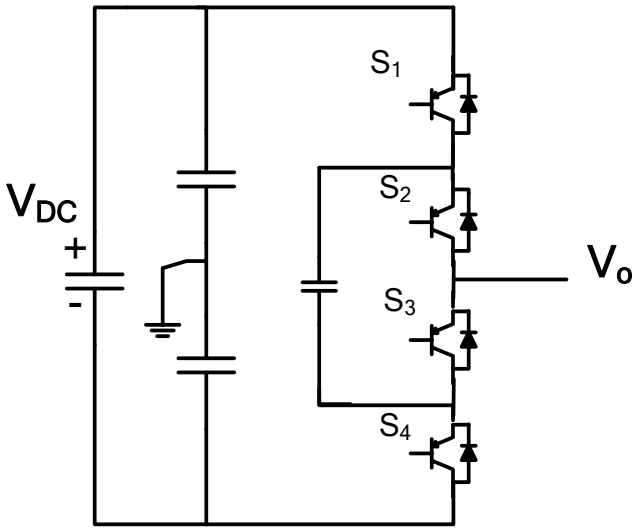


Figure 2.10: Single phase three-level flying capacitor converter.

The switching states are somehow similar to that of diode clamped converter mentioned earlier, offering three output voltage levels ½ V_{dc}, -½ V_{dc} and 0 [64], [65]. The flying capacitor multilevel converter requires a large number of capacitors at the DC side. For this reason, it is impractical to implement such topology in a high voltage transmission system with a large footprint and high cost of the bulky capacitors [66]; in addition to the DC link voltage imbalance mentioned earlier, the applications of this converter in medium voltage power transmission are limited [67].

2.3.3.3 H-bridge cascaded multilevel converter

The cascaded H-bridge multilevel converter is basically a set of series connected H-bridge cells each requiring its own independent DC source [68] as shown in Figure 2.11. This type of converter is not used in HVDC power transmission as there is no

DC link present. Still, H-bridge cascaded converters are used for integrating photovoltaic cells to the grid [69] and electric vehicles [70].

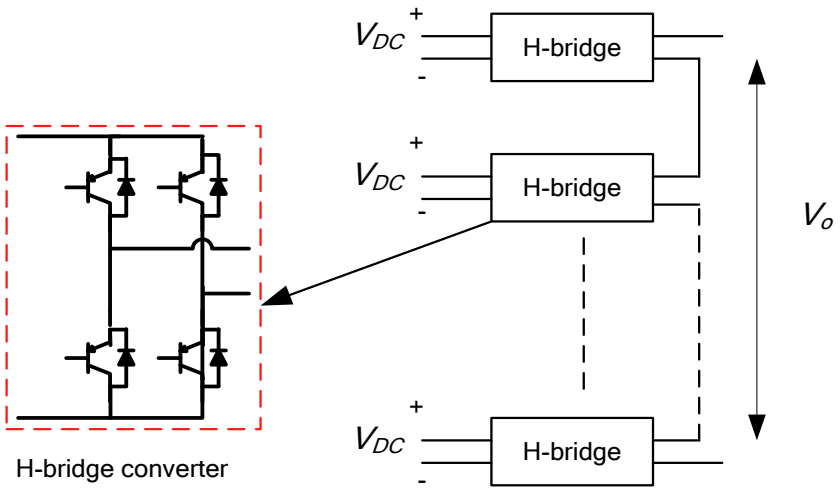


Figure 2.11: H-bridge cascaded multilevel converter.

2.3.3.4 Hybrid H-bridge cascaded multilevel converter

The hybrid H-bridge cascaded multilevel converter's topology is shown in Figure 2.12 with *n* H-bridge cells per phase. The converter can produce up to *4n+1* voltage levels. The voltage rating of each cell capacitor is $\frac{\mathrm{Vdc}}{2\mathrm{n}}$ and it is equal to the voltage stress on each H-bridge cell [57].

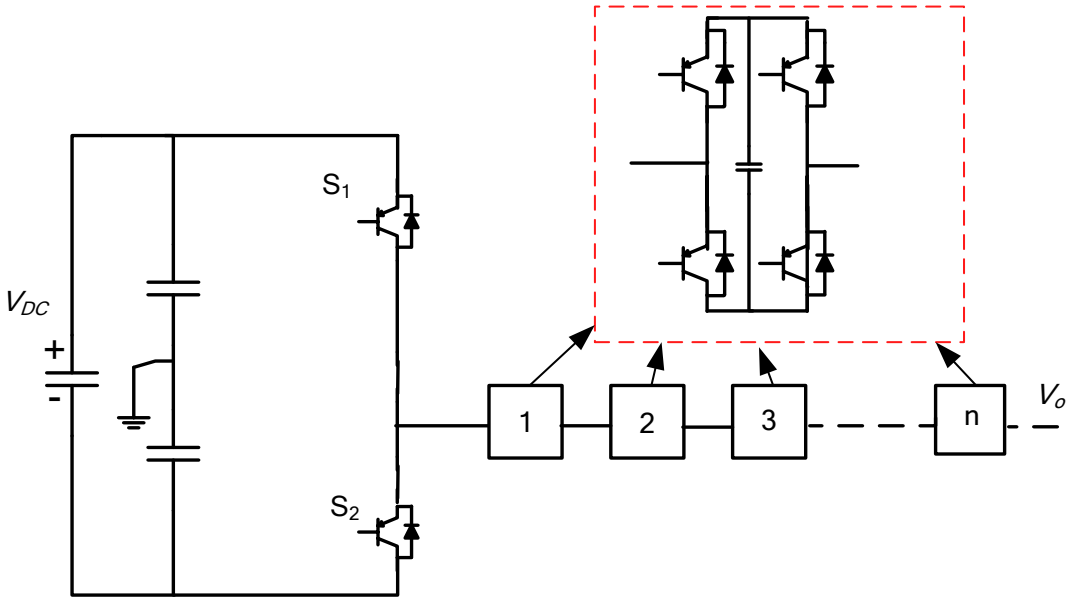


Figure 2.12: Hybrid H-bridge cascaded multilevel converter.

During DC faults, all IGBT switches including H-bridge cells are switched off, and cell capacitors give reverse voltage to suppress the inrush current from the AC grid. This leads to a state where no active or reactive power is exchanged during DC fault condition. The main switches, S_1 and S_2, are subjected to high voltage stress of value V_{dc} which limits the application of this topology in HVDC power transmission.

2.3.3.5 Half bridge modular multilevel converter

Single phase half bridge based modular multi-level converter topology is demonstrated in Figure 2.13 where it is formed of n half bridge cells per arm that is capable of producing *n+1* output voltage levels. The rating of each cell capacitor is $\frac{Vdc}{n}$ and it is the same value of voltage stress that is subjected to each switch. One of the main advantages of this topology is that the output voltage can have nearly a sinusoidal waveform with increased number of levels. Arm inductors are present to suppress the harmonics in arm currents and to limit the AC inrush current during DC side faults. Sinusoidal Pulse Width Modulation (SPWM) and phase shifted carried

modulation [71] are two major modulation methods commonly used in half-bridge MMC control. Cell capacitor voltage balancing techniques are also introduced [72].

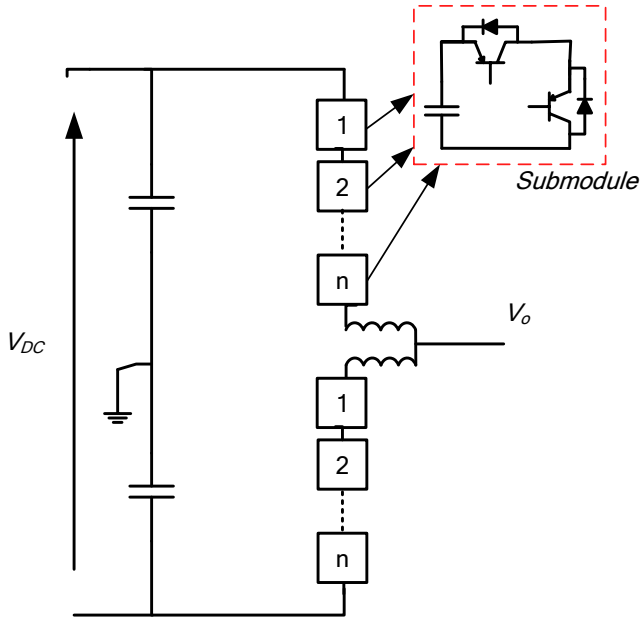


Figure 2.13: Half-bridge modular multilevel converter.

The half-bridge MMC offer several advantages such as the following:

- Low voltage stress on each switching element as mentioned earlier
- No need for bulky capacitors.
- The quality of output waveform increases with the increase of number of levels. Leading to less harmonics and smaller footprints for filters and less cost.
- Decreasing the switching frequency with the increased number of levels leading to less switching losses.

However, this type of converter does not offer DC fault ride through capability and it cannot be controlled in cases of DC link voltage decrease (between 0 and V_{dc}) which is a common case with renewable energy generation as wind speed and solar irradiance cannot be controlled. Another disadvantage of half bridge MMC is that it suffers from arm current harmonics and circulating current in each phase having significant increases in conduction losses.

2.3.3.6 Full bridge modular multilevel converter

With similar advantages of that of Half bridge MMC, the Full bridge MMC shown in Figure 2.14 offers low switching frequency which has direct impact on AC side filters size, low voltage stress on IGBT switches, eliminating bulk DC link capacitor, and excellent AC output voltage waveform that is close to sinusoidal. However, as the full bridge MMC involves more switches when compared to half bridge MMC at the same power level, it has a noticeable draw back that it produces higher switching losses. The full bridge MMC started to gain the attention of both industry leaders and researchers as it adds an important advantage to its half bridge rival, which is the DC fault ride through capability by suppressing AC inrush current with reversed cell voltage and is able to keep cell capacitor voltages to the rated value. Some other advantages such as post fault recovery and active power injection to the AC side by utilising the full range of DC link voltage gave the full bridge MMC superiority over all other topologies discussed earlier.

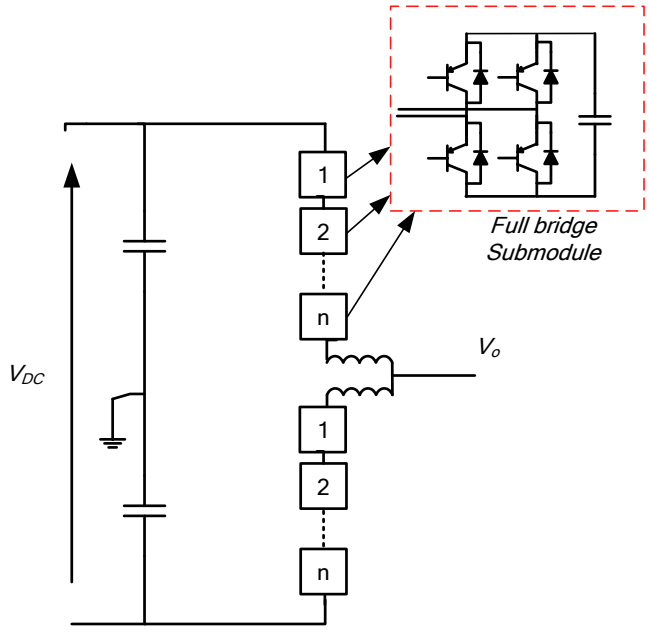


Figure 2.14: Full-bridge modular multilevel converter.

2.3.4 AC/DC converters summary

The most famous converter topologies and their functionalities discussed earlier in section 2.3.3 are compared in Table 2-1.

Table 2-1: Comparison between AC/DC converter topologies.

	Line Commutated	Voltage Source	Half bridge MMC	Full bridge MMC
Switching element	Thyristor	IGBT	IGBT	IGBT
Switching losses	Very low	High	Low	Acceptable
Operational losses	Low	High	Acceptable	Acceptable
Active power control	Yes	Yes	Yes	Yes
Independent reactive and active power control	No	Yes	Yes	Yes
Required reactive power	Yes	No	No	No
Requires filters at AC side	Yes – with large footprint	Yes – small footprint	No	No
DC fault ride through capability	Strong	Weak	Weak	Strong
AC fault ride through capability	Yes – with risk of commutation failure	Yes	Yes	Yes
Ability to operate in boost mode during DC link voltage collapse	No	No	Yes	Yes
Manufacturing cost	Low	Moderate	High	Highest

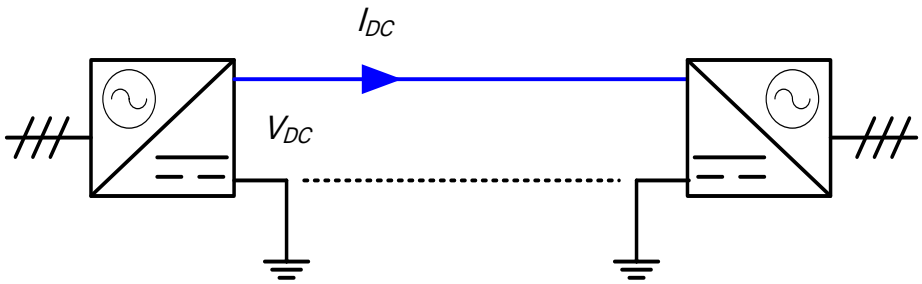
2.4 HVDC Transmission System Configurations

2.4.1 Point to point connections

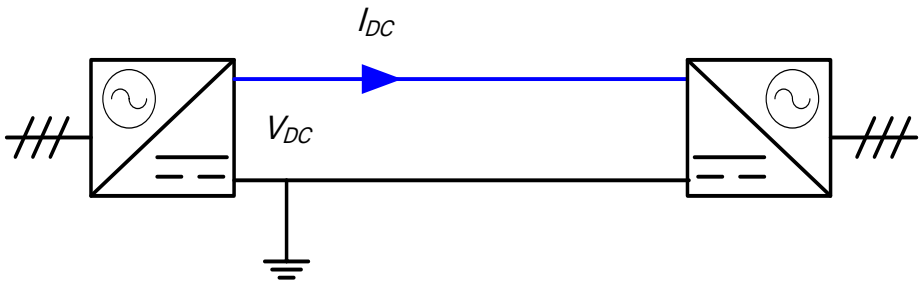
There are several possible HVDC configurations to interconnect any two AC/DC converters together. In the following three subsections, the Monopolar, Bipolar and back to back configurations are discussed in greater detail [73]–[78].

2.4.1.1 Monopolar connections

The monopolar is the most elementary HVDC transmission system arrangement. One pole is used to interconnect the two converter stations together, usually with negative polarity, to minimize corona effects [78]. The monopolar HVDC point to point configuration is possible either with ground return or metallic return as shown in Figure 2.15(a) and Figure 2.15(b), respectively. Ground return arrangement offers lower costs as only one DC cable is needed as shown in Figure 2.15(a). However, in highly populated areas or areas with high earth resistivity, such as fresh water reservoirs, ground return may not be the feasible option to be used. Metallic return can be used in such cases to overcome any environmental or interactions with metal structures. All monopolar configurations suffer from the drawback of losing the whole transmission link if any fault occurs in the converter or to the DC cable.



(a)

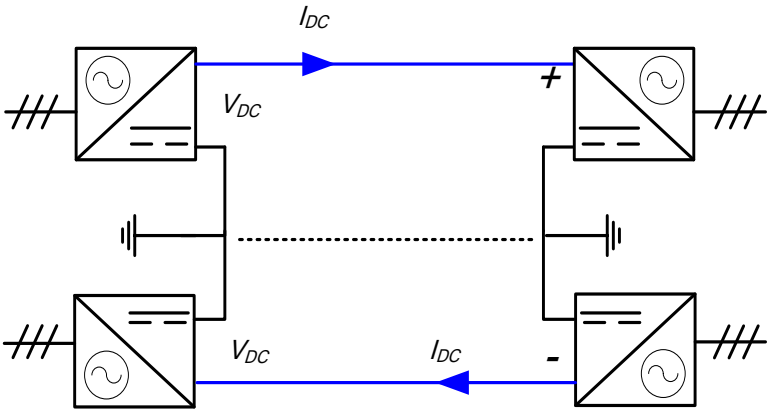


(b)

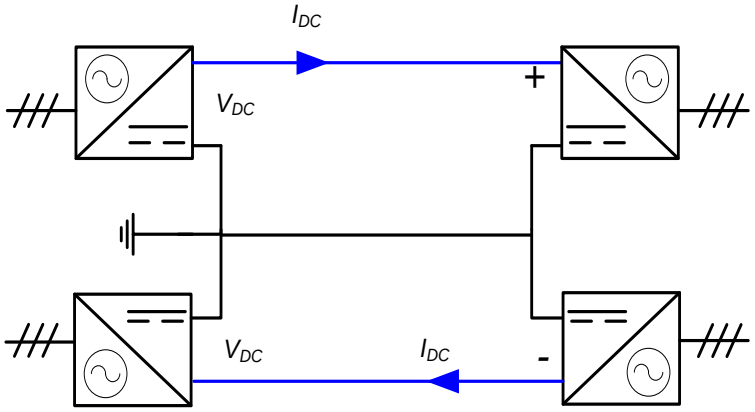
Figure 2.15: Monopolar HVDC point to point connection a) Ground return b) metallic return.

2.4.1.2 Bipolar connections

The bipolar configuration makes use of two HVDC lines/cables with positive and negative polarities. Currents in each cable have the same amplitude and there is no current flowing in the return path during normal operating conditions. For any given power rating, monopolar configuration is more economical to use, but some power ratings to be transmitted are higher than the rating of a single pole. The bipolar configuration can also be either ground return, which is mostly used when there are no environmental restrictions (see Figure 2.16(a)), otherwise metallic return arrangement is used (Figure 2.16(b)) as a path for currents to flow in cases of imbalance. The bipolar configuration offers more redundancy in cases of outage when compared to the monopolar arrangement which is considered to be a significant advantage.



(a)



(b)

Figure 2.16: Bipolar HVDC connection a) Ground return b) metallic return.

2.4.1.3 Back to back connections

Back to back HVDC arrangement, shown in Figure 2.17, is usually deployed in the connection of two asynchronous AC grids together, where the frequencies of the two grids are not the same and no long power transmission lines or cables are needed [73]. In this configuration, usually the two converter stations are built together in the same building, and the voltage level is kept low to minimize the HVDC switches cost [78]. Telecommunication is not needed as there is a short distance that needs to be travelled between the two HVDC converter stations which simplifies the control

and measurements equipment. Almost a quarter of all HVDC transmission projects are back to back configured using LCC converters due to high current capacities of Thyristor valves [76].

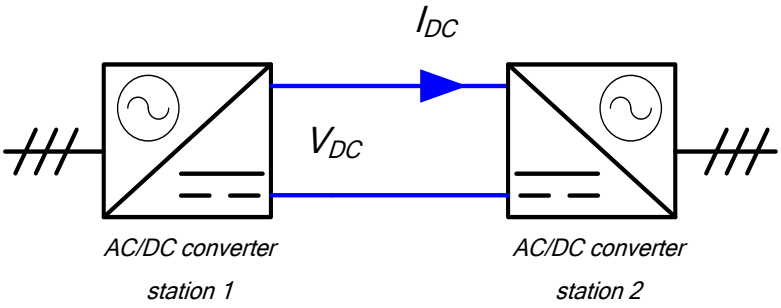


Figure 2.17: Back to back HVDC connection.

2.4.2 Multi-terminal connections

Multi terminal HVDC is a terminology used when more than two converter stations become interconnected through the DC side of the transmission system. Despite their initial proposal long time ago [79]–[82], MTDC connections have seen a revival in recent years primarily due to the advent of offshore wind farms paving the way for DC grids. Until now, only few projects out of more than 100 HVDC projects are known to have more than two terminals: the Hydro Quebec New England project in USA-Canada, the SACOI scheme in France-Italy, Nanao and Zhoushan projects in China [76], [78]. MTDC connections can be either series or parallel and these two types are discussed in greater detail in the following subsections.

2.4.2.1 Series connections

In series MTDC networks, all converter stations share the same DC current, while the voltage rating varies according to the amount of power to be inserted or absorbed from the network (see Figure 2.18).

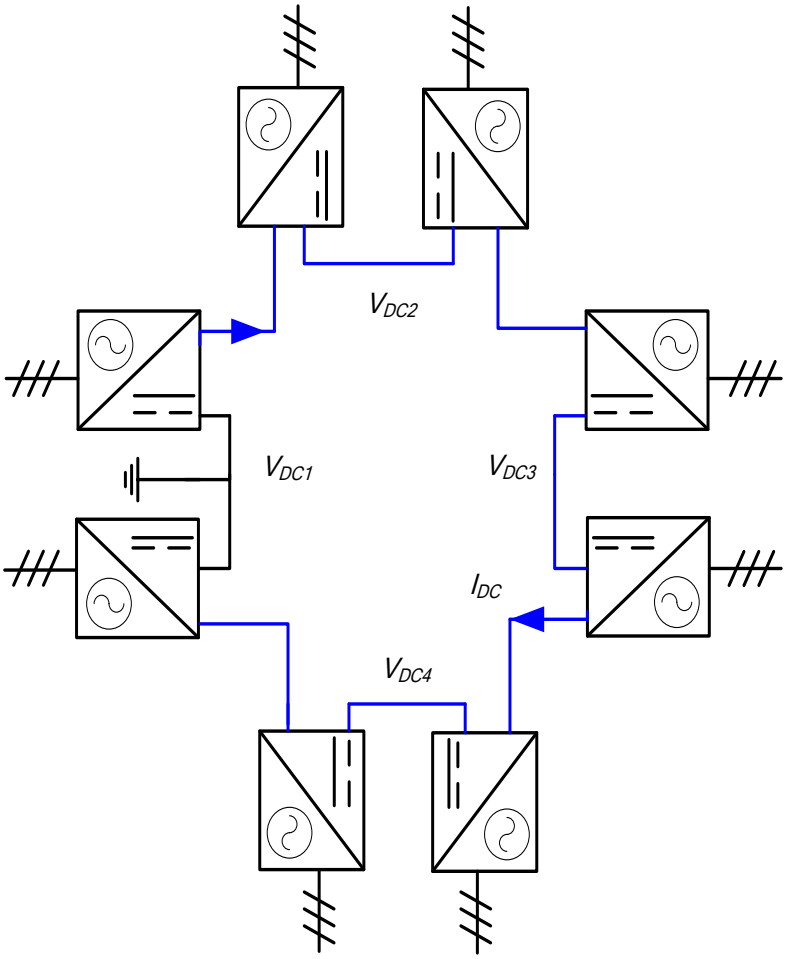
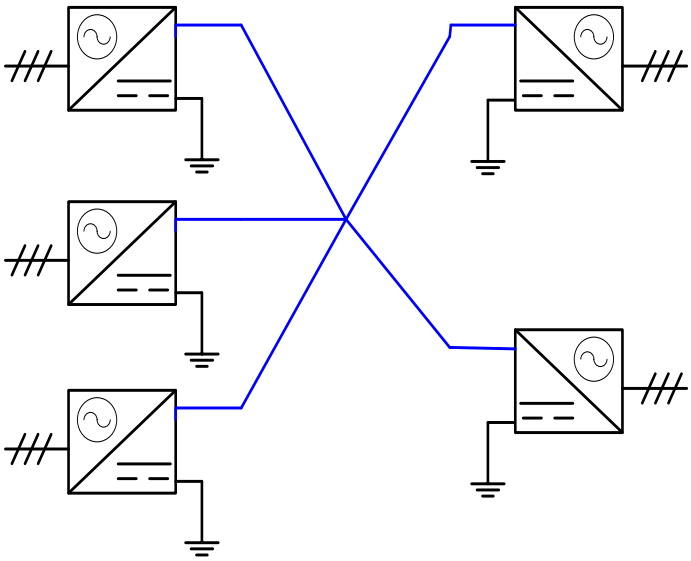


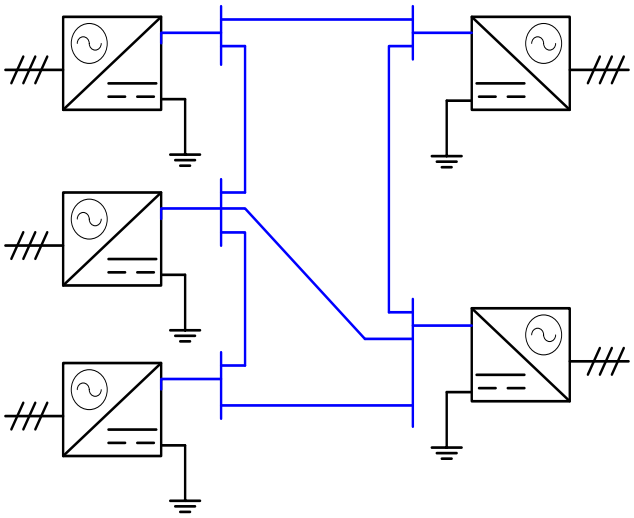
Figure 2.18: Series bipolar MTDC connection.

2.4.2.2 Parallel connections

In contrast to series MTDC connections, in a parallel connected MTDC network, converters share the same DC voltage. Parallel MTDC connections can be subdivided into radial connected MTDC as in Figure 2.19(a) or meshed as in Figure 2.19(b). In radial connections, the outage of one DC transmission line/cable section results in total service interruption for the terminal connected to it. While in meshed MTDC networks, rated operation continues but with higher transmission losses (as currents tend to take longer paths). In Table 2-2, a comparison between series and parallel MTDC network connections is illustrated [38]. Due to the advantages offered by parallel MTDC, this network configuration has been adopted in the already built projects and the upcoming futuristic and research ones.



(a)



(b)

Figure 2.19: Parallel MTDC monopolar connections a) Radial b) Meshed.

Table 2-2: Comparison between series and parallel MTDC network configurations *[83]*.

	Series MTDC network	Parallel MTDC network
Power flow reversal	In LCC based networks power flow reversal can be easily achieved by inverting the station's voltages. But in case of VSC based networks mechanical switches must be used.	In LCC based networks current direction cannot be reversed and hence power reversal can be achieved by mechanical switches. While in VSC based networks the current direction can be easily reversed and power reversal is easily achieved.
Converter station rating	Voltage rating dependant	Current rating dependant
Power losses	High losses and current must be maintained minimum to minimize the losses	Lower losses
Rated Voltage	Different voltage rating.	All converters to be rated with same voltage.
DC faults	May interrupt the whole network service	The affected terminal can be isolated and service continues.
AC faults	Leads to over voltage in terminals.	Leads to over currents in terminals.
Protection	Breakers needed	Breakers needed

2.5 Challenges for the Realisation of MTDC grids

2.5.1 DC Faults Currents

In an AC grid, during an AC fault the conventional mechanical circuit breaker has approximately 400 ms to interrupt the circuit and isolate the fault. The nature of the AC waveform and the presence of zero crossing also facilitate the circuit interruption

process as well. On the other hand, there are mainly two types of fault scenarios that can take place in the MTDC grid. The first one is faults occurring on the power electronic converter AC side, where it may be single phase or three phase. AC side faults represent loss of load or generation to the DC grid. The other type of faults scenario are faults occurring at the DC side, this type of faults are considered a real challenge to handle compared with AC faults [84] due to mainly the rate of rise of DC fault current and magnitude which need to be interrupted in less than 1 to 5 *ms* [84]–[87] as well as the absence of zero crossing (see Figure 2.20).

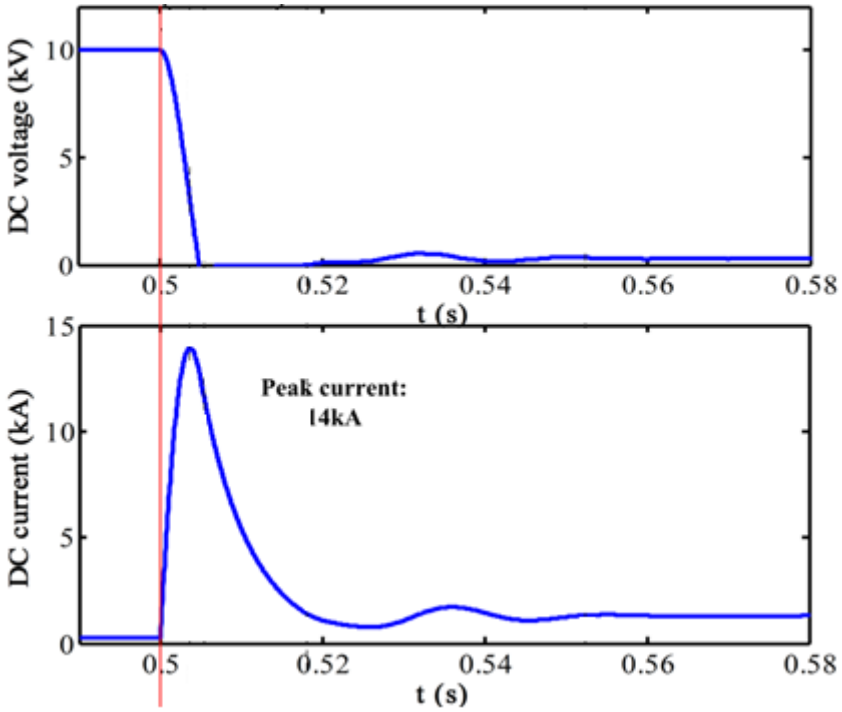
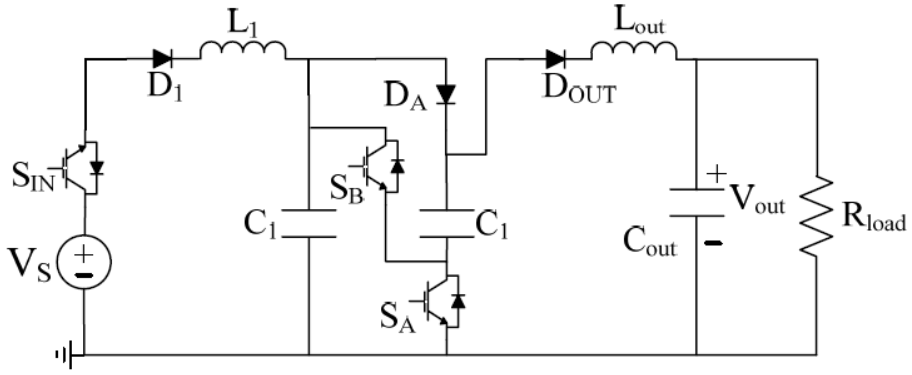


Figure 2.20: DC voltage and current rise during a fault *[88]*.

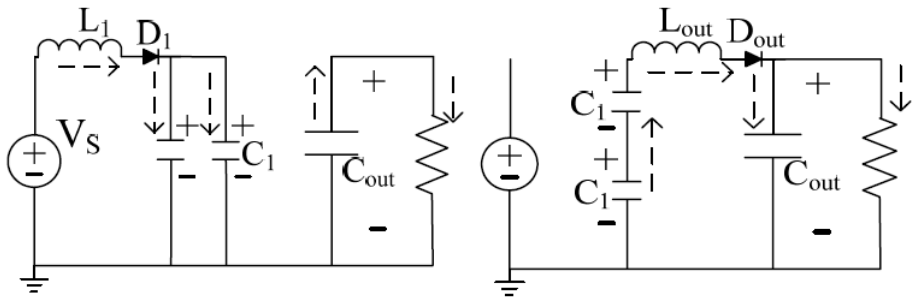
During a DC fault, all connected AC systems contribute to the fault current and because of the DC cables low impedance, the voltage in the MTDC is noticeably reduced and power flow is nearly stopped. Thus, the development of protection schemes and DC power electronic circuit breakers for HVDC grids are critical issues and many researchers have started working on solving these problems [84]–[86], [89], [90].

2.5.2 Absence of DC transformer

Another challenging matter is the absence of DC transformer for stepping the DC voltage up or down. AC transformers are tailored to the magnetic nature characteristics of AC power, and its concept of operation would immediately fail to work with DC. The only other solution is to create highly rated power electronic devices similar to the low power Buck-Boost converters. Without DC transformers or DC/DC converters, it is very difficult to adapt different voltage levels and connect various HVDC connections. A lot of research has proposed solutions and inventions to solve this problem [91]–[96]. Figure 2.21(a) shows a proposed Marx DC/DC converter topology, the idea is to switch the IGBTs to charge the capacitors in parallel as shown in Figure 2.21(b) and then connect them in series to discharge them and add up the voltage as shown in Figure 2.21(c).



(a)



(b) (c)

Figure 2.21: Marx DC/DC converter a) Circuit topology
b) Charging period c) Discharging period [95].

2.5.3 Power and current flow control

There are several established methods of controlling the power flow in AC power transmission systems leading to the concept of Flexible AC Transmission Systems (FACTS), which was introduced in the 1990s [97], [98]. FACTS theory of operation is based on the characteristics of AC real power that can be expressed in the following equation:

$$P_{AC} = \frac{V_1.V_2.\sin(\delta)}{X} \tag{2.1}$$

Where V_1 and V_2 are the sending and receiving end R.M.S. voltages, δ is the power angle and X is the line impedance as shown in Figure 2.22(a). Power flow control can be achieved through varying the line impedance by a number of techniques. However in DC systems, DC power flow is determined by the line resistance according to equation 2.

$$P_{DC} = \frac{V_1.\Delta V}{R} \tag{2.2}$$

Where V_1 is the sending end DC voltage, ΔV is the potential difference between the sending and the receiving end and R is the total resistance of the line as shown in Figure 2.22(b).

Current flow control can be obtained by either introducing new resistances to the subject network, or by injecting series voltage to act as a positive or negative resistance. In the following chapter, several available current (power) flow control methods are discussed.

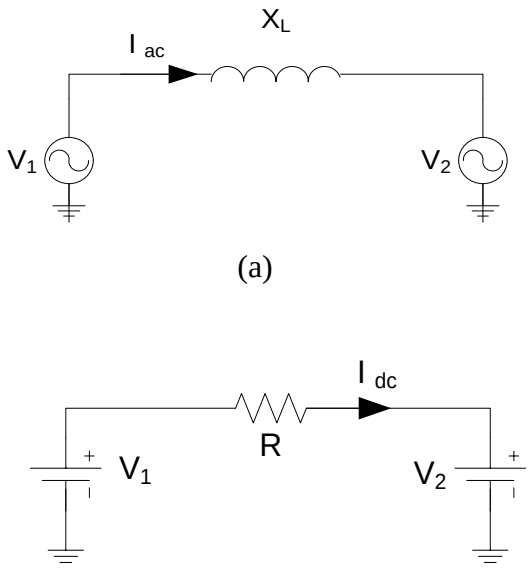


Figure 2.22: Basic electrical connection. a) AC circuit b) DC circuit.

2.6 Summary

This chapter reviews HVDC technology and all its important aspects. Reasons that made HVDC convenient choice for interconnecting remote renewable energy resources to the grid are discussed. Available current and voltage source AC/DC converter topologies are demonstrated and a comparison is carried out to point out technical differences between them. In addition, all possible HVDC point to point and multi terminal network configurations are illustrated and compared. Finally, challenges preventing the realisation of MTDC grids are discussed.

Chapter

3

Current and Power Flow Control in DC grids

3.1 Introduction

As discussed earlier in the last section of the previous chapter, absence of reliable current flow control method in high voltage MTDC grids is an obstacle preventing practical implementation of such grids. Current control is important for the following reasons:

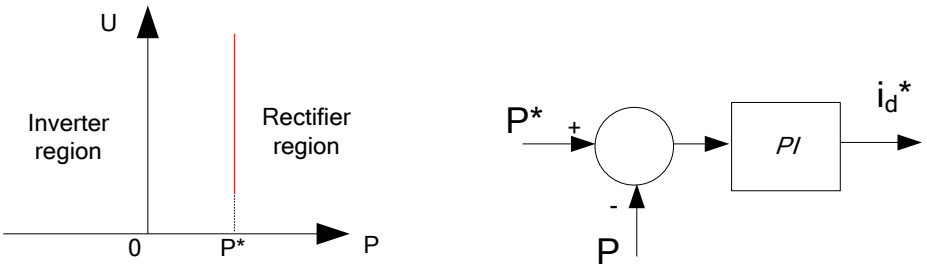
- To prevent the overloading of cables and overhead lines. More currents tend to flow in paths with less resistance, and if not controlled, cables may get overloaded and overheat and may be subject to permanent damage.
- Control of the currents flowing can also be beneficial from the perspective of maintenance of cables (lines), where for any given cable, if the current can be ramped down to zero, it can be easily disconnected using low cost offload disconnector switches and then easily isolated for maintenance.
- To control current/power flowing in different paths based on dispatch centre orders.

In this chapter, published current (and power) control methods for HVDC and MTDC grids are explained.

3.2 Voltage Margin Control

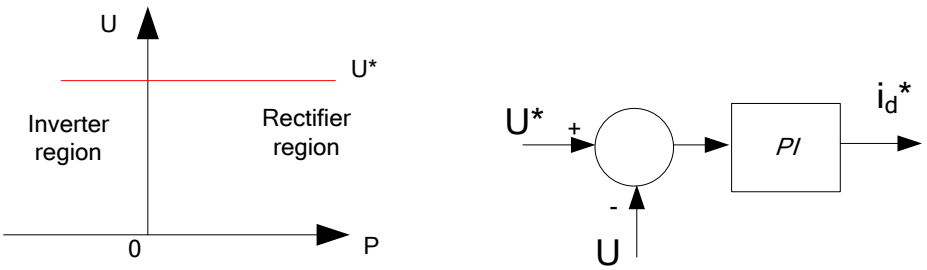
A DC voltage margin control scheme [99]–[101] is aimed to reduce communication burdens. The concept is based on assigning a grid connected terminal (VSC) to regulate and control the DC voltage and the rest of the terminals to their own local power references. Figure 3.1(a) shows DC voltage versus power characteristics for a given VSC DC terminal operating in constant power mode. In this mode, the DC terminal regulates the power only. The control circuit for this case is shown in Figure 3.1(b) where the reference signal is compared with the DC signal and the resultant error passes through a PI controller to result in the d-axis component control reference current. While Figure 3.2(a) shows DC voltage versus power

characteristics for a given VSC DC terminal operating in constant voltage mode, where in this mode a DC terminal is deployed to keep the voltage constant, the corresponding control circuit in this case is shown in Figure 3.2(b). In a given MT-HVDC grid, wind generating terminals have the freedom to generate and track maximum available power depending on wind speed, while the grid connected VSC stations are set to control active power and DC voltage. A case is shown in Figure 3.3 were a voltage margin control strategy is proposed for three grid connected VSCs in a MTDC grid that contains in addition several wind farms connected VSC stations. Terminal 2 controls the voltage across the DC grid and other terminals provide redundant operation and can detect the DC voltage variations in case of loss of terminal 2 for any reason and hence take the voltage regulator role to maintain the DC voltage stability within the grid.



(a) (b)

Figure 3.1: Operation in constant power mode a) DC terminal voltage Vs power.



(a) (b)

Figure 3.2: Operation in constant voltage mode a) DC terminal voltage Vs power characteristics. (b) Controller schematic.

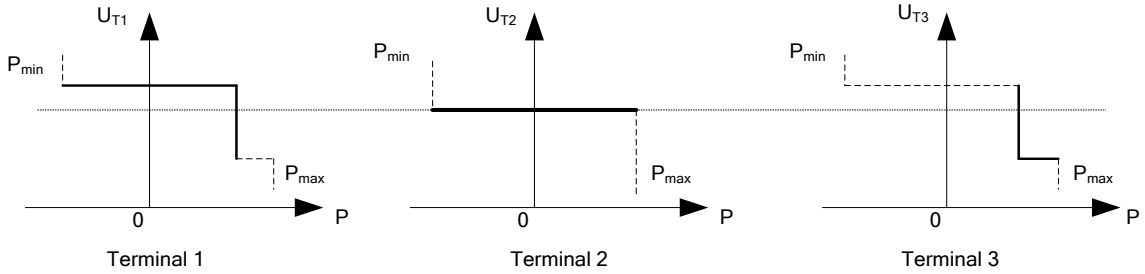
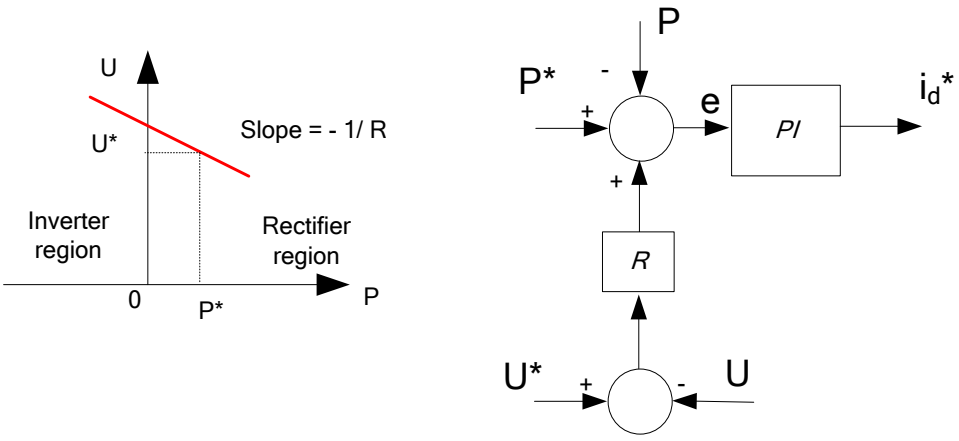


Figure 3.3: DC terminal voltage Vs power characteristics of a three terminals grid with voltage margin control.

However, the voltage margin control scheme has its problems; as it causes increased power variation on both AC and DC sides, increased voltage stresses and DC over voltages. This is due to the fact that one terminal is assigned to balance the power for the whole grid, which is not desirable from a power security point of view.

3.3 Voltage Droop control

The voltage droop control is a combination of voltage control and power control regulator circuits shown earlier in Figure 3.1 and Figure 3.2 [102]–[106]. Figure 3.4(a) shows that the droop controller tends to control power to its reference level and at the same time contributing to the DC voltage control. As these two actions are contradictory, one action happens at the cost of the other and vice versa. The power can be controlled through this process. Figure 3.4(b) shows the droop controller achieved by combining both regulators of voltage and power shown earlier in Figure 3.1(b) and Figure 3.2(b), respectively.



(a) (b)

Figure 3.4: voltage droop control a) DC terminal voltage Vs power characteristics. b) Controller schematic.

Equation 3.1 shows the relationship between the DC voltage response *R* and the droop constant ρ_{DC}, which is responsible for power balancing:

$$R = \frac{P_{rated}}{\rho_{DC} \cdot U_{rated}} \tag{3.1}$$

Where P_{Rated} and U_{Rated} refer to rated power and rated DC voltage of the DC terminal, respectively.

The error can be calculated from the following equation 3.2:

$$e = P^* - P + R\,(U^* - U) \tag{3.2}$$

Where e is the error signal of the voltage droop controller and *P** and *U** are the power and voltage references, respectively (Figure 3.4 (b)).

At steady state, the relation between DC voltage and converter power is the following:

$$U = U^* + \frac{(P^* - P)}{R} \tag{3.3}$$

The droop constant determines the slope in the relationship between the voltage and the power [103]. However, the main disadvantage of DC voltage droop control is that in order to achieve multiple control tasks, the droop characteristics may be very complex as shown in [24]. Also, droop characteristics are related to grid parameters such as cable resistances, leading to further adjustments over time.

3.4 Current control using series resistors

Controlling the current flow using series resistors and switches has been considered [107]–[109]. From Ohm's Law, by varying the transmission cables (lines) resistances, desired current flow control can be achieved (see Figure 3.5). The major disadvantage is the additional power losses that occur by the inserted series resistors as described by equation (3.4).

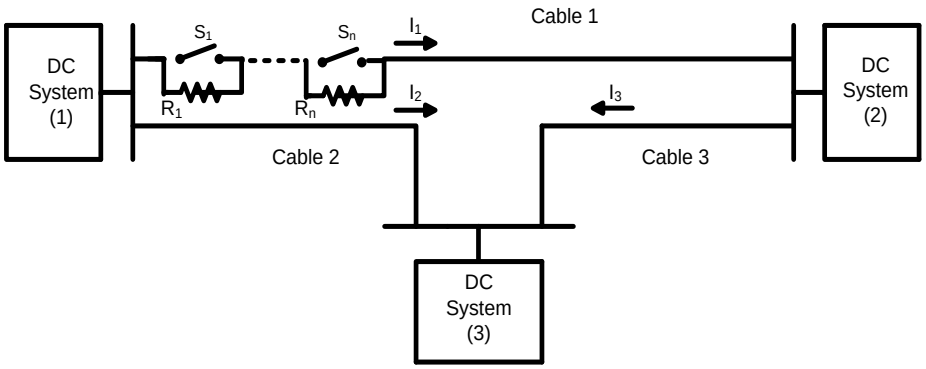


Figure 3.5: Switching series resistors.

$$P_{loss} = I^2 * R \tag{3.4}$$

$$P = (V_A - V_B) * \frac{V_B}{R} \tag{3.5}$$

Equation (3.5) shows that with the variation of the value of *R*, current (power) flow can be achieved. Mechanical switches would offer slow switching operation with low switching losses while electronic switches would offer very fast switching with high switching losses. Resistors can be set into a configuration similar to the binary configuration to achieve more flexible values of resistances with fewer resistors. This method is practical and easy to implement with simple control. However, the power loss in the resistors introduced is very high compared to the line losses; thus, this method is not economical. In addition, the additional losses cause heating which may require cooling systems, leading to additional costs.

3.5 Current control by injection of series voltage

3.5.1 Controlled series voltage sources

Another proposed approach to control the current flowing in a DC circuit is to introduce a DC voltage source in series with any cable [91], [107]–[113]. The concept is to alter the magnitude and direction of the series voltage which influences the flowing current and thus current flow control can be achieved. This can be achieved by inserting a controlled voltage source in series that would be either acting as additional positive resistance or negative resistance based upon the voltage source polarity (See Figure 3.6). This concept is evaluated using MATLAB/SIMULINK computer simulation, where it is assumed that cables 1 and 2 (Figure 3.6) are carrying currents with values 1150A and 840 A, respectively, and it is required to equally redistribute both currents to prevent cable 2 from overloading. A proportional – integral (PI) controller is designed to fulfill this purpose as shown in Figure 3.7, where currents i_1 and i_2 are compared and the output error signal is fed

to a PI controller, which provides the two voltage sources with the required voltage set point to balance the currents as shown in Figure 3.8.

This method is easy to implement in low voltage applications, where controlled DC voltages can be built easily, but in HVDC grids it is not possible to apply it in this simple manner.

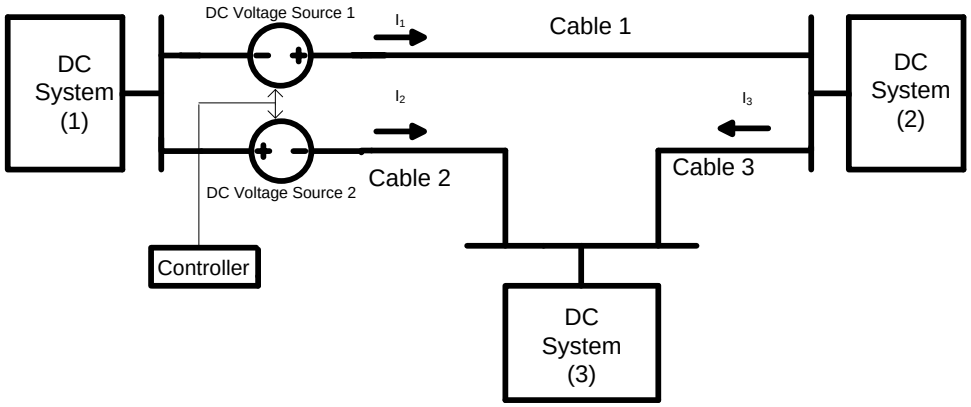


Figure 3.6: Controlled series voltage sources.

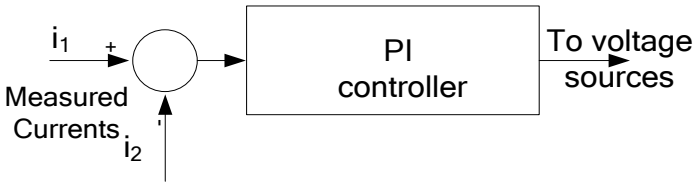


Figure 3.7: Proposed voltage sources controller.

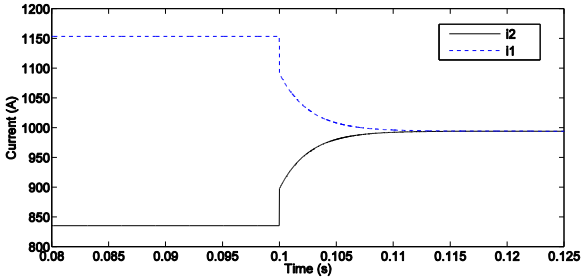


Figure 3.8: Balancing of currents i1 and i2 using series DC voltage sources.

3.5.2 Series DC/DC converters

One way to implement the series voltage injection is to use DC/DC converters as proposed in [91], [107], [113]. The converter is inserted in series as shown in Figure 3.9. To achieve precise current control in several cables, a DC/DC converter is needed for each cable which is a noticeable draw back for this method. Moreover, the presence of inductors and high voltage switches increases the cost, size and complexity [91], [107] , making this a difficult solution for current flow control in offshore applications where size and cost are critical.

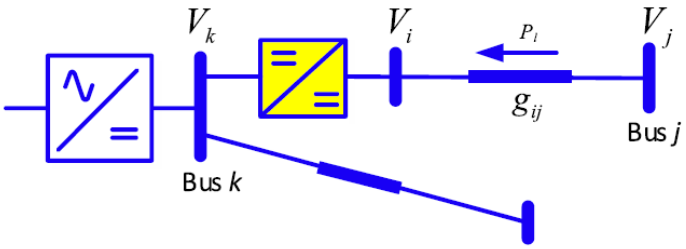


Figure 3.9: DC/DC converter inserted in series to a DC cable *[113]*.

3.5.3 AC/DC converters

Another method to implement the series voltage injection is to use AC/DC converters. (See Figure 3.10). The converters can be supplied by three phase AC voltage through the nearest terminal by stepping down the voltage to the desired level. An IGBT based three-level PWM voltage source converter is used as a current flow controller. Two converters are inserted in the two cables in a network similar to that example shown earlier in Figure 3.6. The controller of the converter is supplied with reference DC voltage; this set point is determined by a PI controller that minimizes the error signal of both currents (Figure 3.11).

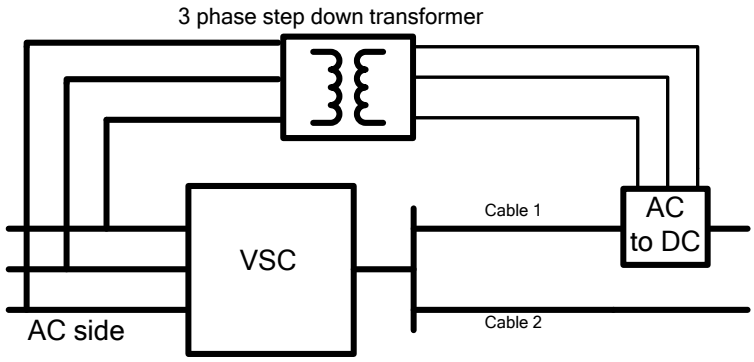


Figure 3.10: AC/DC converter as a power flow controller.

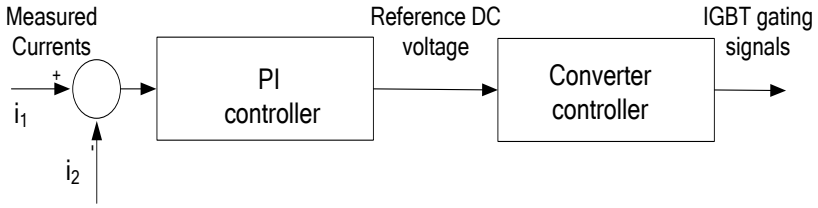
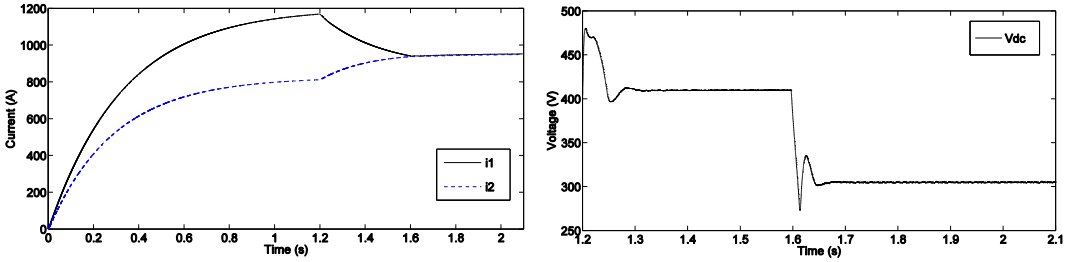


Figure 3.11: Currents balancing through AC/DC converter's control loop.

Converters can be set to limit the current to a required value or to balance the currents as mentioned earlier. Figure 3.12(a) shows a simulated case study where currents i_1 and i_2 are equal to 1180A and 780A respectively, currents are balanced by switching in two series AC/DC converters with the two cables at t= 1.2 s, one converter adds series voltage (see Figure 3.12(b)) and the other subtracts from the cable to achieve the requested set point. The control signal and converters AC side voltage are presented in Figure 3.13 and Figure 3.14, respectively. Similarly, a single AC/DC converter can be used to perform current control with desired set points within any chosen cable as illustrated in Figure 3.15.

The noticeable disadvantage is that stepping the HVAC down from hundreds of *kVs* to few *kVs* to supply the converter requires a relatively bulky, high cost three phase

AC transformer in addition to the AC/DC converter cost and size, which may not be suitable specially in offshore installations.



(a) (b)

Figure 3.12: a) Balancing i_1 and i_2 using two AC/DC converters.
(b) DC voltage added to the grid by converter.

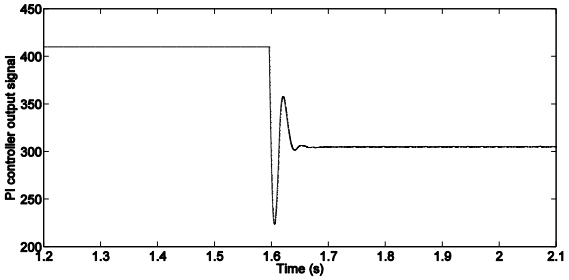


Figure 3.13: PI controller output signal.

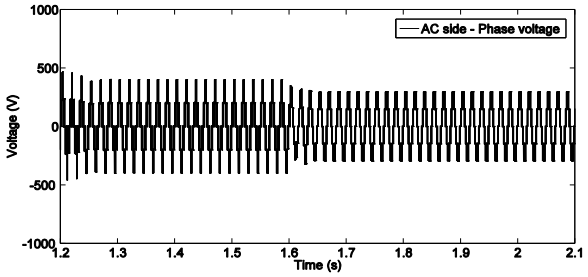
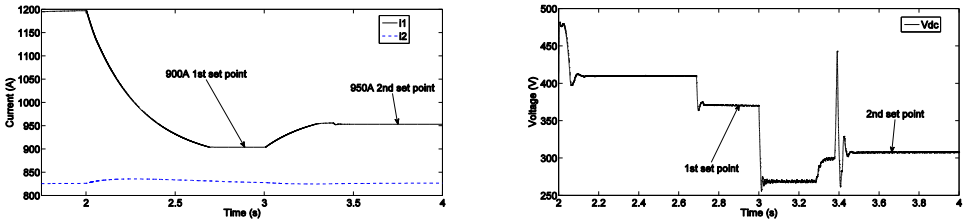


Figure 3.14: Phase to Phase voltage VAB at the AC side of the converter.



(a) (b)

Figure 3.15: a) i1 is set to 900A and 950A using single AC/DC converter.

b) DC voltage added to the grid by converter.

3.6 The Current flow controller

A new power electronics device, termed the Current Flow Controller (CFC), which consists of two full bridge converter modules each connected in series with one of the two cables to be controlled as in Figure 3.16, was introduced by Barker in [109]. The principle is based on transferring energy from one line/cable to the other. This is achieved by charging the cell capacitors from the line carrying the higher current and discharging them into the other line. This effectively adds a voltage to the line with the required polarity and magnitude to increase or decrease the current. This current control method seems to be more practical and promising when compared to

the methods reviewed in the foregoing sections. The CFC has numerous advantages such as:

- Provides precise performance in current flow control and limiting applications.
- Consists of IGBTs and capacitors with low voltage ratings.

The CFC is patented by Alstom, a power system industry leader, and only patent application [114] is available which contains limited information. Therefore, it was concluded that the CFC constitute a worthy research topic. The rest of the thesis is devoted to report the studies carried out to fully develop the concept of CFC for application to a real meshed MTDC grid. The studies were carried out by analysis, simulations using MATLAB/SIMULINK, PSCAD/EMTDC and experimental work.

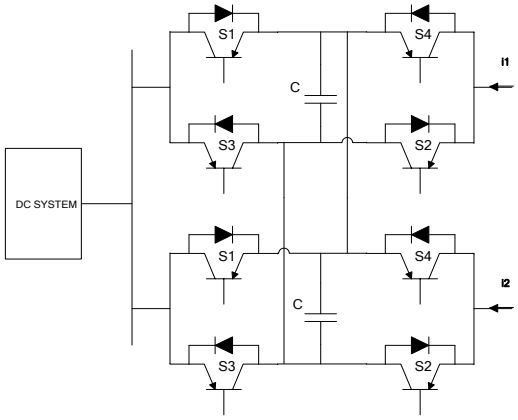


Figure 3.16: Current Flow Controller [13].

3.7 Summary

Current (power) flow control methods in HVDC grids can be divided into two main groups. The first are VSC based methods such as voltage margin control and voltage droop control. The second group is based on achieving the control by introducing new equipment to the grid such as series resistors, series voltage sources or the current flow controller. All the mentioned current and power control methods are

discussed in details in this chapter. Detailed investigation of the operation, control and dynamic modelling of the current flow controller through computer simulation is demonstrated in Chapter four. New generalized and reduced topologies are also discussed in Chapter five. Experimental validation through lower power prototype is carried out and results are presented in Chapter six.

Chapter

4

Proposed Operation and Control for the Current Flow Controller

4.1 Introduction

In this chapter, the CFC topology is discussed in detail along with its principle of operation and possible functionalities. Moreover, the proposed modes of operation are presented and explained and a dynamic mathematical model is developed. Two different control strategies, PID and Hysteresis Current Control (HCC), are proposed to achieve different functionalities. As grid loading may change suddenly, which may require the CFC to operate in a different mode, an automatic mode detection and changing algorithm is developed to allow autonomous operation of the CFC to maintain achieving the desired function even under sudden load changes.

In addition, to allow the CFC to have three ports and be able to control three cable currents, an extended topology is proposed along with its operating modes, mathematical model and control strategies.

Finally, computer simulation for two-port and an extended three-port CFC is carried out to validate the proposed operating modes, mathematical model, control schemes, and the automatic mode detection unit and results are presented at the last section of this chapter.

4.2 Topology

The current flow controller is a power electronic device made of two full bridge IGBT modules each with its own cell capacitor. In its preliminary topology, each module of the CFC is connected in series with a cable to be controlled, and the two cell capacitors are connected in parallel as shown in Figure 4.1. Another approach is to build the CFC using separate eight IGBT switches each with its own anti-parallel freewheeling diode, and to substitute both parallel cell capacitors with one single main capacitor. The single capacitor gives more flexibility in measurements and monitoring tasks as illustrated in Figure 4.2.

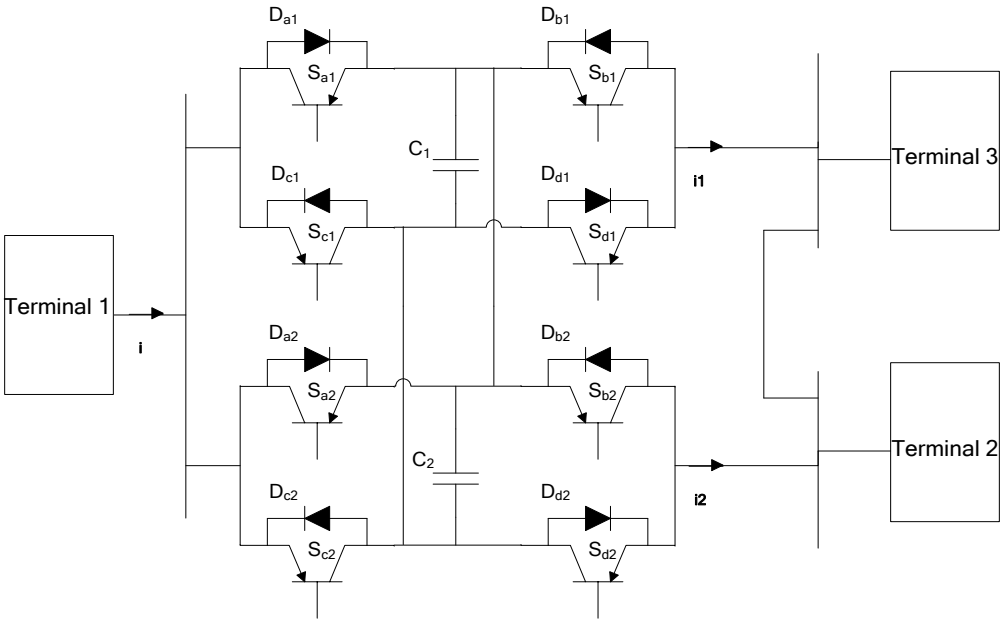


Figure 4.1 Current flow controller preliminary topology.

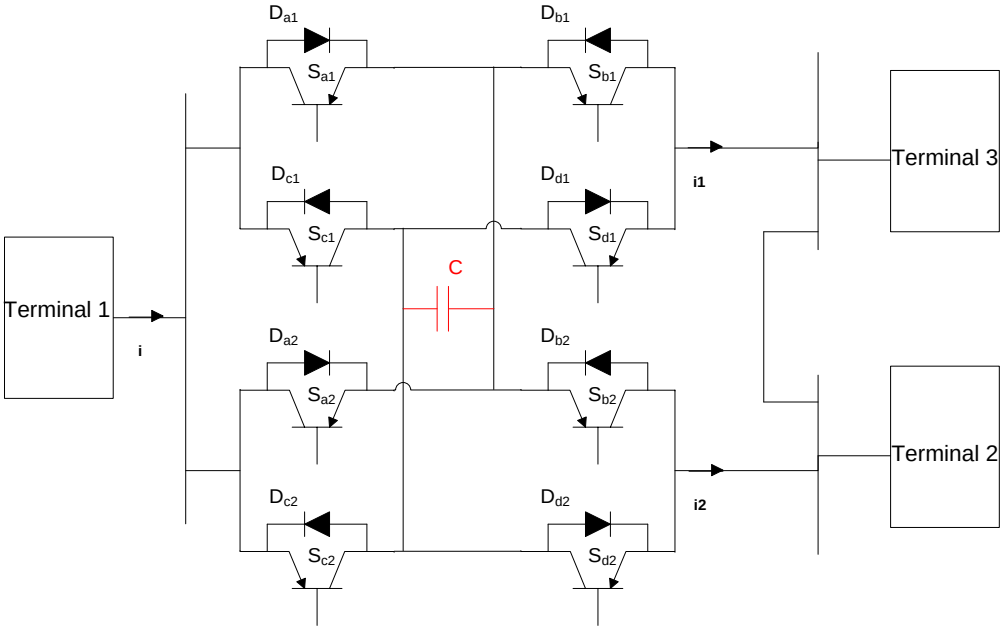


Figure 4.2 Current flow controller with single capacitor.

4.3 Operating principle

The current flow controller can be installed in series at any given terminal in a three terminals meshed MTDC grid (see Figure 4.3). This fact gives the CFC a unique advantage as it is isolated from the ground of the system and from the potential of the cables; hence, relatively low voltage rating IGBTs are needed when compared to the DC grid rated voltage. Each group of four IGBTs are inserted in series with each cable and a capacitor is connected between both cables, and the aim is to switch the capacitor in series to charge from the cable carrying higher current and discharge in the other cable and introduce to it series controlled DC voltage. This process can be controlled by appropriate IGBT gating signals in order to achieve the desired operation, whether it is currents balancing in both cables, setting a current to any desired value or even nulling a current to zero. The speed and duration of switching the capacitor to charge/discharge from a cable depends on the set reference value and is determined by the controller as discussed later in the control strategies section.

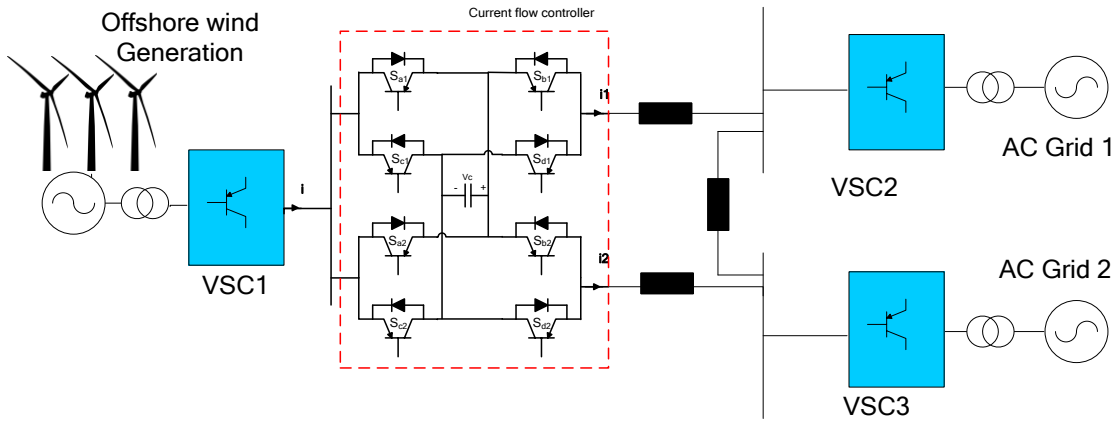


Figure 4.3 CFC inserted in series in a three terminals MTDC grid.

In theory, the CFC introduces no power losses as the net amount of active power taken from one cable is transferred to the other. In practice, IGBT switching causes switching losses, which are still acceptable. The CFC offers several advantages that can be summarized as follows:

- Simple construction with small footprint, facilitating its utilization in offshore purposes where cost and size are critical.
- Low production cost, as it is installed in series and in cable potential, this means that relatively low voltage (typically few *kV* rated) IGBTs and capacitor are needed with very low cost.
- As a result of incorporating low voltage rated IGBTs, the CFC offers much lower switching losses when compared to other available solutions such as AC/DC converters and DC/DC converters. This is due to the fact that switching losses depend mainly on the operating voltage, current and switching frequency of the IGBT.
- Gives full controllability to cable currents, allowing the redistribution of flowing currents for cables overloading prevention.
- Ability to null a current flowing in a certain cable, which may be useful in cases of maintenances where only offload disconnector switches are required to isolate the cable. At the same time, the service is not interrupted as the power is transferred through the other cable.
- If sized adequately, the capacitor can be of low cost as well as the IGBTs as it is not subjected to high voltage and its cost most probably functions in its capacitance.

4.4 Modes of operation

As the CFC is controlling two cables (currents) only, there are four modes of operation for the CFC. Firstly, two forward modes when currents are flowing in the forward direction out of the CFC (one for $i_1 > i_2$ and the other is for $i_2 > i_1$), and two reverse modes when currents are flowing in the opposite direction into the CFC (one

for $i_1 > i_2$ and the other is for $i_2 > i_1$). In the following subsection, operation of all possible modes is discussed in detail.

4.4.1 Operation in forward direction

4.4.1.1 Mode 1: $i_1 > i_2$

The first mode begins with a charging period when i_1 is the higher current, IGBT S_{b2} is switched on to allow current i_2 to flow through D_{a2} and S_{b2} in cable 2, and at the same time to connect the CFC's capacitor in series with cable 1 through D_{a1} and D_{d1} to charge from it as shown in Figure 4.4(a).

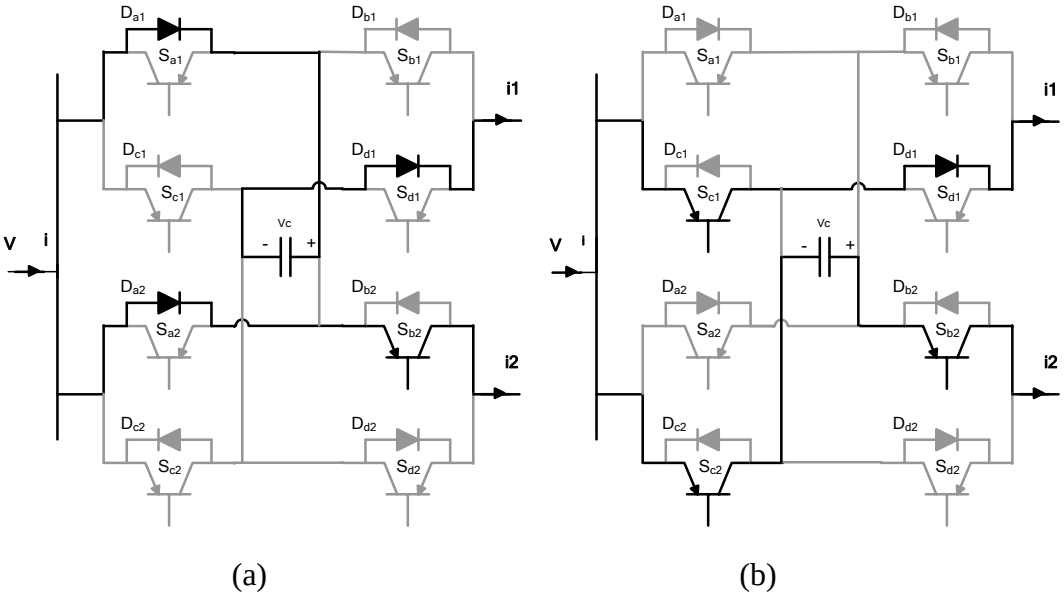
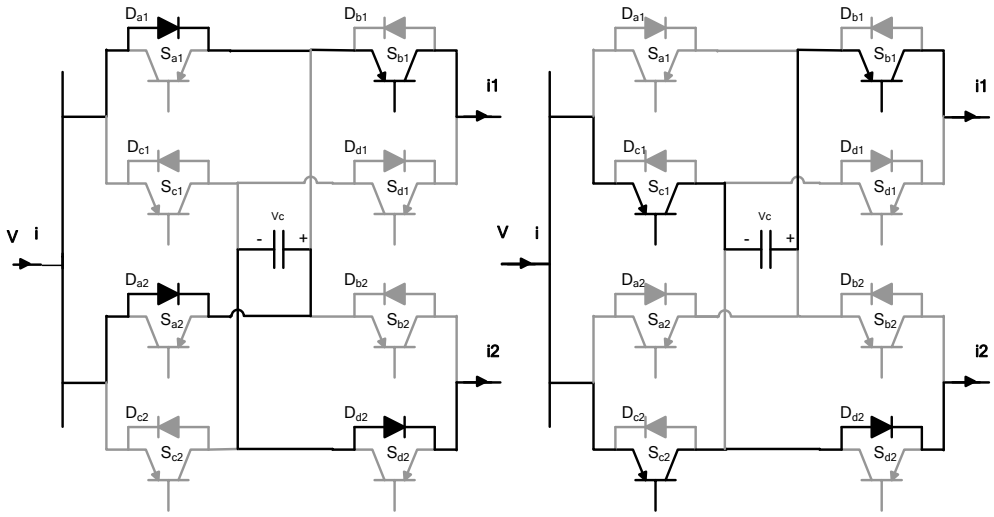


Figure 4.4 CFC operating in mode 1. (a) Charging from cable 1.
(a) Discharging in cable 2.

This is followed by a discharge period where switches S_{c1} and S_{c2} are turned on to allow the current i_1 to flow in cable 1 through both S_{c1} and D_{d1} and at the same time connect the capacitor in series in cable 2 for discharging through S_{c2} and S_{b2} as shown in Figure 4.4(b).

4.4.1.2 Mode 2: $i_2 > i_1$

Similar to mode 1, mode 2 is when current i_2 is higher than current i_1, the operation is identical but S_{b1} switched on instead of S_{b2} as shown in Figure 4.5(a) for charging period and Figure 4.5(b) for discharging period.



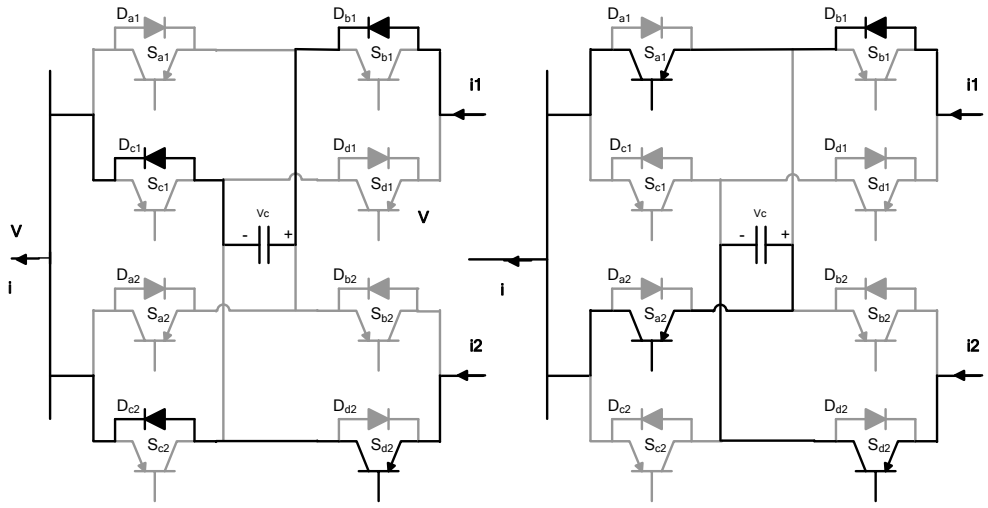
(a) (b)

Figure 4.5 CFC operating in mode 2. (a) Charging from cable 2. (b) Discharging in cable 1.

4.4.2 Operation in reverse direction

4.4.2.1 Mode 3: $i_1 > i_2$

The third mode of operation starts with a charging period when i_1 is the higher current, and both currents are flowing into the CFC. IGBT S_{d2} is switched on to allow current i_2 to flow through D_{c2} and S_{d2} in cable 2, and at the same time to connect the CFC's capacitor in series with cable 1 through D_{c1} and D_{b1} to charge from it as shown in Figure 4.6(a).



(a) (b)

Figure 4.6 CFC operating in mode 3 (reverse). (a) Charging from cable 1. (b) Discharging in cable 2.

This process is followed by a discharge period where switches S_{a1} and S_{a2} are turned on to allow the current i_1 to flow in cable 1 through both S_{a1} and D_{b1} and at the same time connect the capacitor in series in cable 2 for discharging through S_{a2} and S_{d2} as shown in Figure 4.6(b).

4.4.2.2 Mode 4: $i_2 > i_1$

The fourth and last mode of operation is similar to mode 3, where current i_2 is higher than current i_1, the operation is identical but S_{d1} switched on instead of S_{d2} as shown in Figure 4.7(a) for charging period and Figure 4.7(b) for discharging period.

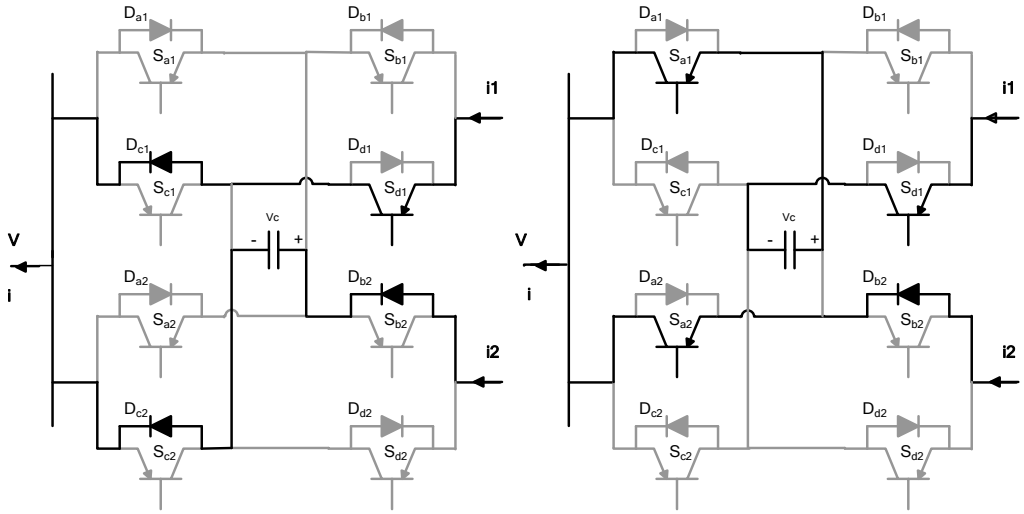


Figure 4.7 CFC operating in mode 4 (reverse). (a) Charging from cable 2. (b) Discharging in cable 1.

All four modes of operation and switching stated of all IGBTs are summarized in*Table 4-1 CFC modes of operation and their relevant switching states.*.

Table 4-1 CFC modes of operation and their relevant switching states.

Mode	Higher Currents	Current Direction	Switching states							
			S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	S_{d1}	S_{d2}
1	i_1	Forward	off	off	off	on	PWM	PWM	off	off
2	i_2	Forward	off	off	on	off	PWM	PWM	off	off
3	i_1	Reverse	PWM	PWM	off	off	off	off	off	on
4	i_2	Reverse	PWM	PWM	off	off	off	off	on	off

All schematic diagrams for the four operating modes are presented in Appendix A.1

4.5 Dynamic modelling

To evaluate the performance of the CFC mathematically, a dynamic model is derived using averaging technique. CFC operation in mode 1 illustrated earlier in Figure 4.4 is considered where cable current i_1 is higher than i_2 and the capacitor is charging from cable 1. The following set of equations describes the circuit presented in Figure 4.8 where the capacitor is charging from the line carrying the higher current, i_1.

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + v_c + V_1 \tag{4.1}$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + V_2 \tag{4.2}$$

$$i_1 = C \frac{dv_c}{dt} \tag{4.3}$$

where r_1 and L_1 are the series resistance and inductance of the first cable, $r_2$and L_2 are the series resistance and inductance of the second cable, v_c is the capacitor voltage, V is the voltage at the bus where the CFC is connected to, V_1 and V_2 are the voltages at the end terminals of the first and second lines, respectively.

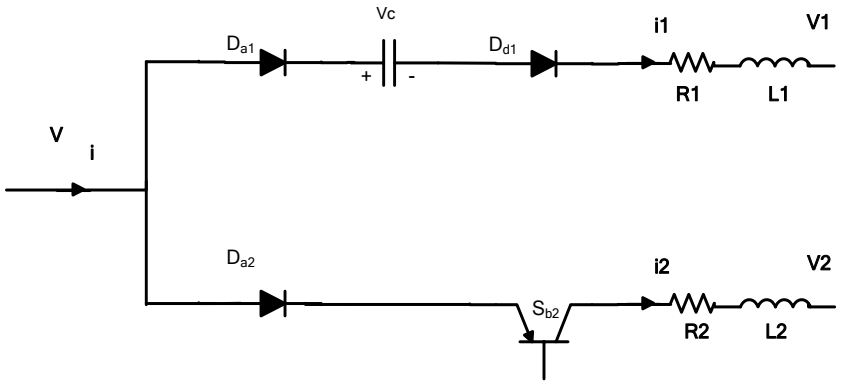


Figure 4.8 C circuit during charging period (mode 1).

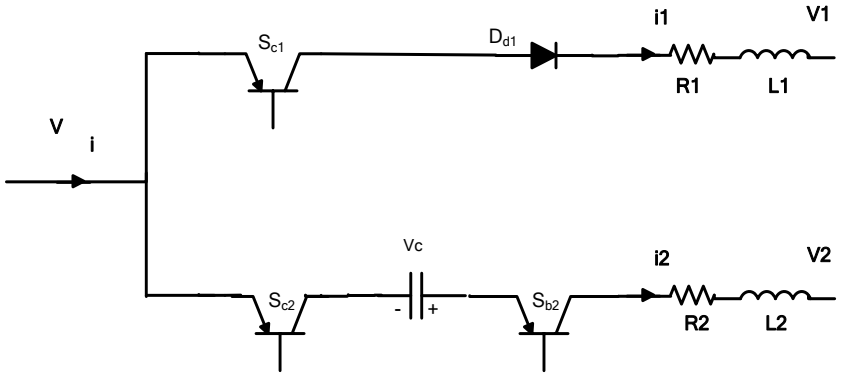


Figure 4.9 CFC circuit during discharging period (mode 1).

By defining $x^T = [i_1 \quad i_2 \quad v_c]$ as state vector, where T refers to the transpose operation, equations (4.1), (4.2), and (4.3) can be arranged in matrix form as:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & -1 \\ 0 & -r_2 & 0 \\ 1 & 0 & 0 \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B_1} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \tag{4.4}$$

Similarly, for the capacitor discharge period of mode 1 shown earlier in Figure 4.5, where the capacitor is discharging into the line carrying the lower current i_2, the equations describing the equivalent circuit shown in Figure 4.9, are as follows:

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + V_1 \tag{4.5}$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} - v_c + V_2 \tag{4.6}$$

$$i_2 = -C \frac{dv_c}{dt} \tag{4.7}$$

And hence, equations (4.5), (4.6) and (4.7) can be rearranged as:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 \\ 0 & -r_2 & 1 \\ 0 & -1 & 0 \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B_2} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \tag{4.8}$$

Assuming that the duty ratio of the charging mode of operation is D, multiplying

(4.4) and (4.8) by *D* and *(1-D)*, respectively, and adding the result to obtain the average model for the CFC when $i_1 > i_2$, results in the following:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & -D \\ 0 & -r_2 & 1-D \\ D & -1+D & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \quad (4.9)$$

Where *A=DA1+(1-D)A2* and *B=DB1+(1-D)B2*. At steady state, (4.9) is written as follows:

$$\begin{bmatrix} -r_1 & 0 & -1 \\ 0 & -r_2 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ V_c \end{bmatrix} + \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix} = 0 \quad (4.10)$$

Solving (4.10), the dc steady state value of the capacitor voltage can be expressed as follows:

$$V_c = \frac{\frac{r_2}{r_1} D(V - V_1) + (V_2 - V)(1-D)}{\frac{r_2}{r_1} D^2 + (1-D)^2} \quad (4.11)$$

Equation (4.11) gives an expression for the capacitor voltage as a function of the network parameters and the voltage drops across the cables connected to the CFC which represents the loading condition of the grid. It is worth mentioning that the rated voltage of the CFC switches, which is equal to the rated capacitor voltage, can be estimated from (4.11) as well.

In order to calculate the capacitor voltage ripple, (4.3) is integrated over the charging period as follows:

$$\int_0^{DT} i_1 \, dt = C \int_{V_{cmin}}^{V_{cmax}} v_c \quad (4.12)$$

where T refers to the switching period which is the reciprocal of the switching frequency fs. Neglecting the current ripples compared to the average value, i_1, results in linear charging of the capacitor from initial minimum voltage V_{cmin} to maximum voltage V_{cmax}. Therefore, the capacitor voltage ripple, ΔV_c can be estimated from (4.13):

$$\Delta V_c = V_{cmax} - V_{cmin} = \frac{D\, I_1}{C\, f_s} \quad (4.13)$$

Eq. (4.13) shows that increasing the capacitance reduces the capacitor voltage ripple,

as expected. As illustrated by equation (4.9), the parameters of the DC grid and loading conditions influence the line current which affects the capacitor voltage ripple. Moreover, the capacitor voltage ripple depends on the mode of operation as the charging current, which is i_1 for mode 1, changes from mode to another. For mode 1, the capacitance can be roughly estimated from (4.11) and (4.13) to meet a required percentage voltage ripple, $\Delta V_{c\,pu} = \Delta V_c / V_c$, at the extreme deviations of the line currents. Similarly, the capacitance can be calculated for each mode of operation for the CFC. Finally, the maximum value of the capacitance is considered to meet the desired level of voltage ripple for all modes of operation.

In complex MTDC grids, capacitor sizing using calculations may be very sophisticated. Hence, it is a good practice to perform detailed computer simulation to the network to obtain the CFC switches and capacitor voltage rating.

4.6 Control Strategies

A robust controller needs to be designed in order to achieve different functionalities of the CFC such as cable currents balancing, setting a current to follow a desired reference value or even damp a current in a given cable to zero. The main role of the controller is to measure cable currents and produce eight gating signals for all IGBTs to satisfy user command at any given time. Two different types of controllers are proposed and discussed in details in the following subsections.

4.6.1 PI based current control technique

The first proposed controller is based on Proportional Integral (PI) control. Cable currents are measured and supplied to the controller as an input. Based on the measured currents and the chosen user command, the firing PWM signals to relevant IGBTs are produced to achieve the desired function. For currents balancing function, the sum of currents in the two cables is calculated and then divided by 2 to obtain the average value of the desired current, i^*. This value is considered the reference value to be compared with the measured current that needs to be redistributed. The

error signal is processed using a PI controller which produces the proper duty cycle value. The duty cycle is then supplied to the PWM generator (along with user defined switching frequency) to produce gating signals to the relevant switches as shown in Figure 4.10. Similarly, the user can assign a value directly to i^* to achieve the other desired functions of current nulling or setting the current to any chosen value, as illustrated in the Figure. This value is set as the reference value for the controller and switches are controlled to let the capacitor charge from the chosen cable and discharge in the other two cables. If the reference value is set to zero, the capacitor will charge from the desired cable until it is fully charged to stop the current flow in this cable. As there are theoretically no power losses except for the switching losses of IGBTs, when the current is decreased in any cable by a certain amount, it increases by the same amount in the remaining cable. It is always important to check the capacity of these cables to prevent overloading problems.

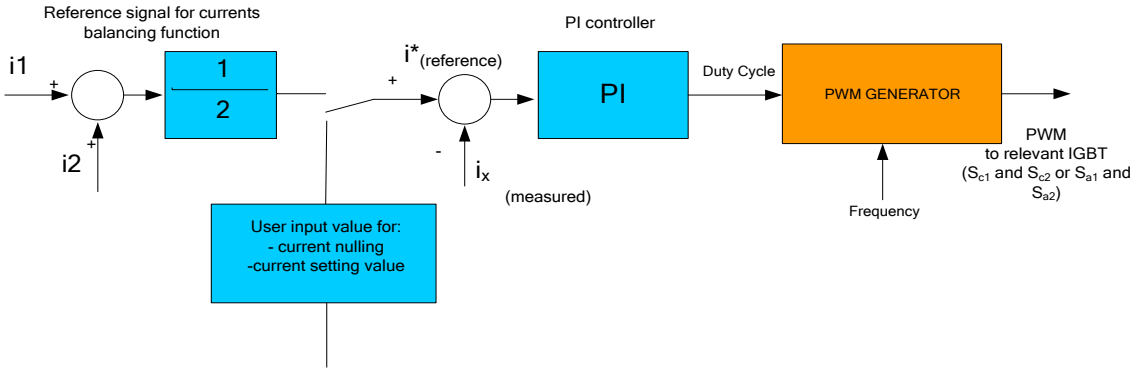


Figure 4.10 Proposed PI controller for CFC.

Furthermore, Figure 4.11 illustrates another proposed controller for the CFC not only to control the current flow, but also to regulate the capacitor voltage. The outer controller, which is the current control loop, is realized by a simple PI controller, similar to that of Figure 4.10, to process the error between the reference value i^* and the actual current i_x. The output of this outer control loop is considered the reference capacitor voltage v_c^*. A limiter can be used to prevent exceeding the

rated capacitor voltage. This reference value is then passed to the inner control loop which is dictated to regulate the capacitor voltage at its estimated value from the outer one using another PI controller. Finally, the output of this inner control loop is the duty cycle where the PWM generator operates at.

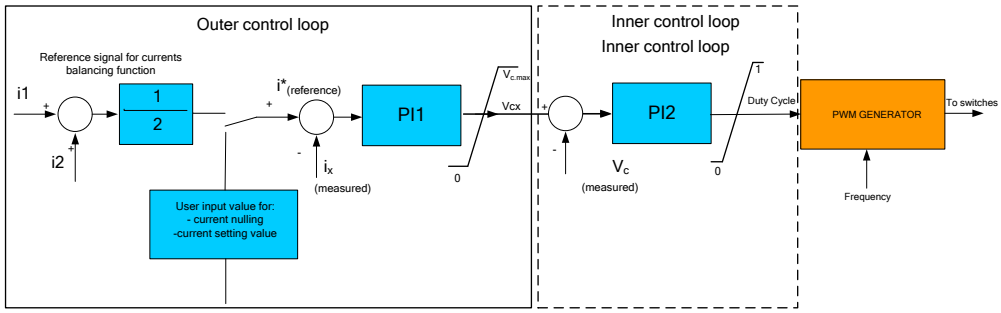


Figure 4.11 Proposed PI controller with capacitor voltage regulation.

PI controllers are very common in industry and they offer a robust, economical and reliable control solution. Such controllers offer very good dynamic performance if their proportional and integral constants are set correctly.

4.6.2 Hysteresis band current control

The second proposed CFC controller is based on a different approach, where Hysteresis Band Current Controller (HCC) is deployed instead of the PI controller as shown in Figure 4.12. It is based on the HCC technique to derive the PWM switches directly by producing either an on or off signal. In a similar manner to what have been discussed in the previous sub-section, in case of currents balancing, the average value of both currents is calculated, and the result is set as a reference value to the controller, i^*. The calculated reference value is compared with the measured actual value of the current that needs to be decreased, either i_1 or i_2. The error signal is considered as the input of the HCC as shown in Figure 4.12. The on/off states determined by the HCC are assigned to the PWM switches directly based on the current direction (forward or reverse). Considering forward currents, the HCC

initially turns-off switches S_{c1} and S_{c2} to charge the capacitor from the cable carrying the highest current. When the actual current exceeds the reference current with the user predefined hysteresis band (HB), the HCC turns-on switches S_{c1} and S_{c2} to disconnect the capacitor and allow it to discharge in the other cable. As a result, the actual current decreases to a value less than the reference current by HB and then the same process is repeated as shown in Figure 4.13. As a result, the switching frequency and accuracy depend mainly on the set value of the HB. The HB is inversely proportional with the switching frequency and the accuracy. There are many advantages of the HCC technique such as simplicity and ease of implementation. Moreover, there are no complicated tunning and parameter setting similar to that in Proportional Integral controllers (PI).

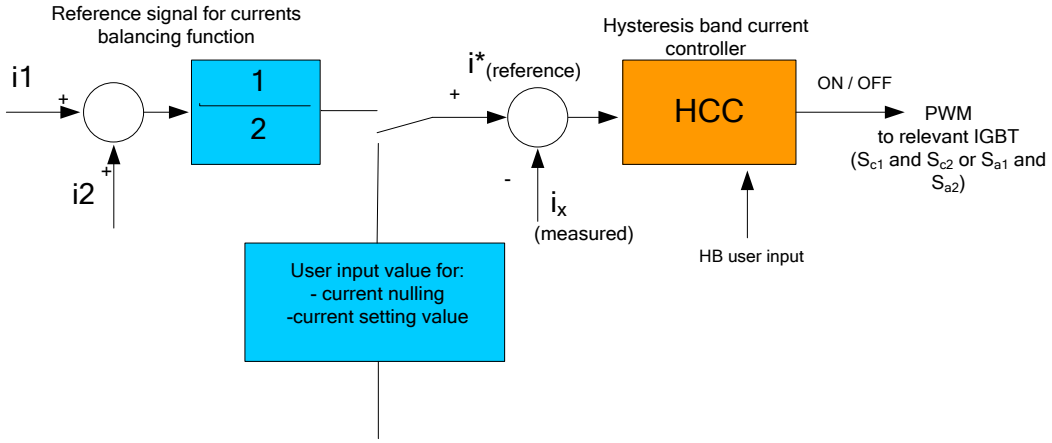


Figure 4.12 Proposed Hysteresis band current controller for CFC.

Similarly, external reference values can be applied directly to the proposed control system for cases of current nulling and current setting as explained earlier.

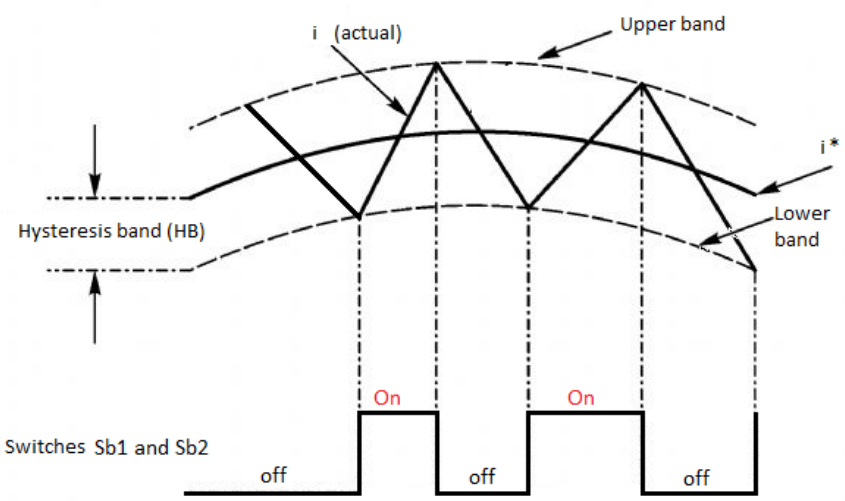


Figure 4.13 Hysteresis band current controller operation.

4.7 Automatic mode detection and change unit

For each particular mode of operation of the CFC, as explained earlier in section 4.4 and Table 4-1, some of the CFC IGBTs are switched on, others are off, while the rest are pulse width modulated. These IGBTs swap their states based on the operating mode. Therefore, a master control unit needs to be implemented to assign each IGBT its correct switching state based on the operating mode at any given time. The control unit monitors the currents directions and magnitudes; hence, it can detect the present mode of operation. Afterwards, the controller looks up Table 4-1 and decides the correct switching states for all IGBTs and also supplies the PID (or HCC) controller with the correct measured current as shown in Figure 4.14.

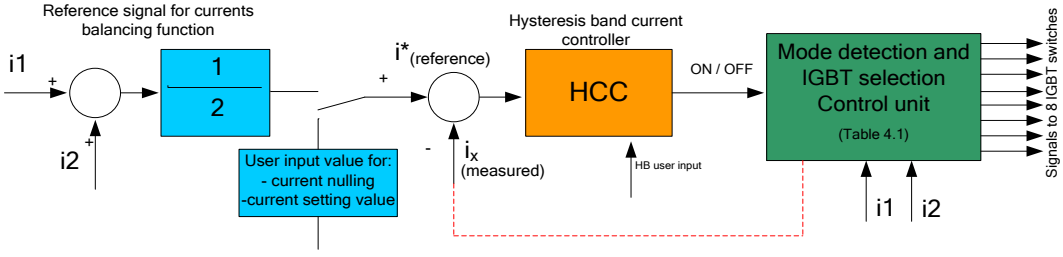


Figure 4.14 Mode detection control unit.

During the CFC operation, if any of the currents flowing are changed in the grid (whether in direction or magnitude), the operating mode may change and the CFC continues supplying the wrong IGBTs resulting in wrong switching states. To overcome this problem, the master control unit is modified to detect any change in the operating mode and accordingly change the switching state to keep the CFC user defined function maintained as it is. The developed control algorithm is based on monitoring all currents, and during operation, the operating mode must be changed if any current hits a hysteresis window centred around the average value with ± ε which is user defined. Consequently, the CFC controller is deactivated if one of the two currents hits the user defined hysteresis window, for a short time t_{off} (user defined as well), to identify the new mode precisely before reactivating once again with the new mode settings and correct switching states. The flow chart shown in Figure 4.15 demonstrates the developed control algorithm in details.

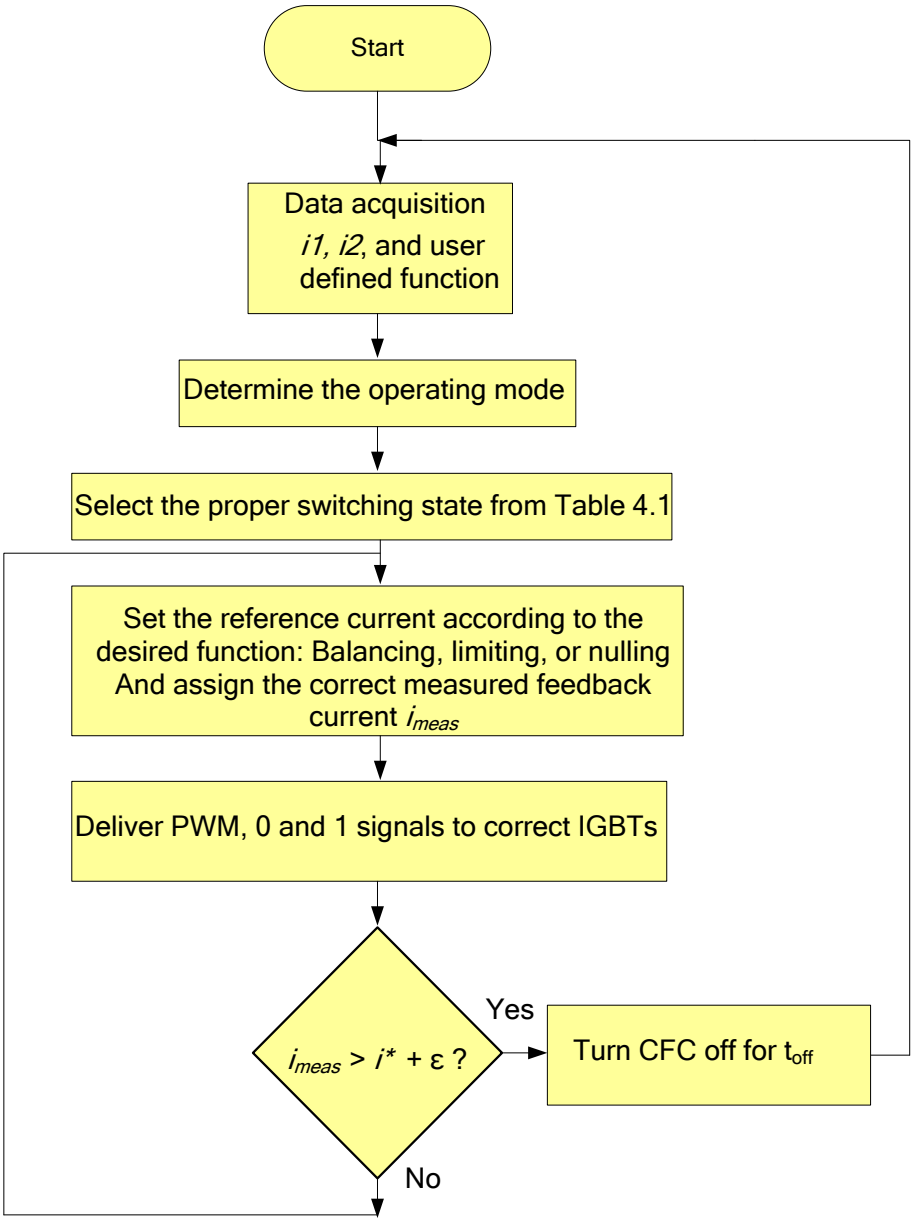


Figure 4.15 Flow chart for automatic mode detection and change algorithm.

4.8 The proposed extended CFC topology

An extended topology for the CFC is proposed, which allows the CFC to be connected to three cables simultaneously and control the currents flowing through

them. This proposed three-port CFC topology is formed by adding only four IGBTs with their anti-parallel freewheeling diodes to be connected to the third cable as shown in Figure 4.16.

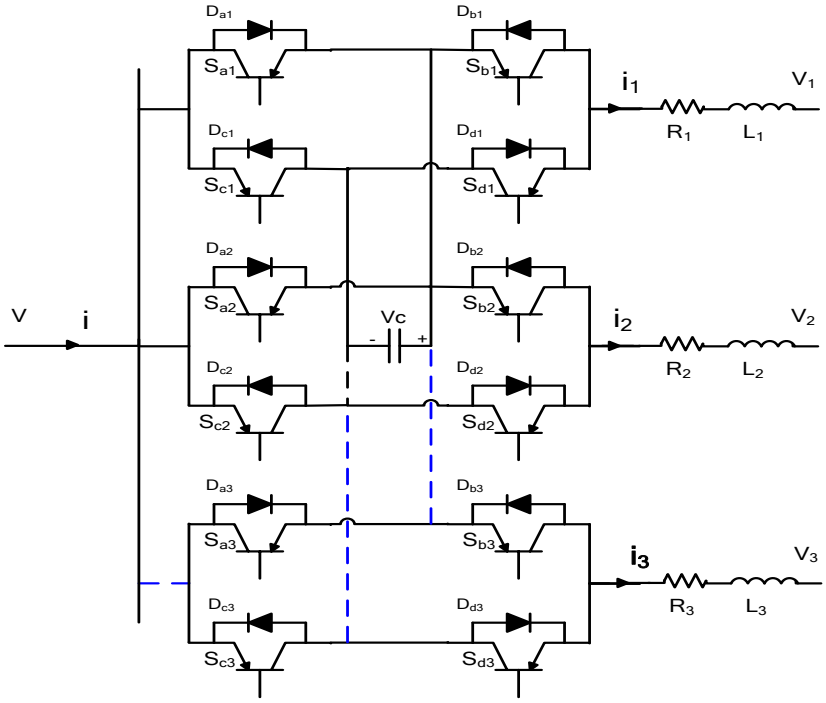
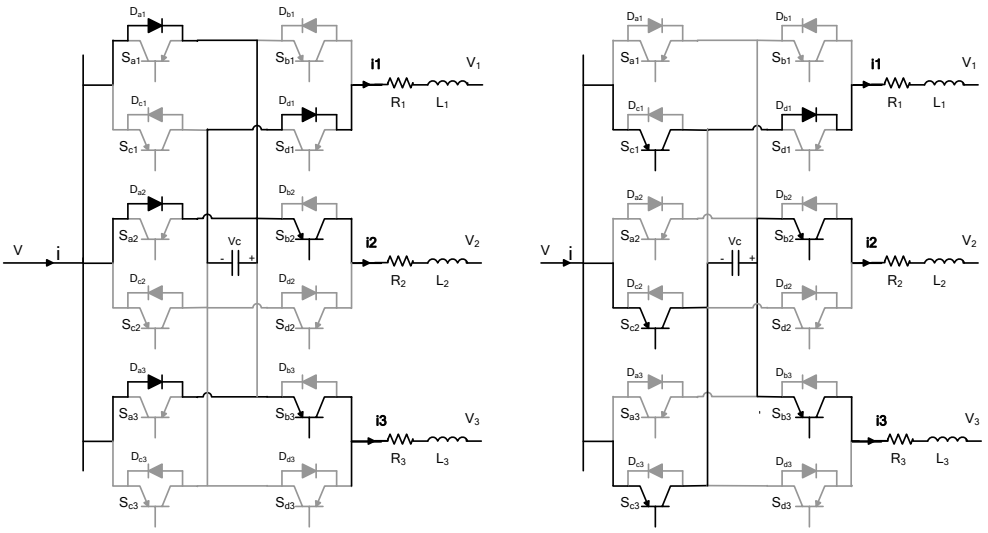


Figure 4.16 Proposed extended three-port CFC topology.

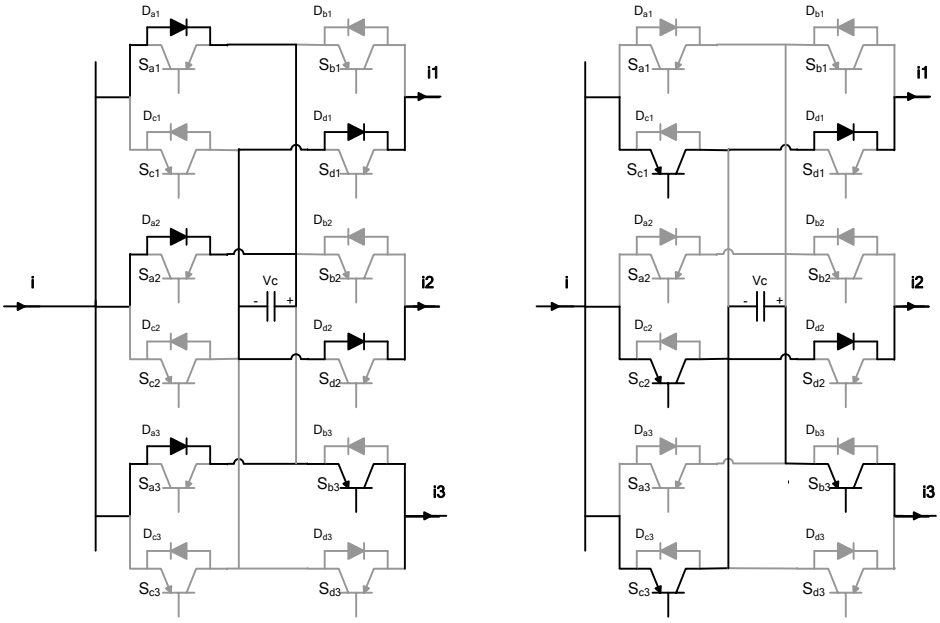
4.8.1 Modes of operation

As the topology of CFC has been extended, new modes of operation appear. The modes of operation can be grouped into six modes for forward current and another six for the reverse direction. If only one cable current is higher than it should be, the capacitor can be switched to charge from this cable and discharge in the other two carrying lower currents. An example is shown in Figure 4.17 where i_1 is the highest current (mode 1). In a similar manner, if two cables are carrying currents higher than the average value, the capacitor is switched in series with both cables in order to decrease their currents and increase the current flowing in the third cable. Figure 4.18 shows an example for this case where i_1 and i_2 are considered higher than the average value. Consequently, by considering all current combinations, there are 12 modes of operation as shown in Table 4-2.



(a) (b)

Figure 4.17 CFC extended topology mode 1 a) Charging from cable 1 (mode 1). b) Discharging in cables 2 and 3.



(a) (b)

Figure 4.18 CFC extended topology mode 4 a) Charging from cables 1 and 2, b) Discharging in cable 3.

Table 4-2 Extended three-port CFC modes of operation and their relevant switching states.

Mode	i	Direction	Switching states											
			S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	S_{c1}	S_{c2}	S_{c3}	S_{d1}	S_{d2}	S_{d3}
1	i_1	Forward	off	off	off	off	on	on	P	P	P	off	off	off
2	i_2	Forward	off	off	off	on	off	on	P	P	P	off	off	off
3	i_3	Forward	off	off	off	on	on	off	P	P	P	off	off	off
4	i_1 & i_2	Forward	off	off	off	off	off	on	P	P	P	off	off	off
5	i_2 & i_3	Forward	off	off	off	on	off	off	P	P	P	off	off	off
6	i_1 & i_3	Forward	off	off	off	off	on	off	P	P	P	off	off	off
7	i_1	Reverse	P	P	P	off	off	off	off	off	off	off	on	on
8	i_2	Reverse	P	P	P	off	off	off	off	off	off	on	off	on
9	i_3	Reverse	P	P	P	off	off	off	off	off	off	on	on	off
10	i_1 & i_2	Reverse	P	P	P	off	off	off	off	off	off	off	off	on
11	i_2 & i_3	Reverse	P	P	P	off	off	off	off	off	off	on	off	off
12	i_1 & i_3	Reverse	P	P	P	off	off	off	off	off	off	off	on	off

Where P refers to the PWM signal. All schematic diagrams for the twelve operating modes are presented in Appendix A.2

4.8.2 Dynamic modelling

The dynamic model of the two-port CFC presented earlier in section 4.5 has been expanded as well to describe the extended topology mathematically. By considering operating mode 1 shown earlier in Figure 4.17(a), where current i_1 is considered the highest current flowing and the capacitor is charging from cable 1, the following set of equations describes the circuit in this case:

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + v_c + V_1 \tag{4.13}$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + V_2 \tag{4.14}$$

$$V = r_3 i_3 + L_3 \frac{di_3}{dt} + V_3 \tag{4.15}$$

$$i_1 = C \frac{dv_c}{dt} \tag{4.16}$$

where r_x and L_x are the resistance and the inductance of the line number x originates from the CFC bus and carrying an instantaneous current i_x, v_c is the capacitor voltage, V is the voltage at the bus where the CFC is connected to, V_1, V_2 *and* V_3 are the voltages at the end terminals of the first, second, and third lines, respectively. By defining $x^T = [i_1 \quad i_2 \quad i_3 \quad v_c]$ as state vector, where the super-suffix T refers to the transpose operation, equations (4.13), (4.14), (4.15), and (4.16) can be arranged in matrix form as follows:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & L_3 & 0 \\ 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -1 \\ 0 & -r_2 & 0 & 0 \\ 0 & 0 & -r_3 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B_1} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{4.17}$$

Similarly, the equations describing Figure 4.17(b), where the capacitor is discharging into the two other lines carrying currents i_2 and i_3, are as follows:

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + V_1 \tag{4.18}$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} - v_c + V_2 \tag{4.19}$$

$$V = r_3 i_3 + L_3 \frac{di_3}{dt} - v_c + V_3 \tag{4.20}$$

$$i_2 + i_3 = -C\frac{dv_c}{dt} \tag{4.21}$$

And equations (4.18), (4.19), (4.20) and (4.21) can be arranged in the state equation:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & L_3 & 0 \\ 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & 0 \\ 0 & -r_2 & 0 & 1 \\ 0 & 0 & -r_3 & 1 \\ 0 & -1 & -1 & 0 \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_c \end{bmatrix}}_{X} +$$

$$\underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B_2} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{4.22}$$

Assume the duty ratio of the charging mode of operation is *D*. Multiplying (4.17) and (4.22) by *D* and *(1-D)*, respectively, and adding the results to obtain the average model for the CFC for mode 1 as follows:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & L_3 & 0 \\ 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -D \\ 0 & -r_2 & 0 & 1-D \\ 0 & 0 & -r_3 & 1-D \\ D & -1+D & -1+D & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_c \end{bmatrix}}_{X} +$$

$$\underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{4.23}$$

where $A=DA_1+(1-D)A_2$ and $B=DB_1+(1-D)B_2$. At steady state, (4.24) is written as follows:

$$\underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -D \\ 0 & -r_2 & 0 & 1-D \\ 0 & 0 & -r_3 & 1-D \\ D & -1+D & -1+D & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} = 0 \tag{4.25}$$

where I_1, I_2, I_3, and V_c are the steady state values of i_1, i_2, i_3, and v_c, respectively. By solving (4.26), the steady state value of capacitor voltage is obtained as follows:

$$V_c = \frac{D(V-V_1)-r_1(1-D)\{\frac{V-V_2}{r_2}+\frac{V-V_3}{r_3}\}}{D^2+r_1(\frac{1}{r_2}+\frac{1}{r_3})(1-D)^2} \tag{4.26}$$

Equation (4.26) gives an expression for the capacitor voltage as a function of the network parameters and the voltage drops across the cables connected to the CFC which represents the loading condition of the grid. It is worth mentioning that the rated voltage of the CFC switches, which is equal to the rated capacitor voltage, can be estimated from (4.26).

In order to estimate the capacitor voltage rippleΔV_c, in a similar manner to that of the two-port CFC mentioned earlier, the following equation can be used:

$$\Delta V_c = V_{cmax} - V_{cmin} = \frac{D\, I_1}{C\, f_s} \tag{4.27}$$

4.8.3 Control strategy

The control strategies presented earlier for the two-port CFC are implemented in a similar manner to the proposed extended topology, with only modifying the reference value and the table of switching states to that of the extended CFC to accommodate the new operating modes. Figure 4.19 and Figure 4.20 show both PID and HCC control schemes after modifications, respectively.

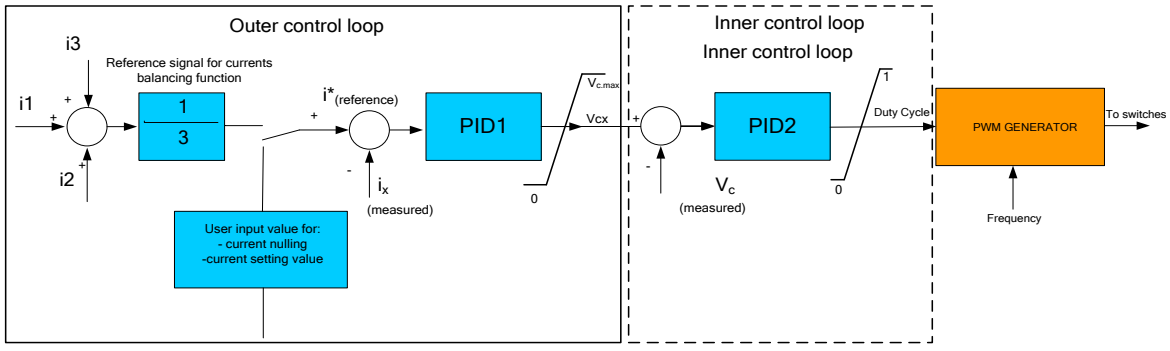


Figure 4.19 Proposed PID control scheme for the extended 3 ports CFC.

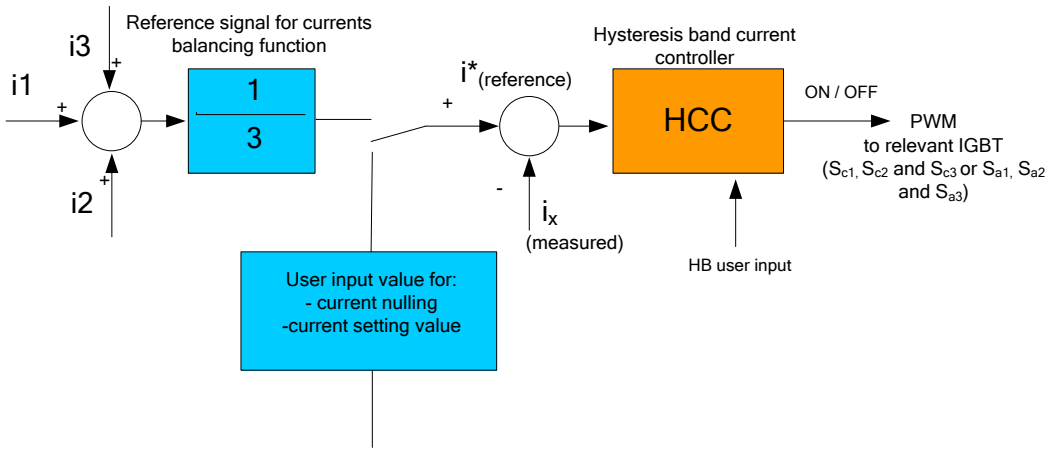


Figure 4.20 Proposed HCC control scheme for the extended 3 ports CFC.

4.9 Simulation Results

In order to validate the proposed control strategy and modes of operation for the two-port and extended three-port CFC, several simulation case studies are carried on MATLAB/SIMULINK software and presented in the following sub-sections. Proposed PID and HCC controllers are simulated as well as the proposed mode detection and change unit in order to investigate their performance and validity. The simulation is carried out on a simplified MTDC grid initially and then followed by testing the two-port CFC on a VSC based three terminals DC grid. More details of the simulation models used are available in Appendix B.

4.9.1 Two-port CFC

In this subsection, a two-port CFC is tested to evaluate the proposed control strategies and operation modes. Figure 4.21 shows a three terminals DC grid similar to the one used in [114] with parameters listed in Table 4-3. This MTDC grid is simulated and different functionalities of the CFC are demonstrated in the following subsections.

Table 4-3 Simulation parameters.

Parameter	Value
Grid voltage rating	320kV
Main capacitor	10mF
Cable 1-2	1.42Ω
	0.021 H
Cable 1-3	2.42Ω
	0.021 H
Cable 2-3	2.42 Ω
	0.021 H

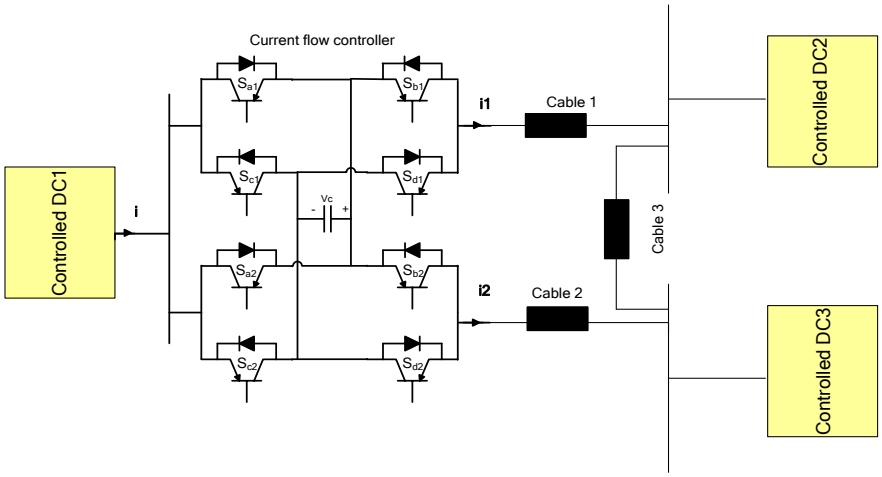


Figure 4.21 Three terminals MTDC grid with 2 ports CFC inserted.

4.9.1.1 Currents balancing using PID control.

In this simulation case, currents i_1 and i_2 are set to be initially 700 A and 412A, respectively. It is required to operate the CFC such that it redistributes the currents

on both cables to achieve a balanced current flow operation. Figure 4.22 shows the CFC switched on at t= 1 s to perform the currents balancing. *Figure 4.22* (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signal, respectively. The controller switches the two PWM IGBTs S_{c1} and S_{c2} off to allow the capacitor to be charged and then Pulse width modulates the switches to maintain the balanced operation of the two currents at approximately 550A successfully. The capacitor voltage is with steady state value of 1.4kV in this case. The operating mode in this case is mode one as i_1 is higher than i_2. This is shown in Figure 4.23 along with the reference current.

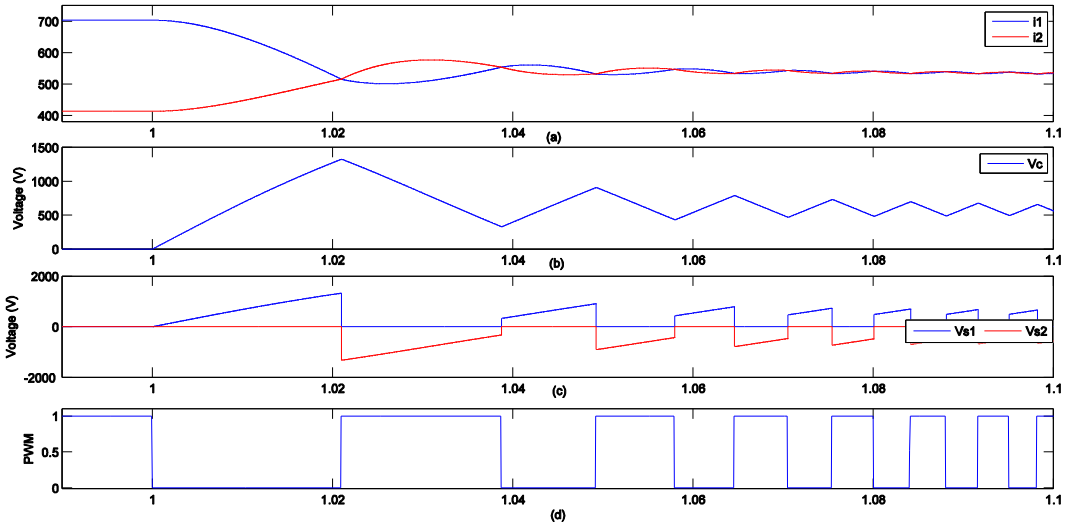


Figure 4.22 Currents balancing. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal

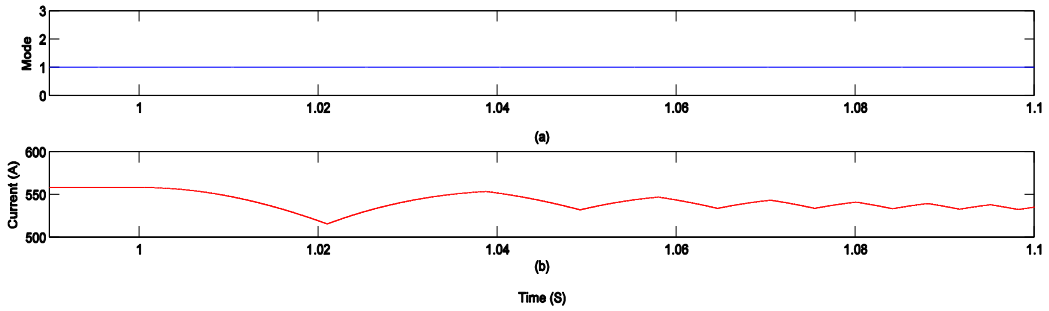


Figure 4.23 Currents balancing. (a) Operating mode, (b) Reference current

4.9.1.2 Current limiting using PID control.

Another CFC function is to let any desired current to follow a given set point value. Currents i_1 and i_2 are set to be initially 700 A and 412A, respectively. It is required to limit current i_1 to 300A. Figure 4.24 shows the CFC switched on at t= 1 s to perform this operation. Figure 4.24 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signal, respectively. The controller switches the two IGBTs S_{c1} and S_{c2} off to allow the capacitor to be charged until i_1 reaches the set point and then pulse width modulates the switches to maintain the value of i_1 at 300A successfully. The capacitor voltage is with steady state value of 1.6kV in this case. The capacitor voltage is higher than the previous case as the amount of energy transferred is higher as the set reference point is lower than that of the previous case. Figure 4.25 shows the operating mode along with the reference current.

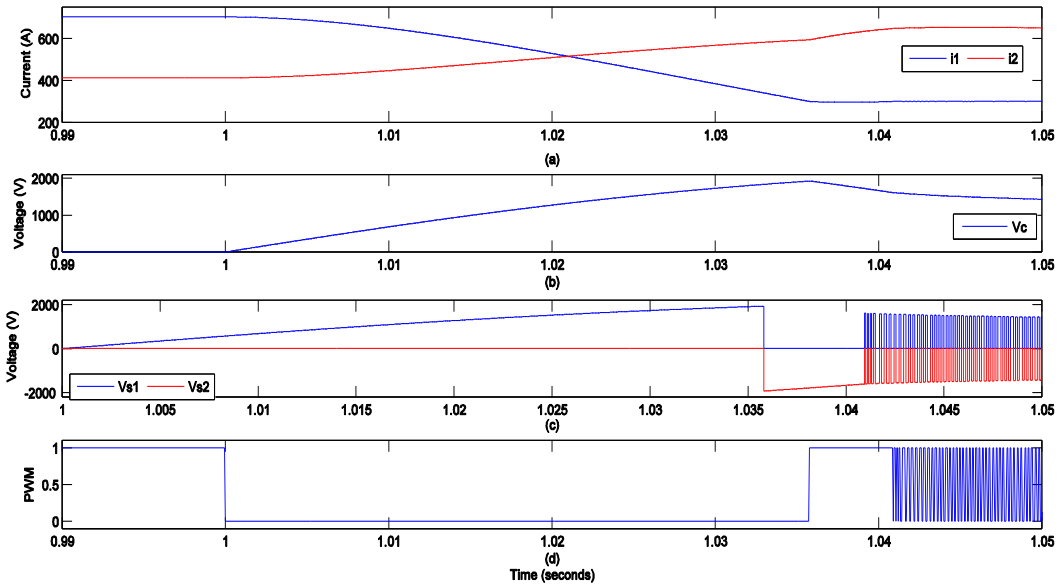


Figure 4.24 Current limiting. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal

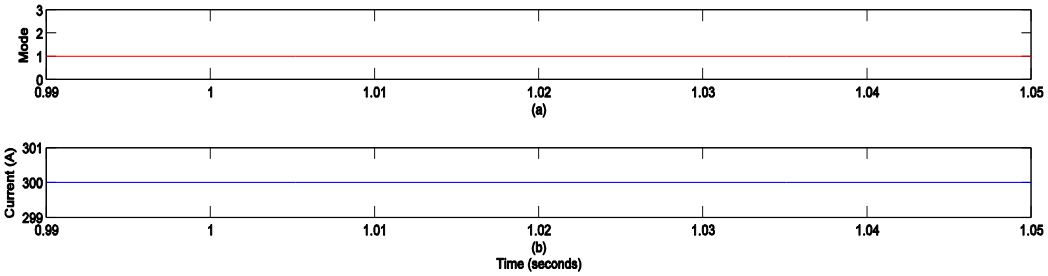


Figure 4.25 Current limiting. (a) Operating mode, (b) Reference current

4.9.1.3 Current nulling using PID control.

In this case, the reference value is set to zero in order to null current i_1. Figure *4.26* shows the CFC switched on at t= 1 s to perform this operation. Figure 4.26 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signal, respectively. The controller switches the two IGBTs S_{c1} and S_{c2} off to allow the capacitor to be charged from cable 1 until i_1 decreases from 700A to finally reach 0A and current i_2 increases consequently. The capacitor voltage is 2.1kV in this case. Figure 4.27 shows the operating mode along with the reference current.

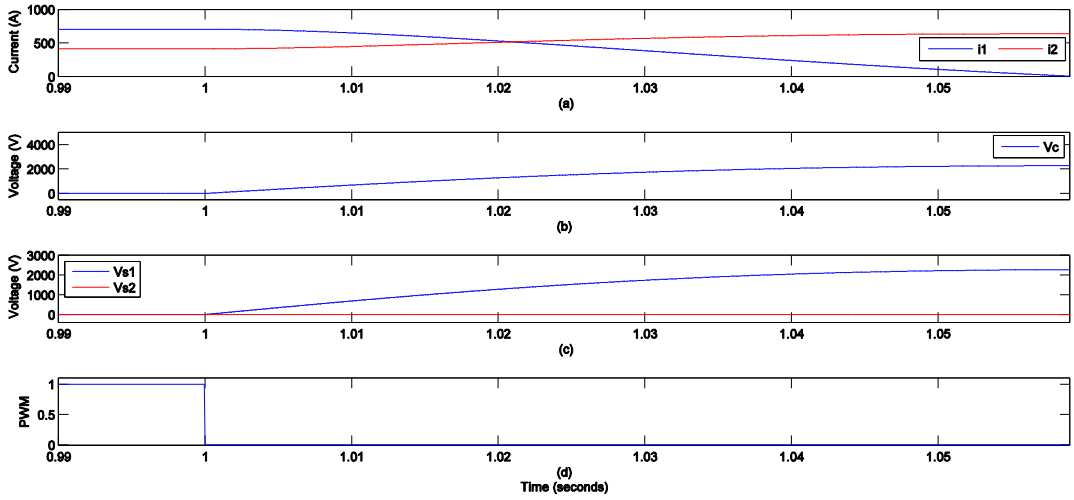


Figure 4.26 Current nulling. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal

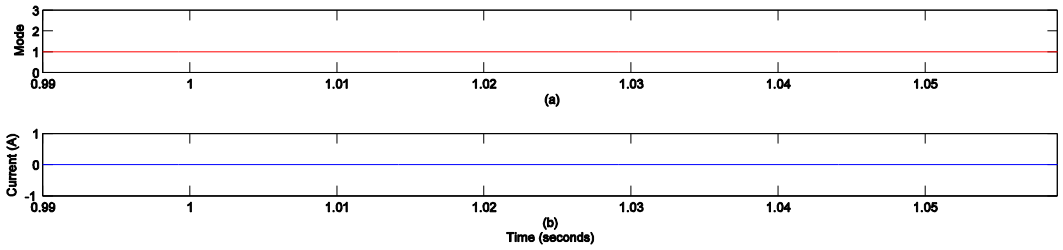


Figure 4.27 Current nulling. (a) Operating mode, (b) Reference current

4.9.1.4 Mode detection and change.

As discussed earlier in section 4.7, an automatic mode detection and change control unit is developed in order to maintain CFC operation even under sudden load changes that may result in different operating mode and hence needs changes in the switching states. Figure 4.28 shows a case where current balancing is initially successfully performed by the CFC for two currents i_1 and i_2. At t= 1.94 s, a sudden load change is performed that results in making i_2 higher than i_1, and hence the new operating mode should be mode 2. Without the mode detection and change control, the switching state remains incorrect and the CFC continues to operate in mode 1 and the currents balancing operation will be lost as shown in Figure 4.27.

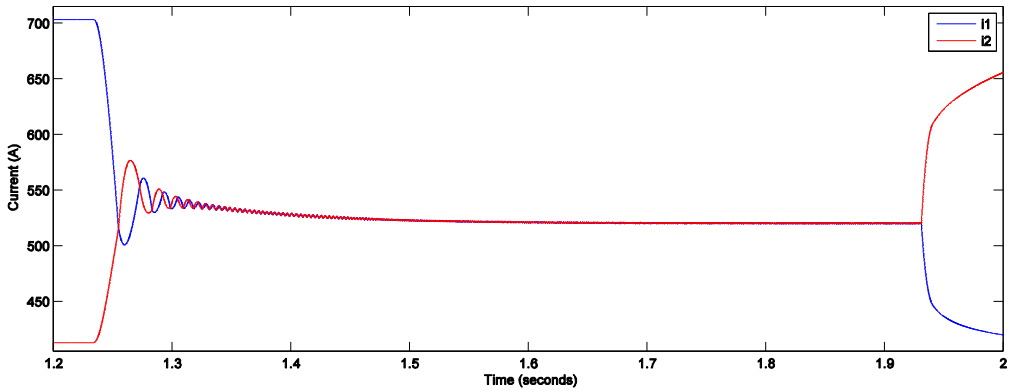


Figure 4.28 Sudden mode change with mode detection unit switched off.

The same case is repeated with applying the proposed mode detection and change control algorithm. Figure 4.29 shows the CFC switched on at t= 1.275 s to perform the currents balancing function. Figure 4.29 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signal, respectively. The control unit detects mode 1 as i_1 is higher than i_2 and sends to all switches the relevant correct states. At t= 1.44 s, a load change is applied such that currents i_1 and i_2 swap their values. As current i_2 starts to increase and bypasses the predefined threshold value epsilon (100A in this case), the control unit detects the mode change and corrects the switching states to that of mode 2 to maintain the currents balancing operation. The CFC is finally switched off at t= 1.77 s to show the new values of currents i_1 and i_2. Figure 4.30 shows the operating mode along with the reference current.

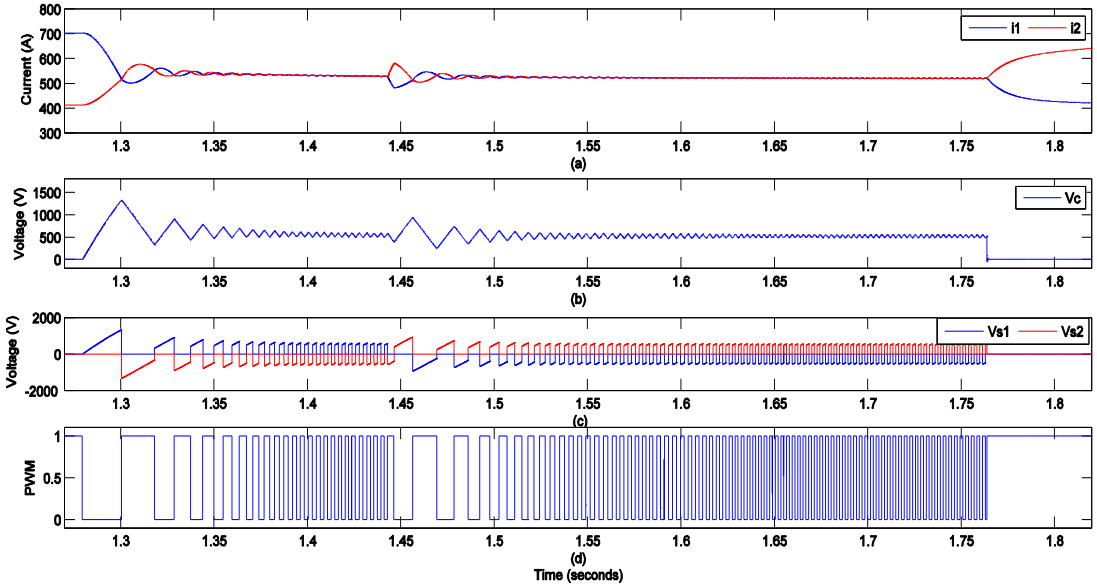


Figure 4.29 Mode detection and change. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal

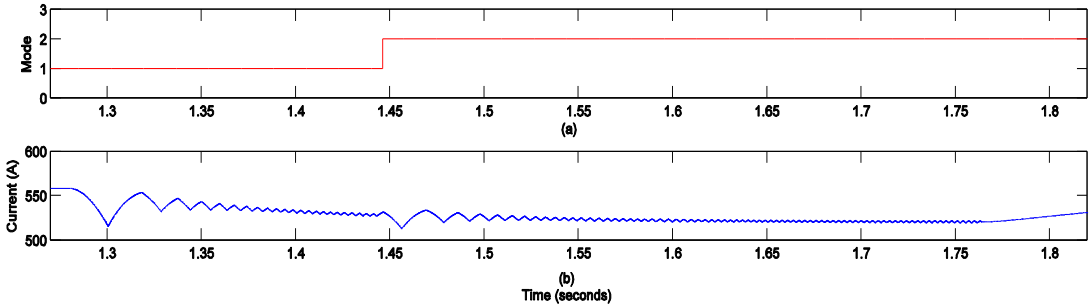


Figure 4.30 Mode detection and change. (a) Operating mode, (b) Reference current.

4.9.1.5 Hysteresis current control.

Another proposed control strategy for the CFC is using HCC as discussed in detail earlier in sub-section 4.6.2. The HCC is applied to perform currents balancing operation for the same MTDC grid, where currents i_1 and i_2 are initially 700A and 412A, respectively. Figure 4.31, Figure 4.32 and Figure 4.33 show HCC with hysteresis bands 50A, 5A and 0.01A, respectively. The CFC is switched on at t= 1 s to perform the currents balancing function.

Decreasing the HB gives more accurate performance and less voltage and current ripples, but at the same time, the switching frequency increases accordingly.

Figure 4.34 shows the performance of the HCC control strategy under sudden load changes where currents i_1 and i_2 are initially 700A and 412A, respectively, and the sudden load change influences current i1 to be 1400A. The CFC is switched on and the load change is applied at t=1.4 s. It is noticed that the CFC maintains the balanced operation and the capacitor voltage increases from 0.5 kV to 1.0 kV to compensate for the sudden rise of current i_1.

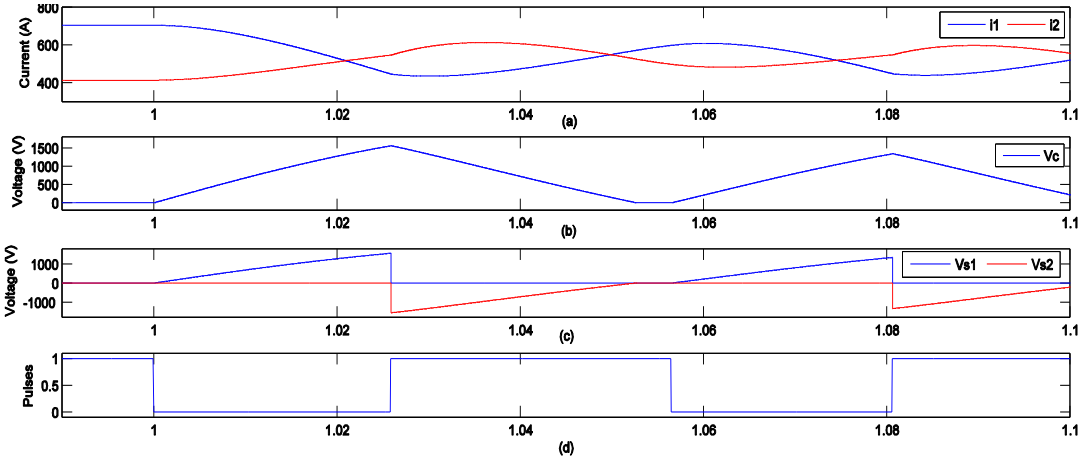


Figure 4.31 Currents balancing with HB=50A. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

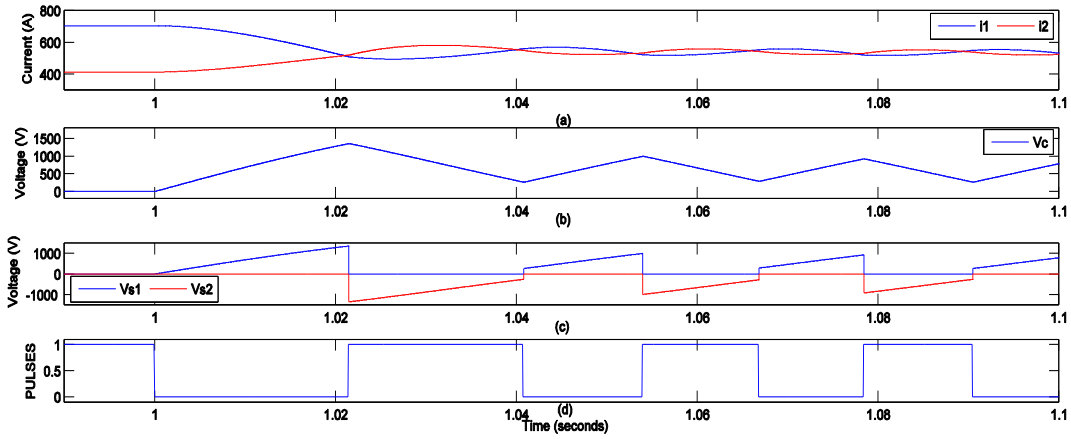


Figure 4.32 Current balancing with HB=5A. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal

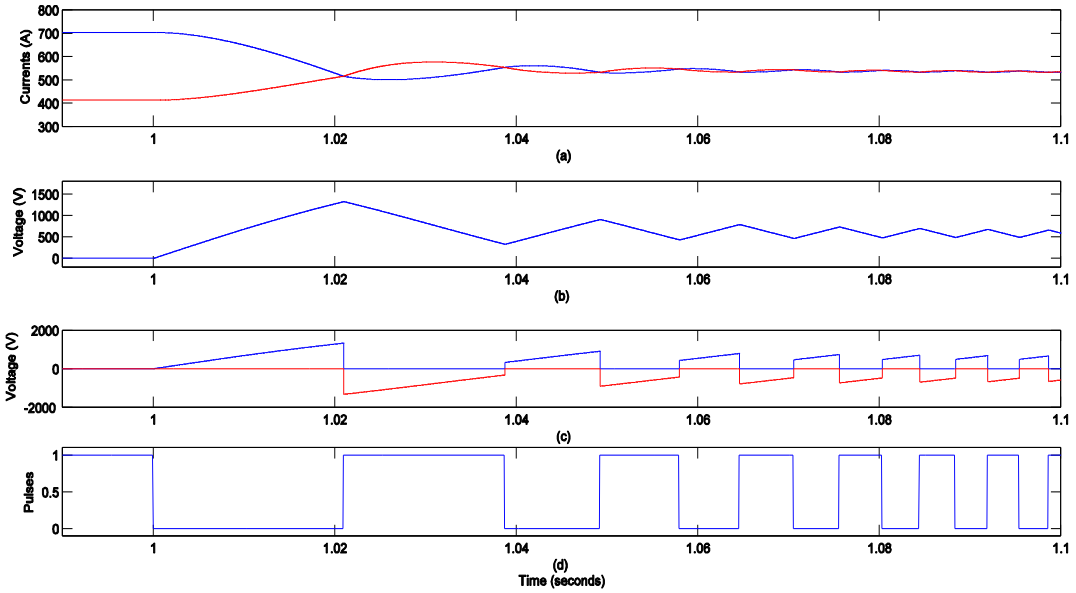


Figure 4.33 Current balancing with HB=0.001A. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal

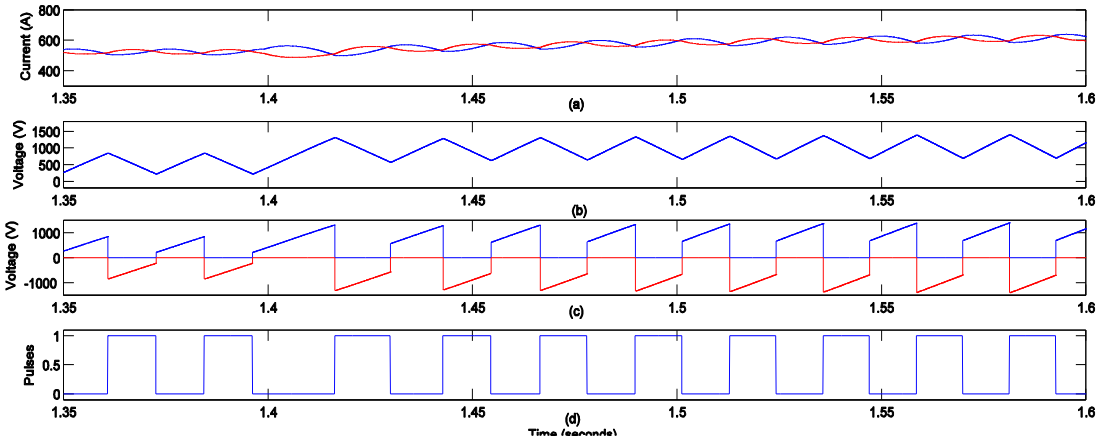


Figure 4.34 Performance under sudden load changes. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal

4.9.2 Extended 3 ports CFC

In this subsection, the proposed extended three-port CFC is tested to evaluate the proposed topology and operation modes. The same MTDC is used but is extended to four terminals with parameters listed in Table 4-4. This MTDC grid is simulated and different proposed operating modes of the CFC are demonstrated in the following subsections.

Table 4-4 Extended topology simulation parameters.

Parameter	Value
Grid voltage rating	320kV
Main capacitor	10mF
Cable 1-2	1.42Ω
	0.021 H
Cable 1-3	2.42Ω
	0.021 H
Cable 1-4	2.42 Ω
	0.021 H
Cable 2-3	2.42 Ω
	0.021 H
Cable 3-4	2.42 Ω
	0.021 H

4.9.2.1 Currents balancing

In this simulation case, currents i_1, i_2 and i_3 are set to be initially 700A, 412A and 740A, respectively. It is required to operate the CFC such that it redistributes the currents on both cables to achieve a balanced current flow operation. This can be achieved by connecting the capacitor in series with both cables 1 and 3 as both carry high currents (mode 4). The CFC switched on at t= 1 s to perform the currents balancing. Figure 4.35 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signals, respectively. The figures show that the controller successfully reaches balanced operation for the three currents at approximately 575 A. The capacitor voltage with steady state value of less than 0.7 kV is shown in Figure 4.35(b). It is important to note that series voltages of cables 1 and 3 are overlapping in Figure 4.35 (c) as the capacitor is connected and disconnected to both cables at the same time.

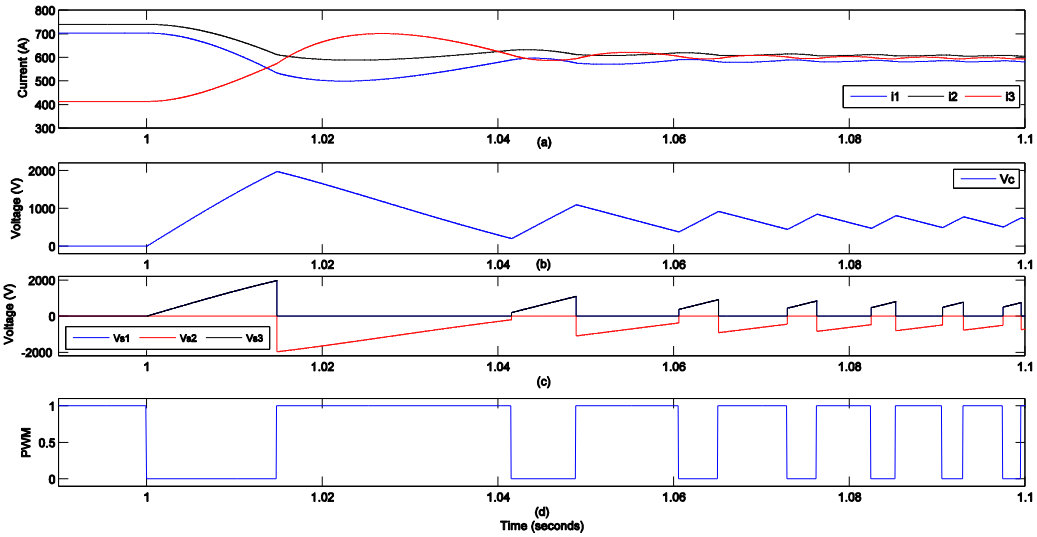


Figure 4.35 Extended CFC currents balancing mode 4 - extended topology. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

Another similar case is simulated where currents i_1, i_2 and i_3 are equal to 700A, 412A and 424A, respectively. To achieve the balanced operation, the CFC operates in mode 1 as current i_1 is higher than the average value and needs to be decreased. Figure 4.36 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signals for this case, respectively.

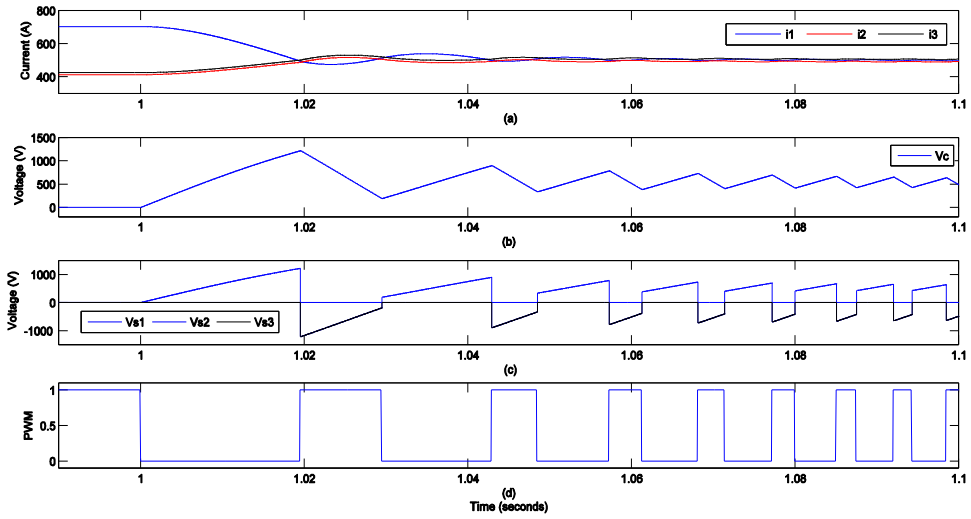


Figure 4.36 Extended CFC currents balancing mode 1 - extended topology. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

All functionalities demonstrated earlier on the two-port CFC can also be utilised with the extended topology. A similar case to the previous where current i_1 needs to be decreased from 700A to 250A is simulated. Figure 4.37 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signals for this case, respectively.

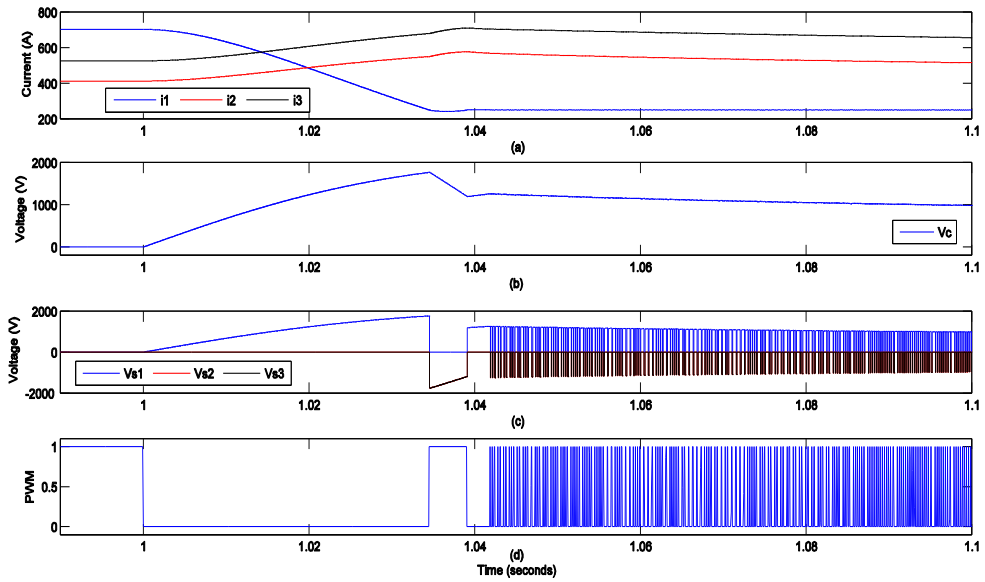


Figure 4.37 Extended CFC limiting i1 to 250A (mode 1) - extended topology. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

4.9.2.2 Extended topology limitations

As discussed earlier, this extended topology has some limitations. If two currents are higher than the average value, and at the same time there is a significant difference in magnitude between them, connecting the capacitor to both cables at the same time results in decreasing both of them with the same amount; hence, accurate balancing operation is not possible. This particular case is simulated in Figure 4.38. In this simulation case, currents i_1, i_2 and i_3 are set to be initially 700A, 412A and 1000A, respectively. Figure 4.38 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signals, respectively. These figures show that the controller fails to reach accurately balanced operation for the three currents.

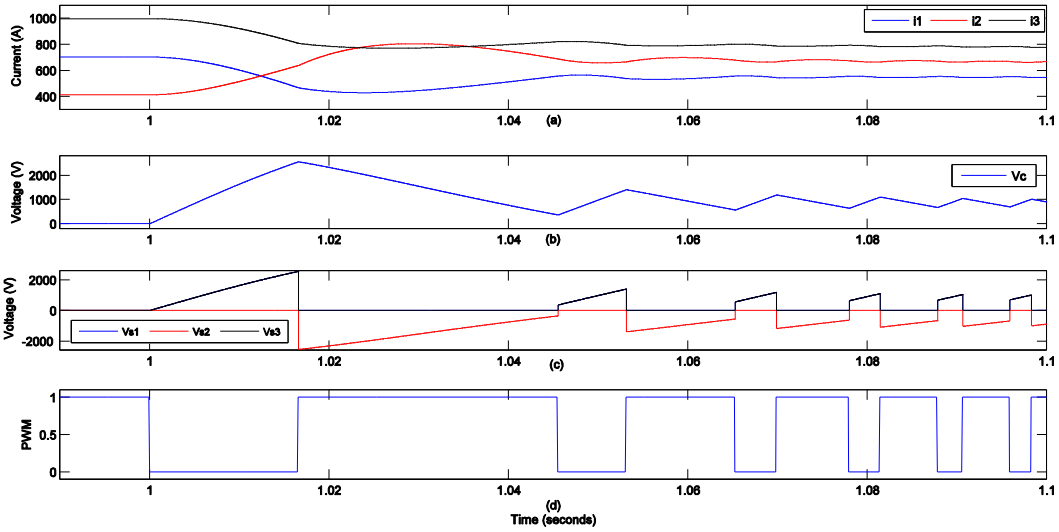


Figure 4.38 Extended CFC unsuccessful balancing (mode 4) - extended topology. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

Similarly, if the two currents are below the average value and have a significant difference in magnitude between them, connecting the capacitor to both cables at the same time will result increases both of them with the same amount; hence, accurate currents balancing operation is not possible. This case is simulated in Figure 4.39. In this simulation case, currents i_1, i_2 and i_3 are set to be initially 700A, 412A and 525A, respectively. Figure 4.39 (a), (b), (c) and (d) show cable currents, capacitor

voltage, series voltages and PWM signals, respectively. The figures show that the controller also fails to reach accurate balanced operation for the three currents.

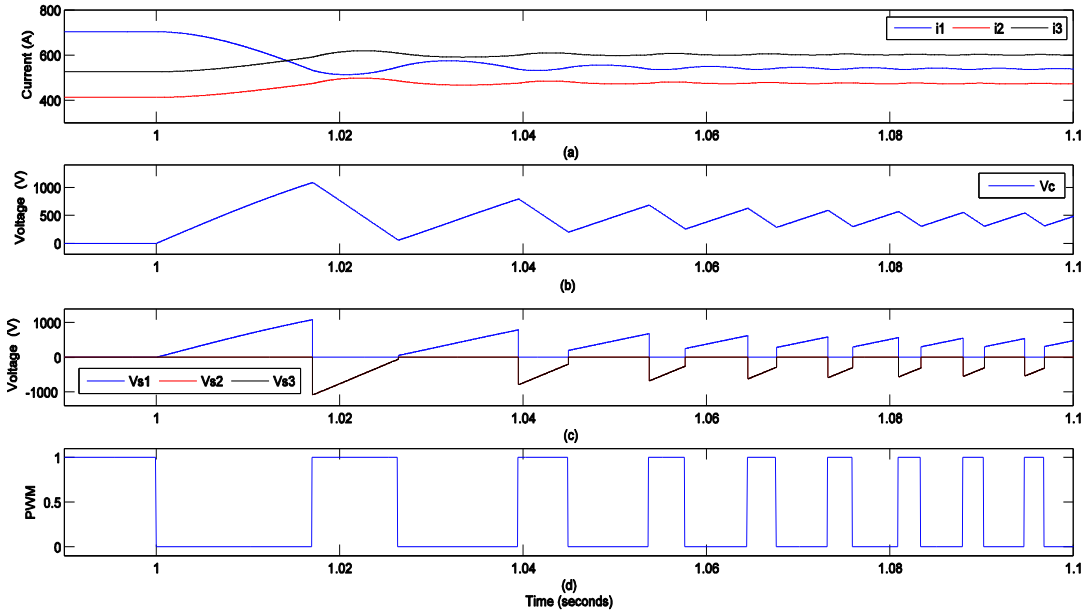


Figure 4.39 Extended CFC unsuccessful balancing (mode 1) - extended topology. (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

4.9.3 Testing the CFC in VSC based HVDC grid

After validating all the proposed CFC operating modes and control strategies by simulation using a simplified MTDC grid, a more realistic voltage source converter based HVDC model [115] is simulated in this subsection to demonstrate the validity of CFC for more real applications.

The simulation model rating is 200 MVA, +/- 100 kV DC where forced-commutated VSC interconnection is used to transmit power from a 230 kV, 2000 MVA, 50 Hz system to another identical AC system which acts as a second terminal and a load which acts as a third terminal. The rectifier and the inverter are three-level Neutral Point Clamped (NPC) VSC converters using IGBT/Diodes. The SPWM switching uses a single-phase triangular carrier wave with a frequency of 1350 Hz. Along with the converters, the station includes on the AC side: step down *Yg-D* transformer, AC filters, converter reactor; and on the DC side: capacitors, DC filters. The transformer tap changers and saturation characteristics are not simulated. The rectifier terminal is interconnected to both load terminal and the inverter terminal through two 75 km

cable (i.e. 2 pi sections) and two 8 mH smoothing reactors as shown in Figure 4.40. All simulation parameters are shown in Table 4-5.

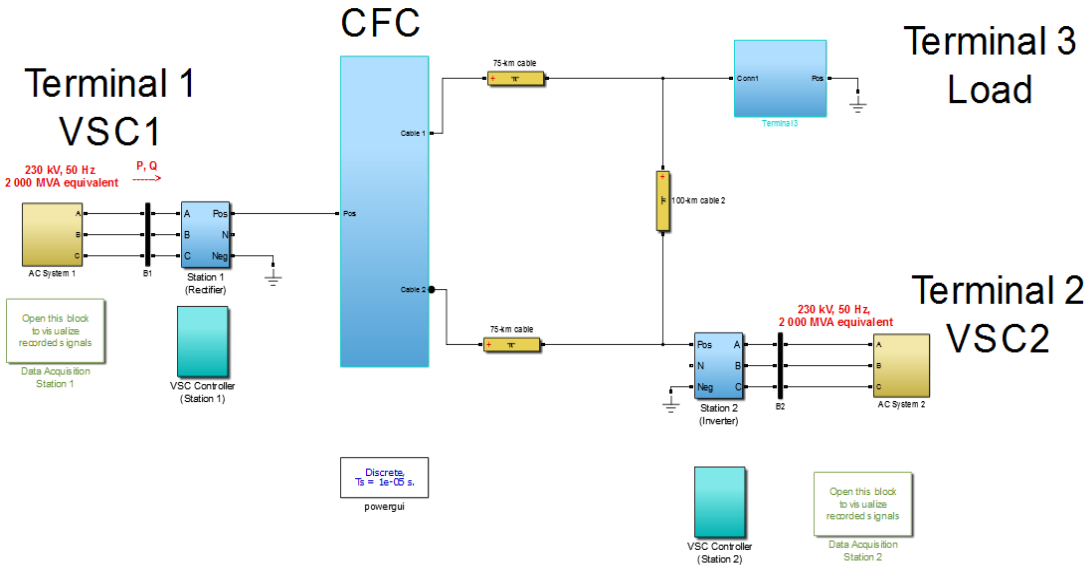


Figure 4.40 VSC based SIMULINK model.

Table 4-5 VSC based model simulation parameters.

Parameter	Value
DC Grid voltage rating	100kV
Main capacitor	10mF
Terminal 1	Rectifier station
Terminal 2	Load
Terminal 3	Inverter station
Cable resistance	0.14Ω/km
Cable inductance	15 mH/km
Cable capacitance	23uF/km
Cable 1-2 length	75km
Cable 1-3 length	75km
Cable 2-3 length	100km

4.9.3.1 Currents balancing

A case study is demonstrated where currents i_1 and i_2 are initially equal to 700A and 300A, respectively. It is required to operate the CFC such that it allows the amount of the current flowing in cable 1 to transfer to cable 2 in order to achieve a balanced current flow operation (mode 1). The CFC switched on at t= 1.2 s to perform the required task. Figure 4.41(a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signals, respectively. These figures show that the controller successfully performs the balancing operation for the two currents. The capacitor voltage is with steady state value of less than 0.7 kV as Figure 4.41(b). It is important to note that switching frequency in this case is approximately 750 Hz as can be observed from Figure 4.41(d).

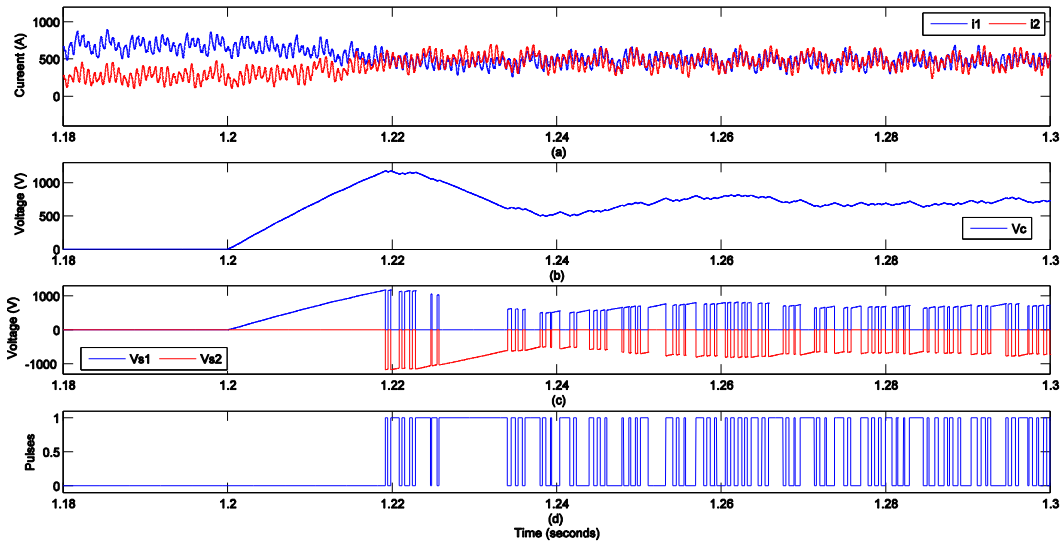


Figure 4.41 VSC based model with CFC currents balancing (mode 1) (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

4.9.3.2 Current limiting

For a similar case study, currents i_1 and i_2 are initially equal to 700A and 300A, respectively. It is required to operate the CFC such that it limits the amount of the current flowing in cable 1 to 300A. The CFC is set to operate at t = 1.2 s to perform the required task. Figure 4.42 (a), (b), (c) and (d) show cable currents, capacitor voltage, series voltages and PWM signals, respectively. The controller successfully

performs the current limiting operation for current i_1 at 300 A. The capacitor voltage is with steady state value of less than 1.2 kV as noted from Figure 4.42(b). The switching frequency in this case is approximately 1.2 kHz as it can be observed from Figure 4.42(d).

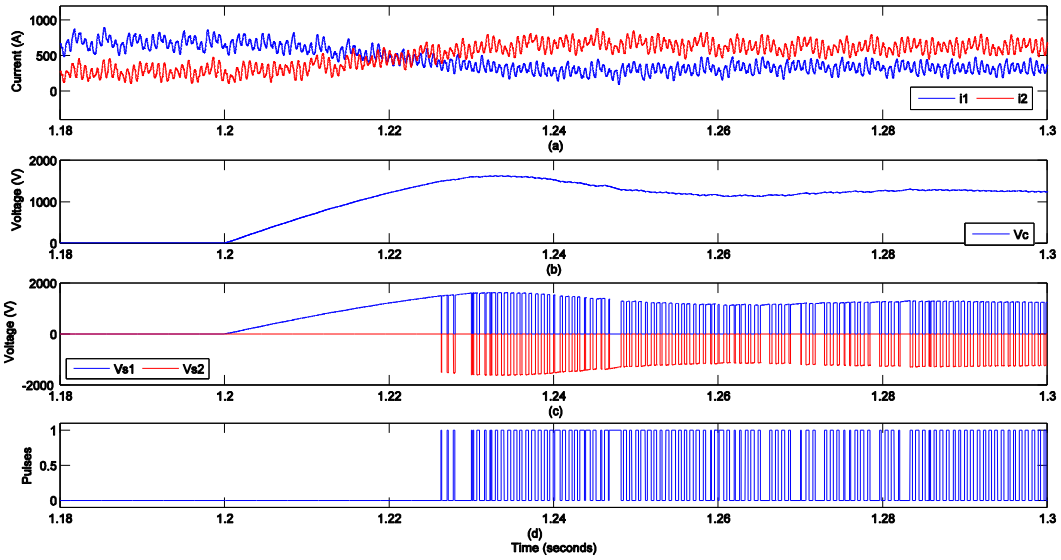


Figure 4.42 VSC based model with CFC currents limiting (mode 1) (a) Cable currents, (b) Capacitor voltage, (c) Series voltages, (d) PWM signal.

4.9.4 Validation of the dynamic model

The mathematical model discussed earlier in sub-section 4.8.2 is validated through PSCAD computer simulation. The mathematical model is used to calculate the currents and capacitor voltage with the same parameters used in the MTDC model. The simulation output values are plotted and currents i_1, i_2 and capacitor voltage V_c are shown in Figure 4.43. In a similar manner, mathematical calculation output currents i1m, i2m and capacitor voltage V_{cm} are shown in Figure 4.44. In order to prove the validity of the proposed mathematical model, both simulated and calculated currents are plotted together in Figure 4.45(a), while the modelled capacitor voltage is plotted against the calculated capacitor voltage in Figure 4.45(b). It is noticed that the modelled and calculated results are inline.

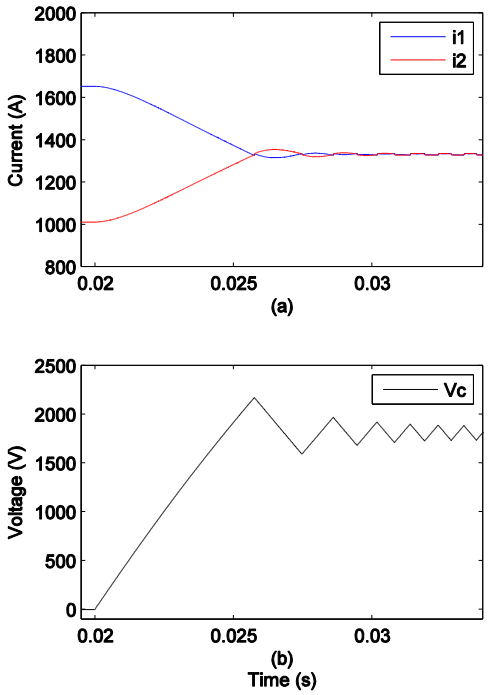


Figure 4.43 Simulation model outputs (a) Cable currents, (b) Capacitor voltage.

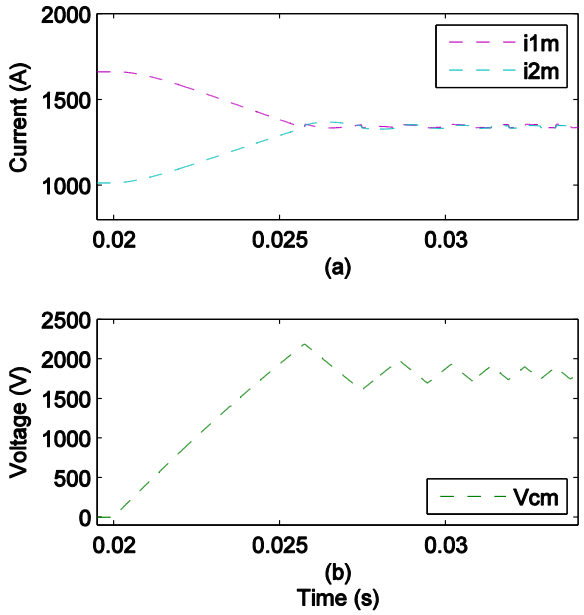


Figure 4.44 Calculated mathematical model outputs (a) Cable currents, (b) Capacitor voltage

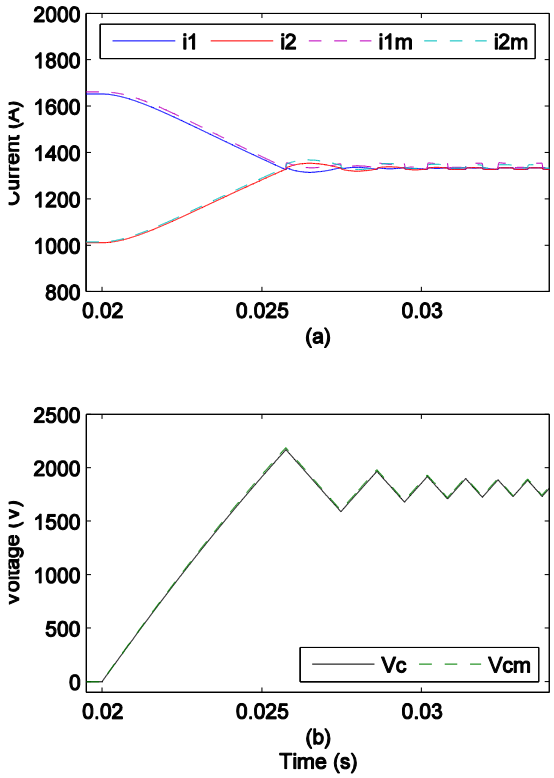


Figure 4.45 Comparison between simulation and calculation results (a) Cable currents, (b) Capacitor voltage.

4.10 Summary

In this chapter, the circuit topology of the CFC is presented along with its theory of operation. The proposed operation modes are set based on the magnitude and direction of the currents flowing. A mathematical model is developed for both the two-port and proposed extended topology three-port CFC and validated by comparing the calculated values with the simulated CFC circuit.

Different functionalities of CFC such as currents balancing, currents limiting and nulling are demonstrated using computer simulation on both a simplified and a VSC based MTDC grid. The proposed control strategies are validated and simulation results show accurate and fast dynamic performance. Both PID and HCC control schemes produced excellent results when designed correctly. Moreover, the proposed automatic mode detection and changing control unit is tested and results

showed fluent interchange in the switching modes to allow continuous proper operation of the CFC.

The proposed extended topology showed limitations throughout the computer simulation process especially when the difference in magnitude between the two controlled currents is significant. Therefore, the proposed extended topology may fail to perform accurately under certain loading circumstances due to the presence of a single capacitor and hence a better topology is needed in order to expand the CFC for operation in large MTDC grids.

Chapter

5

The Proposed Generalized Modular Current Flow Controller Topology

5.1 Introduction

To implement the CFC in real MTDC grid applications, where several cables at a given terminal may be connected, a generalized modular current flow controller (MCFC) is proposed in this chapter. A three-port MCFC is chosen to describe in details its circuit topology, operating modes, mathematical model and proposed control strategies. The proposed topology gave dual functionality when compared with the extended topology as each cable current can be controlled independently. Moreover, a reduced switches count topology is proposed which reduces the manufacturing cost of the MCFC to almost half. The reduced topology may be used in cases where current control of reverse direction is not required. Finally, the proposed MCFC topology is validated through different simulation case studies.

5.2 Proposed Generalized MCFC Topology

The proposed MCFC topology consists of mainly sub-modules and capacitors. These sub-modules are considered to be the building blocks of the MCFC with each containing four IGBT switches as shown in Figure 5.1. The number of cables (ports) connected to the MCFC determines its topology as shown in Figure 5.2, for two, three, four, and *n* ports. The number of sub-modules required can be calculated from the following equation:

$$n_s = n\,(n-1) \tag{5.1}$$

Where n_s is the total number of submodules and n is the number of cables to be connected to the MCFC. In addition, the number of the involved capacitors n_c can be obtained from the following equation:

$$n_c = (n-1) \tag{5.2}$$

The principle of operation of the MCFC is based on switching capacitors in series with cables carrying higher currents, one capacitor to one cable. This action allows each capacitor to charge independently from its connected cable and hence reducing the current flow in them and increasing the current flow in the cable carrying the lowest current.

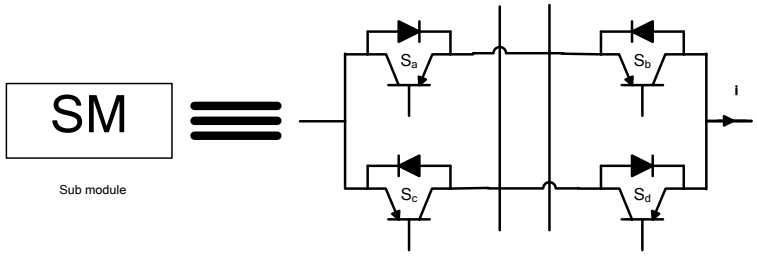


Figure 5.1 Building block of the MCFC.

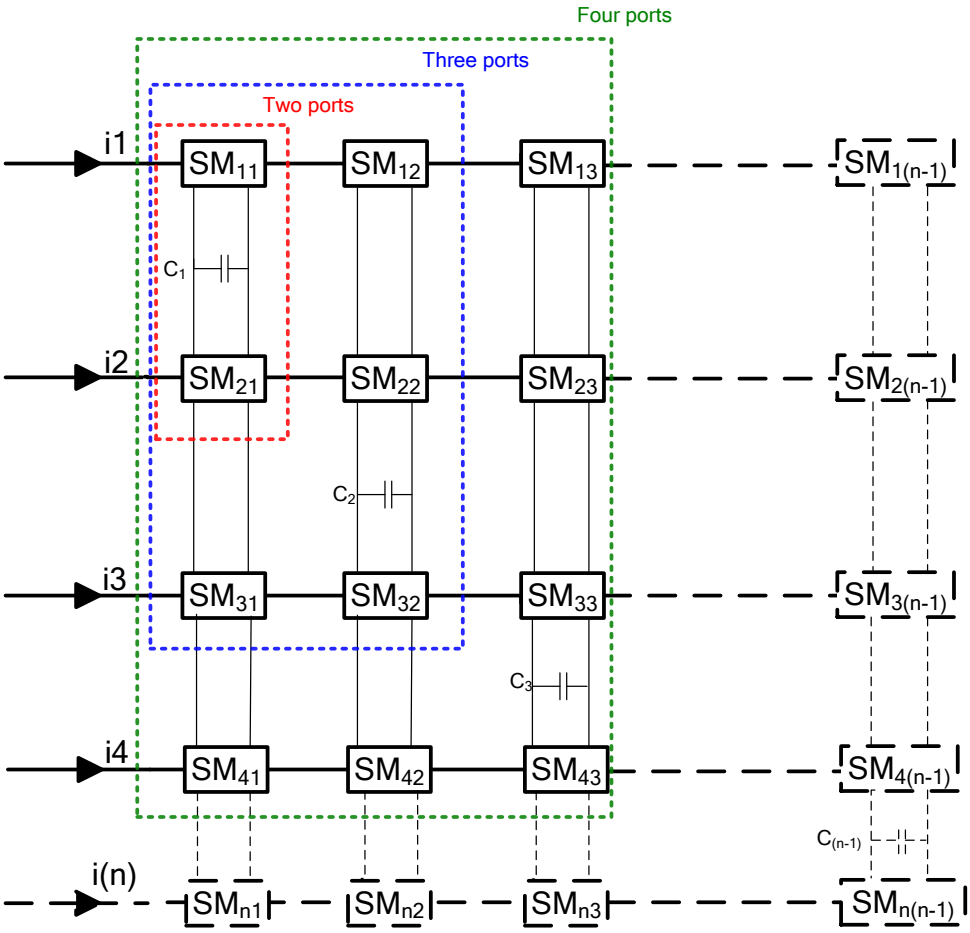


Figure 5.2 Proposed MCFC modular topology for 2, 3, 4, and n ports.

For each capacitor, a dedicated control circuit is developed, allowing it to be connected to the desired cable with the desired charging and discharging times based on the requested set point. As a result, the main drawback of the extended topology presented earlier in the previous chapter can be solved. Consequently, the proposed MCFC is able to control all currents flowing in a given MTDC grid independently.

5.3 Modes of Operation

By studying a three-port MCFC with circuit shown in Figure 5.3, where six sub-modules are used (two connected to each cable) and two capacitors are involved. The three-port MCFC modes of operation can be grouped into two groups. The first group is when currents are flowing in the forward direction (out of the MCFC), three operating modes are present where any of i_1, i_2 and i_3 may be the lowest current. The second group is similar to the first one but contains three modes of operations when currents are flowing in the reverse direction (into the MCFC). The six modes of operations and their switching states are shown in Table 5-1.

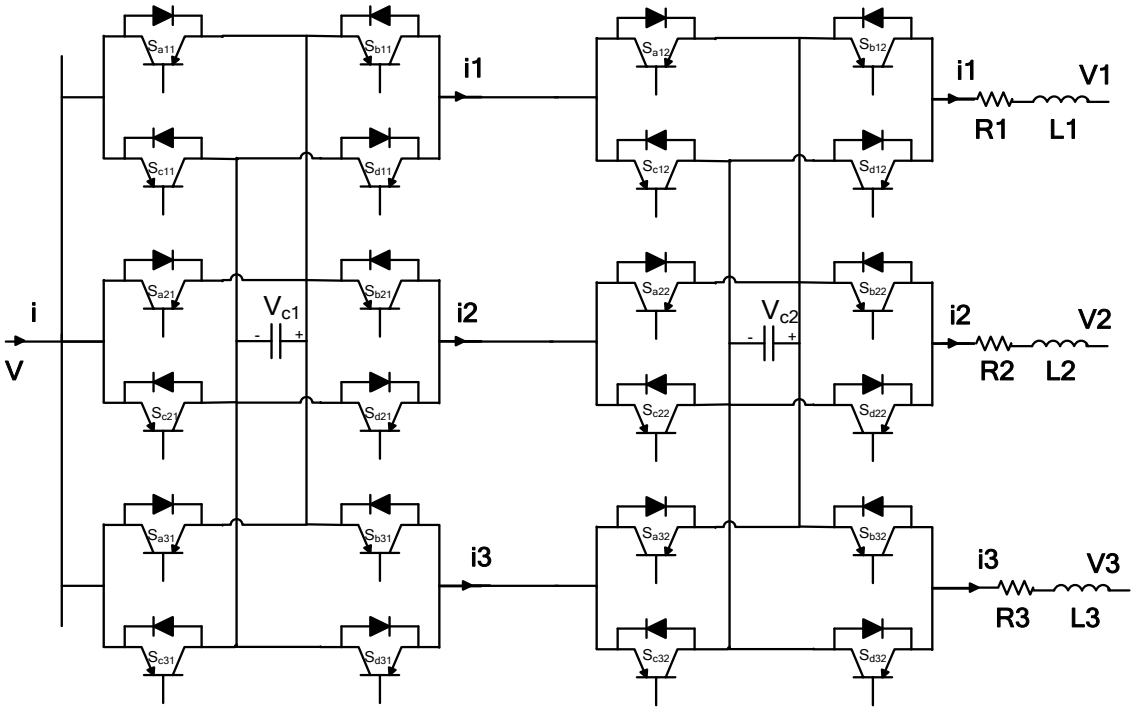


Figure 5.3 Proposed three-port MCFC topology.

Table 5-1 Three-port MCFC modes of operation and switching states.

Operating modes						
Direction:	Forward			Reverse		
Higher currents:	i_1 & i_2	i_2 & i_3	i_1 & i_3	i_1& i_2	i_2 & i_3	i_1 &i_3
Mode:	**1**	**2**	**3**	**4**	**5**	**6**
S_{a11}	0	0	0	P_1	P_1	P_1
S_{a21}	0	0	0	0	P_1	P_1
S_{a31}	0	0	0	P_1	0	0
S_{b11}	0	1	0	0	0	0
S_{b21}	1	0	1	0	0	0
S_{b31}	1	1	1	0	0	0
S_{c11}	P_1	P_1	P_1	0	0	0
S_{c21}	0	P_1	P_1	0	0	0
S_{c31}	P_1	0	0	0	0	0
S_{d11}	0	0	0	0	1	0
S_{d21}	0	0	0	1	0	1
S_{d31}	0	0	0	1	1	1
S_{a12}	0	0	0	0	P_2	0
S_{a22}	0	0	0	P_2	0	P_2
S_{a32}	0	0	0	P_2	P_2	P_2
S_{b12}	1	1	1	0	0	0
S_{b22}	0	1	1	0	0	0
S_{b32}	1	0	0	0	0	0
S_{c12}	0	P_2	0	0	0	0
S_{c22}	P_2	0	P_2	0	0	0
S_{c32}	P_2	P_2	P_2	0	0	0
S_{d12}	0	0	0	1	1	1
S_{d22}	0	0	0	0	1	1
S_{d32}	0	0	0	1	0	0

All schematic diagrams for the six operating modes are presented in Appendix A.3.

By inspecting mode 1 as an example, it is assumed that both currents i_1 and i_2 are higher than current i_3. It is required to redistribute the three currents to achieve balanced operation, and this action is done by connecting capacitor C_1 to cable 1 and capacitor C_2 to cable 2 to charge them in the charging period as shown in Figure 5.4.

After that, each capacitor is connected in series with cable 3 to discharge in it in the discharging period as demonstrated in Figure 5.5. The fact that each capacitor is switched by a different control signal, gives accurate performance as each control signal has its own distinct reference value and duty cycle.

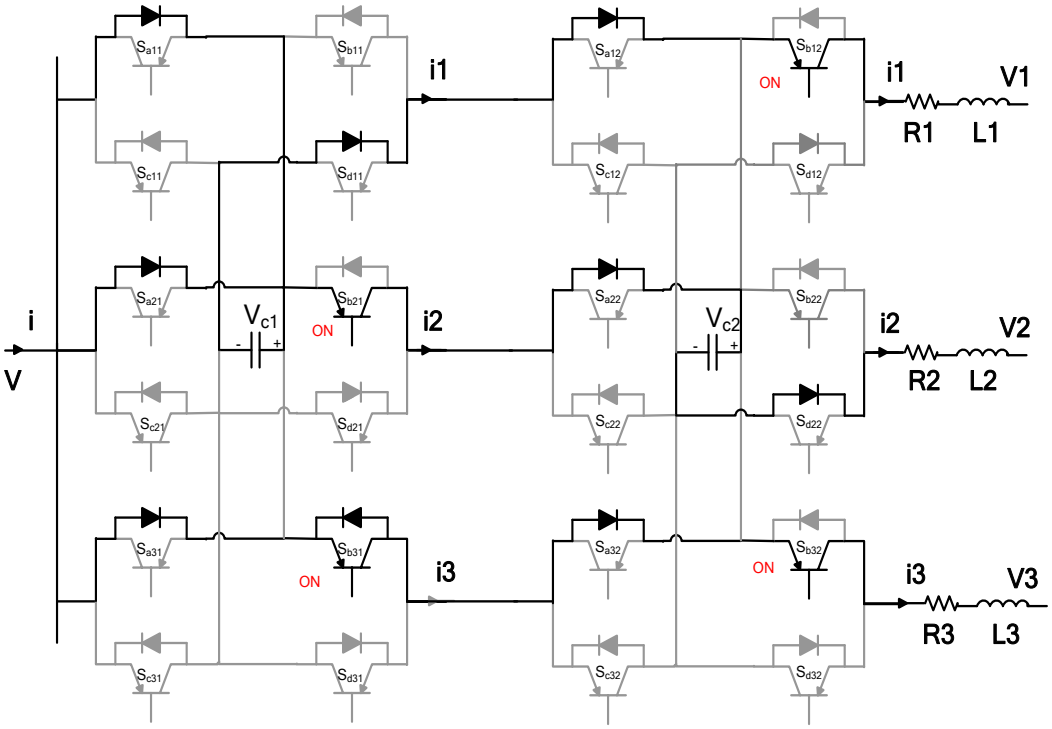


Figure 5.4 Three-port MCFC operating in mode 1(charging period).

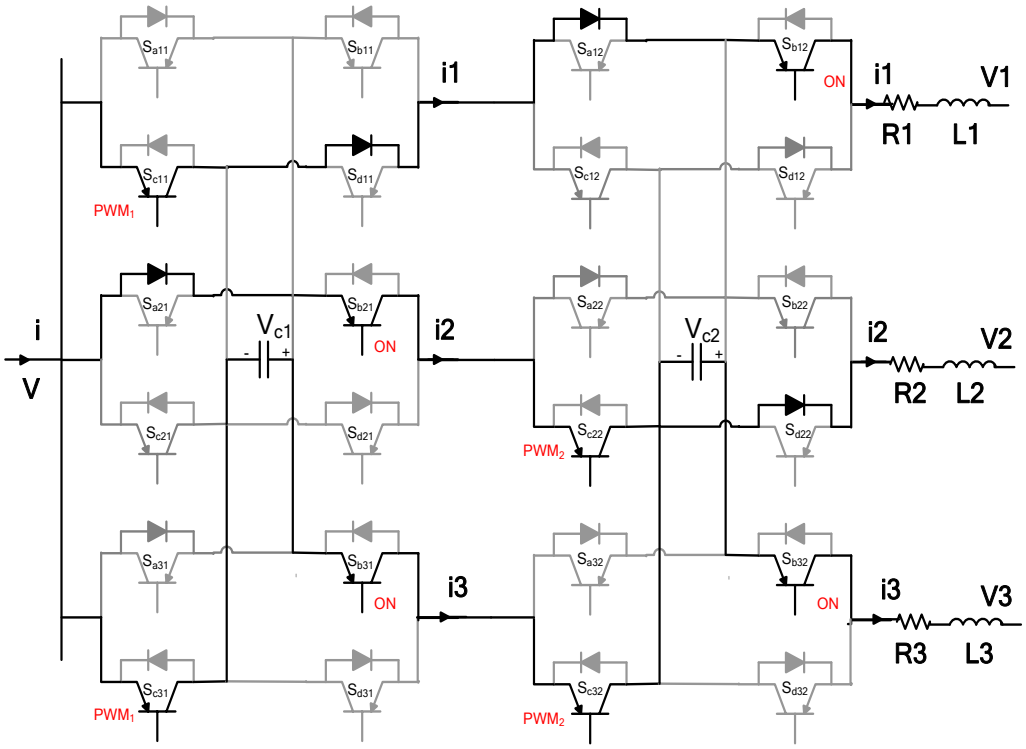


Figure 5.5 Three-port MCFC operating in mode 1(discharging period).

5.4 Mathematical Modelling

In this section, the averaging technique is used to derive a dynamic model for the three-port MCFC. Considering mode 1 of operation, i_1 *and* i_2 are both greater than current i_3 flowing in cable three. The proposed MCFC transfer currents from cable 1 and cable 2 through C_1 and C_2, respectively, to cable 3. The MCFC charges C_1 from cable 1 for a time interval of D_1T, while it charges C_2 from cable 2 for a time interval of D_2T, where D_1 and D_2 are duty ratios for charging periods of C_1 and C_2, respectively, and T is the switching period. Assuming i_1 is greater than i_2, consequently, D_1 becomes greater than D_2. Therefore, the operation of the proposed MCFC in mode 1 can be divided into three consecutive intervals of periods D_2T, $(D_1\text{-}D_2)$ T, and $(1\text{-}D_1)$ T. Figure 5.4 presents the operating devices of the MCFC during the first interval where both C_1 and C_2 are charging from cable 1 and cable 2,

respectively. The circuit equations that describe the MCFC during this interval, D_2T, can be written as:

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + v_{c1} + V_1 \tag{5.3}$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + v_{c2} + V_2 \tag{5.4}$$

$$V = r_3 i_3 + L_3 \frac{di_3}{dt} + V_3 \tag{5.5}$$

$$i_1 = C \frac{dv_{c1}}{dt} \tag{5.6}$$

$$i_2 = C \frac{dv_{c2}}{dt} \tag{5.7}$$

where r_1 and L_1 are the resistance and the inductance of the first cable, r_2 and L_2 are the resistance and the inductance of the second cable, r_3 and L_3 are the resistance and the inductance of the third cable, v_{c1} and v_{c2} are the capacitors voltages of the three-port MCFC capacitors, V is the bus voltage where the MCFC is connected, V_1, V_2 and V_3 are the voltages at the end terminals of the first, second, and third cables, respectively. The state-space model representation of (5.3)–(5.7) is given by the following:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -1 & 0 \\ 0 & -r_2 & 0 & 0 & -1 \\ 0 & 0 & -r_3 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{5.8}$$

In the second interval, C_2 is switched to discharge in cable 3 while C_1 remains charging from cable 1. The duration of this interval is $(D_1\text{-}D_2)T$. The equations describing the circuit in this case can be as follows:

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + v_{c1} + V_1 \tag{5.9}$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + V_2 \tag{5.10}$$

$$V = r_3 i_3 + L_3 \frac{di_3}{dt} - v_{c2} + V_3 \tag{5.11}$$

$$i_1 = C \frac{dv_{c1}}{dt} \tag{5.12}$$

$$i_3 = -C \frac{dv_{c2}}{dt} \tag{5.13}$$

In a similar way, the state equations representing the second interval are written as follows:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -1 & 0 \\ 0 & -r_2 & 0 & 0 & 0 \\ 0 & 0 & -r_3 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} +$$

$$\underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{5.14}$$

During the third interval, *(1-D_1) T*, C_1 is switched to cable 3. Hence, both C_1 and C_2 are discharging into cable 3, as indicated in Figure 5.5. The circuit equations in this case are as follows:

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + V_1 \tag{5.15}$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + V_2 \tag{5.16}$$

$$V = r_3 i_3 + L_3 \frac{di_3}{dt} - v_{c2} - v_{c1} + V_3 \tag{5.17}$$

$$i_3 = -C \frac{dv_{c1}}{dt} \tag{5.18}$$

$$i_3 = -C \frac{dv_{c2}}{dt} \tag{5.19}$$

The mathematical state space representation of the MCFC during this interval is given by the following:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & 0 & 0 \\ 0 & -r_2 & 0 & 0 & 0 \\ 0 & 0 & -r_3 & 1 & 1 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix}}_{A_3} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} +$$

$$\underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{5.20}$$

Multiplying (5.8), (5.14) and (5.20) by their duty ratios, D_2, D_1-D_2, and 1-D_1, respectively, and summing the results to get the average model for the MCFC for mode 1 presents the following:

$$K\dot{X} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -D_1 & 0 \\ 0 & -r_2 & 0 & 0 & -D_2 \\ 0 & 0 & -r_3 & 1-D_1 & 1-D_2 \\ D_1 & 0 & -(1-D_1) & 0 & 0 \\ 0 & D_2 & -(1-D_2) & 0 & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} + B\,U \tag{5.21}$$

where $A = D_2 A_1 + (D_1\text{-}D_2) A_2 + (1\text{-}D_1) A_3$. At steady state, (5.21) is written as the following:

$$A\,X + B\,U = 0 \tag{5.22}$$

Rearranging (5.22), the capacitors' voltages can be expressed as the following:

$$V_{c1} = \frac{((1-D_2)^2 + r_3 D_2^2/r_2)a - b/(1-D_1)(1-D_2)}{1-((1-D_2)^2 + r_3 D_2^2/r_2)((1-D_1)^2 + r_3 D_1^2/r_1)} \tag{5.23}$$

$$V_{c2} = \frac{(1-D_1)(1-D_2)a - \left((1-D_1)^2 + \frac{r_3}{r_1} D_1^2\right) b}{\frac{r_3}{r_1 r_2}((D_1 D_2)^2 + (1-D_1)^2 (r_1 D_2^2 + r_2 D_1^2))} \tag{5.24}$$

where $a = (1 - D_1)(V - V_3) - r_3 D_1 (V - V_1)/r_1$ and $b = (1 - D_2)(V - V_3) - r_3 D_2 (V - V_2)/r_2$. The rated voltage of the capacitors and hence the MCFC switches can be calculated from the maximum of (5.23) and (5.24). These equations show that the capacitor voltage depends on the network parameters and the voltage drops across the cables connected to the MCFC are related to the loading condition of the grid.

5.5 MCFC Control Strategy

The control system proposed for the MCFC is different from the one of the two-port CFC proposed earlier in the previous chapter. For an n-port MCFC having *(n-1)* capacitors, *(n-1)* control loops will be required each with its own unique reference value and feedback signals. Figure 5.6 shows the proposed control system for a three-port MCFC.

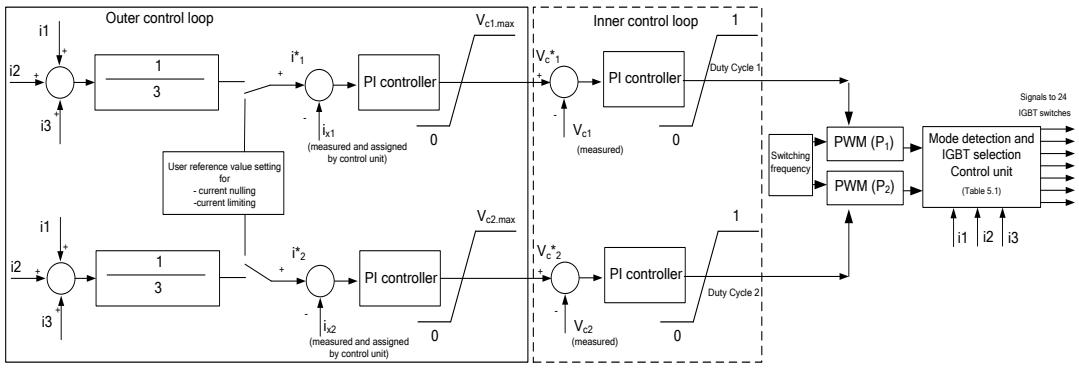


Figure 5.6 Proposed three-port MCFC control loops.

As noticed from Figure 5.6, two selector switches are utilized to determine the function of the MCFC. For currents balancing, in each of the two control loops, the sum of currents in the three branches is measured and then divided by the number of branches to obtain the average value of the desired current, i^*. This value is considered the reference value to be compared with the measured value of the current i_x (which depends on the operating mode) that needs to be redistributed. The error signal is processed using a PI controller, where the output of this outer current

control loop is considered the reference value of the capacitor voltage v_c^*. A limiter is used to prevent exceeding the rated capacitor voltage. The inner control loop is dictated to regulate the capacitor voltage at its estimated value from the outer one using another PI controller. The output of this controller is the duty cycle of the modulating switches. Similarly, a reference signal can be inserted directly to the controller based on the required function whether it is current setting or current nulling.

A master control unit similar to that proposed earlier in the previous chapter may be developed in order to look up Table 5-1, and based on the measured currents i_1, i_2 and i_3 the appropriate mode of operation can be chosen and hence the switching states of all twenty-four IGBTs can be determined (whether on, off, PWM_1 or PWM_2).

5.6 Proposed Reduced Switches Count Topology

By inspecting any given MTDC grid, some nodes (terminals) would always operate in a unidirectional power flow scheme. For example, a terminal connecting several offshore wind farms together or a terminal having solar power generating arrays always act as a generating terminal and all currents flow out of it. Consequently, a reduced switches count topology is proposed to decrease the number of switches by half by eliminating the switches responsible for the reverse currents control. The building block of the MCFC is changed to a reduced one that contains two IGBTs and two diodes as shown in Figure 5.7 and the general MCFC topology remains the same.

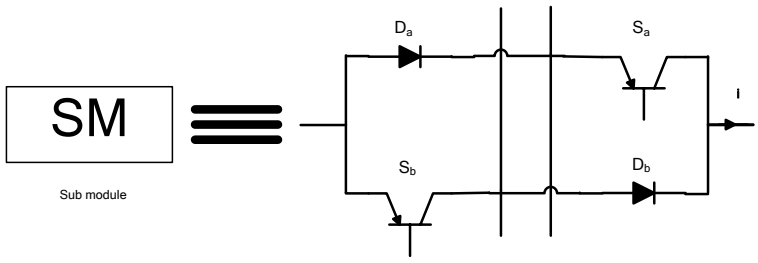


Figure 5.7 Building block of the reduced switches count MCFC.

Figure 5.8 shows a two-port MCFC with the reduced topology as an example, where only four diodes and IGBTs are needed in this case. The operating modes for the two-port MCFC is reduced to two modes only as the other two responsible for reverse currents control are eliminated as illustrated in Table 5-2. For operation in mode 1, where i_1 is assumed to be higher than i_2, the capacitor is allowed to charge from cable 1 through diodes D_{a1} and D_{b1}, while current i_2 flows regularly in cable 2 by switching S_{a2} on as indicated in Figure 5.9(a). As for the discharge period, in addition to S_{a2} both S_{b1} and S_{b2} are switched on to connect the capacitor in cable 2 as in Figure 5.9(b). Similarly, mode 2 is operated when i_2 is the higher current and Switch S_{a1} is switched on instead of switch S_{a2} in that case.

In case of installing the reduced MCFC at a terminal with wind generating units only, care must be taken as wind turbines need power at the starting up process and the reduced topology allows power to flow in one direction only. The solution can include using batteries to supply the wind turbines at start up or installing bypass switches for the MCFC to allow reverse power flow.

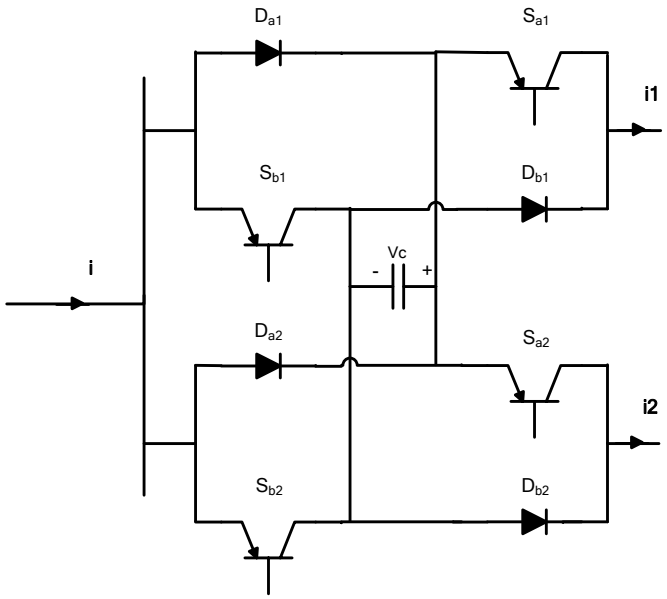
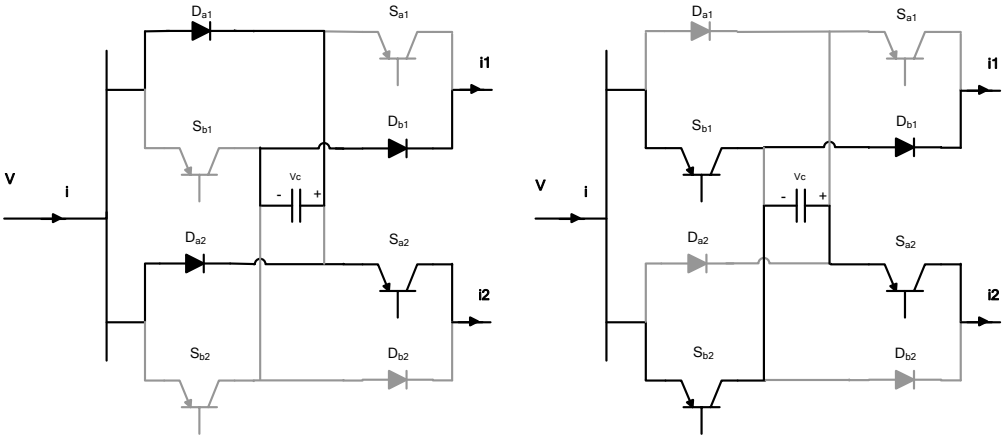


Figure 5.8 Reduced switches count topology of two-port MCFC.



(a) (b)

Figure 5.9 Reduced switches count topology MCFC operating in mode 1, (a) charging (b) discharging.

Table 5-2 Two-port reduced MCFC modes of operation and switching states.

Mode	Higher Current	Switching states			
		S_{a1}	S_{a2}	S_{b1}	S_{b2}
1	i_1	off	on	PWM	PWM
2	i_2	on	off	PWM	PWM

All schematic diagrams for the two operating modes are presented in Appendix A.4.

5.7 Simulation Results

In the following subsections, the proposed MCFC topology is validated using PSCAD/EMTDC environment. However, the reduced MCFC topology is not

simulated nor tested as it offers the exact behavior of any MCFC operating in the forward direction modes. Additional details of the models used are presented in Appendix B.2.

5.7.1 Currents balancing: MCFC

In this case study, currents i_1, i_2 and i_3 are set to be initially 640A, 540A and 700A, respectively. It is required to operate the CFC such that it redistributes the currents higher than the average value (i_1 and i_3) on all cables to achieve a balanced current flow operation. This can be achieved by connecting the capacitor C_1 in series with cable 3 and capacitor C_2 in series with cable 1 as both are carrying high currents (mode 3). The CFC switched on at t= 1.5 s to perform the desired currents balancing. Figure 5.10(a), (b), (c), (d) and (e) show cable currents, capacitor voltage V_{c1}, capacitor voltage V_{c2}, PWM_1 signal and PWM_2 signal, respectively. These figures show that the controller successfully force the currents to reach balanced operation at approximately 620 A. The capacitor voltages V_{c1} and V_{c2} are equal to 1.2 kV and 0.5 kV respectively.

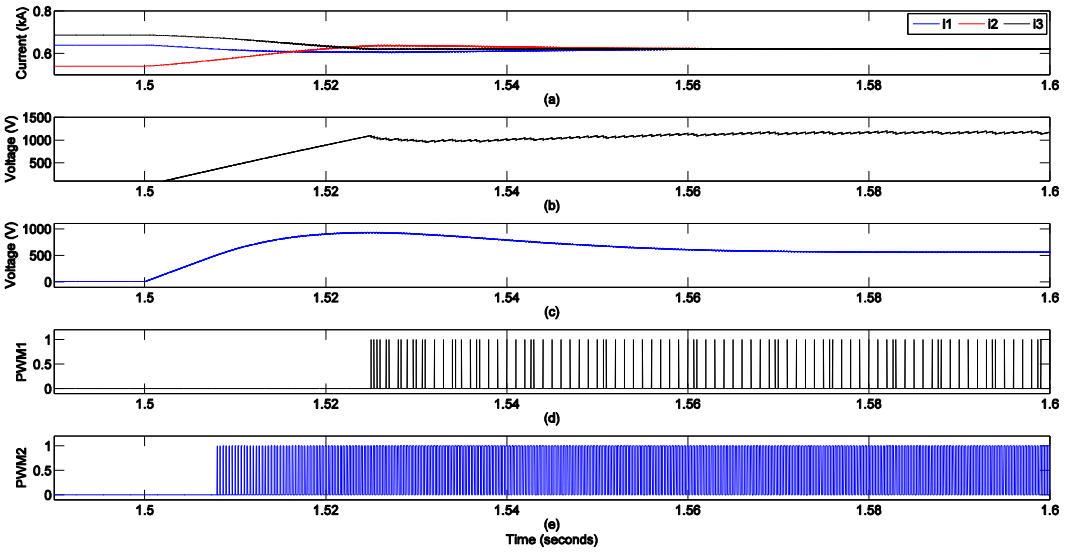


Figure 5.10 MCFC currents balancing - mode 3. (a) Cable currents, (b) Capacitor voltage V_{c1}, (c) Capacitor voltage V_{c2}, (d) PWM_1 signal, (e) PWM_2 signal

Another similar case study is shown in Figure 5.11(a), where currents i_1 and i_2 are both below the average value of the three cable currents with values 620 A and 580 A. And i_2 is considered to be the lowest current. The MCFC is operated at t= 1.5 s

and accurate current balancing operation is achieved by limiting the highest current i_3. Figure 5.11(b) and (c) show both capacitor voltages V_{c1} and V_{c2}, respectively. Finally, both PWM_1 and PWM_2 signals are shown in Figures 5.11(d) and (e), respectively.

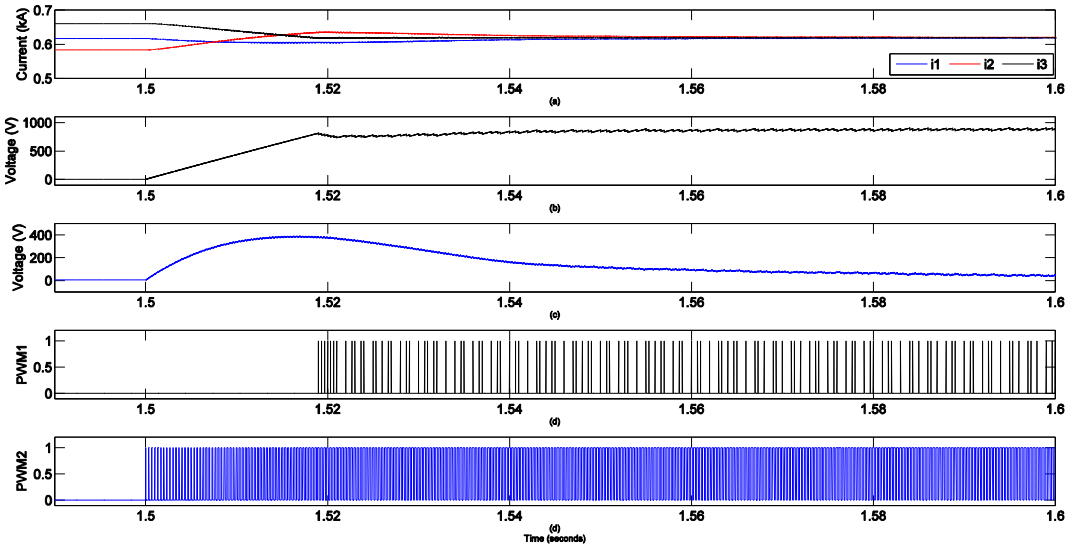


Figure 5.11 MCFC currents balancing - mode 3. (a) Cable currents, (b) Capacitor voltage V_{c1}, (c) Capacitor voltage V_{c2}, (d) PWM_1 signal, (e) PWM_2 signal.

By comparing these simulation results with the one shown earlier in Chapter 4 for the three-port CFC extended topology, the MCFC offers more accurate results as an additional capacitor is introduced. Each current is controlled with a dedicated capacitor leading to better performance specially when there are significant differences in magnitude between the currents being controlled.

5.7.2 MCFC: setting currents i_1 and i_3

The proposed MCFC topology indicates that for each controlled current a dedicated capacitor is needed; this fact adds independent control opportunity for each controlled current. A simulation case is proposed to validate this concept, where currents i_1, i_2 and i_3 are set to be initially 640 A, 570A and 660 A, respectively. It is required to operate the CFC such that it limits both currents i_1 and i_3 to 600 A. This can be achieved by connecting the capacitor C_1 in series with cable 3 and capacitor

C_2 in series with cable 1. The MCFC *switched on at t= 1.5 s*, *Figure 5.12 (a)*, (b), (c), (d) and (e) show cable currents, capacitor voltage V_{c1}, capacitor voltage V_{c2}, PWM_1 signal and PWM_2 signal, respectively. These figures show that the controller succeeded in limiting the two currents, i_1 and i_3, to reach the predefined reference value. As both currents i_1 and i_3 are decreased throughout the MCFC operation, current i_2 increases consequently to achieve the balance in the grid.

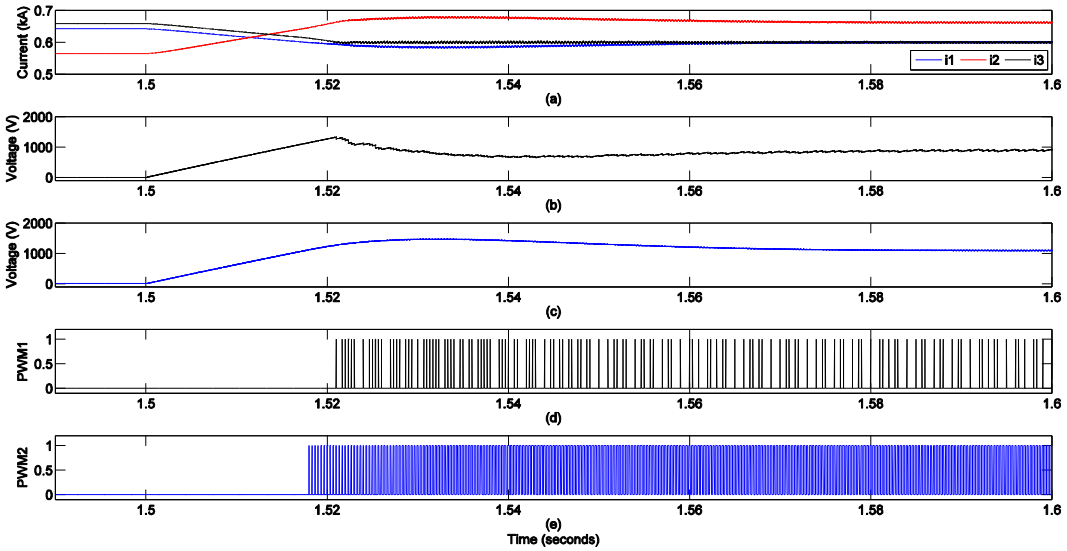


Figure 5.12 MCFC currents i_1 and i_3 setting. (a) Cable currents, (b) Capacitor voltage V_{c1}, (c) Capacitor voltage V_{c2}, (d) PWM_1 signal, (e) PWM_2 signal

5.7.3 MCFC: currents nulling

Another case study is presented in this subsection, where dual functionality of the proposed three-port MCFC is demonstrated. Currents i_3 and i_1 are both to be controlled, the first is to be set to 600 A while the second is to be ramped to zero. The three cable currents are shown in Figure 5.13(a) where the MCFC is switched on at t= 1.5 s and successfully performs the desired task. For current i_3, Figure 5.13(b) and (d) show the relevant capacitor voltage V_{c1} and PWM_1 signal, respectively. These figures show that the capacitor voltage reaches a maximum value of 2.2 kV. Similarly, for current i_1, Figure 5.13(c) and (e) show the relevant capacitor voltage V_{c2} and PWM_2 signal, respectively. The PWM_2 signal is equal to

zero as the capacitor C_2 is connected in series with cable 1 to charge to 4.1 kV and block the current flowing.

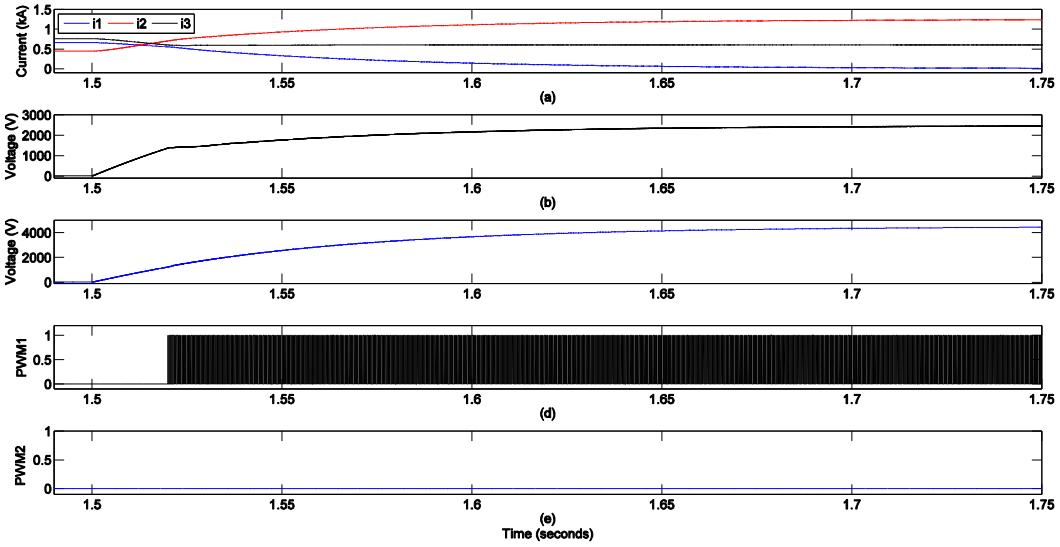


Figure 5.13 MCFC nulling i_3 and setting i_1. (a) Cable currents, (b) Capacitor voltage V_{c1}, (c) Capacitor voltage V_{c2}, (d) PWM_1 signal, (e) PWM_2 signal

More simulation results for MCFC tested in a VSC based four terminals MTDC grid are presented in Appendix B.2.

5.8 Summary

This chapter presents a generalized MCFC topology that can be installed in a MTDC to control currents flowing in any number of cables. The proposed topology succeeded in solving the limitations introduced by the extended topology proposed in chapter 4. In addition, introducing two capacitors instead of one in the three-port topology not only enhanced the performance in currents balancing, but also introduced dual functionality ability where each capacitor can be used to control a cable current independently. A reduced switch count topology is also proposed in this chapter where the switches and diodes responsible for reverse current control are eliminated, offering lower cost and smaller footprint MCFC in cases of

unidirectional power flow control. The proposed MCFC is simulated in different case studies and accurate results and fast dynamic performance are noticed. The validated proposed MCFC topology revealed that it can be used in real MTDC grid current flow control applications.

Chapter

6

Experimental Validation

6.1 Introduction

To obtain experimental results and validate the MCFC topologies and control strategies proposed in this research project, a scaled down laboratory MCFC prototype is designed and built. The prototype is tested in a scaled down three and four MTDC grids. Two different physical controllers are used: OPAL RT OP4500 real-time simulator and NI-Crio real-time FPGA-based controller to acquire the measurement signals and provide the IGBTs with all the firing signals based on the current operating mode. A graphical user interface (GUI) is designed for each controller in order to facilitate the control of all MCFC parameters and switch between the two proposed control strategies during operation. Experimental results for two-port CFC, extended topology three-port CFC, and three-port MCFC are obtained and presented in this chapter.

6.2 Experimental System Configuration

6.2.1 Scaled down MTDC grid

A scaled down MTDC grid is prepared to allow realistic testing of the proposed MCFC control and topologies as shown in Figure 6.1. The grid consists of one generating terminal based on DC power supplies with a rating of up to 150 VDC, and two/three load terminals each connected to an electronic active load. Electronic loads give the flexibility of precisely controlling the flowing current in each cable and mimicking instantaneous load variations when compared with passive loads. The load terminals are programmed to apply sudden load changes in order to test the developed MCFC mode detection and change control algorithm. More details of the experimental setup are available in Appendix C.

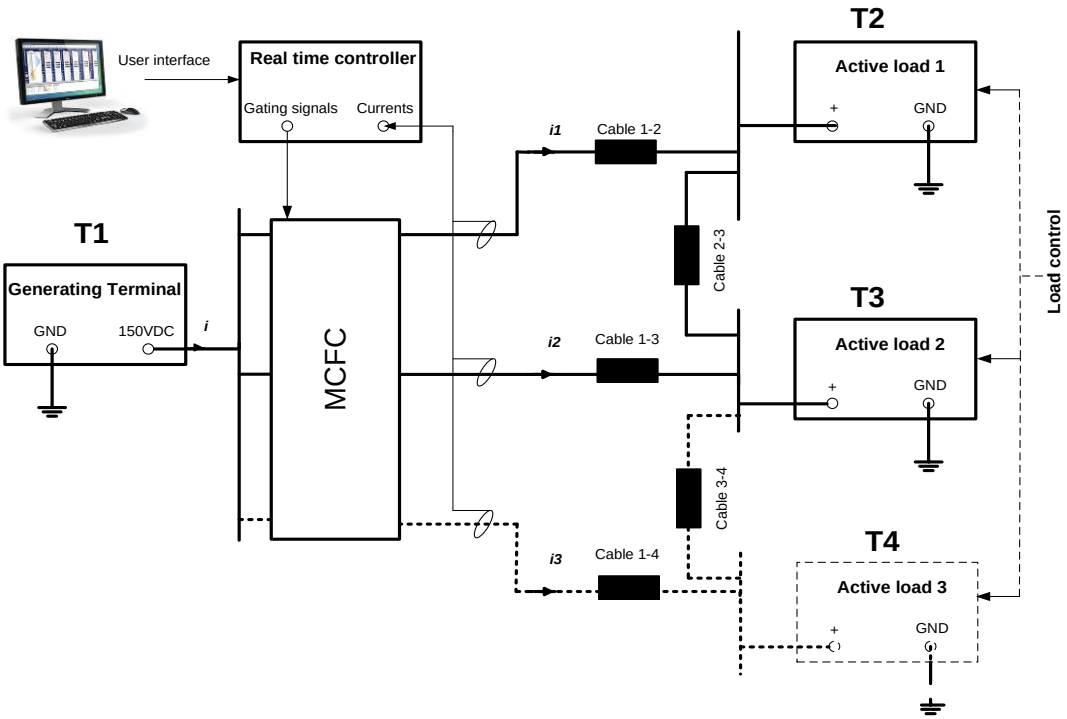


Figure 6.1: Three and four-terminal MTDC grid schematic diagram.

6.2.2 MCFC prototype

The submodule circuit is designed using the Proteus software package as shown in Figure 6.2 and is produced using a printed circuit board milling CNC machine. Each submodule contains four IGBTs, each with its own gate driving circuit and isolated power supply. The main role of the gate driving circuit is to provide optical isolation between both the low power control signal side and high power switch side and the supply switches with the required power. The current-measurement amplification circuit is designed for signal conditioning purposes.

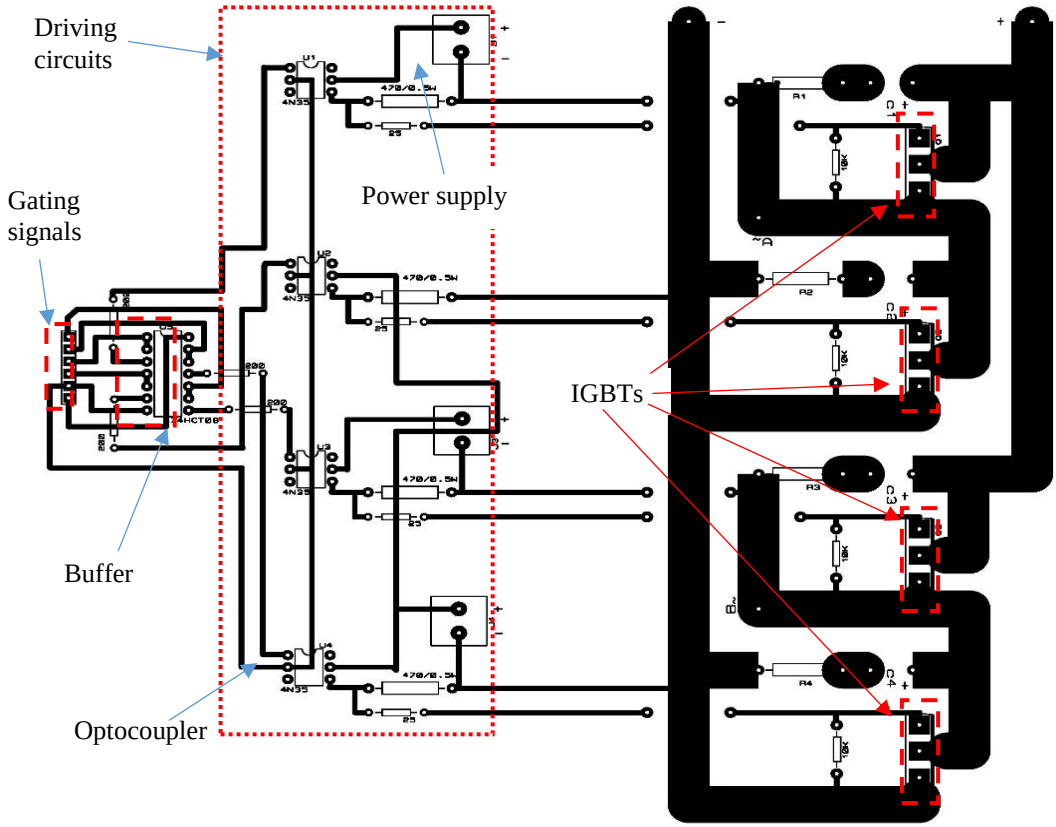


Figure 6.2: MCFC submodule schematic diagram.

6.2.3 Controllers and user interface

The MCFC prototype is tested using two different controllers. The first controller is the OP4500 Opal real-time simulator. The programming is carried out by building the control algorithms in the MATLAB/SIMULINK environment and then transferring them to the OP4500. This type of control is termed a rapid control prototyping (RCP), as modifications can be done quickly through the model, and all simulation parameters can be controlled online during operation. The full setup of the three-port MCFC controlled via OP4500 is shown in Figure 6.3.

The second controller used is the FPGA-based National Instruments (NI) Compact Rio (Crio) real-time controller. The programming is carried out using the LABVIEW simulation environment and then the developed code is compiled and translated into VHDL and transferred to the FPGA. The full setup is shown in Figure 6.4.

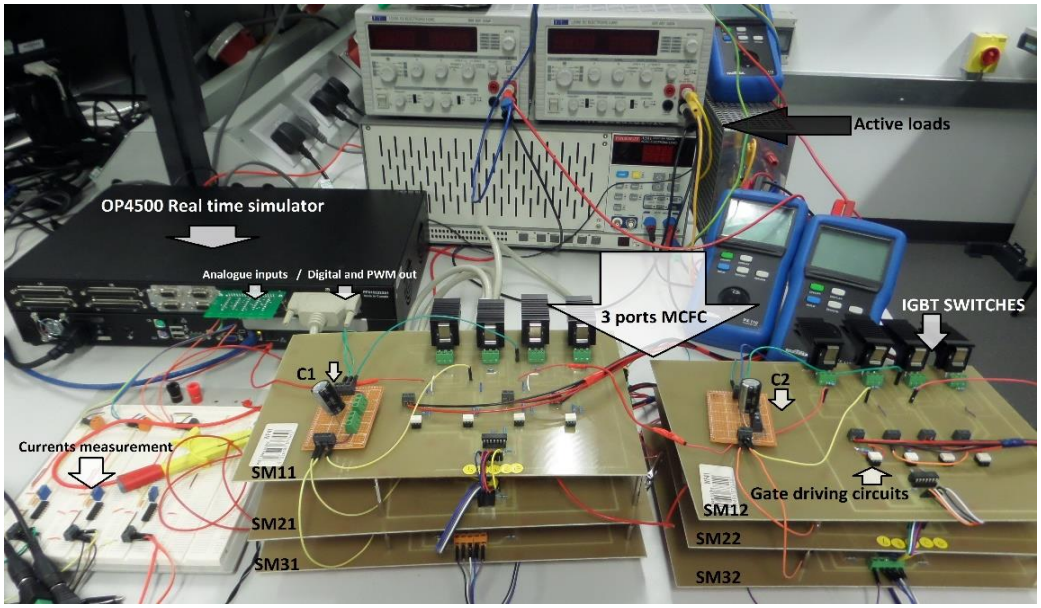


Figure 6.3: MCFC with OP4500 controller experimental setup.

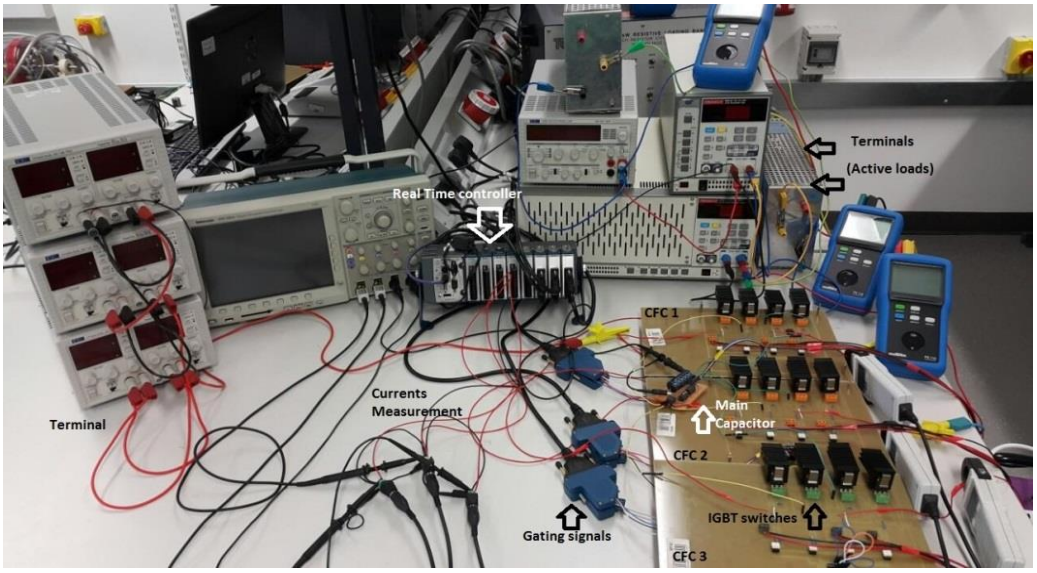
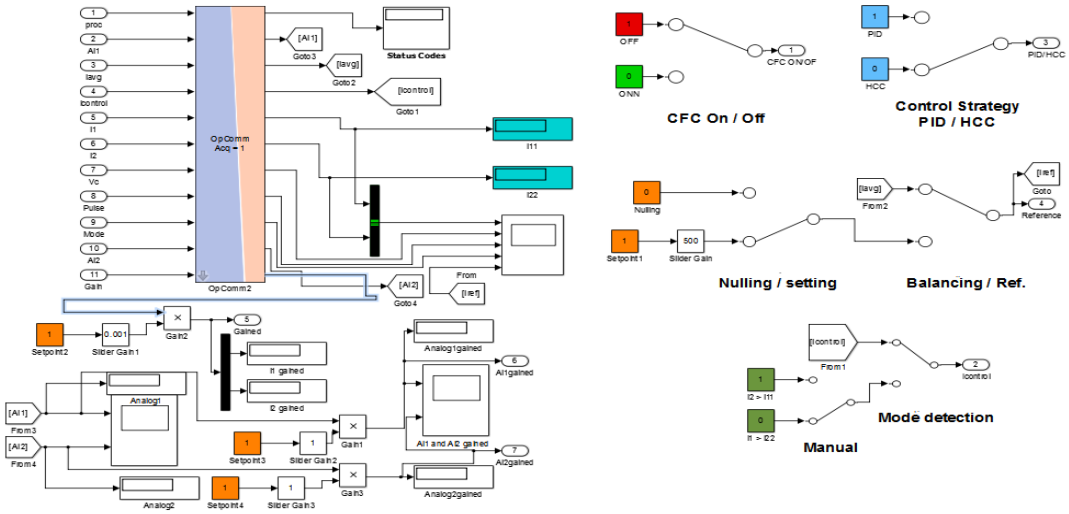
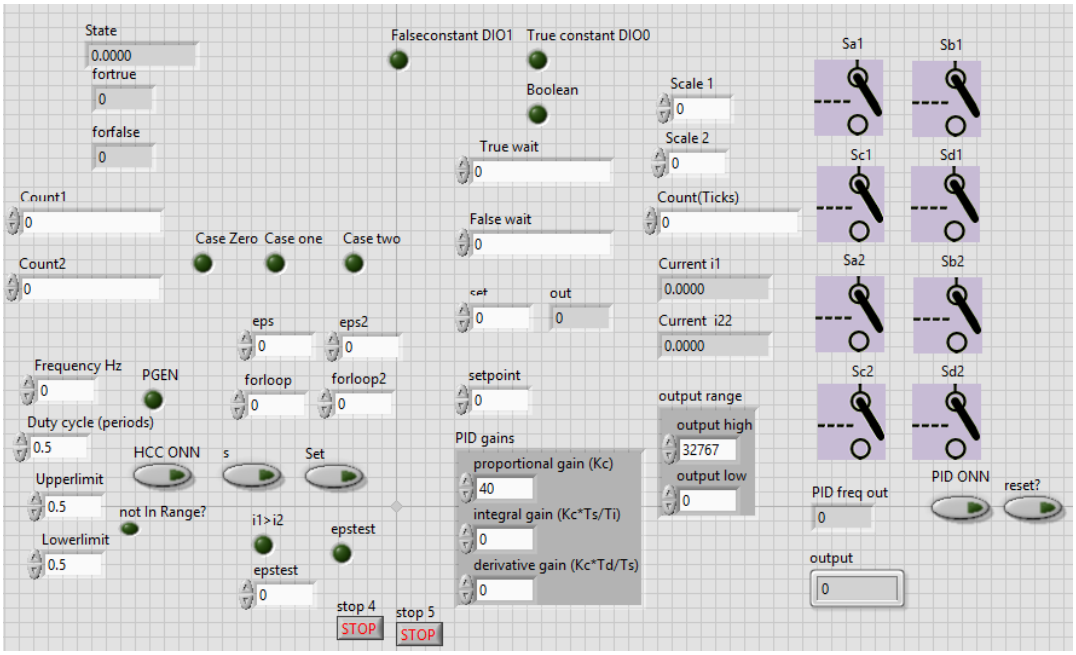


Figure 6.4: Extended topology CFC with NI-Crio controller experimental setup.

For each controller, a GUI is designed in order to provide online control of the MCFC. Through this interface, the user can turn on/off the MCFC, swap between control strategies HCC/PID, change any desired control parameter, choose the MCFC function, and monitor current magnitudes and present the operating mode. Figure 6.5(a) and Figure 6.5(b) show both the developed GUIs.



(a)



(b)

Figure 6.5: User interface: (a) MATLAB, (b) LABVIEW.

6.3 Experimental Results

The prototype is used to test the dynamic and steady state performance of the proposed MCFC control strategies and topologies. Table 6-1 shows the main parameters of the experimental setup. In the following subsections, two-port, extended three-port, and modular three-port CFC will be tested.

Table 6-1: Laboratory test prototype main parameters.

Parameter	Value
Terminal 1	70 – 150 V dc Power supply
Terminal 2	Prodigit 3261 300 V/18 A Active load
Terminal 3	Prodigit 3251 150 V/8A Active load
Terminal 4	80V Active load
Cables resistance	1.2 Ohm
Cables inductance	1 mH
CFC capacitor	1 mF
N-channel IGBT	HGTG10N60A4D – 70 A – 600 V
Proportional gain	150
Integral gain	0.01
Controller time cycle	25nS

6.3.1 Two-port CFC

6.3.1.1 Current balancing and limiting using PID controller

Currents i1 and i2 are initially set to 3 A and 2.2 A, respectively. The CFC is switched on to perform the current-balancing operation. Figure 6.6 (a) and Figure 6.6 (b) show the currents, capacitor voltage, and PWM signal at two different time scales. The switching frequency has a value of approximately 1.5 kHz. Figure 6.6 (c) shows the same operation but with a sudden load change where i1 drops from 3 A to 2.9 A and i2 drops from 2.2 A to 1.2 A. As the difference between the two currents has significantly increased after the load change, the capacitor voltage has increased from 4 V to 6 V to maintain the current-balancing process.

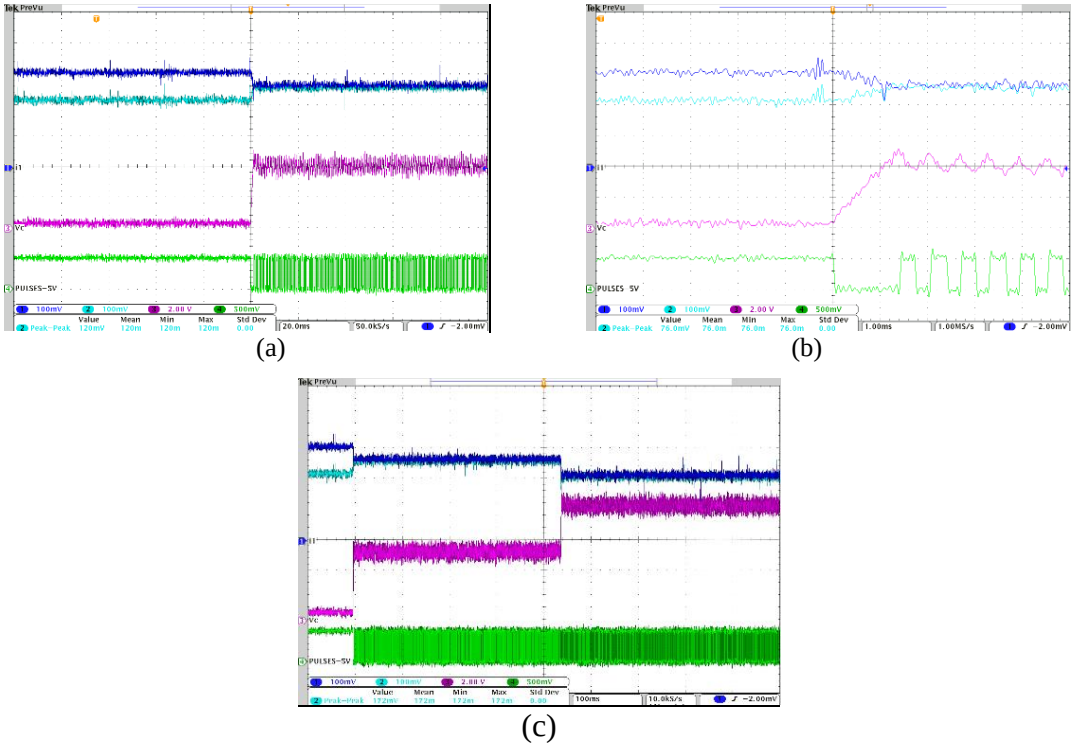
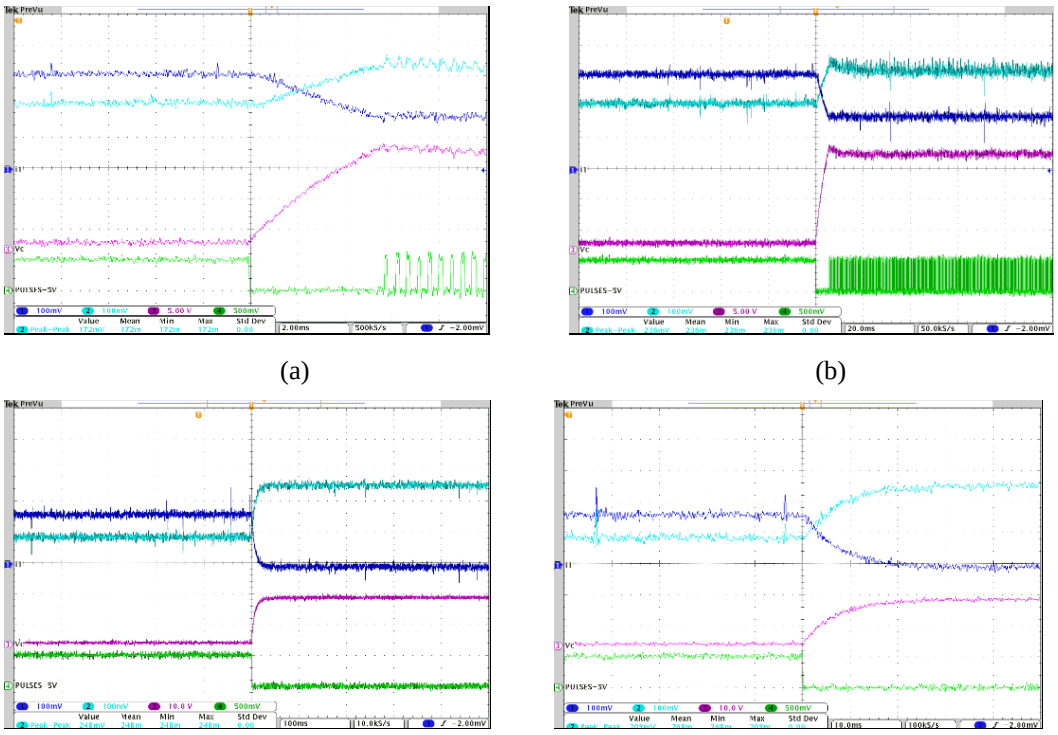


Figure 6.6: Current balancing (Y axis: 1 A/Div for i1 and i2, 2 V/Div for Vc, and 5 V/Div for PWM): (a) balancing i1 into i2 (X axis: 20 ms/Div), (b) balancing i1 into i2 (X axis: 1 ms/Div), (c) sudden load change (X axis: 100 ms/Div).

To test the current limiting capabilities, the CFC is supplied by a reference value of 1.7 A for current i1, as shown in Figure 6.7 (a) andFigure 6.7 (b). The CFC succeeded in injecting the required voltage in series with cable 1 to follow the reference signal where the capacitor voltage in this case is equal to 10 V. Similarly, Figure 6.7(a) and Figure 6.7 (b) show the same operation but with reference signal zero in order to dampen the current i1. The CFC capacitor fully charges, and once the CFC is switched on, the PWM signals are equal to zero to allow the capacitor to remain connected to cable 1.



(a) (b)

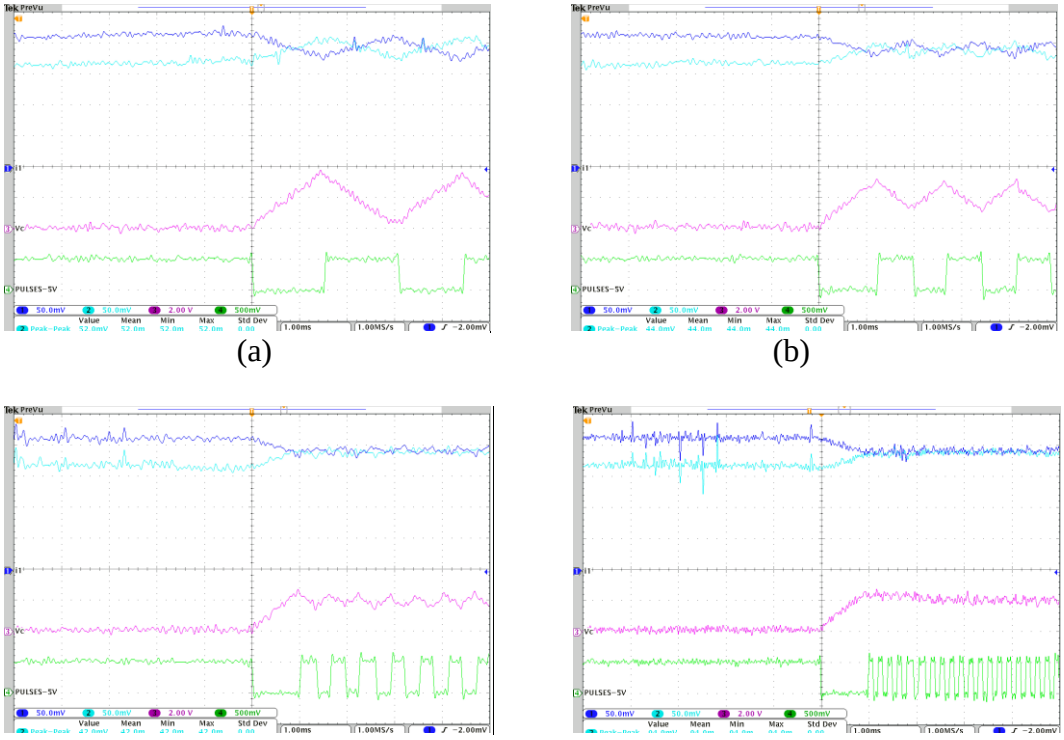
(c) (d)

Figure 6.7: Current limiting (Y axis: 1 A/Div for i1 and i2, 5 V/Div and 10 V/Div for Vc, and 5 V/Div for PWM): (a) setting i1 to 1.7 A (X axis: 2 ms/Div), (b) setting i1 to 1.7 A (X axis: 20 ms/Div), (c) nulling i1 (X axis: 100 ms/ Div), (d) Nulling i1 (X axis: 10 ms/Div).

6.3.1.2 Testing of HCC

Another control strategy for the CFC discussed earlier in Chapter 4 is generating the PWM signals using HCC. To investigate the effect of varying the HB, four case studies are presented in Figure 6.8(a), Figure 6.8(b), Figure 6.8(c) and Figure 6.8(d) with hysteresis bands of 150 mA, 80 mA, 30 mA, and 5 mA, respectively. In each of the figures, current i1, current i2, capacitor voltage Vc, and generated pulses are demonstrated. In Figure 6.8(a), as the HB is very high, the current ripple is very high as well as the capacitor voltage ripple, which is approximately equal to 4 V in this case. On the other hand, the switching frequency is very low with a value of 300 Hz. By decreasing the HB to 80 mA, the voltage ripples have decreased to 2 V, and the switching frequency has increased to 650 Hz, as shown in Figure 6.8(b). Figure 6.8(c) shows the result of decreasing the HB to a lower value of 30 mA. In the final

case, when applying a 5 mA HB, the voltage ripples are minimised to approximately 0.4 V because of the switching frequency, which has significantly increased to 4.5 kHz, as indicated in Figure 6.8 (d). The current-balancing operation is most accurate and both the capacitor peak voltage and voltage ripples are minimum when the CFC is operated at the lowest possible HB. Decreasing the HB allows the control loop to track the reference current as closely as possible, incurring higher switching frequencies and thus higher switching losses. However, acceptable results can be obtained with low switching frequencies, as shown in Figure 6.8(c), and the maximum switching frequency can always be limited to the desired value through the controller programming process.



(a) (b)

(c) (d)

Figure 6.8: Current limiting (Y axis: 0.5 A/Div for i1 and i2, 2 V/Div for Vc, and 5 V/Div for PWM. X axis: 1 ms/Div): (a) balancing currents HB = 150 mA, (b) balancing currents HB = 80 mA, (c) balancing currents HB = 30 mA, (d) balancing currents HB = 5 mA.

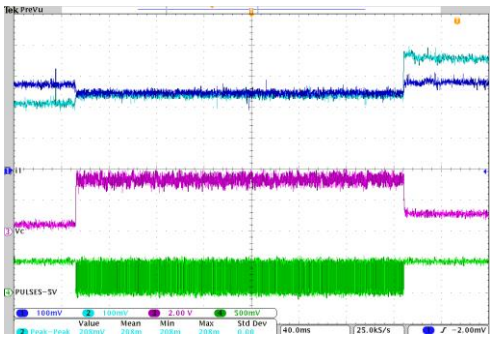
6.3.1.3 Mode detection and changing algorithm

The mode detection algorithm is developed using both SIMULINK and LABVIEW and is programmed using both OP4500 and Crio. A sudden mode load change is

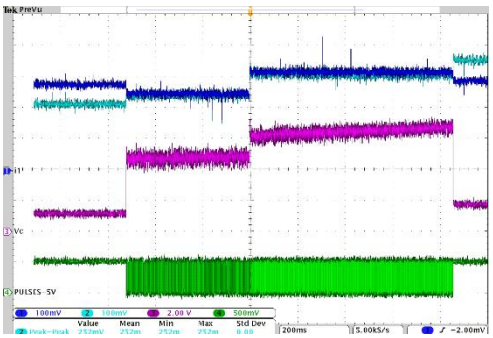
applied during the CFC current-balancing operation to investigate the performance of the proposed mode detection and change algorithm. A case is presented where the CFC is successfully operating in mode 1, which balances both currents i1 and i2 with values 2.7 A and 2.2 A, respectively. A load change is applied such that the new values of i1 and i2 are 2.8 A and 3.6 A, respectively, leading to operation in mode 2. Figure 6.9(a) illustrates that, without activating the mode detection algorithm, the balancing operation will stop under the sudden load change as the CFC continues with the wrong switching states.

In Figure 6.9(b), the proposed mode detection and change algorithm is activated, and for the same case study, the mode change is detected instantaneously, and the current-balancing operation continuous fluently. Due to the high difference in the currents that resulted due to the mode change process, the capacitor voltage consequently increases to maintain balanced currents. A closer view is shown in Figure 6.9(c) for the same case, where once i2 increased and crossed the predefined window, the CFC can detect the mode change. Figure 6.9(d) shows a similar case where the CFC is already operating in mode 2, and a load change is applied to swap the current values and to change the operating mode to 1. In this case, the CFC turn off time is inserted as 100 ms to show how the mode detection and change algorithm perform.

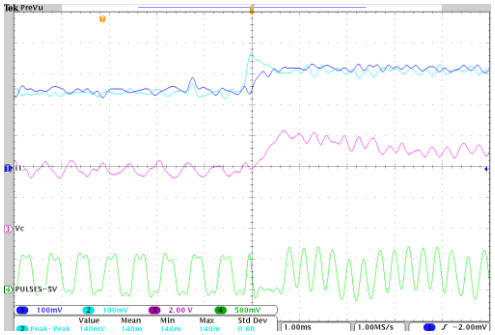
The same proposed algorithm can be expanded easily to be applied to n-port MCFCs and can be designed based on the desired operating conditions.



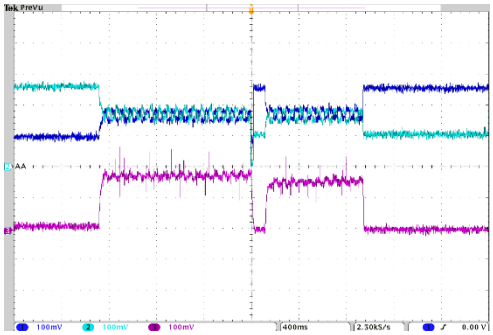
(a)



(b)



(c)



(d)

Figure 6.9: Mode detection (Y axis: 1 A/Div for i1 and i2, 2 V/Div for Vc, and 5 V/Div for PWM): (a) mode change without detection (X axis: 40 ms/Div), (b) mode change with detection (X axis: 200 ms/Div), (c) mode change with detection (X axis: 1 ms/Div), (d) mode change with 100 ms CFC off time (X axis: 400 ms/Div).

6.3.1.4 Effect of varying capacitance

The CFC capacitor is one of the key elements in designing the CFC, and as discussed in Chapter 4, the value of the capacitor can be estimated based on the network parameters. An experimental case study is proposed with four different capacitor values and a fixed 30 mA HB, in order to investigate the effect of varying the capacitance and its effect on the functionalities and performance of the CFC. By installing a very low capacitor in the CFC with a value of 47 uF, Figure 6.10(a) shows that the small capacitance increases the capacitor voltage to a value of 8 V, high current ripples, and high voltage ripples, leading to poor performance. Installing a small capacitor also increases the switching frequency, which reaches 3 kHz in this case. By increasing the capacitor value to 220 uF and 1 mF, as shown in Figure 6.10(b) and Figure 6.10(c), respectively, the capacitor voltage has decreased to 2.8 V and 2.2 V, respectively. Finally, a large 9.6 mF capacitor is installed, and the results are shown in Figure 6.10(d), where the minimum current and voltage ripples are observed. The capacitor voltage is equal to 2 V, and the switching frequency has dropped to 875 Hz in this scenario.

As implied by the results, the CFC capacitor must be chosen with a value that is as high as possible. Higher capacitance provides smoother CFC operation with minimum capacitor voltage and low current and voltage ripples. Another advantage

of installing a large capacitor is minimising the switching frequency, which leads to minimising the switching losses.

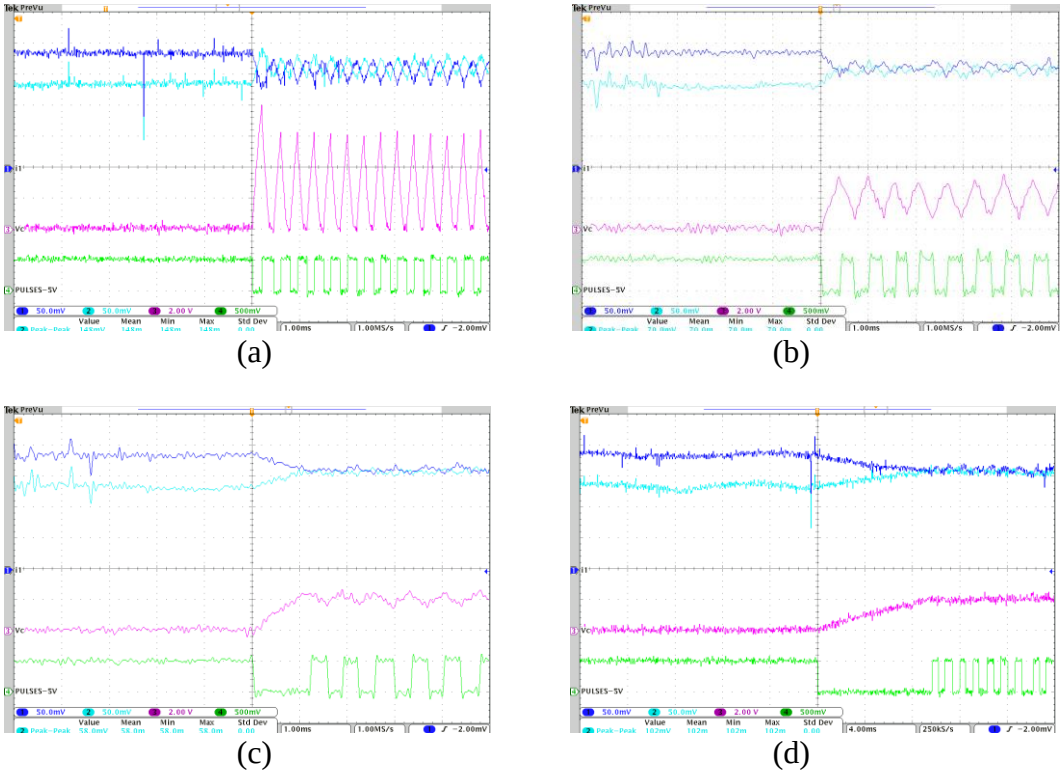
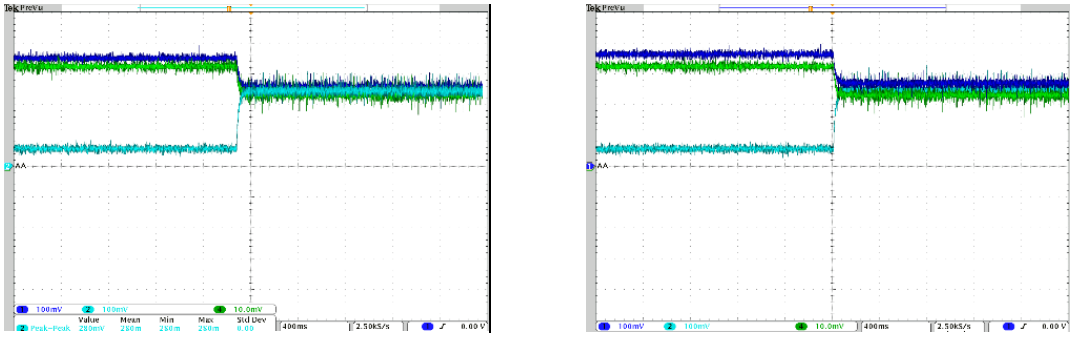


Figure 6.10: Effect of CFC capacitor value (Y axis: 0.5 A/Div for i1 and i2, 2 V/Div for Vc, and 5 V/Div for PWM): (a) CFC capacitor = 47 uF (X axis: 1 ms/Div), (b) CFC capacitor = 220 uF (X axis: 1 ms/Div), (c) CFC capacitor = 1 mF (X axis: 1 ms/Div), (d) CFC capacitor = 9.6 mF (X axis: 4 ms/Div).

6.3.2 Extended three-port CFC

The proposed extended topology is tested by building a three-port CFC prototype, using three submodules and a single capacitor, as shown earlier in Figure 6.4. A case study is presented where i1, i2, and i3 are initially equal to 3.5 A, 0.5 A, and 3.2 A, respectively, as shown in Figure 6.11(a). The CFC is switched on to operate in mode 6 and performs the current-balancing operation, providing satisfactory results. By changing the values of i1 and i3 to 3.7 A and 3.1 A, respectively, the drawback of this extended topology starts to appear, as illustrated in Figure 6.11(b). When the single capacitor is inserted in series with both cables 1 and 3 at the same time, both

currents i1 and i3 will decrease by the same amount and hence maintain the difference between them, which may not result in an optimum balancing operation.



(a) (b)

Figure 6.11: Extended topology (Y axis: 1 A/Div for i1, i2 and i3, X axis: 400 ms/Div): (a) low differences in current (b) high differences in current.

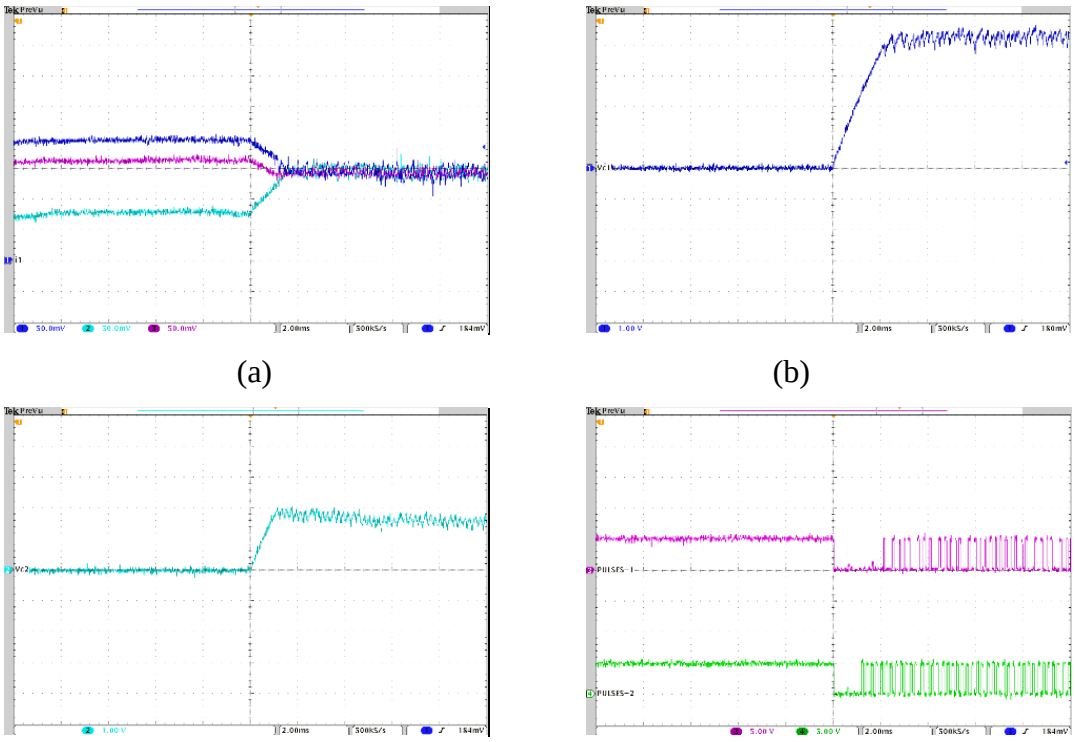
6.3.3 Three-port MCFC

In this subsection, a three-port MCFC prototype is built using six submodules and two single capacitors, as shown earlier in Figure 6.3. Three case studies are presented to evaluate the performance and validate the proposed topology.

6.3.3.1 MCFC current balancing

Cable currents i1, i2, and i3 are initially equal to 2A, 0.75 A, and 1.75 A, respectively. The MCFC is turned on to perform the current-balancing operation in mode 3, as illustrated in Figure 6.12(a). The currents are balanced successfully to an approximate value of 1.5 A. Capacitor voltages, in this case Vc1 and Vc2, are portrayed in Figure 6.12(b) and Figure 6.12(c), respectively. Additionally, Vc1 is higher than Vc2, as current i1 is relatively higher than current i3. Finally, the two PWM signals, P1 and P2, are shown in Figure 6.12(d) where P2 starts switching earlier than P1, as current i3 is closer to the reference value than i1.

The results from this case study can be compared to extended topology results presented in the previous section, where currents can be controlled independently based on their values and very accurate performance can be obtained by dedicating a single capacitor with its dependant control circuit for each cable.



(a) (b)

(c) (d)

Figure 6.12: Current balancing – three-port MCFC (Y axis: 0.5 A/Div for i1, i2, and i3, 1 V/Div for Vc, and 5 V/Div for PWM, X axis: 2 ms/Div): (a) balanced currents, (b) capacitor voltage Vc1, (c) capacitor voltage Vc2, (d) PWM signals P1 and P2.

6.3.3.2 MCFC current setting

Another case study is presented where currents i1 and i2 are the higher currents (mode 1) and the reference values of the controllers are set as zero for i1 and 1.25 A for i2. The proposed MCFC succeeds in nulling current i1 and setting current i2 at the desired value, as demonstrated in Figure 6.13(a); i3 is increased to a value that maintains the energy balance in the grid. The corresponding capacitor voltages, Vc1 and Vc2, are presented in Figure 6.13(b) and Figure 6.13(c), respectively. The capacitor C1 is charged to block current i1. The relevant PWM signals are shown in Figure 6.14(d), where P1 remains zero to allow C1 to charge from cable 1, and P2 is the pulse width, modulated to let i2 achieve the required set-point value. Fluent operation of the MCFC can be noticed.

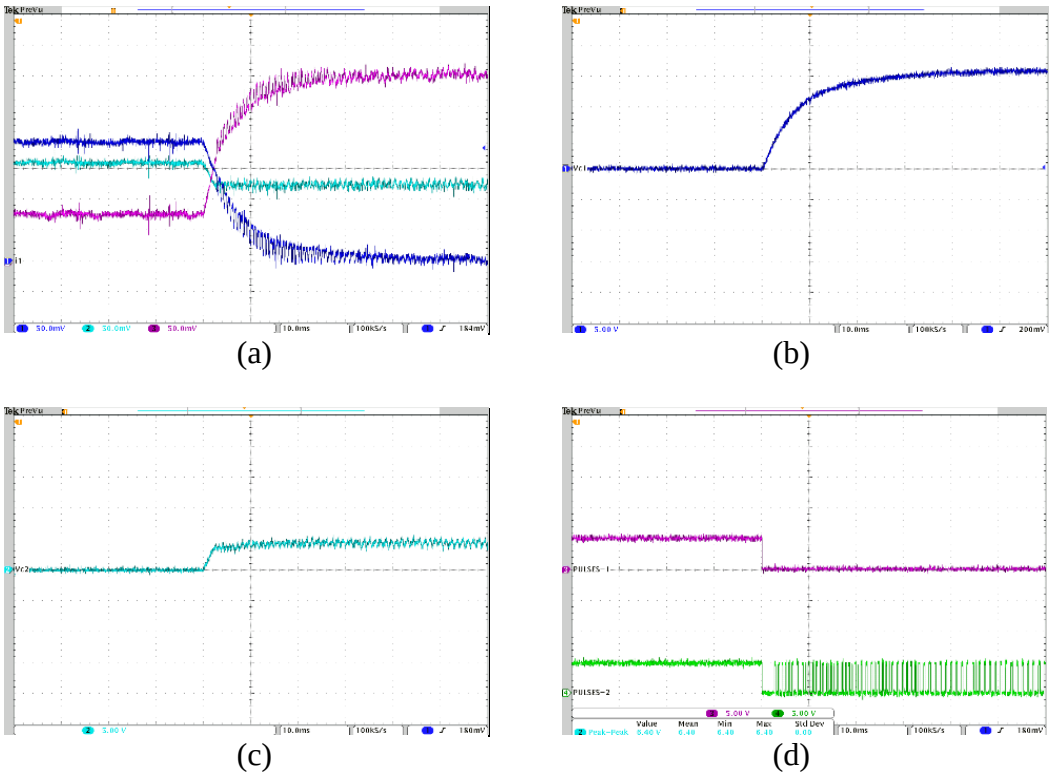
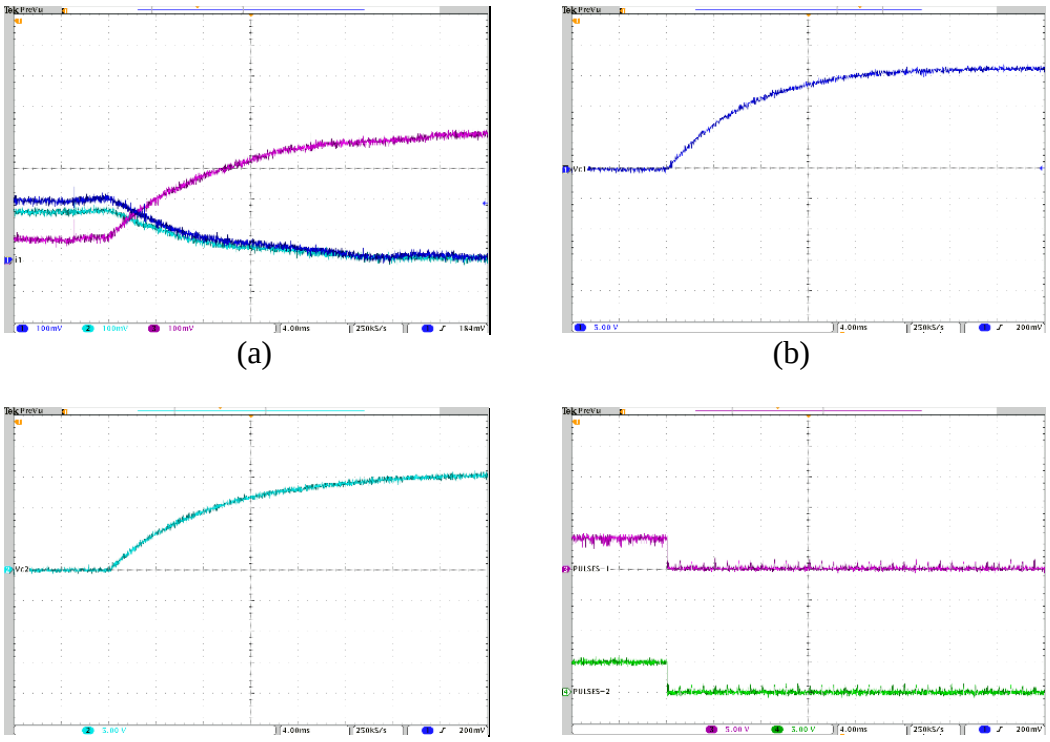


Figure 6.13: Setting i2 and nulling i1 – MCFC (Y axis: 0.5 A/Div for i1, i2, and i3, 5 V/Div for Vc, and 5 V/Div for PWM, X axis: 10 ms/Div): (a) cable currents, (b) capacitor voltage Vc1, (c) capacitor voltage Vc2, (d) PWM signals P1 and P2.

6.3.3.3 MCFC current nulling

Similarly, both reference values of currents i1 and i2 are set to zero to ramp both currents down to zero. For this case, currents i1, i2, and i3 are presented in Figure 6.14(a). Capacitor voltages Vc1 and Vc2 are shown in Figure 6.14(b) and Figure 6.14(c), and both capacitors charge to block currents flowing in cables 1 and 2. The PWM signals are shown in Figure 6.14(d), as both signals are equal to zero all the time to keep capacitors C1 and C2 connected in series with cables 1 and 2, respectively.



(a) (b)

(c) (d)

Figure 6.14: Nulling i1and i2 – MCFC (Y axis: 1 A/Div for i1, i2, and i3, 5 V/Div for Vc, and 5 V/Div for PWM, X axis: 4 ms/Div): (a) cable currents, (b) capacitor voltage Vc1, (c) capacitor voltage Vc2, (d) PWM signals P1 and P2.

6.4 Summary

In this chapter, the details of designing and building the scaled down CFC and MCFC prototypes are explained in detail. Proposed modes of operation and control strategies for the CFC are validated using the experimental prototype. The effect of varying the CFC's capacitor value is demonstrated, and it is concluded that larger capacitors give better performance, and less capacitor peak voltage and current ripples are experienced. The HCC is tested closely under several different HB values, and the results indicated that lower HB values give more accurate performance because of the increase of switching frequency and losses.

Finally, both the proposed extended three-port CFC and the MCFC topology are tested, and more accurate results are achieved with the MCFC, when comparing their results. In addition, the dual functionality offered by the three-port MCFC is demonstrated in simultaneously controlling the cable currents.

Chapter

7

Conclusions

7.1 Conclusions

The concept of forming Multi Terminal HVDC grids is being considered due to the increase of offshore wind farms recently in the North Sea area. As a result, researchers and industry leaders biased their work towards solving emerging challenges that prevent the idea of multi terminal super grids from being established reliably. The difference in characteristics between AC and DC power prevents the use of available AC power system protection schemes, circuit breakers, transformers and power flow control methods with new DC grids.

In this thesis, AC/DC converter topologies and MT-HVDC grids configurations are reviewed. Available power and current flow control methods are investigated as well, and methods such as voltage droop control, voltage margin control, insertion of series resistors, insertion of series voltage sources and utilization of AC/DC converters are investigated. Furthermore, operating modes, a dynamic mathematical model and control schemes are developed for a two-port CFC and validated using both computer simulation and scaled down laboratory experiments. The CFC capacitor and IGBTs are subjected to relatively low voltage when compared the grid rated voltage, resulting in low cost and small footprint of the CFC, giving it superiority as a solution for offshore installations. A number of functionalities such as currents balancing, current limiting, and current nulling of the CFC are discussed and evaluated. Results shows that the proposed CFC can be utilized reliably for the current flow control applications in multi-terminal HVDC systems. A three-port extended topology is proposed along with its relevant modes of operation and control circuit. This simple extended topology gave acceptable results only in cases where the controlled currents are close in magnitude; as it utilizes only one capacitor no matter how many ports it has. To overcome this drawback, a new generalized modular CFC topology is proposed with the aim to allow each current to be controlled with a dedicated capacitor and a control circuit with an independent reference signal. Furthermore, a reduced switched count topology is proposed cutting the cost and footprint of the MCFC to half in cases of unidirectional current

flow control. The proposed MCFC topologies are tested in three-port configuration using both computer simulation and experimental prototyping. The MCFC revealed its ability to control subject currents accurately and independently when compared to the extended topology. Fast dynamic response and accurate performance of the proposed MCFC are explored and results show that the newly proposed MCFC topology, control and operation offer a low cost - small footprint promising solutions for next generations DC grids current flow control problems. The produced work forms solid ground for further research and development in this area.

7.2 Summary of Contributions

The summary of contributions achieved in this project is listed below:

- Conducting a detailed review on AC/DC converter topologies, MT-HVDC grid configuration and available power and current control methods in the literature.
- Development of operating modes, mathematical model and two control strategies based on PI and HCC for the two-port current flow controller and validating them through computer simulation and experimental prototyping.
- Conducting a single capacitor extended CFC topology, and highlighting its advantages and drawbacks.
- Design of an automatic operating mode detection and changing control unit, allowing continuous operation of the CFC during load variations that may lead to sudden operating mode changes.
- Development of a modular generalized topology for the CFC, allowing it to be applied in more complex MTDC grids, and solving the drawbacks generated from the single capacitor extended CFC topology where independent currents control is achieved accurately.

- Proposing a reduced switches count topology, which may reduce the cost and footprint of the MCFC by half in cases of unidirectional current control.

7.3 Recommendation for Future Research

The author recommendations for future research are as follows:

- Investigation of the CFC ability to contribute to DC protection.
- Finding out the necessity of deploying more than one MCFC in large MTDC grids and whether a master control unit will be needed.
- Investigation of the effect of CFC on power system stability.
- Determine the significance of incorporating Artificial Intelligent (AI) control strategies such as Artificial Neural Networks (ANN) on the mode detection and change control unit.
- Quantitative evaluation of MCFC operating losses under different operating modes and conducting a detailed comparison with losses resulting from AC/DC and DC/DC converters performing similar tasks.

References

[1] ‘International Energy Outlook 2016-Electricity - Energy Information Administration’.[Online].Available:http://www.eia.gov/forecasts/ieo/electricity.cfm. [Accessed: 28-Jun-2016].

[2] ‘Global Warming’s Terrifying New Chemistry’, The Nation. [Online]. Availble: https://www.thenation.com/article/global-warming-terrifying-new-chemistry/.[Accessed: 20-Jun-2016]

[3] ‘The End Of Fossil Fuels - Our Green Energy - Ecotricity’. [Online]. Available: https://www.ecotricity.co.uk/our-green-energy/energy-independence/the-end-of-fossil-fuels. [Accessed: 28-Jun-2016].

[4] ‘Cost & Benefits Analyses - Nuclear Energy Institute’. [Online]. Available: http://www.nei.org/Issues-Policy/Economics/Cost-Benefits-Analyses. [Accessed: 28-Jun-2016].

[5] ‘Timeline: Nuclear plant accidents’, BBC News. [Online]. Available: http://www.bbc.co.uk/news/world-13047267. [Accessed: 28-Jun-2016].

[6] A. Press, ‘Germany votes to end nuclear power by 2022’, The Guardian, 30-Jun-2011.

[7]‘EWEA.Annual.Statistics.2015’.[Online].Availble:http://www.ewea.org/fileadmin/files/library/publications/statistics/EWEA-Annual-Statistics-2015.pdf

[8] P. Alamdari, O. Nematollahi, and M. Mirhosseini, ‘Assessment of wind energy in Iran: A review’, Renew. Sustain. Energy Rev., vol. 16, no. 1, pp. 836–860, Jan. 2012.

[9] T. Ackermann and L. Söder, ‘An overview of wind energy-status 2002’, Renew. Sustain. Energy Rev., vol. 6, no. 1–2, pp. 67–127, 2002.

[10] A. Hepbasli and O. Ozgener, ‘A review on the development of wind energy in Turkey’, Renew. Sustain. Energy Rev., vol. 8, no. 3, pp. 257–276, Jun. 2004.

[11] B. Rabelo and W. Hofmann, ‘Wind generator control in compliance with new norms’, in 2003 IEEE International Symposium on Industrial Electronics, 2003. ISIE ’03, 2003, vol. 2, pp. 798–803 vol. 2.

[12] ‘EDF Energy Renewables - FAQ’. [Online]. Available: http://www.edf-er.com/AboutWindEnergy/FAQ.aspx. [Accessed: 03-July-2016].

[13] ‘Wind energy frequently asked questions (FAQ)| EWEA’. [Online]. Available: http://www.ewea.org/wind-energy-basics/faq/. [Accessed: 09-May-2016].

[14] "V164-8.0 MW breaks world record for wind energy production". [Online]. Available:http://www.mhivestasoffshore.com/wp-content/uploads/2015/03/21-10-2014-Press-release.pdf. [Accessed: 20-May-2016]

[15] F. Blaabjerg and K. Ma, ‘Future on Power Electronics for Wind Turbine Systems’, IEEE J. Emerg. Sel. Top. Power Electron., vol. 1, no. 3, pp. 139–152, Sep. 2013.

[16] B. Grainger and T. Thorogood, ‘Beyond the harbour wall [offshore wind farm]’, IEE Rev., vol. 47, no. 2, pp. 13–17, Mar. 2001.

[17] ‘Europe’s onshore and offshore wind energy potential — European Environment.Agency’.[Online].Available:http://www.eea.europa.eu/publications/europes-onshore-and-offshore-wind-energy-potential. [Accessed: 28-Jun-2016].

[18] ‘RENEWABLE ENERGY TECHNOLOGIES: COST ANALYSIS SERIES’.vol.1,no5.[Online].Available:https://www.irena.org/documentdownloads/publications/re_technologies_cost_analysis-wind_power.pdf [Accessed: 20-Jun-2016].

[19]‘GLOBAL.WIND.STATISTICS.2015’.[Online].Available:http://www.gwec.net/wp-content/uploads/vip/GWEC-PRstats-2015_LR_corrected.pdf. [Accessed: 28-Jun-2016].

[20] ‘Technical advantages - Why choose HVDC over HVAC | ABB’. [Online]. Available: http://new.abb.com/systems/hvdc/why-hvdc/technical-advantages. [Accessed: 28-Jun-2016].

[21] ‘Friends of the Supergrid | Interconnecting Electricity for Europe’s Sustainable Future’. [Online]. Available: http://www.friendsofthesupergrid.eu/. [Accessed: 28-Jun-2016].

[22] T. K. Vrana, R. E. Torres-Olguin, B. Liu, and T. M. Haileselassie, ‘The North Sea Super Grid - a technical perspective’, in 9th IET International Conference on AC and DC Power Transmission, 2010. ACDC, 2010, pp. 1–5.

[23] V. F. Lescale, A. Kumar, L. E. Juhlin, H. Bjorklund, and K. Nyberg, ‘Challenges with Multi-Terminal UHVDC Transmissions’, in Joint International Conference on Power System Technology and IEEE Power India Conference, 2008. POWERCON 2008, 2008, pp. 1–7.

[24] R. S. Whitehouse, ‘Technical challenges of realising multi-terminal networking with VSC’, in Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011), 2011, pp. 1–12.

[25] R. Rudervall, J. P. Charpentier, and R. Sharma, ‘High voltage direct current (HVDC) transmission systems technology review paper’, Energy Week, vol. 2000, p. 2, 2000.

[26] M. W. Stoddart, ‘The role of HVDC in the electrical development of Canada’, Electr. Eng., vol. 82, no. 10, pp. 602–609, Oct. 1963.

[27] J. S. Hess and L. R. Rice, ‘Three Megawatt HVDC Transmission Simulator’, IEEE Trans. Ind. Gen. Appl., vol. IGA-3, no. 6, pp. 531–537, Nov. 1967.

[28] H. Guo, K. Rudion, C. Heyde, and Z. A. Styczynski, ‘Stability studies of offshore wind farms’, in 2010 5th International Conference on Critical Infrastructure (CRIS), 2010, pp. 1–7.

[29] ‘High-voltage direct-current transmission’. [Online]. Available: http://www.siemens.com/about/sustainability/en/environmental-portfolio/products-solutions/power-transmission-distribution/high-voltage-direct-current-transmission.htm. [Accessed: 28-May-2015].

[30] P. Bresesti, W. L. Kling, R. L. Hendriks, and R. Vailati, ‘HVDC Connection of Offshore Wind Farms to the Transmission System’, IEEE Trans. Energy Convers., vol. 22, no. 1, pp. 37–43, Mar. 2007.

[31] P. Higgins and A. Foley, ‘The evolution of offshore wind power in the United Kingdom’, Renew. Sustain. Energy Rev., vol. 37, pp. 599–612, Sep. 2014.

[32] S. Gordon, ‘Supergrid to the rescue’, Power Eng., vol. 20, no. 5, pp. 30–33, Oct. 2006.

[33] D. Van Hertem and M. Ghandhari, ‘Multi-terminal VSC HVDC for the European supergrid: Obstacles’, Renew. Sustain. Energy Rev., vol. 14, no. 9, pp. 3156–3163, Dec. 2010.

[34] M. P. Bahrman and B. K. Johnson, ‘The ABCs of HVDC transmission technologies’, IEEE Power Energy Mag., vol. 5, no. 2, pp. 32–44, Mar. 2007.

[35] M. H. Okba, M. H. Saied, M. Z. Mostafa, and T. M. A.- Moneim, ‘High voltage direct current transmission - A Review, Part II - Converter technologies’, in 2012 IEEE Energytech, 2012, pp. 1–7.

[36] B. R. Andersen, ‘HVDC transmission-opportunities and challenges’, in The 8th IEE International Conference on AC and DC Power Transmission, 2006. ACDC 2006, 2006, pp. 24–29.

[37] Z. Chen, Z. Chen, and E. Spooner, ‘Current source thyristor inverter and its active compensation system’, Transm. Distrib. IEE Proc. - Gener., vol. 150, no. 4, pp. 447–454, Jul. 2003.

[38] K. R. Padiyar, HVDC Power Transmission Systems. New Academic Science, 2011.

[39] Z. Chen, ‘Compensation schemes for a SCR converter in variable speed wind power systems’, IEEE Trans. Power Deliv., vol. 19, no. 2, pp. 813–821, Apr. 2004.

[40] J. de Andrés, M. Pérez, M. Mühlenkamp, D. Retzmann, and R. Walz, ‘Prospects for HVDC: getting more power out of the grid’, in Presentation prepared for Siemens AG and presented at the CIGRE Conference, Madrid, Spain, 2006, pp. 29–30.

[41] F. Yang and Y. Chang, ‘Study on Capacitor Commutated Converter applied in HVDC projects’, in IEEE Power Engineering Society General Meeting, 2007, 2007, pp. 1–5.

[42] L. Zhang, ‘Modeling and control of VSC-HVDC links connected to weak AC systems’, 2010.

[43] A. Bayo Salas, ‘Operation, control and optimization of a Meshed-HVDC system’, 2013.

[44] P. M. Meshram, A. N. Kadu, R. N. Nagpure, and K. L. Thakre, ‘VSC-HVDC for improvement of quality of power supply’, in TENCON 2004. 2004 IEEE Region 10 Conference, 2004, vol. C, p. 256–259 Vol. 3.

[45] R. Feldman, M. Tomasini, E. Amankwah, J. C. Clare, P. W. Wheeler, D. R. Trainer, and R. S. Whitehouse, ‘A Hybrid Modular Multilevel Voltage Source Converter for HVDC Power Transmission’, IEEE Trans. Ind. Appl., vol. 49, no. 4, pp. 1577–1588, Jul. 2013.

[46] S. Allebrod, R. Hamerski, and R. Marquardt, ‘New transformerless, scalable Modular Multilevel Converters for HVDC-transmission’, in 2008 IEEE Power Electronics Specialists Conference, 2008, pp. 174–179.

[47] G. P. Adam, S. J. Finney, K. H. Ahmed, and B. W. Williams, ‘Modular multilevel converter modeling for power system studies’, in 2013 Fourth International Conference on Power Engineering, Energy and Electrical Drives (POWERENG), 2013, pp. 1538–1542.

[48] M. Spichartz, V. Staudt, and A. Steimel, ‘Modular Multilevel Converter for propulsion system of electric ships’, in 2013 IEEE Electric Ship Technologies Symposium (ESTS), 2013, pp. 237–242.

[49] A. Nabae, I. Takahashi, and H. Akagi, ‘A New Neutral-Point-Clamped PWM Inverter’, IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[50] P. M. Bhagwat and V. R. Stefanovic, ‘Generalized Structure of a Multilevel PWM Inverter’, IEEE Trans. Ind. Appl., vol. IA-19, no. 6, pp. 1057–1069, Nov. 1983.

[51] A. Lesnicar and R. Marquardt, ‘An innovative modular multilevel converter topology suitable for a wide power range’, in Power Tech Conference Proceedings, 2003 IEEE Bologna, 2003, vol. 3, p. 6 pp. Vol.3-pp.

[52] T. A. Meynard and H. Foch, ‘Multi-level conversion: high voltage choppers and voltage-source inverters’, in , 23rd Annual IEEE Power Electronics Specialists Conference, 1992. PESC ’92 Record, 1992, pp. 397–403 vol.1.

[53] G. P. Adam, S. J. Finney, A. M. Massoud, and B. W. Williams, ‘Capacitor Balance Issues of the Diode-Clamped Multilevel Inverter Operated in a Quasi Two-State Mode’, IEEE Trans. Ind. Electron., vol. 55, no. 8, pp. 3088–3099, Aug. 2008.

[54] K. Friedrich, ‘Modern HVDC PLUS application of VSC in Modular Multilevel Converter topology’, in 2010 IEEE International Symposium on Industrial Electronics, 2010, pp. 3807–3810.

[55] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. Mcdonald, ‘Modular multilevel inverter: Pulse width modulation and capacitor balancing technique’, IET Power Electron., vol. 3, no. 5, pp. 702–715, Sep. 2010.

[56] C. Chen, G. P. Adam, S. J. Finney, and B. W. Williams, ‘DC power network post-fault recharging with an H-bridge cascaded multilevel converter’, in 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2013, pp. 2569–2574.

[57] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, ‘New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System’, IEEE Trans. Power Syst., vol. 28, no. 1, pp. 335–346, Feb. 2013.

[58] G. P. Adam, I. A. Abdelsalam, K. H. Ahmed, and B. W. Williams, ‘Hybrid Multilevel Converter With Cascaded H-bridge Cells for HVDC Applications:

Operating Principle and Scalability', IEEE Trans. Power Electron., vol. 30, no. 1, pp. 65–77, Jan. 2015.

[59] C. Newton and M. Sumner, 'Neutral point control for multi-level inverters: theory, design and operational limitations', in , Conference Record of the 1997 IEEE Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97, 1997, vol. 2, pp. 1336–1343 vol.2.

[60] G. P. Adam, S. J. Finney, O. Ojo, and B. W. Williams, 'Quasi-two-level and three-level operation of a diode-clamped multilevel inverter using space vector modulation', IET Power Electron., vol. 5, no. 5, pp. 542–551, May 2012.

[61] S. Busquets-Monge, J. Rocabert, P. Rodriguez, S. Alepuz, and J. Bordonau, 'Multilevel Diode-Clamped Converter for Photovoltaic Generators With Independent Voltage Control of Each Solar Array', IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2713–2723, Jul. 2008.

[62] S. Gauthier and F. Okou, 'Transformer-less five-level diode-clamped converter based active power filter with auxiliary balancing circuit', in 2010 23rd Canadian Conference on Electrical and Computer Engineering (CCECE), 2010, pp. 1–5.

[63] J. Rodriguez, J.-S. Lai, and F. Z. Peng, 'Multilevel inverters: a survey of topologies, controls, and applications', IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, 2002.

[64] J.-S. Lai and F. Z. Peng, 'Multilevel converters-a new breed of power converters', IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 509–517, May 1996.

[65] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, 'A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters', in 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010, pp. 58–62.

[66] W.-K. Lee, S.-Y. Kim, J.-S. Yoon, and D.-H. Baek, ‘A comparison of the carrier-based PWM techniques for voltage balance of flying capacitor in the flying capacitor multilevel inverter’, in Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC ’06., 2006, p. 6 pp.-pp.

[67] W.-K. Lee, T.-J. Kim, D.-W. Kang, and D.-S. Hyun, ‘A carrier-rotation strategy for voltage balancing of flying capacitors in flying capacitor multi-level inverter’, in The 29th Annual Conference of the IEEE Industrial Electronics Society, 2003. IECON ’03, 2003, vol. 3, p. 2173–2178 Vol.3.

[68] W. Song and A. Q. Huang, ‘Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM’, IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2700–2708, Aug. 2010.

[69] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, ‘Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems’, IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[70] L. A. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, ‘Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles’, IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

[71] K. Ilves, L. Harnefors, S. Norrga, and H. P. Nee, ‘Analysis and operation of modular multilevel converters with phase-shifted carrier PWM’, in 2013 IEEE Energy Conversion Congress and Exposition, 2013, pp. 396–403.

[72] X. Zhao, G. Li, and C. Zhao, ‘Research on submodule capacitance voltage balancing of MMC based on carrier phase shifted SPWM technique’, in CICED 2010 Proceedings, 2010, pp. 1–6.

[73] E. W. Kimbark, Direct current transmission. Wiley-Interscience, 1971.

[74] H. W. Meyer, History of Electricity and Magnetism. Cambridge, Mass: MIT Press, 1971.

[75] U. Lamm, ‘Mercury-arc valves for high-voltage dc transmission’, Electr. Eng. Proc. Inst. Of, vol. 111, no. 10, pp. 1747–1753, 1964.

[76] D. G. Fink and H. W. Beaty, Standard Handbook for Electrical Engineers, 15 edition. New York: McGraw-Hill Professional, 2006.

[77] H. Huang, M. Uder, R. Barthelmess, and J. Dorn, ‘Application of high power thyristors in HVDC and FACTS systems’, in 17th Conference of Electric Power Supply Industry (CEPSI), 2008, pp. 1–8.

[78] J. Arrillaga, Y. H. Liu, and N. R. Watson, Flexible Power Transmission: The HVDC Options. John Wiley & Sons, 2007.

[79] J. P. Norton and B. J. Cory, ‘Control-system stability in multiterminal hvdc systems’, in Proceedings of the Institution of Electrical Engineers, 1968, vol. 115, pp. 1828–1834.

[80] R. Foerst, G. Heyner, K. W. Kanngiesser, and H. Waldmann, ‘Multiterminal Operation of HVDC Converter Stations’, IEEE Trans. Power Appar. Syst., vol. PAS-88, no. 7, pp. 1042–1052, Jul. 1969.

[81] R. L. Vaughan, J. P. Bowles, and J. Dalzell, ‘The control and performance of a series connected multiterminal HVDC transmission system’, IEEE Trans. Power Appar. Syst., vol. 94, no. 5, pp. 1868–1877, Sep. 1975.

[82] J. Reeve, ‘Multiterminal HVDC Power Systems’, IEEE Trans. Power Appar. Syst., vol. PAS-99, no. 2, pp. 729–737, Mar. 1980.

[83] R. Pinto, ‘MULTI-TERMINAL DC NETWORKS; SYSTEM INTEGRATION, DYNAMICS AND CONTROL’, PhD Thesis, Technical university of Delft, 2014.

[84] Kyeon Hur, M. Boddeti, N. D. R. Sarma, J. Dumas, J. Adams, and Soon-Kin Chai, ‘High-wire act’, IEEE Power Energy Mag., vol. 8, no. 1, pp. 37–45, Jan. 2010.

[85] I. Dallas and C. Booth, ‘Teleprotection in multi-terminal HVDC supergrids’, in 12th IET International Conference on Developments in Power System Protection (DPSP 2014), 2014, pp. 1–6.

[86] Ha, Hengxu, and Sankara Subramanian. "Implementing the protection and control of future dc grids." Alstom Grid Technology Centre, Innovation and Technology Department (2015).

[87] J. Sneath and A. D. Rajapakse, ‘Fault Detection and Interruption in an Earthed HVDC Grid Using ROCOV and Hybrid DC Breakers’, IEEE Trans. Power Deliv., vol. 31, no. 3, pp. 973–981, Jun. 2016.

[88] S. Xue, F. Gao, W. Sun, and B. Li, ‘Protection Principle for a DC Distribution System with a Resistive Superconductive Fault Current Limiter’, Energies, vol. 8, no. 6, pp. 4839–4852, May 2015.

[89] A. Shukla and G. D. Demetriades, ‘A Survey on Hybrid Circuit-Breaker Topologies’, IEEE Trans. Power Deliv., vol. 30, no. 2, pp. 627–641, Apr. 2015.

[90] C. D. Barker and R. S. Whitehouse, ‘An alternative approach to HVDC grid protection’, in 10th IET International Conference on AC and DC Power Transmission (ACDC 2012), 2012, pp. 1–6.

[91] D. Jovcic, ‘Bidirectional, High-Power DC Transformer’, IEEE Trans. Power Deliv., vol. 24, no. 4, pp. 2276–2283, Oct. 2009.

[92] D. Jovcic and B. T. Ooi, ‘Developing DC Transmission Networks Using DC Transformers’, IEEE Trans. Power Deliv., vol. 25, no. 4, pp. 2535–2543, Oct. 2010.

[93] C. D. Barker, C. C. Davidson, D. R. Trainer, and R. S. Whitehouse, ‘Requirements of DC-DC Converters to facilitate large DC Grids’, Cigre SC B4 HVDC Power Electron., 2012.

[94] T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, ‘High-Frequency Operation of a DC/AC/DC System for HVDC Applications’, IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4107–4115, Aug. 2014.

[95] E. Veilleux and B. T. Ooi, ‘Marx-dc-dc converter for connecting offshore wind farms to multiterminal HVDC’, in 2013 IEEE Power Energy Society General Meeting, 2013, pp. 1–5.

[96] P. W. Lehn, B.-T. Ooi, and E. Veilleux, ‘Marx dc–dc converter for high-power application’, IET Power Electron., vol. 6, no. 9, pp. 1733–1741, Nov. 2013.

[97] G. N. Taranto, L. M. V. G. Pinto, and M. V. F. Pereira, ‘Representation of FACTS devices in power system economic dispatch’, IEEE Trans. Power Syst., vol. 7, no. 2, pp. 572–576, May 1992.

[98] S. G. Helbing and G. G. Karady, ‘Investigations of an advanced form of series compensation’, IEEE Trans. Power Deliv., vol. 9, no. 2, pp. 939–947, Apr. 1994.

[99] T. Nakajima and S. Irokawa, ‘A control system for HVDC transmission by voltage sourced converters’, in IEEE Power Engineering Society Summer Meeting, 1999, 1999, vol. 2, pp. 1113–1119 vol.2.

[100] T. M. Haileselassie, M. Molinas, T. Undeland, and others, ‘Multi-terminal VSC-HVDC system for integration of offshore wind farms and green electrification of platforms in the North Sea’, in Nordic Workshop on Power and Industrial Electronics (NORPIE/2008), June 9-11, 2008, Espoo, Finland, 2008.

[101] J. Zhu and C. Booth, ‘Future multi-terminal HVDC transmission systems using Voltage source converters’, in Universities Power Engineering Conference (UPEC), 2010 45th International, 2010, pp. 1–6.

[102] T. M. Haileselassie and K. Uhlen, ‘Impact of DC line voltage drops on power flow of MTDC using droop control’, IEEE Trans. Power Syst., vol. 27, no. 3, pp. 1441–1449, 2012.

[103] W. Wang and M. Barnes, ‘Power Flow Algorithms for Multi-Terminal VSC-HVDC With Droop Control’, IEEE Trans. Power Syst., vol. 29, no. 4, pp. 1721–1730, Jul. 2014.

[104] C. Gavriluta, I. Candela, A. Luna, A. Gomez-Exposito, and P. Rodriguez, ‘Hierarchical Control of HV-MTDC Systems With Droop-Based Primary and OPF-Based Secondary’, IEEE Trans. Smart Grid, vol. 6, no. 3, pp. 1502–1510, May 2015.

[105] K. Rouzbehi, A. Miranian, A. Luna, and P. Rodriguez, ‘DC Voltage Control and Power Sharing in Multiterminal DC Grids Based on Optimal DC Power Flow and Voltage-Droop Strategy’, IEEE J. Emerg. Sel. Top. Power Electron., vol. 2, no. 4, pp. 1171–1180, Dec. 2014.

[106] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, and P. Rodriguez, ‘A Generalized Voltage Droop Strategy for Control of Multiterminal DC Grids’, IEEE Trans. Ind. Appl., vol. 51, no. 1, pp. 607–618, Jan. 2015.

[107] D. Jovcic, M. Hajian, H. Zhang, and G. Asplund, ‘Power flow control in DC transmission grids using mechanical and semiconductor based DC/DC devices’,

in 10th IET International Conference on AC and DC Power Transmission (ACDC 2012), 2012, pp. 1–6.

[108] Q. Mu, J. Liang, Y. Li, and X. Zhou, ‘Power flow control devices in DC grids’, in 2012 IEEE Power and Energy Society General Meeting, 2012, pp. 1–7.

[109] C. D. Barker and R. S. Whitehouse, ‘A current flow controller for use in HVDC grids’, in 10th IET International Conference on AC and DC Power Transmission (ACDC 2012), 2012, pp. 1–5.

[110] E. Veilleux and B. T. Ooi, ‘Multiterminal HVDC With Thyristor Power-Flow Controller’, IEEE Trans. Power Deliv., vol. 27, no. 3, pp. 1205–1212, Jul. 2012.

[111] W. Chen, X. Zhu, L. Yao, X. Ruan, Z. Wang, and Y. Cao, ‘An Interline DC Power-Flow Controller (IDCPFC) for Multiterminal HVDC System’, IEEE Trans. Power Deliv., vol. 30, no. 4, pp. 2027–2036, Aug. 2015.

[112] S. Balasubramaniam, J. Liang, and C. E. Ugalde-Loo, ‘An IGBT based series power flow controller for multi-terminal HVDC transmission’, in Power Engineering Conference (UPEC), 2014 49th International Universities, 2014, pp. 1–6.

[113] K. Rouzbehi, J. I. Candela, A. Luna, G. B. Gharehpetian, and P. Rodriguez, ‘Flexible Control of Power Flow in Multiterminal DC Grids Using DC-DC Converter’, IEEE J. Emerg. Sel. Top. Power Electron., vol. 4, no. 3, pp. 1135–1144, Sep. 2016.

[114] R. S. Whitehouse and C. D. Barker, ‘Current flow controller’, EP2670013 A1, 04-Dec-2013.

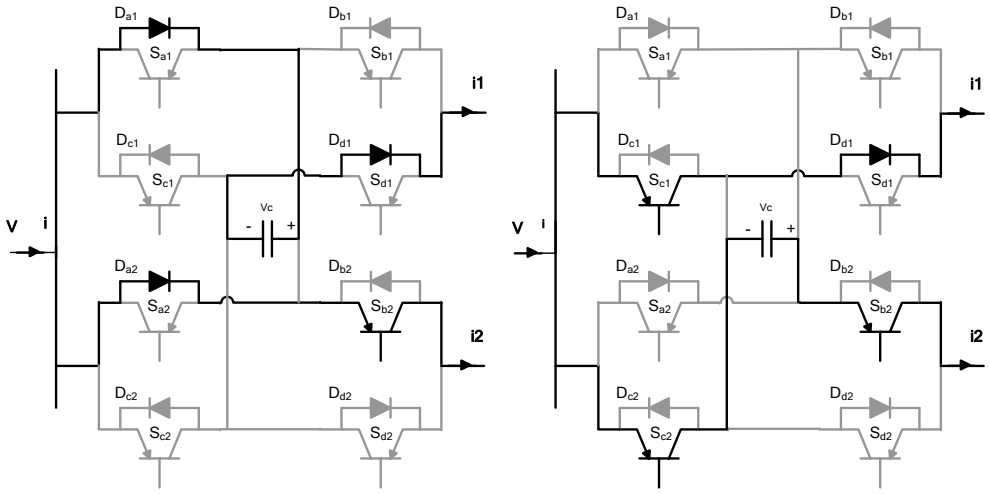
[115] ‘VSC-Based HVDC Transmission System (Detailed Model) - MATLAB & Simulink Example - MathWorks United Kingdom’. [Online]. Available: http://uk.mathworks.com/help/physmod/sps/examples/vsc-based-hvdc-transmission-system-detailed-model.html. [Accessed: 18-Aug-2016].

Appendix

A.

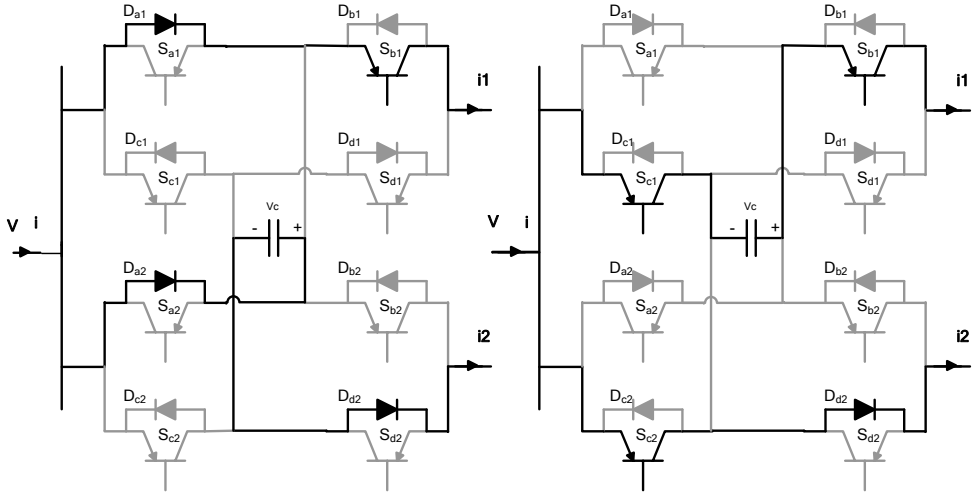
Current Flow Controller Schematic Diagrams

A.1 Two ports CFC schematics



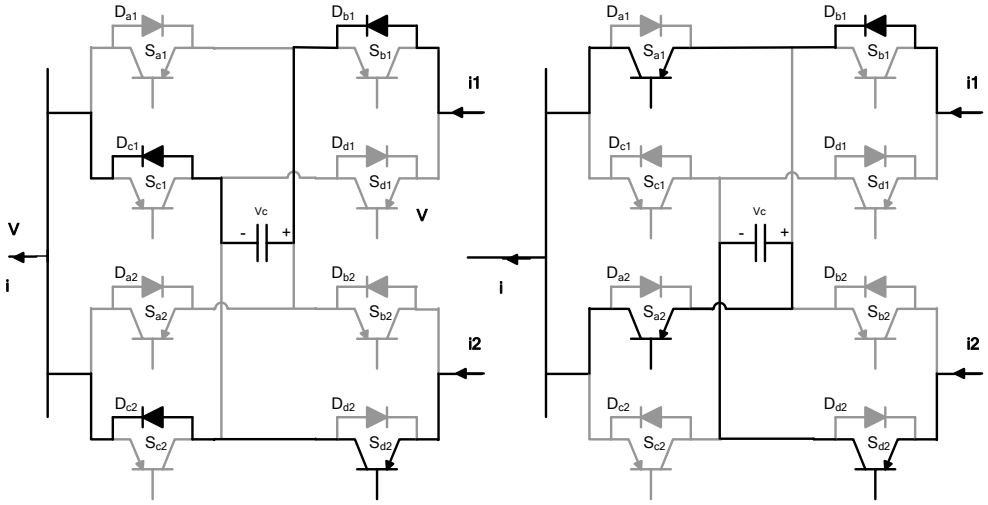
(a) (b)

Figure A.1: Two port CFC in mode 1. (a) Charging from cable 1. (b) Discharging in cable 2.



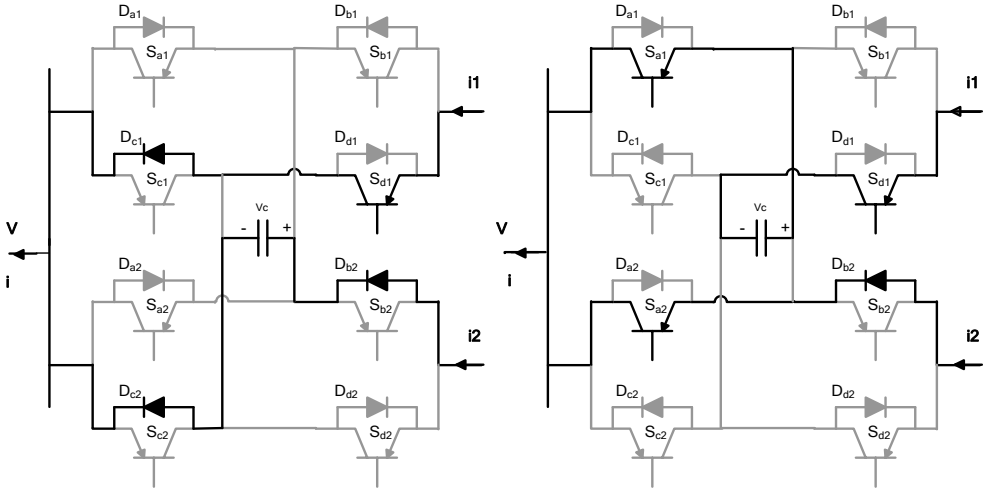
(a) (b)

Figure A.2 Two port CFC in in mode 2. (a) Charging from cable 2. (b) Discharging in cable 1.



(a) (b)

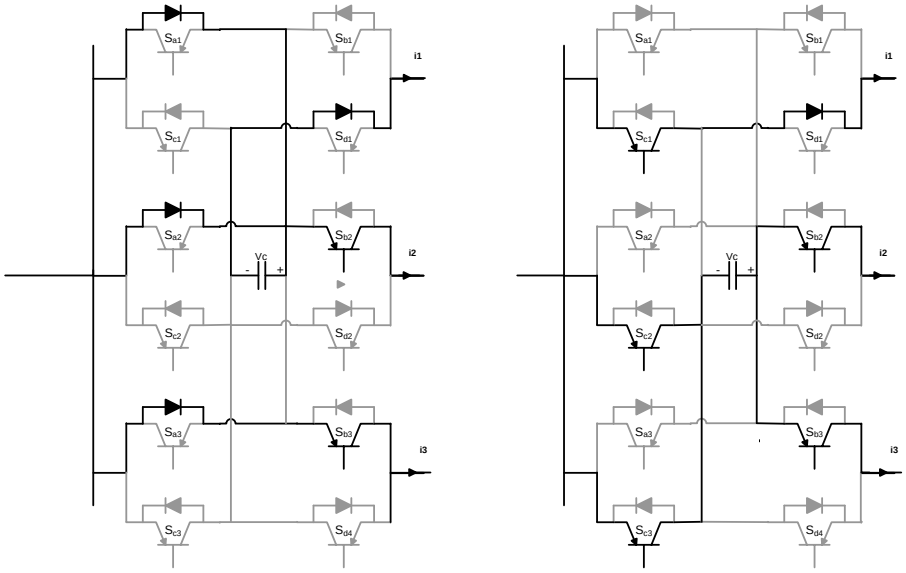
Figure A.3 Two port CFC in in mode 3 (reverse). (a) Charging from cable 1. (b) Discharging in cable 2.



(a) (b)

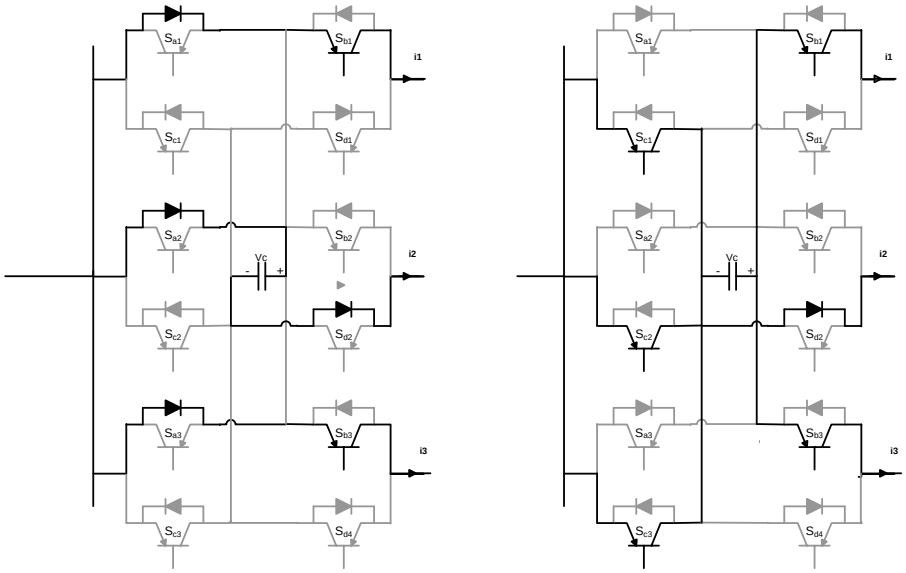
Figure A.4 Two port CFC in mode 4 (reverse). (a) Charging from cable 2. Discharging in cable 1.

A.2 Three ports CFC (extended topology) schematics



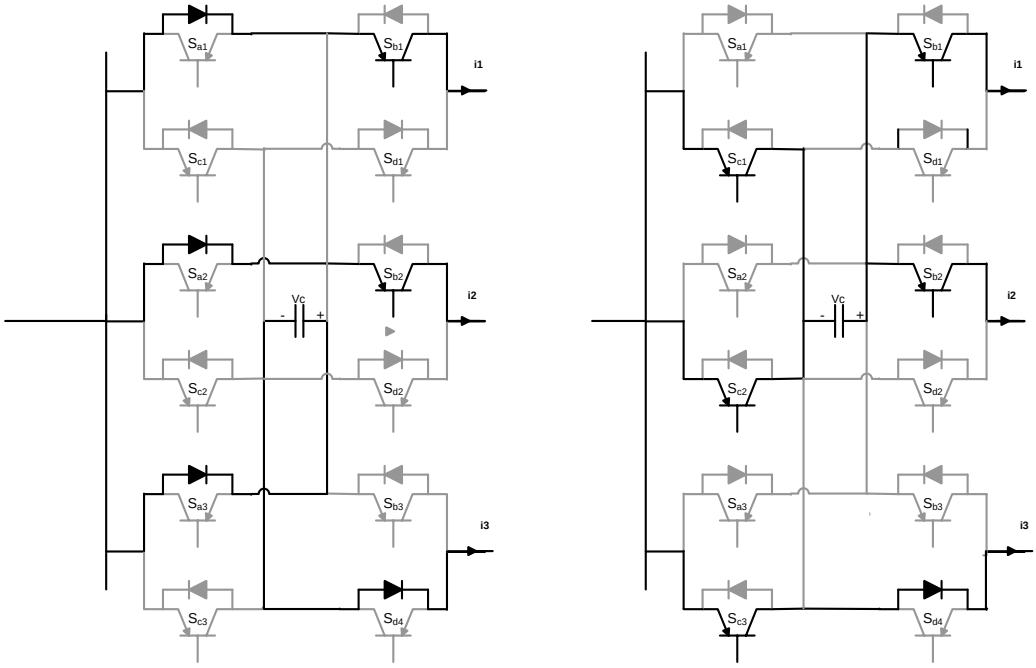
(a) (b)

Figure A.5 Extended CFC mode 1. a) Charging from cable 1, b) Discharging in cables 2 and 3.



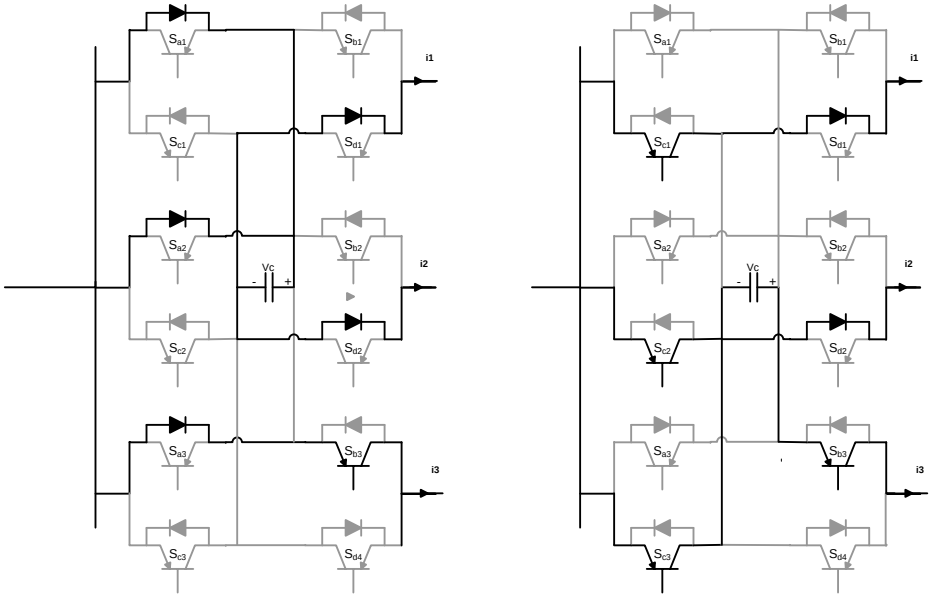
(a) (b)

Figure A.6 Extended CFC mode 2 a) Charging from cable 2, b) Discharging in cables 1and 3.



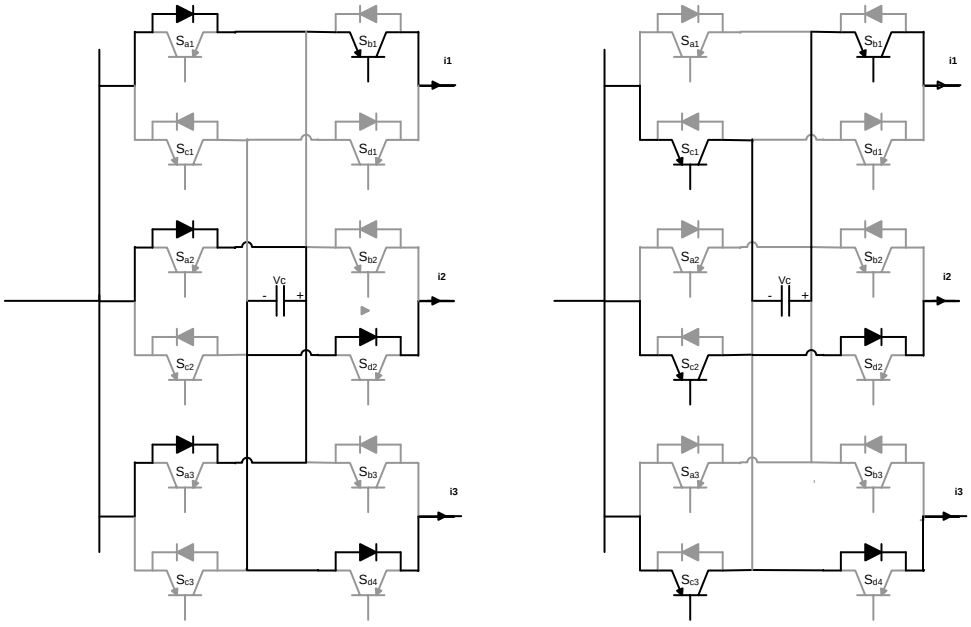
(a) (b)

Figure A.7 Extended CFC mode 3 a) Charging from cable 3, b) Discharging in cables 2 and 3.



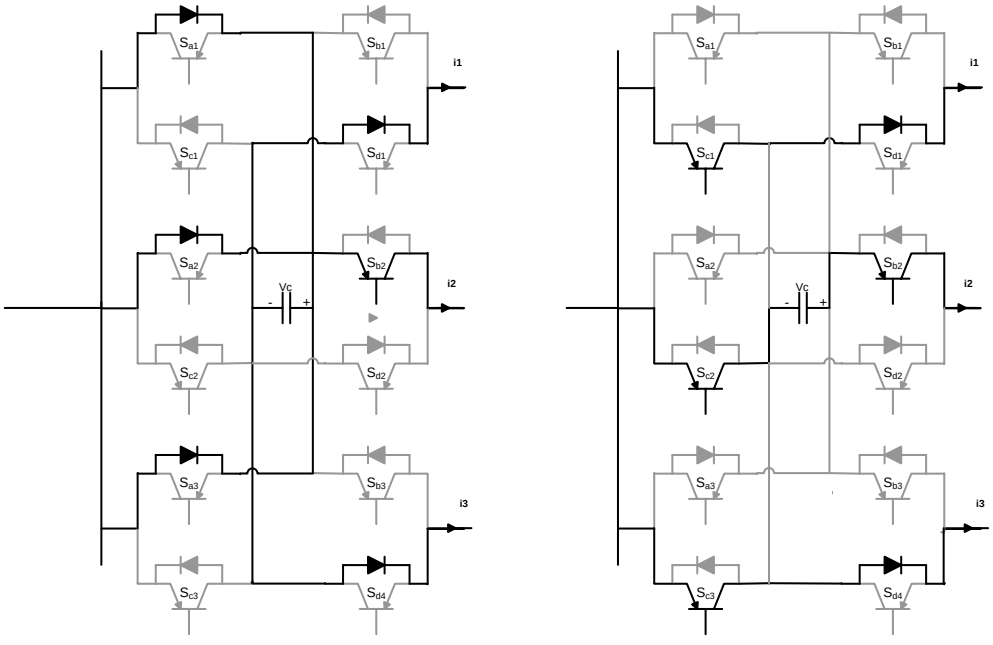
(a) (b)

Figure A.8 Extended CFC mode 4 a) Charging from cables 1 and 2, b) Discharging in cable 3.



(a) (b)

Figure A.9 Extended CFC mode 5 a) Charging from cables 2 and 3, b) Discharging in cable 1.



(a) (b)

Figure A.10 Extended CFC mode 6 a) Charging from cables 1 and 3, b) Discharging in cable 2.

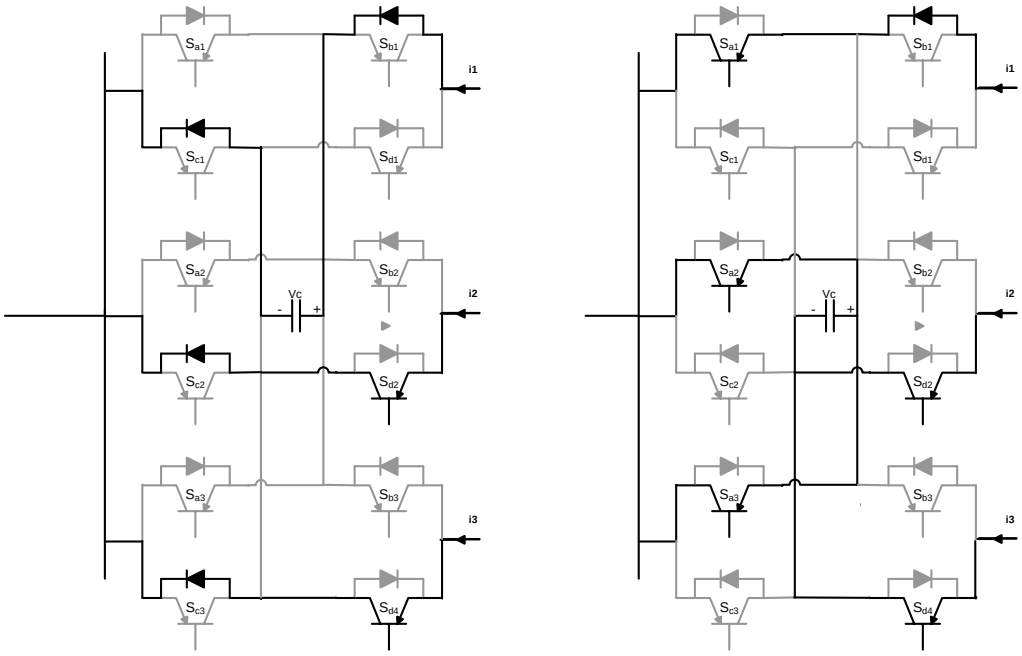


Figure A.11 Extended CFC m ode 7 (reverse) a) Charging from cable 1, b) Discharging in cables 2 and 3.

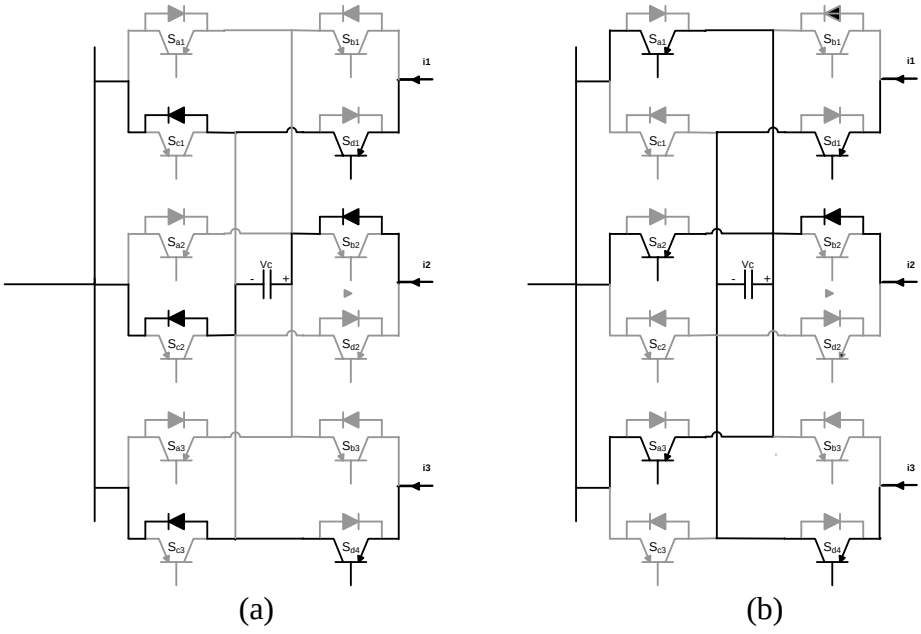
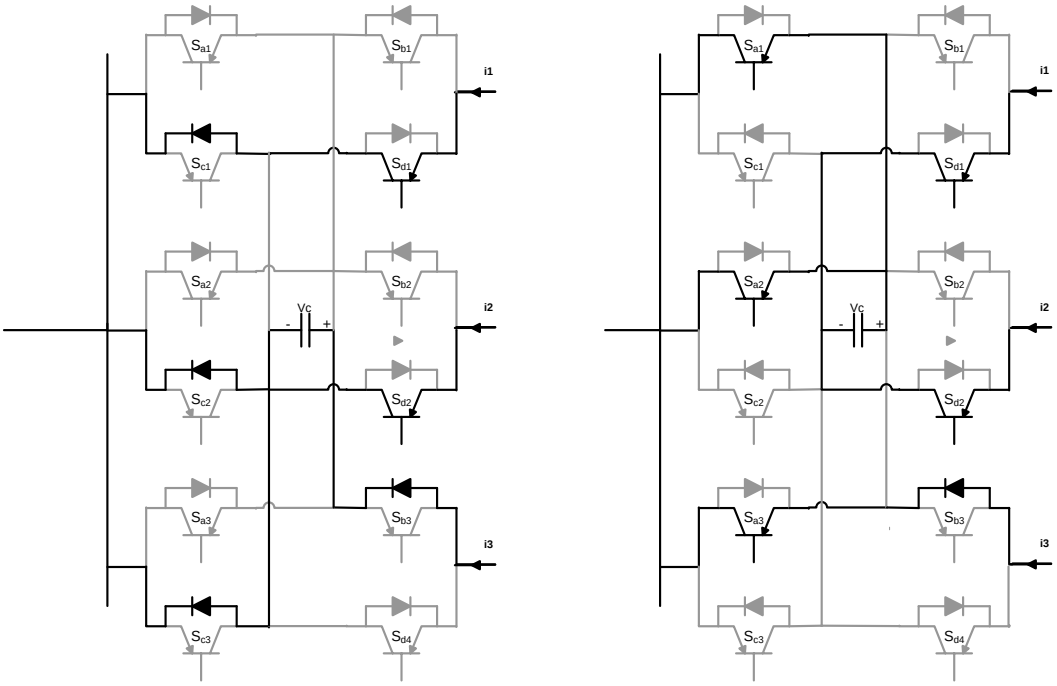
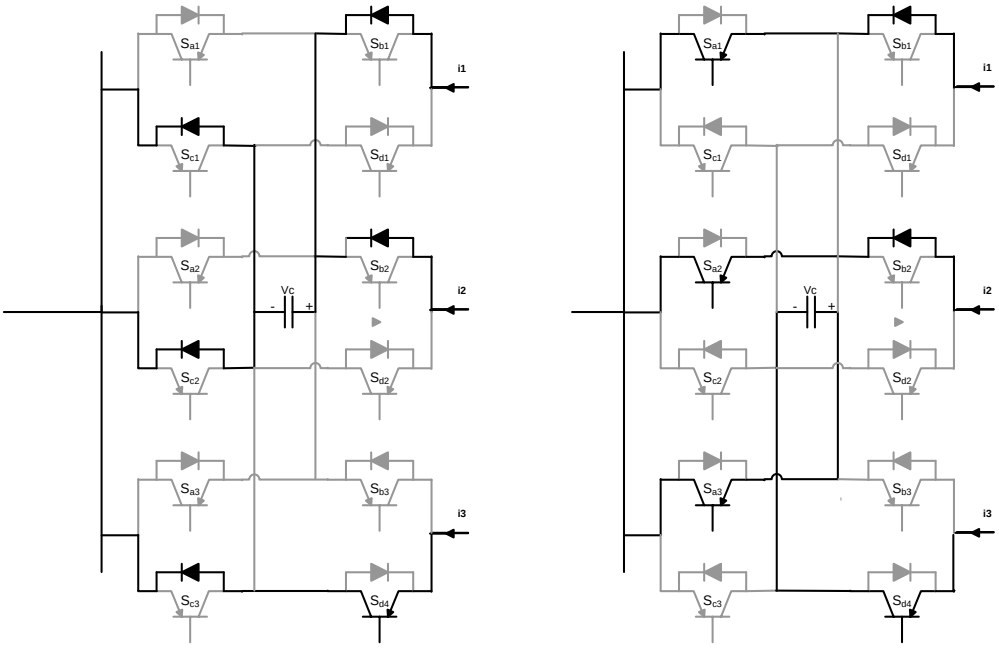


Figure A.12 Extended CFC mode 8 (reverse) a) Charging from cable 2, b) Discharging in cables 1 and 3.



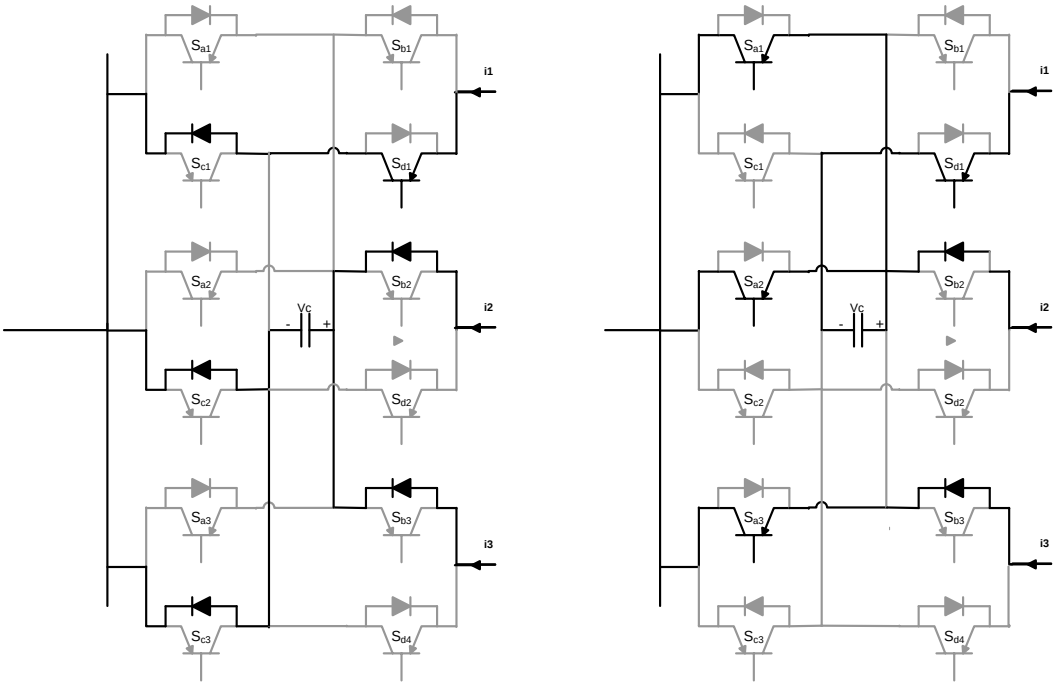
(a) (b)

Figure A.13 Extended CFC mode 9 (reverse) a) Charging from cable 3, b) Discharging in cables 1 and 2.



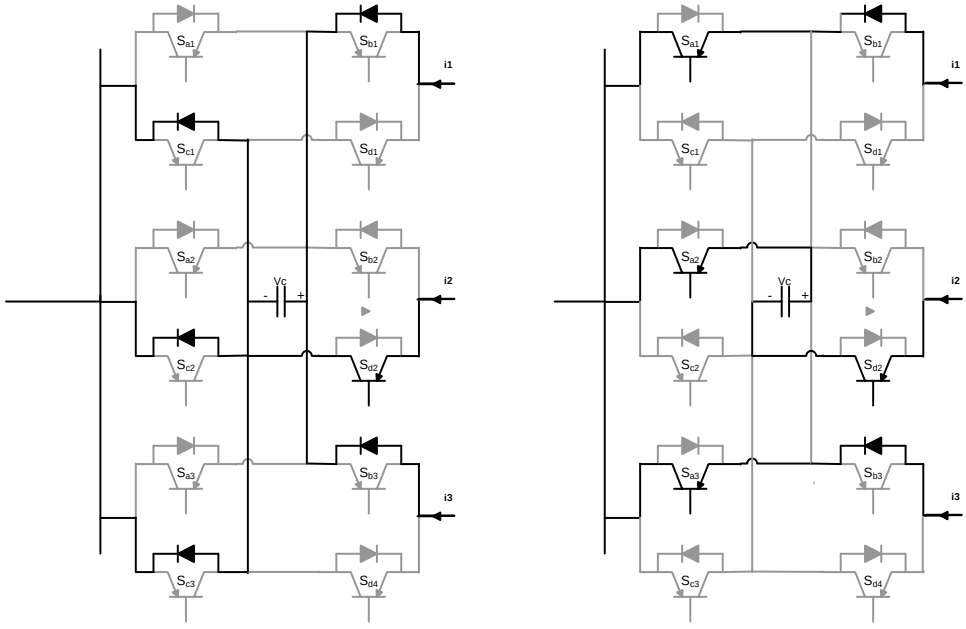
(a) (b)

Figure A.14 Extended CFC mode 10 (reverse) a) Charging from cables 1 and 2, b) Discharging in cable 3.



(a) (b)

Figure A.15 Extended CFC mode 11 (reverse) a) Charging from cables 2 and 3, b) Discharging in cable 1.



(a) (b)

Figure A.16 Extended CFC mode 12 (reverse) a) Charging from cables 1 and 3, b) Discharging in cable 2.

A.3 Three ports modular CFC schematics

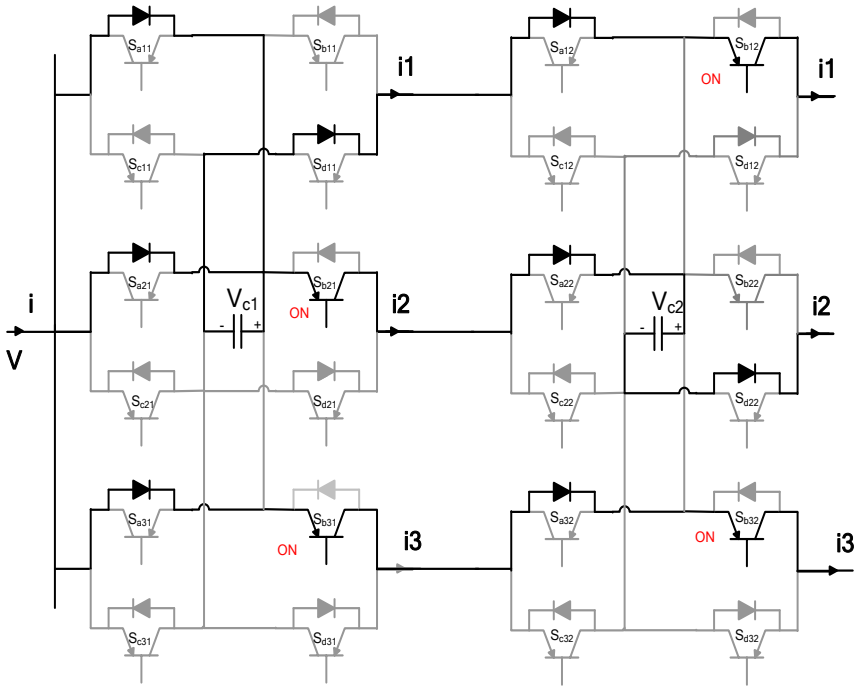


Figure A.17 Three port MCFC operating in mode 1(charging period).

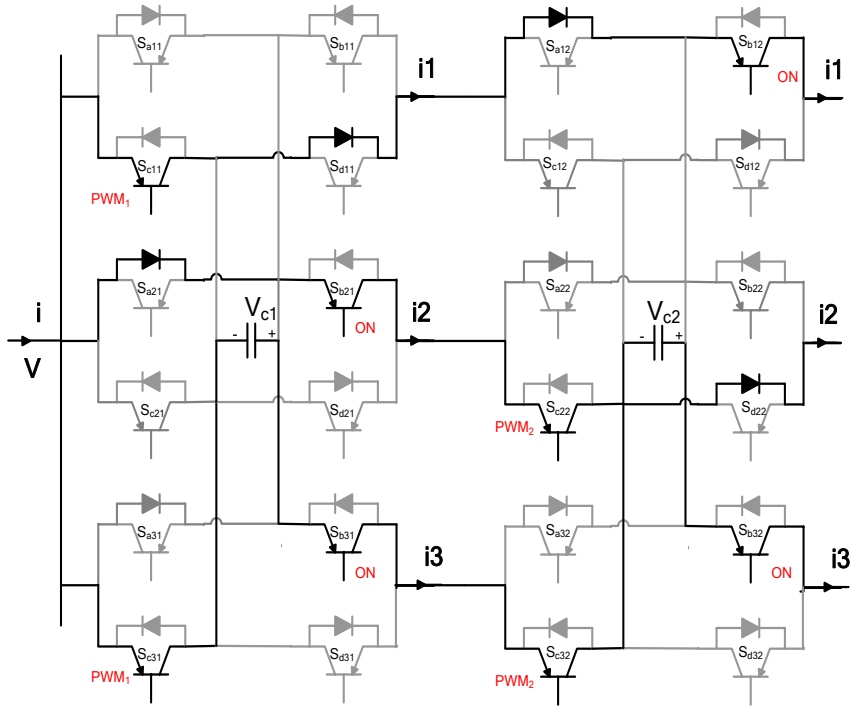


Figure A.18 Three port MCFC operating in mode 1(discharging period).

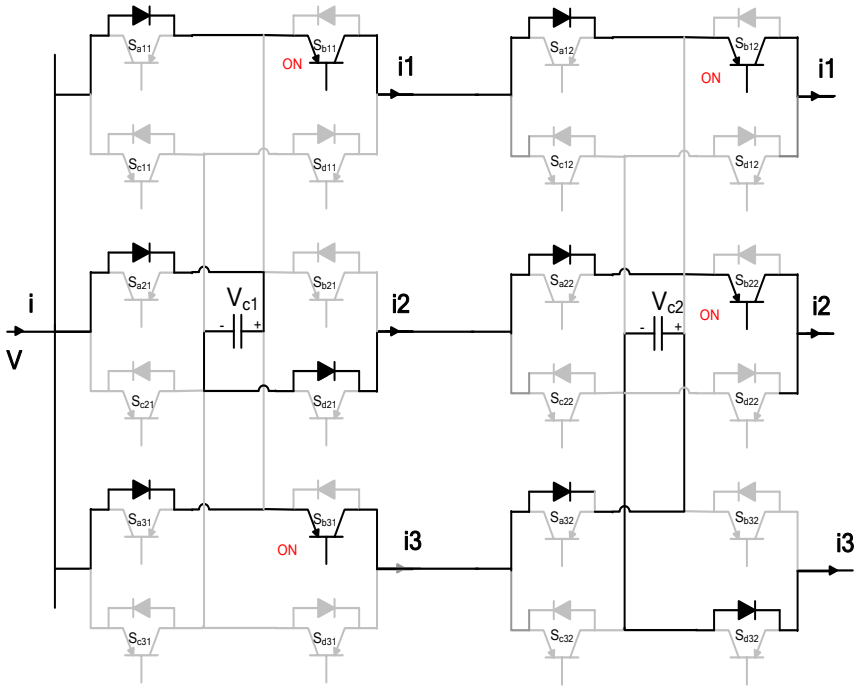


Figure A.19 Three port MCFC operating in mode 2 (charging period).

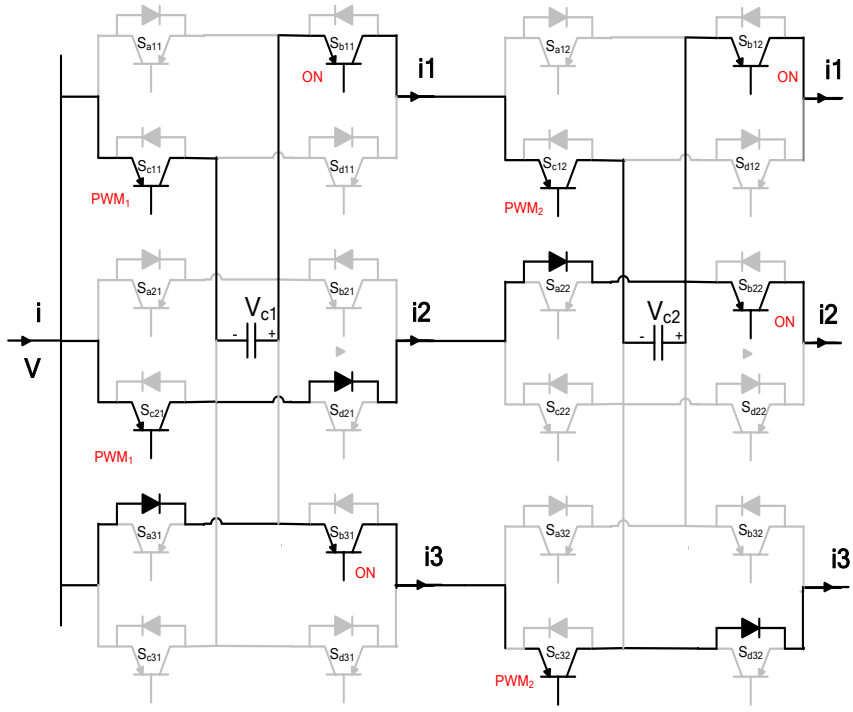


Figure A.20 Three ports MCFC operating in mode 2 (discharging period).

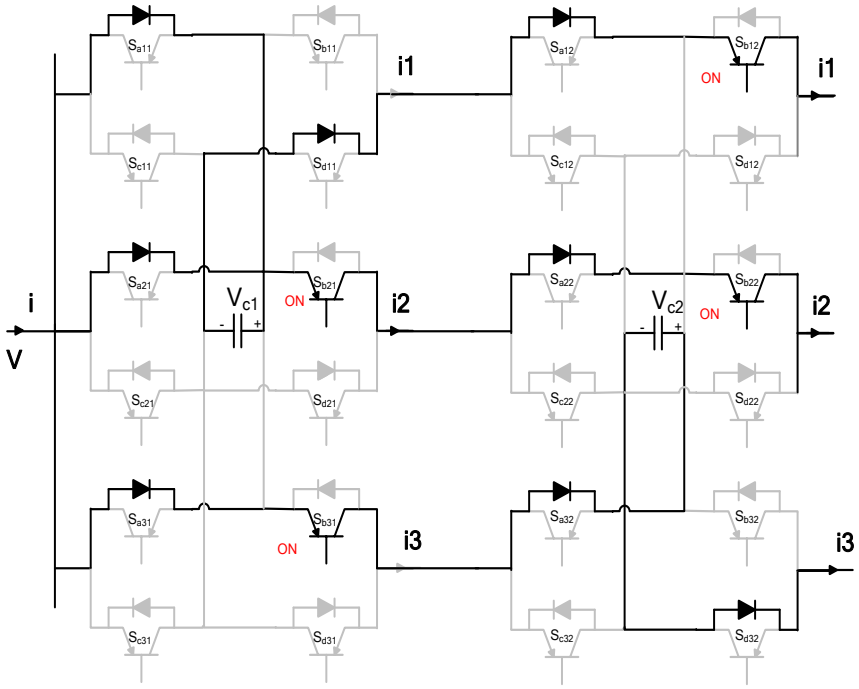


Figure A.21 Three ports MCFC operating in mode 3 (charging period).

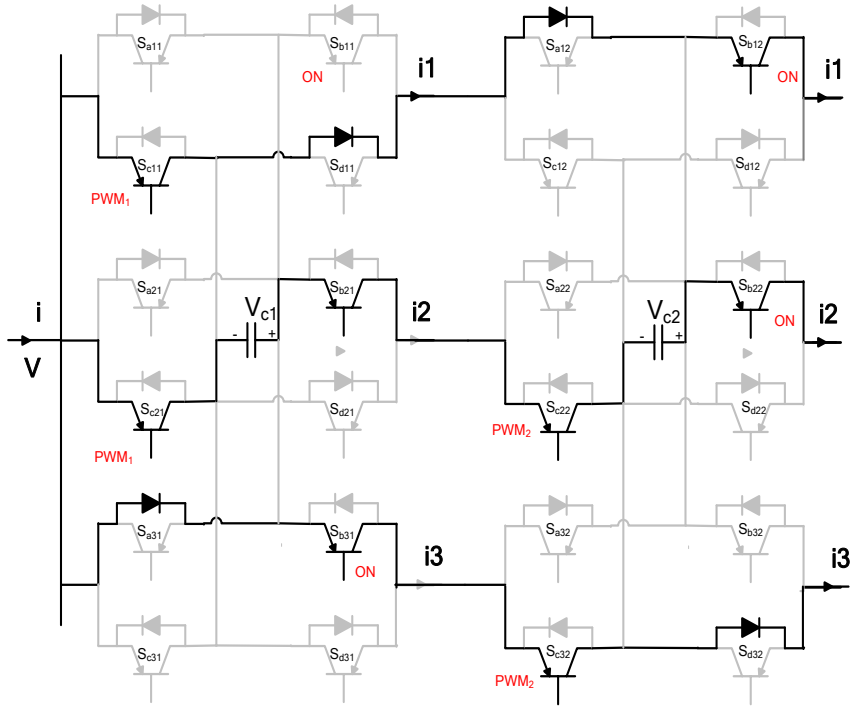


Figure A.22 Three ports MCFC operating in mode 3 (discharging period).

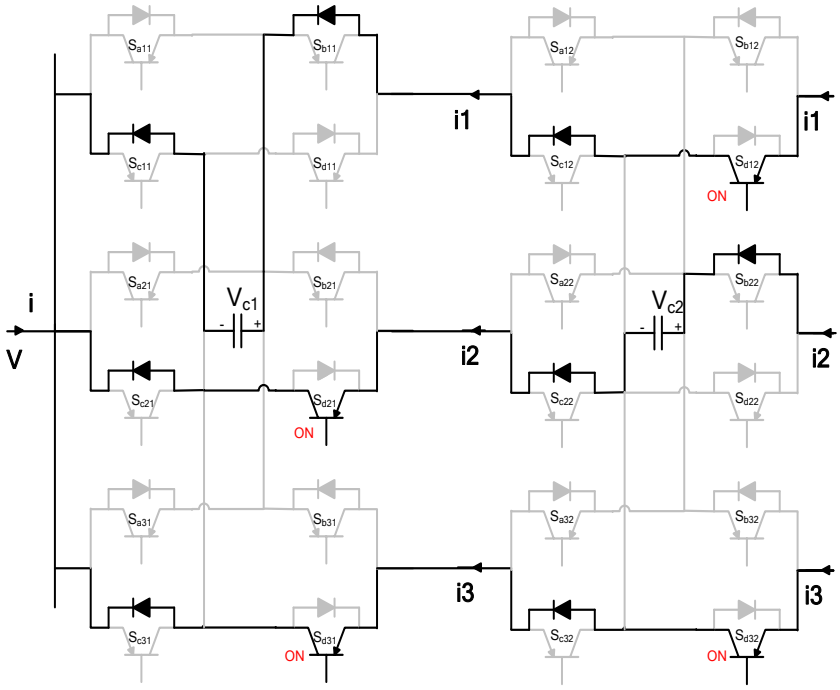


Figure A.23 Three ports MCFC operating in mode 4 - reverse (charging period).

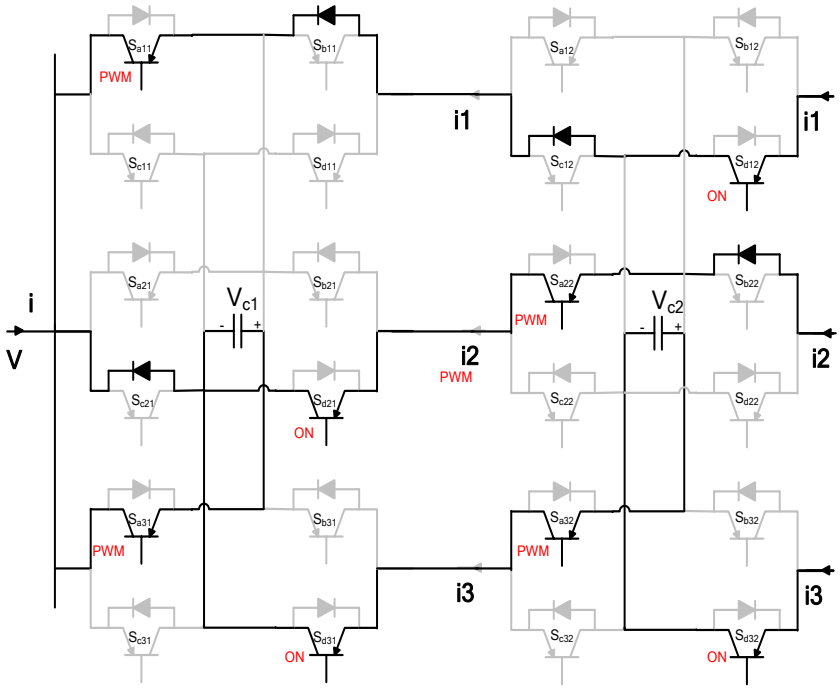


Figure A.24 Three ports MCFC operating in mode 4 - reverse (discharging period).

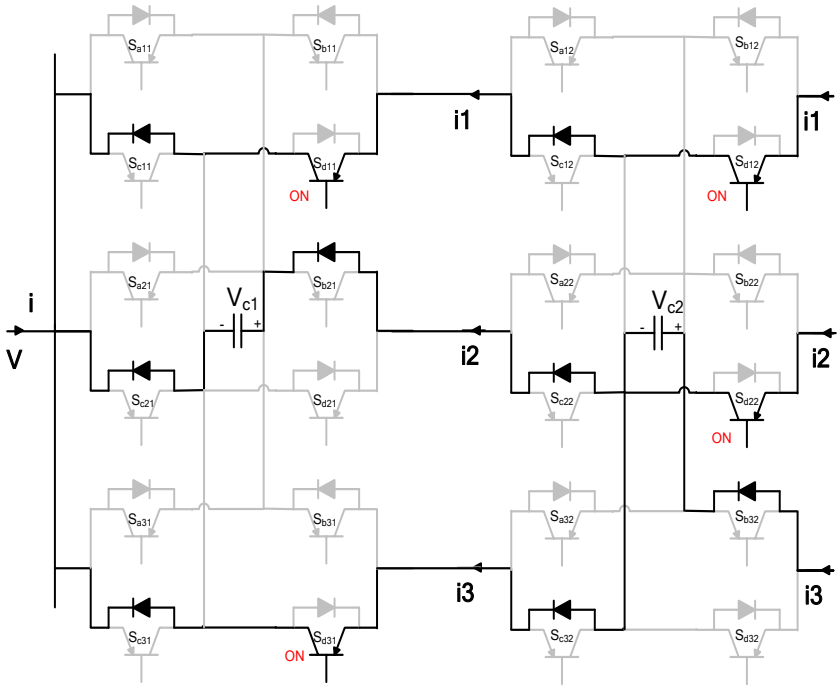


Figure A.25 Three ports MCFC operating in mode 5 - reverse (charging period).

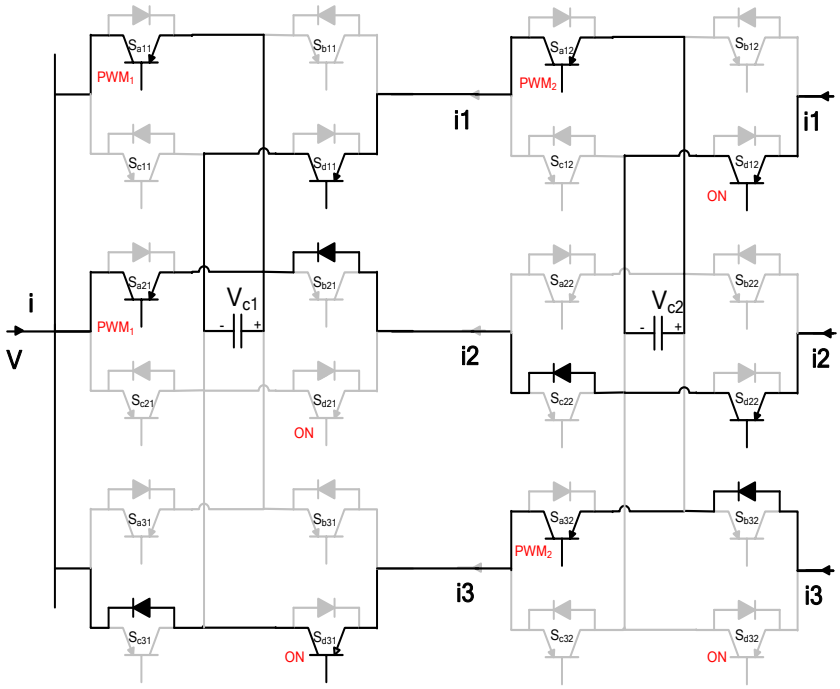


Figure A.26 Three ports MCFC operating in mode 5 - reverse (discharging period).

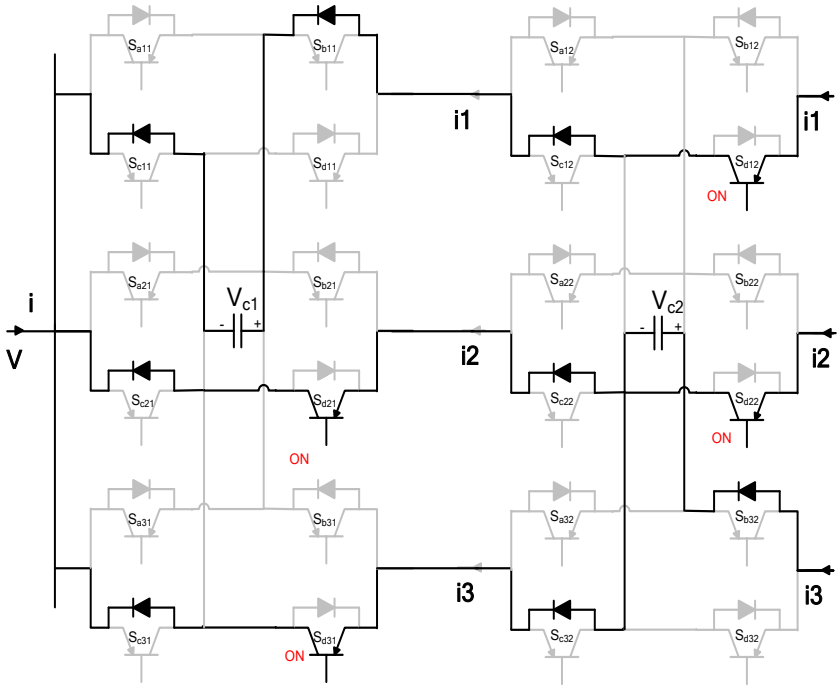


Figure A.27 Three ports MCFC operating in mode 6 - reverse (charging period).

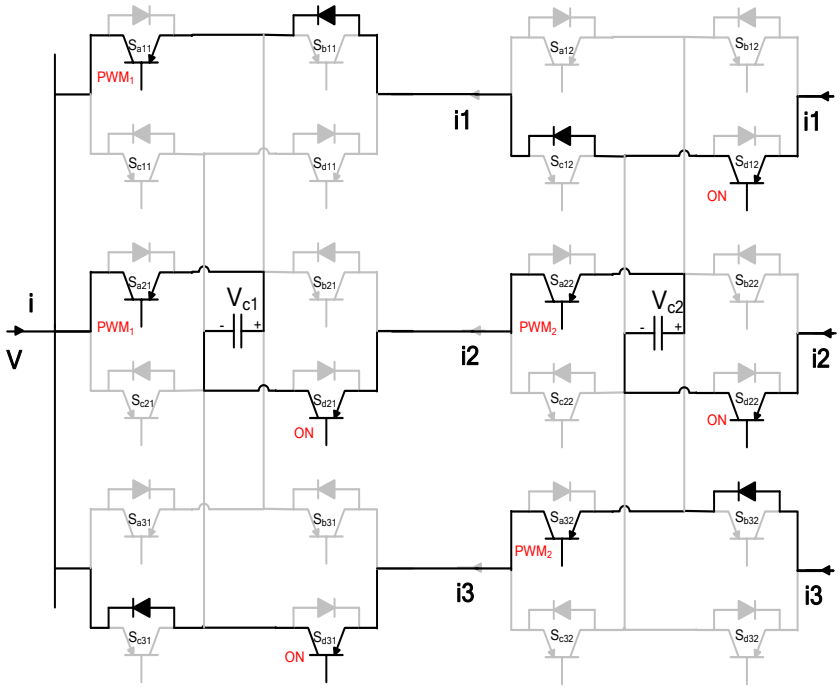
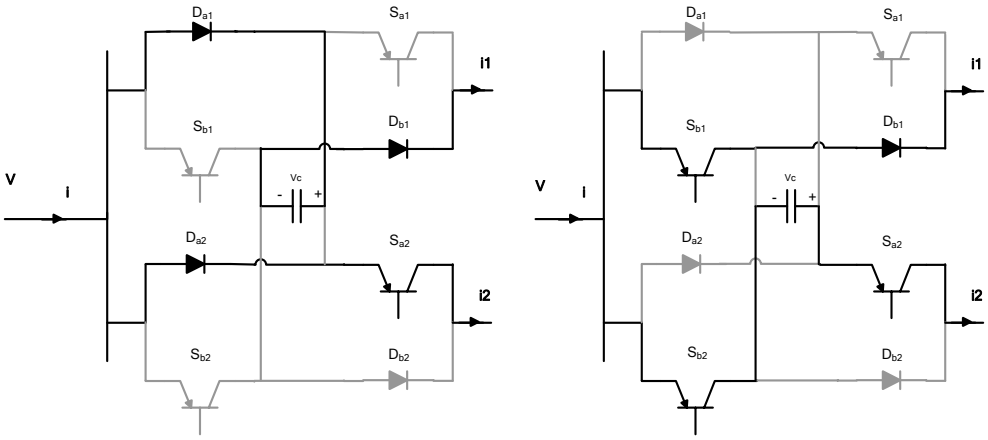


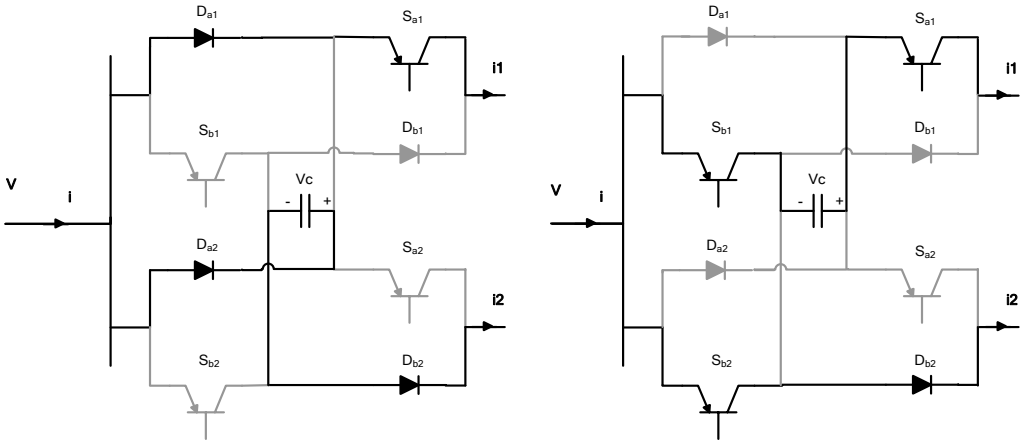
Figure A.28 Three ports MCFC operating in mode 6 - reverse (discharging period).

A.4 Two Ports CFC Reduced Topology Schematics



(a) (b)

Figure A.29 Reduced switches count topology MCFC operating in mode 1. a) Charging period, b) discharging period.



(a) (b)

Figure A.30 Reduced switches count topology MCFC operating in mode 2. a) Charging period, b) discharging period.

Appendix

B.

Details of Simulation Models

B.1 MATLAB/SIMULINK Simulation Models

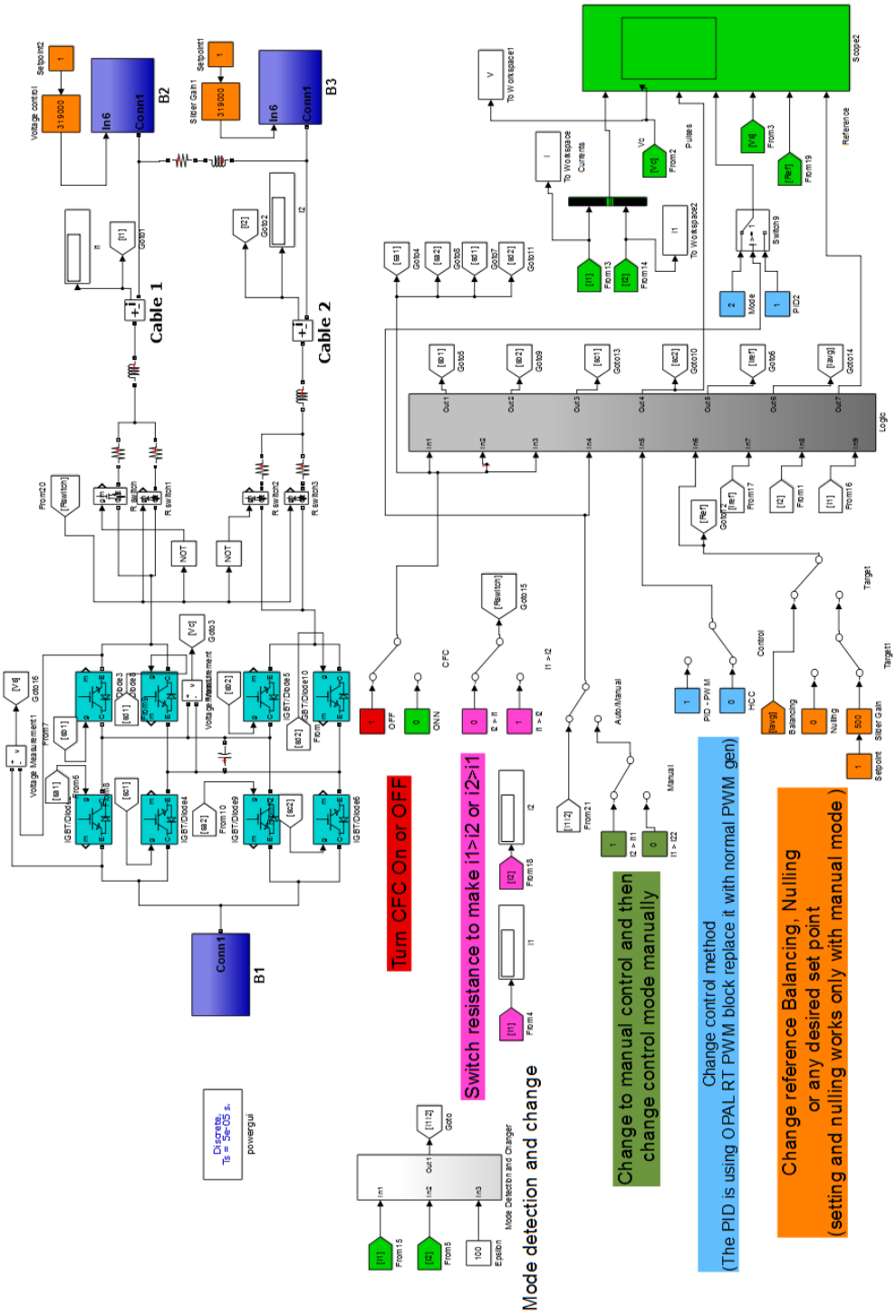


Figure B.1 Two port CFC MATLAB model.

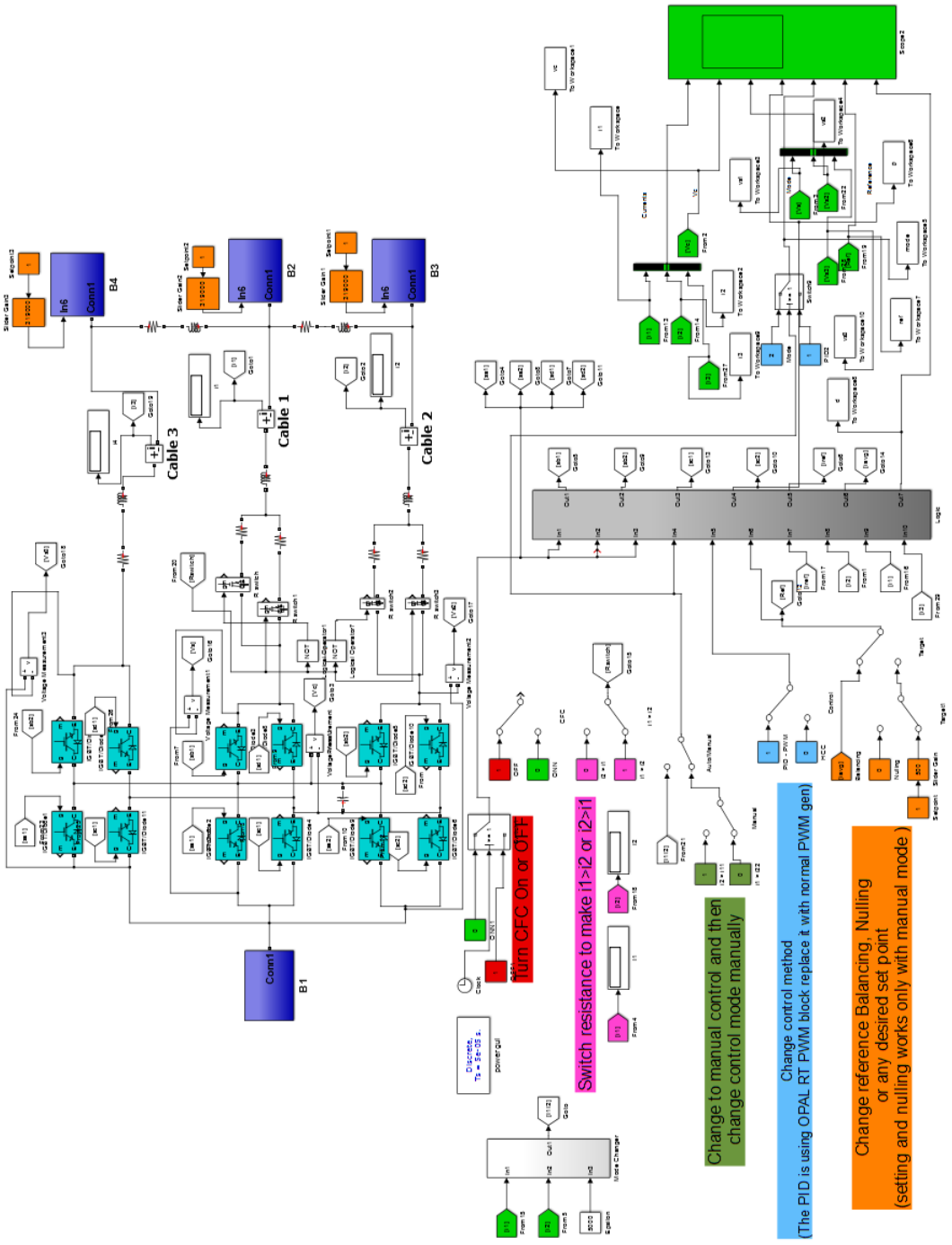


Figure B.2 Three port CFC MATLAB model.

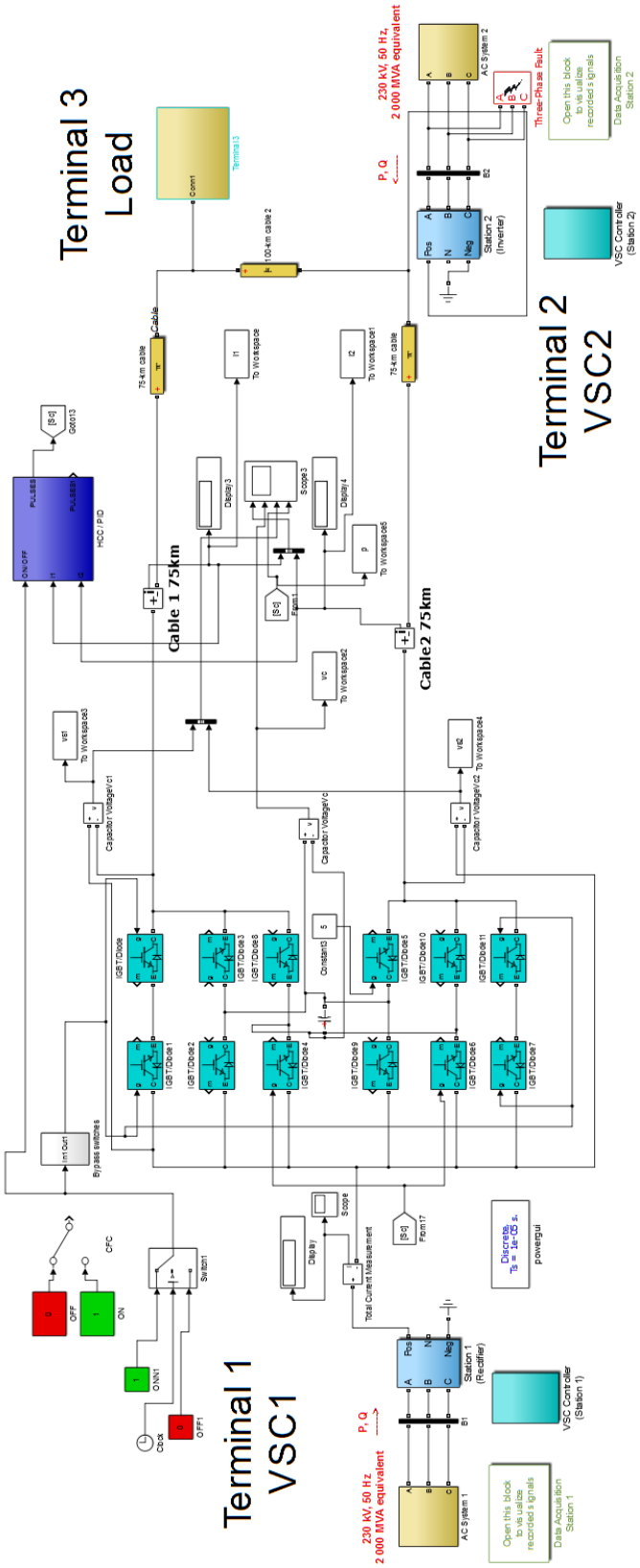


Figure B.3 MATLAB model of VSC based three terminals grid with CFC.

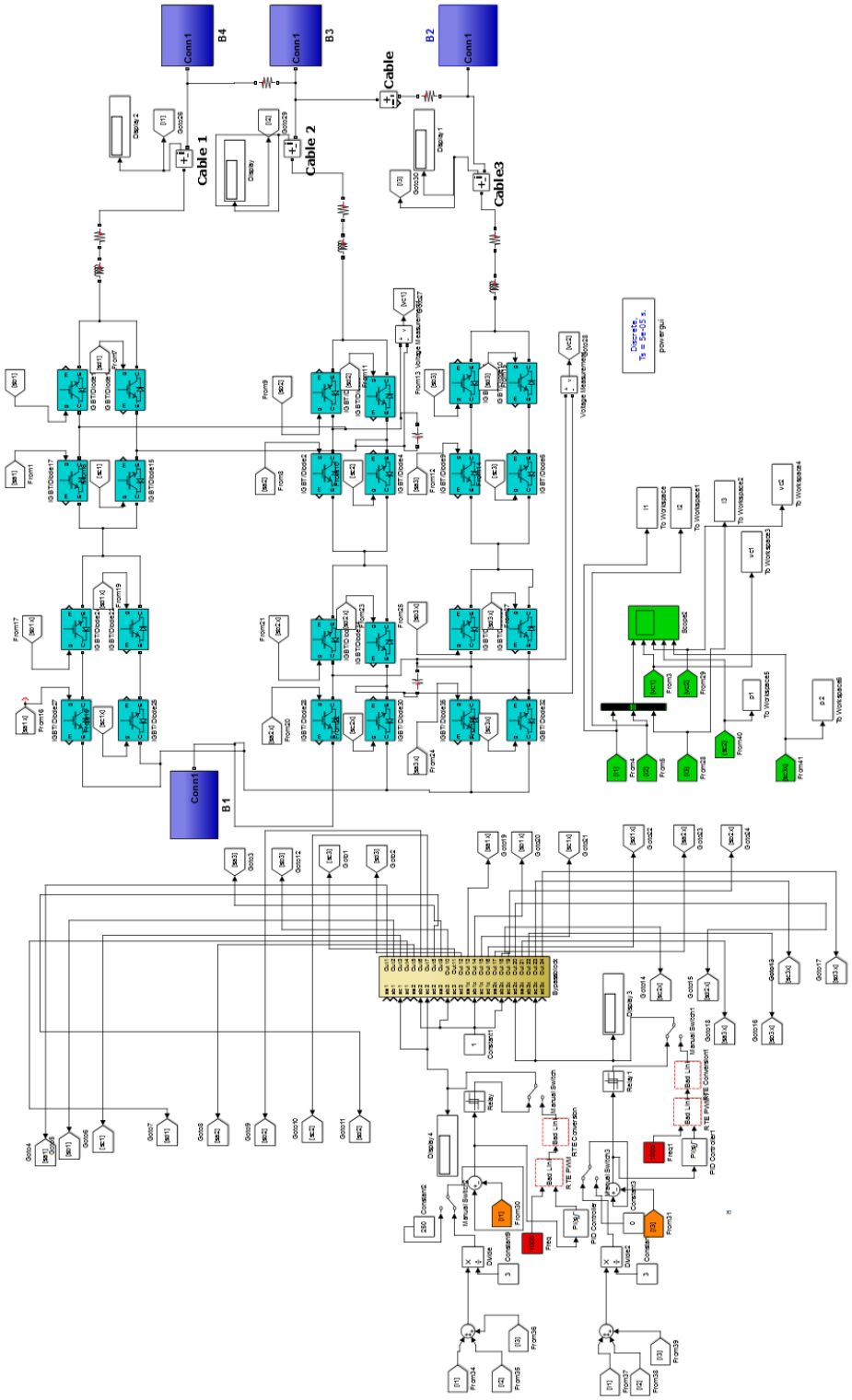


Figure B.4 MATLAB model of three port MCFC.

B.2 PSCAD/EMDTC Simulation Models and Additional Results

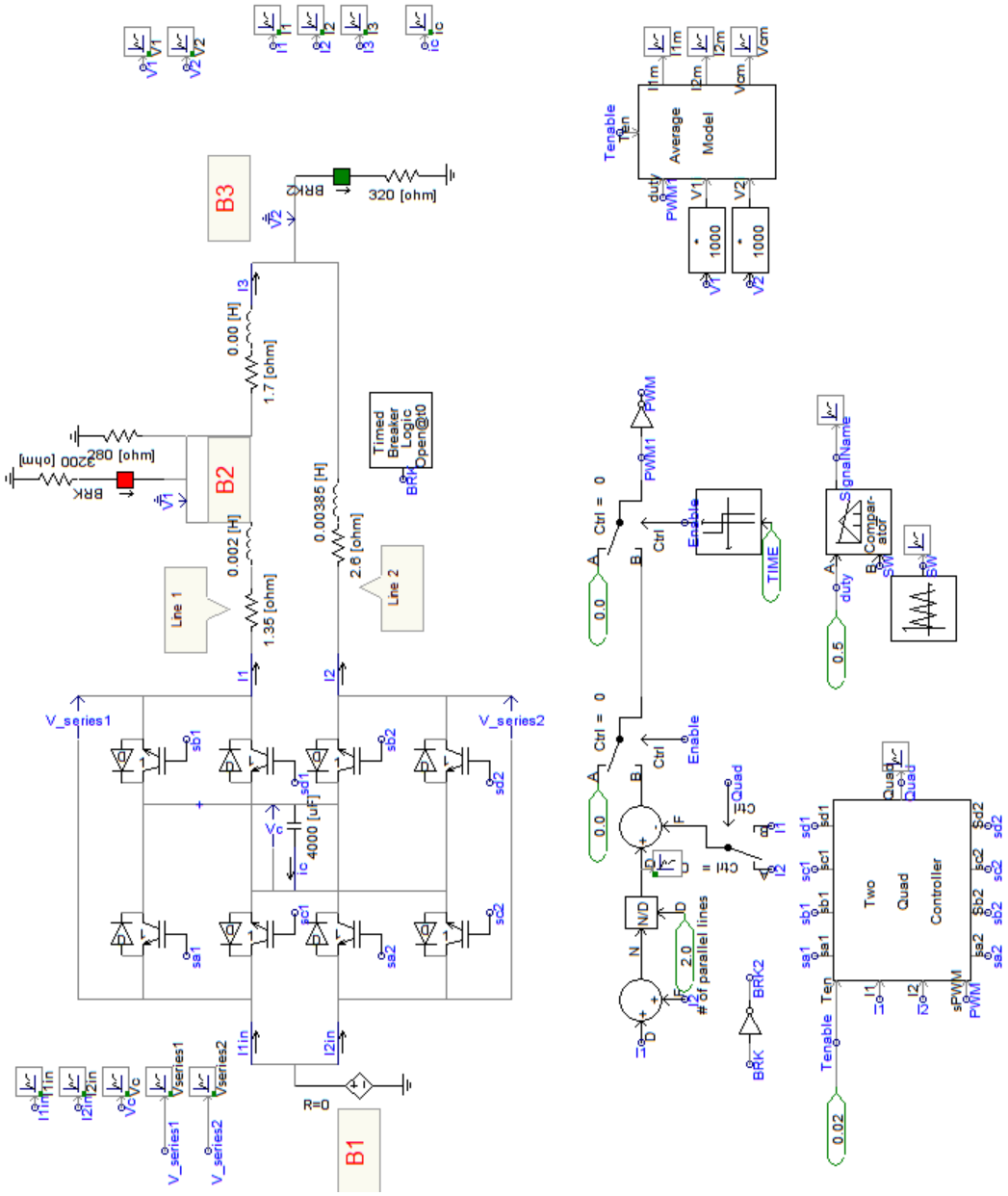


Figure B.5 PSCAD model for two port CFC and dynamic model verification.

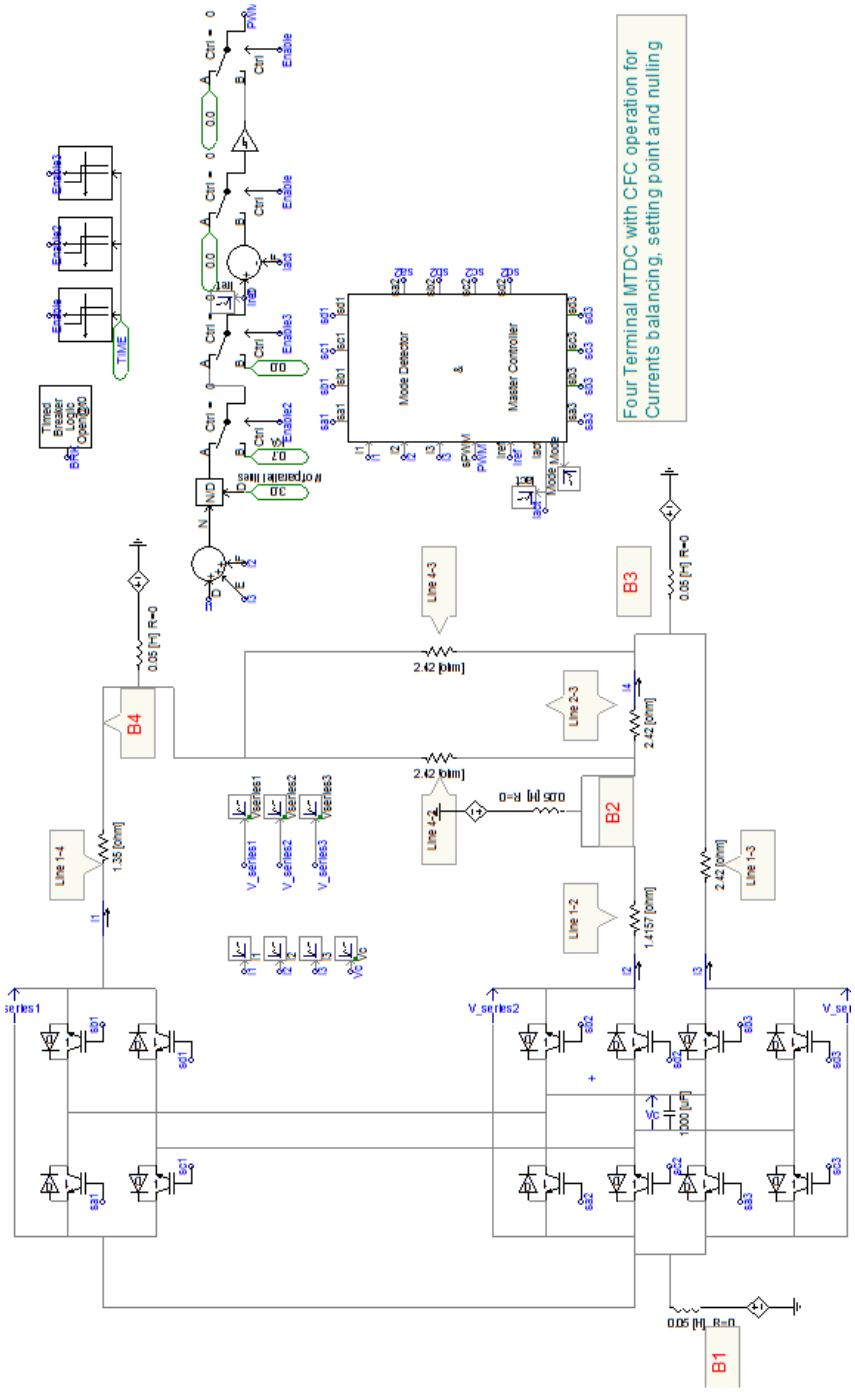


Figure B.6 PSCAD three port CFC extended topology with HCC.

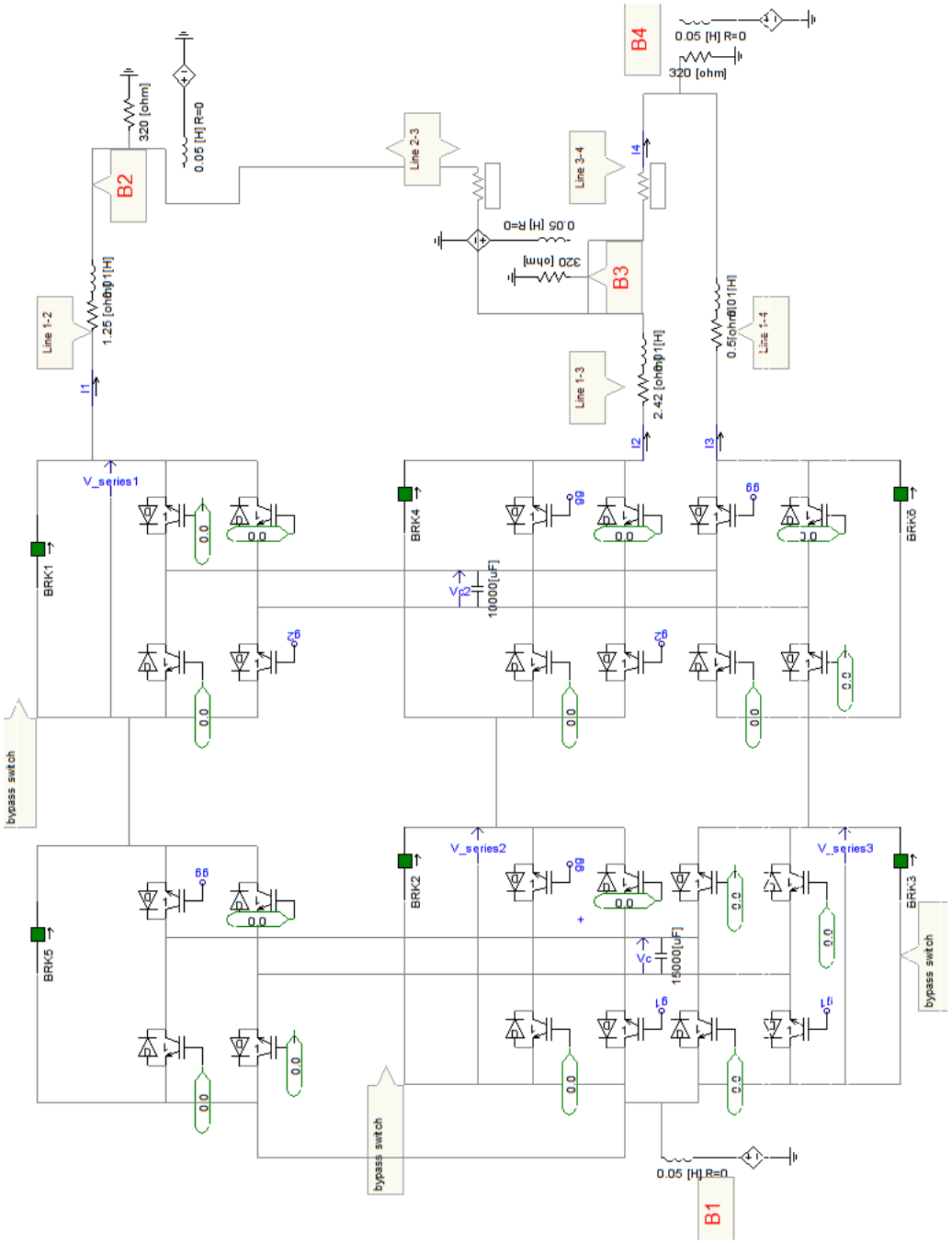


Figure B.7 PSCAD model of three port MCFC.

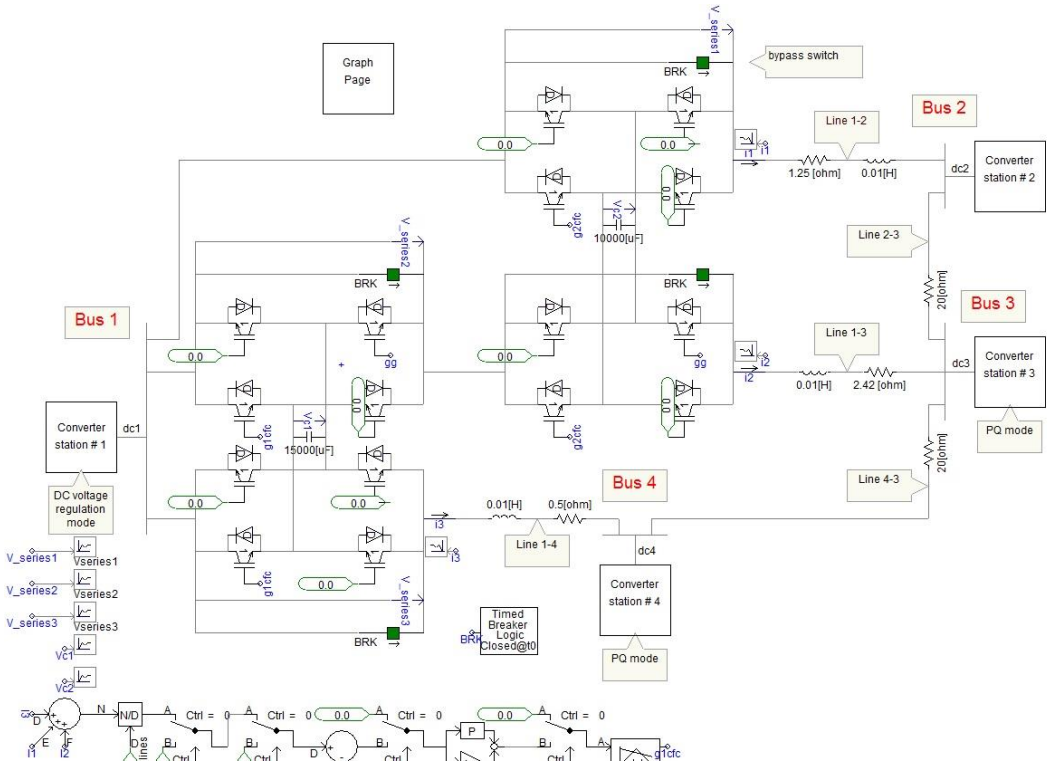


Figure B.8 VSC based four terminals DC grid with MCFC inserted simulation model.

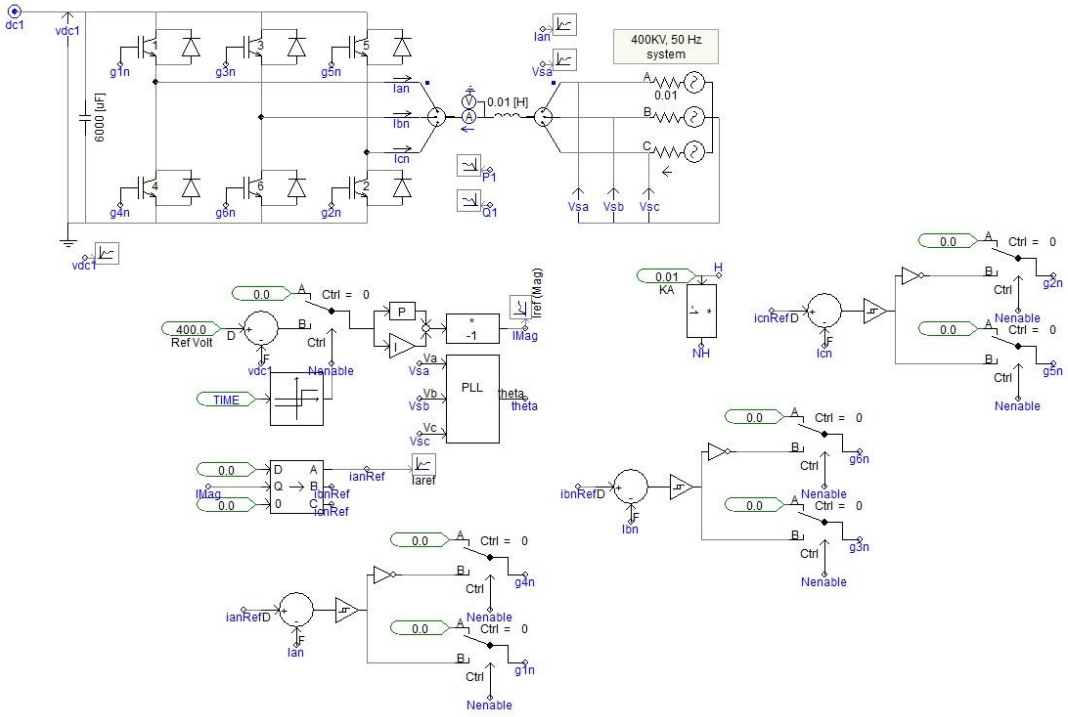


Figure B.9 Converter station 1 control circuits (voltage regulating).

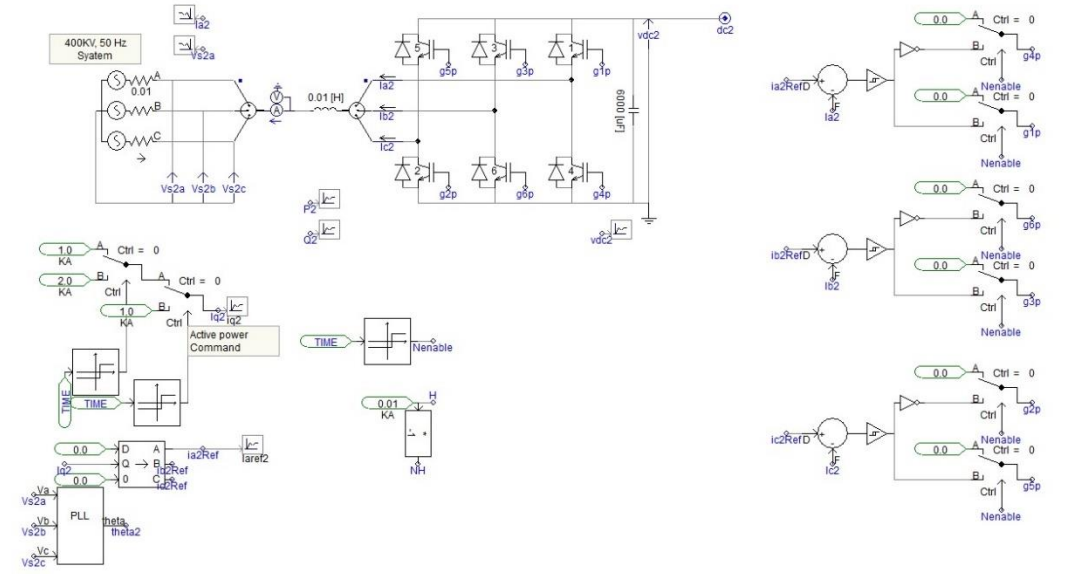


Figure B.10 Converter station 2 control circuit (power control).

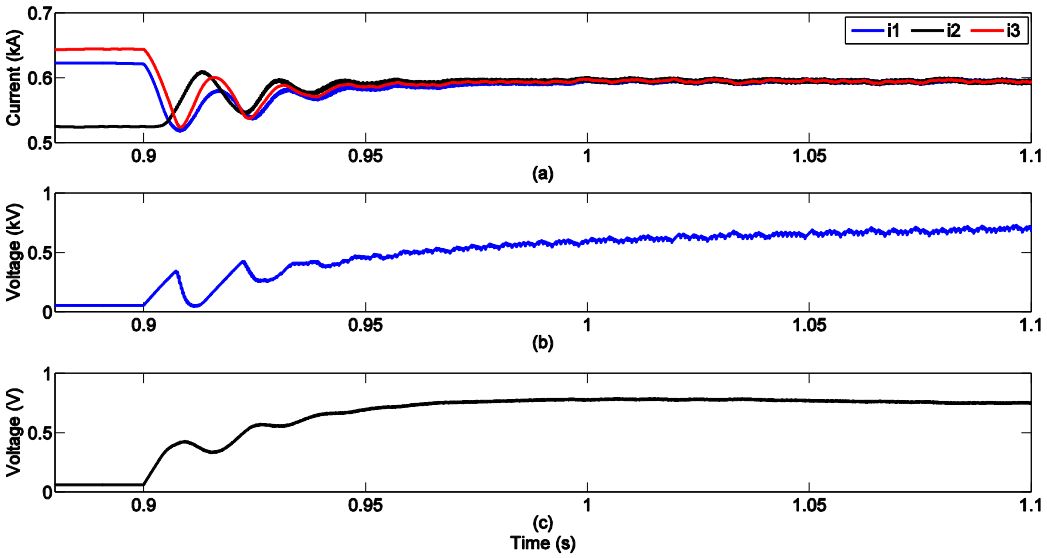


Figure B.11 MCFC performing currents balancing: mode 3. a) Cable currents, b) Capacitor voltage Vc1, c) Capacitor voltage Vc2

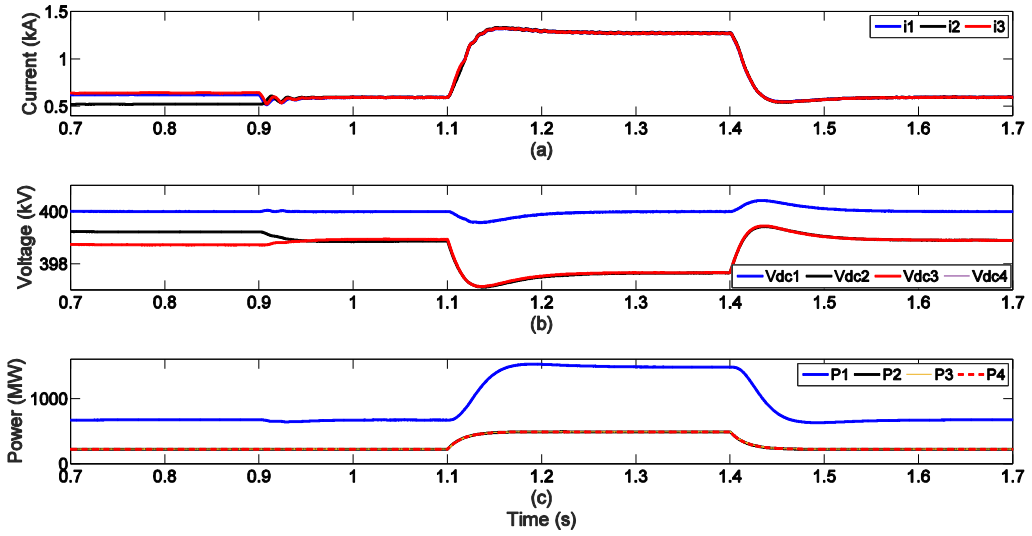


Figure B.12 Dynamic performance of MCFC under sudden load change.
(a) Cable currents, (b) Terminal voltages, (c) Active powers.

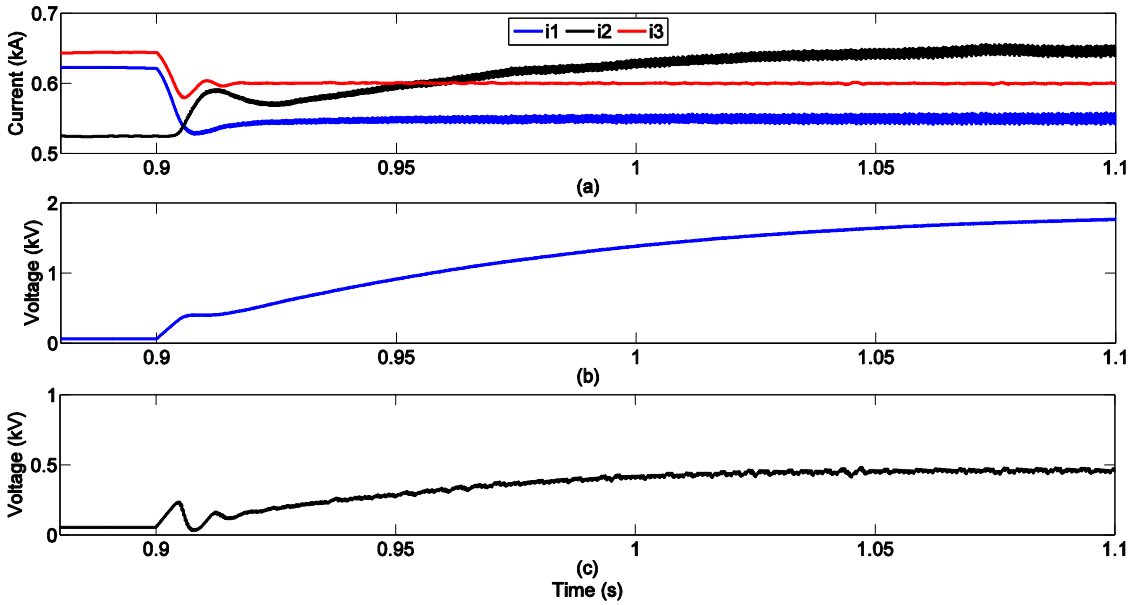


Figure B.13 Setting i1 and i3. (a) Cable currents, (b) Capacitor voltage Vc1, (c) Capacitor voltage Vc2.

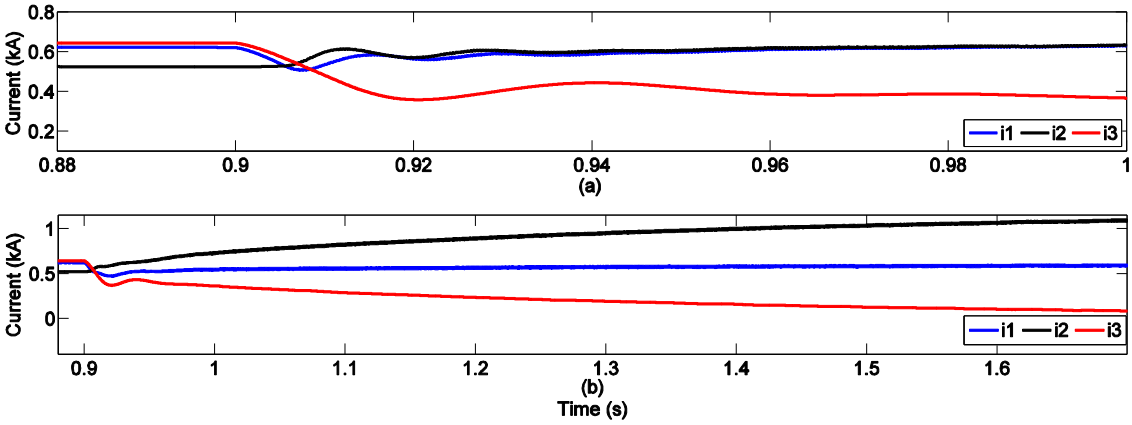


Figure B.14 MCFC performing simultaneous tasks. (a) Setting i3 to 0.375kA and balancing i1 and i2, (b) Nulling i3 and setting i1 to 0.6kA.

Appendix

C.

Details of the Experimental Setup

C.1 OPAL RT Programming Code

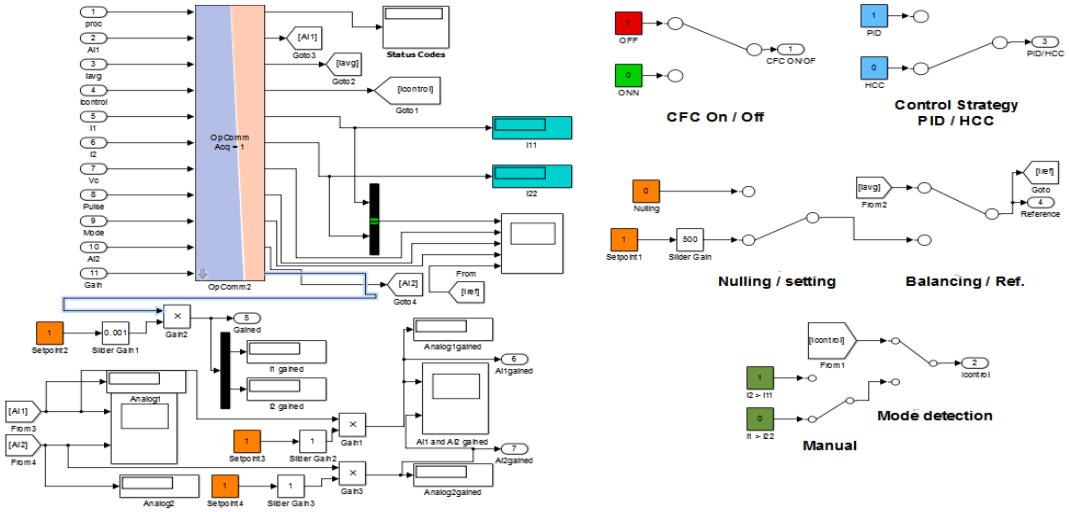


Figure C.1 OPALT RT GUI.

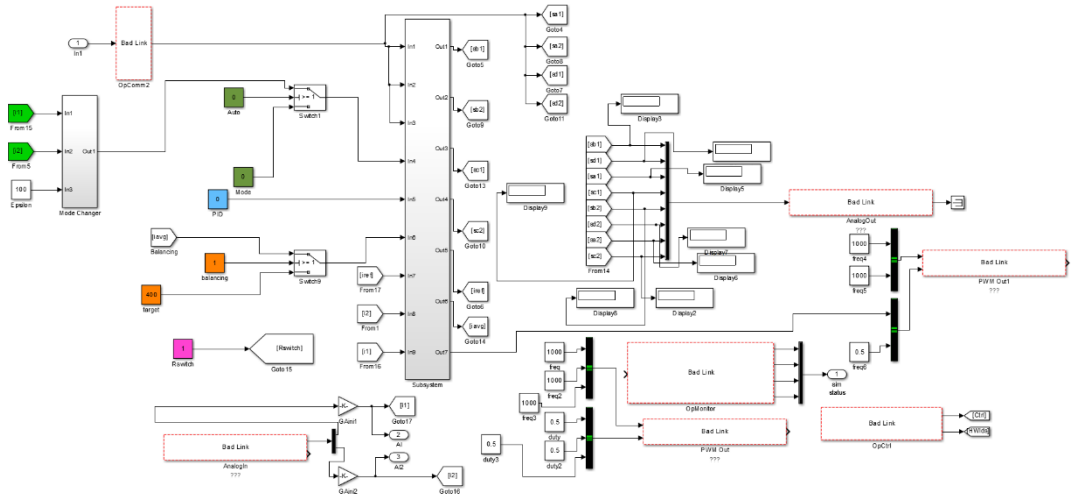


Figure C.2 OPAL RT master code.

C.2 LABVIEW Programming Code

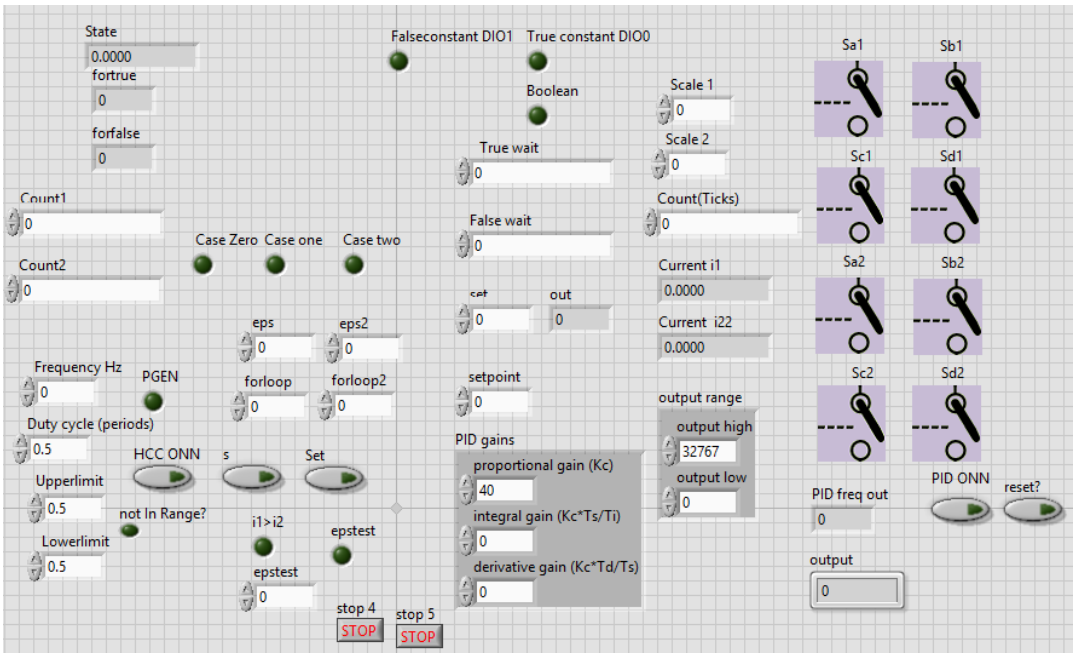


Figure C.3 LABVIEW front panel GUI.

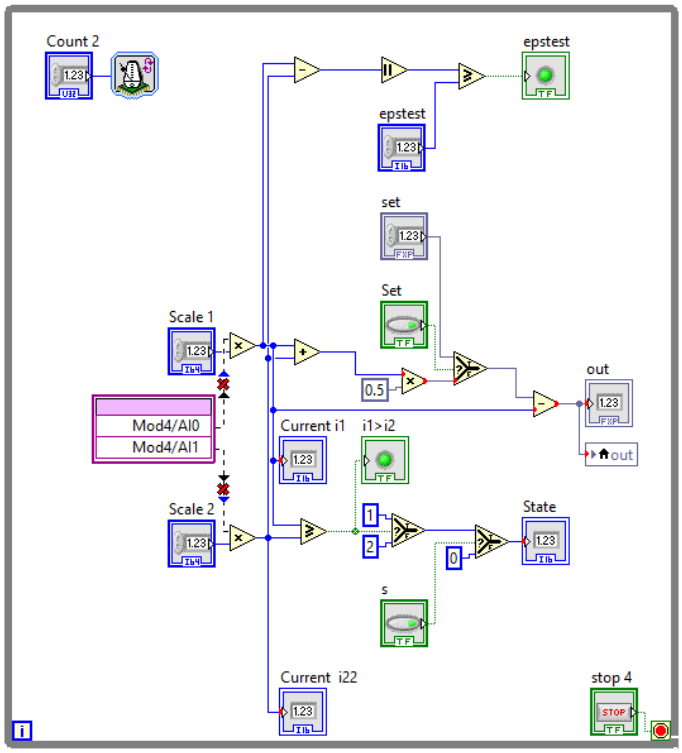


Figure C.4 LABVIEW currents reading and comparing loop.

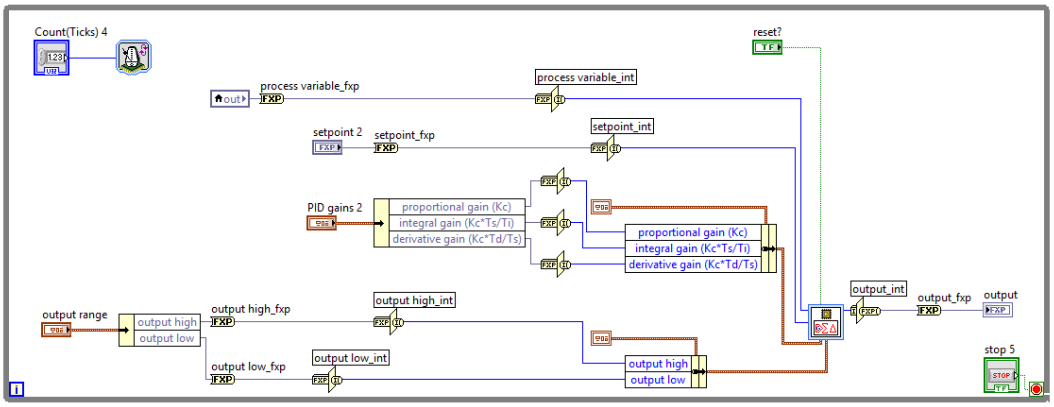


Figure C.5 LABVIEW PID controller loop.

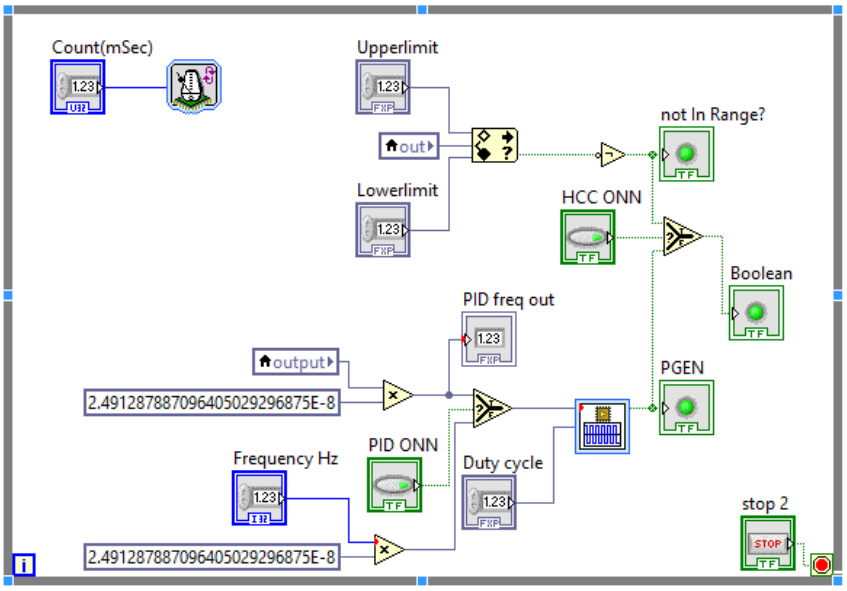


Figure C.6 LABVIEW controller selection loop.

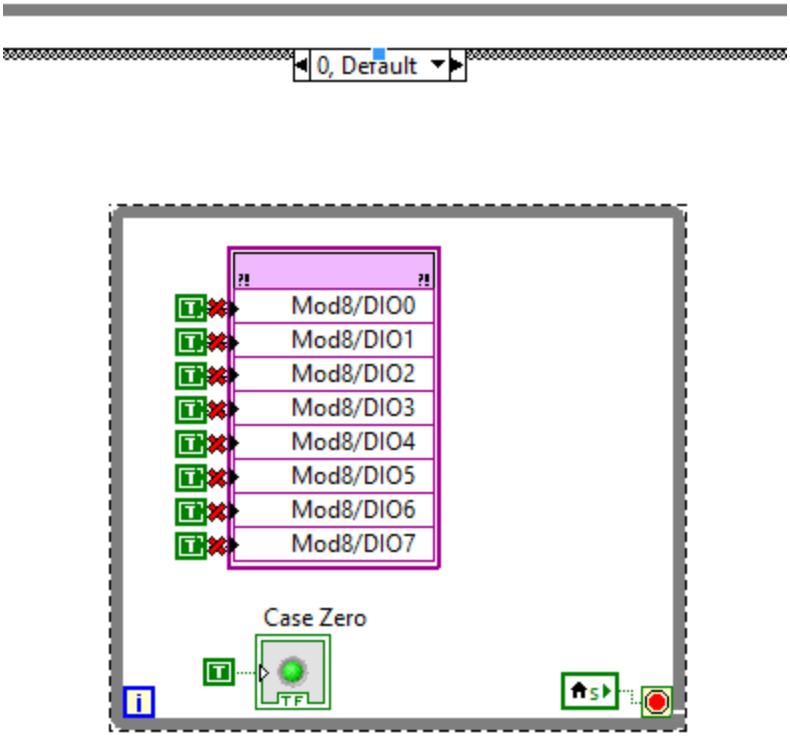


Figure C.7 LABVIEW CFC bypass case 0.

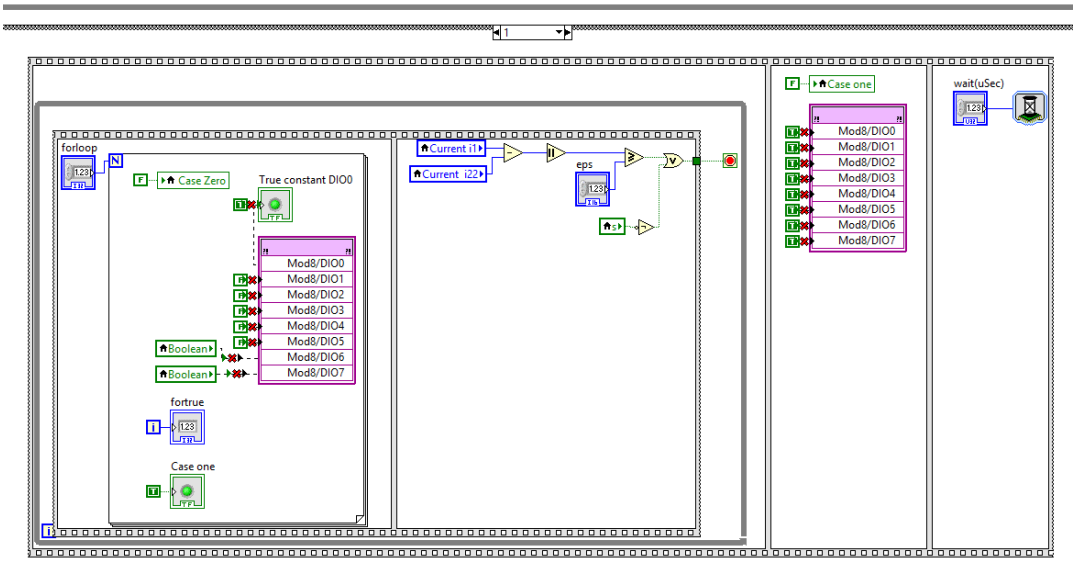


Figure C.8 LABVIEW CFC mode 1.

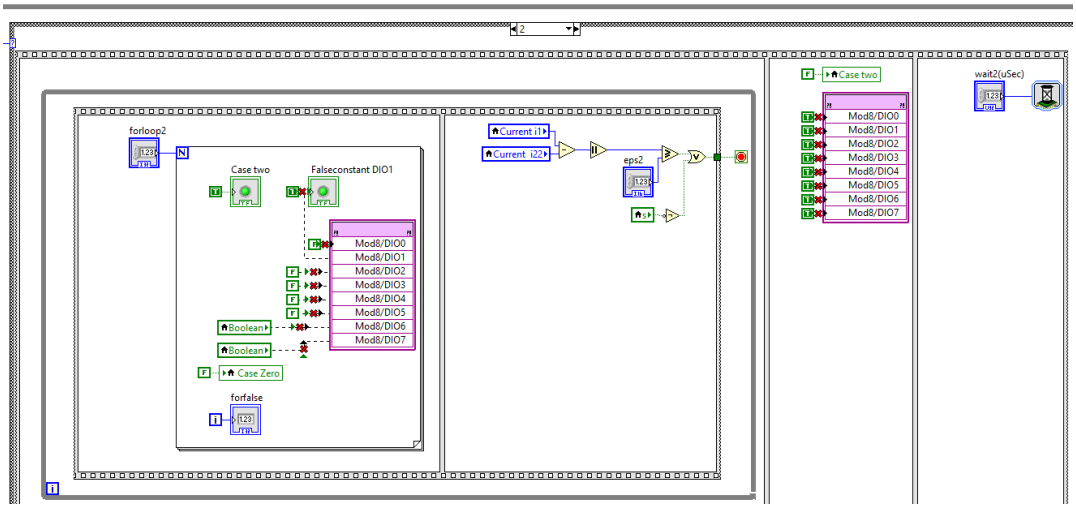


Figure C.9 LABVIEW CFC mode 2.

Appendix

D.

Selected Publications by the Author

IET Power Electronics

Special Issue on Converters and Semiconductor Circuit Breakers for HVDC and DC Grids

IET Journals
The Institution of Engineering and Technology

Operation and control of an insulated gate bipolar transistor-based current controlling device for power flow applications in multi-terminal high-voltage direct current grids

ISSN 1755-4535
Received on 3rd July 2015
Revised on 5th November 2015
Accepted on 4th December 2015
doi: 10.1049/iet-pel.2015.0525
www.ietdl.org

Hatem Yassin Diab[1] ✉, *Mostafa Ibrahim Marei*[2], *Sarath Bandara Tennakoon*[1]

[1]*School of Engineering, Faculty of Computing, Engineering and Science, Staffordshire University, Stoke on Trent, UK*
[2]*Electrical Power and Machines Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt*
✉ *E-mail: hatem.diab@research.staffs.ac.uk*

Abstract: One of the main problems that need to be solved to allow the realisation of multi-terminal high-voltage direct current (HVDC) transmission systems is the absence of a practical power flow control method. Industry leaders and researchers have proposed a few methods of power flow control based on either the control of converter station or the connection of new power electronic equipment to the grid. This study presents the operation and control of a three-port insulated gate bipolar transistor-based current flow control (CFC) device suitable for multi-terminal HVDC systems. Key features and functionalities of the proposed controller including the balancing of cable currents, limiting the magnitude of cable current and current nulling are demonstrated. The three-port CFC was simulated using power system computer aided design (PSCAD)/electromagnetic transient and direct current (EMTDC), network simulation software to evaluate its steady state and dynamic performance. Furthermore, low-power prototypes are implemented for a two and three-ports CFC to experimentally validate their different functionalities. Simulation and experimental studies explore the fast dynamic response and the results show that the CFC studied may have a significant role to play in the control of power flows in multi-terminal high-voltage DC systems.

1 Introduction

As more and more offshore wind farms are being installed in the North Sea area in the recent few years [1–4], the concept of a multi-terminal high-voltage DC grid (MTDC) to interconnect the wind farms owned by European countries has emerged [5–9]. The idea of forming an MTDC grid has been proposed since the early use of high-voltage direct current (HVDC) transmission systems [10], but it was not possible to develop this idea into practical devices until the recent emergence of high-voltage source converters (VSCs). Still major challenges [11, 12] are investigated by researchers and industry such as the need for HVDC circuit breakers and protection schemes and algorithms [13–15], DC transformers [16–19] and power flow control methods. Approaches to develop power flow control in MTDC are based either on modifying the control of the VSC's [20–28] or adding additional devices to the grid itself [29–35]. This paper presents an insulated gate bipolar transistor (IGBT)-based current flow control (CFC) device [35] for precise CFC in MTDC grids to achieve different functionalities such as balanced cables loading and current nulling in one cable to ease the maintenance of cables. The CFC can be installed in series with the cables at a terminal of the grid and isolated from the system ground as shown in Fig. 1. The circuit topology of the proposed CFC is determined by the number of cables that it controls. The CFC's major advantage is that inserting it in series with the cables means that relatively low-voltage rating IGBTs with low cost are needed when compared with the grid voltage rating. Complete operation and control of a three-port CFC is presented in this paper to balance the three currents, set a current to desired reference point or even null a current in any chosen cable. Simulation results show accurate performance of the CFC and fast dynamic response even under transient load conditions. Furthermore, experimental validation is carried out by building two-ports and three-port prototypes to test different cases.

This paper is organised as follows: in Section 2, DC power flow control problem is explained in comparison with the AC power flow control problem. While in Section 3, the CFC circuit topology and theory of operation is explained. In Section 4, the mathematical model of the CFC is discussed followed by the proposed CFC control, simulation results and experimental validation in Sections 5–7, respectively. Finally, conclusions are drawn in Section 8.

2 Power flow control concepts

There are several established methods of controlling the power flow in AC power transmission systems leading to the concept of flexible AC transmission systems (FACTS), appears in the 1990s [36, 37]. FACTS theory of operation is based on the characteristics of AC real power that can be expressed in the following equation

$$P_{AC} = \frac{V_1 \cdot V_2 \sin(\delta)}{X} \tag{1}$$

where V_1 and V_2 are the sending and receiving end root mean square voltages, δ is the power angle and X is the line impedance as shown in Fig. 2*a*. Power flow control can be achieved through varying the line impedance by a number of techniques.

However in DC systems, DC power flow is determined by the line resistance according to (2)

$$P_{DC} = \frac{V_1 \cdot \Delta V}{R} \tag{2}$$

where V_1 is the sending end DC voltage, ΔV is the potential difference between the sending and the receiving ends and R is the total resistance of the line as shown in Fig. 2*b*. One obvious method is to insert series resistors to control the current flow using conventional mechanical switches or fast power electronic devices such as IGBT or thyristor switches [29, 30]. However, the power losses introduced by the inserted resistances and thermal problems make this impractical specially in HVDC applications where currents are high. Another proposed approach is to add or subtract

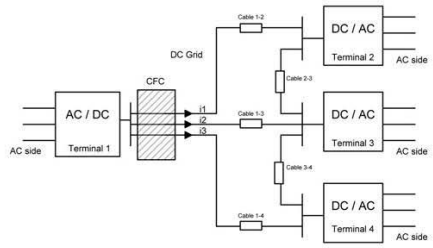


Fig. 1 *Four terminal meshed HVDC grid with CFC inserted in series*

power from a certain line by introducing additional bidirectional three-phase converter that acts as a series DC voltage source [32, 34]. The need of a relatively large AC transformer to feed the series converter from the high-voltage grid makes this approach not economical though the required lower voltage can be obtained via tertiary winding of the main converter's transformer.

The CFC topology presented in this paper consists of four IGBT switches with parallel freewheeling diodes for each cable and a common capacitor as shown in Fig. 3*a*. The capacitor is charged and discharged to transfer voltage from a cable to another with theoretically no power loss, except for the switching losses of the IGBTs. The proposed topology can be applied to any number of cables by expanding the circuit with four more IGBTs for each added cables. The proposed multi-port CFC offers an economical solution for current balancing and limiting as it is inserted in series with the cables and without connection to the system ground resulting in relatively cheap low-voltage rated IGBTs. In the following section, the operation of the CFC is explained.

3 Modes of operation of the proposed three-port CFC

The basic idea of the CFC is to use the capacitor to transfer energy from the cables carrying current higher than the average value to the cables that carries low current. This action results in balancing the current in the cables connected to the CFC. There are many modes of operations for the proposed CFC depending on the cable current directions and magnitudes. The following sections discuss the switching states of the proposed three-port CFC for different modes of operation.

3.1 Operation in forward direction

Figs. 3*b* and *c* illustrate the three-port CFC operation in the forward direction, where the currents are assumed to be outgoing from the CFC. In this case, two modes are considered. The first mode where one cable carries the highest current while the currents of the other cables are lower than the average value of the three cable currents. In the second mode, two cables are carrying currents higher than the balanced value. For mode 1, assuming i_1 is the highest current, switches S_{b2} and S_{b3} are turned-on during the charging period to allow for the currents i_2 and i_3 to flow directly in their cables, while cable 1 is connected to the capacitor through the feedback diodes of S_{a1} and S_{d1}, as shown in Fig. 3*b*. As a result, i_1 is reduced by charging the capacitor. In the discharging period of the capacitor, switches S_{c2} and S_{c3} are turned-on to insert the capacitor to cables 2 and 3 with reverse polarity, as shown in Fig. 3*c*. This action is similar to introducing opposite voltage source to these cables. In addition, S_{c1} is turned-on to allow the flow of i_1 in its cable. The charging and discharging states are kept interchanging to transfer of power from cable 1 to cables 2 and 3. This mode of operation is useful when cable 1 is carrying much more current and it is needed to redistribute it among the other two cables.

Another mode of operation is where two cables, 1 and 2, for example, are carrying high currents and it is required to transfer power from these cables to cable 3 (mode 4). In charging state, the capacitor is charging from cables 1 and 2 through the feedback diodes of S_{a1}, S_{d1} and S_{a2}, S_{d2}, respectively. Moreover, switch S_{b3} is turned-on to allow the flow of i_3 directly in its cable, as indicated in Fig. 4*a*. During the discharging state, switches S_{c1}, S_{c2} and S_{c3} are turned-on to transfer energy stored in the capacitor from cables 1 and 2 to cable 3 as shown in Fig. 4*b*.

3.2 Operation in reverse direction

In this case, the three cable currents are reversed in direction to go into the CFC from the right side, as illustrated in Figs. 4*c* and *d*. All the switching sequences discussed for modes 1–6 of the forward direction are changed. Modes 7–12 are similar to modes 1–6, but the currents are reversed. For mode 9, if i_3 is the highest current magnitude, switches S_{d1} and S_{d2} are turned-on to bypass their currents and the capacitor is charged from cable 3 as demonstrated in Fig. 4*c*. During the discharge state, the capacitor with reverse polarity is inserted in cables 1 and 2 by turning-on S_{a1} and S_{a2}, respectively, as shown in Fig. 4*d*. In addition, S_{a3} is turned-on to allow the flow of i_3 in its cable. Similarly, the previous switching algorithm can be modified so that currents can be transferred from any desired cable(s) to the remaining cable(s).

On the basis of the previous discussion of the different modes of operation of the proposed three-port CFC, the switching states for different conditions of the cable currents are shown in Table 1. The second column of Table 1 includes the currents with magnitudes higher than the average value of the three cables originated from the CFC. As indicated, three possibilities for the highest current at each mode, and hence a total of 12 switching states are presented.

4 Modelling of the proposed three-port CFC

This section presents the dynamic model of the proposed three-port CFC using averaging technique where the terminals voltages are taken into consideration as setting values. Figs. 3*b* and *c* illustrate the circuit diagrams of the three-port CFC for the charging and

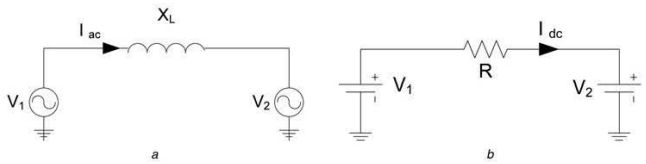


Fig. 2 *Point-to-point electrical connections*
a AC circuit
b DC circuit

discharging operation mode 1. The following set of equations describes the circuit of Fig. 3*b* when the capacitor is charging from the line carrying the highest current, i_1

$$V = r_1 i_1 + L_1 \frac{\mathrm{d}i_1}{\mathrm{d}t} + v_\mathrm{c} + V_1 \tag{3}$$

$$V = r_2 i_2 + L_2 \frac{\mathrm{d}i_2}{\mathrm{d}t} + V_2 \tag{4}$$

$$V = r_3 i_3 + L_3 \frac{\mathrm{d}i_3}{\mathrm{d}t} + V_3 \tag{5}$$

$$i_1 = C \frac{\mathrm{d}v_\mathrm{c}}{\mathrm{d}t} \tag{6}$$

where r_x and L_x are the resistance and the inductance of the line number x originated from the CFC bus and carrying an instantaneous current i_x, v_c is the capacitor voltage, V is the voltage at the bus where the CFC is connected to, V_1, V_2, and V_3 are the voltages at the end terminals of the first, second and third lines, respectively. By defining $\boldsymbol{x}^\mathrm{T} = [i_1 \;\; i_2 \;\; i_3 \;\; v_\mathrm{c}]$ as state vector, where the super-suffix T refers to the transpose operation, (4)–(6) can be arranged in matrix form as (see (7))

Similarly, the state equations of Fig. 3*c*, where the capacitor is discharging into the two other lines carrying currents i_2 and i_3, are as follows: (see (8))

Assume the duty ratio of the charging mode of operation is D. Multiplying (7) and (8) by D and $(1-D)$, respectively, and adding the results to obtain the average model for the CFC for mode 1 as follows: (see (9))

where $A = DA_1 + (1-D)A_2$ and $B = DB_1 + (1-D)B_2$. At steady state, (9) is written as (see (10))

where I_1, I_2, I_3 and V_c are the steady-state values of i_1, i_2, i_3 and v_c, respectively. Solving (10), the steady-state value of capacitor voltage is obtained as

$$V_\mathrm{c} = \frac{D(V - V_1) - r_1(1-D)\{V - V_2/r_2 + V - V_3/r_3\}}{D^2 + r_1(1/r_2 + 1/r_3)(1-D)^2} \tag{11}$$

Equation (11) gives an expression for the capacitor voltage as a function of the network parameters and the voltage drops across the cables connected to the CFC which represents the loading condition of the grid. It is worth mentioning that the rated voltage of the CFC switches, which is equal to the rated capacitor voltage, can be estimated from (11).

To calculate the capacitor voltage ripple, (6) is integrated over the charging period as follows

$$\int_0^{DT} i_1 \,\mathrm{d}t = C \int_{V_\mathrm{cmin}}^{V_\mathrm{cmax}} v_\mathrm{c} \tag{12}$$

where T refers to the switching period which is the reciprocal of the switching frequency f_s. Neglecting the current ripples compared with the average value, I_1, results in linear charging of the capacitor from initial minimum voltage V_cmin to maximum voltage V_cmax. Therefore, the capacitor voltage ripple, ΔV_c can be estimated from (12)

$$\Delta V_\mathrm{c} = V_\mathrm{cmax} - V_\mathrm{cmin} = \frac{D\,I_1}{C\,f_\mathrm{s}} \tag{13}$$

It can be seen from (13) that increasing the capacitance reduces the capacitor voltage ripple, as expected. As can be seen from (10), the parameters of the DC grid and loading condition influence the line current which affects the capacitor voltage ripple. Moreover, the capacitor voltage ripple depends on the mode of operation as the charging current, which is I_1 for mode 1, changes from mode to another. For mode 1, the capacitance can be roughly estimated from (11) and (13) to meet a required percentage voltage ripple, $\Delta V_{\mathrm{c\_pu}} = \Delta V_\mathrm{c}/V_\mathrm{c}$, at the extreme deviations of the line currents. In a similar way, the capacitance can be calculated for each mode of operation for the CFC. Finally, the maximum value of the capacitance is considered to meet the desired level of voltage ripple for all modes of operation. In this paper, the capacitance of the CFC is selected using trial and

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & L_3 & 0 \\ 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_\mathrm{c} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -1 \\ 0 & -r_2 & 0 & 0 \\ 0 & 0 & -r_3 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_\mathrm{c} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B_1} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{7}$$

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & L_3 & 0 \\ 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_\mathrm{c} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & 0 \\ 0 & -r_2 & 0 & 1 \\ 0 & 0 & -r_3 & 1 \\ 0 & -1 & -1 & 0 \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_\mathrm{c} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B_2} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{8}$$

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & L_3 & 0 \\ 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_\mathrm{c} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -D \\ 0 & -r_2 & 0 & 1-D \\ 0 & 0 & -r_3 & 1-D \\ D & -1+D & -1+D & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_\mathrm{c} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \tag{9}$$

$$\underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -D \\ 0 & -r_2 & 0 & 1-D \\ 0 & 0 & -r_3 & 1-D \\ D & -1+D & -1+D & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_\mathrm{c} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} = 0 \tag{10}$$

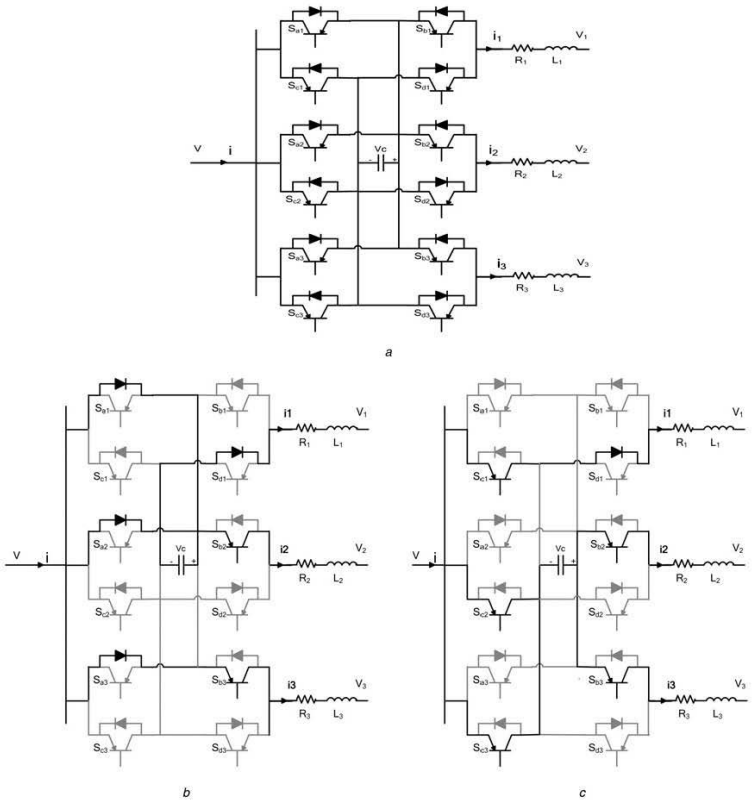


Fig. 3 *Proposed three-port CFC*

a Schematic diagram of the proposed three-port CFC
b Charging the capacitor from cable 1 (mode 1 – forward operation)
c Discharging the capacitor in cables 2 and 3 (mode 1 – forward operation)

error since the practical limitations of the DC grid under study are not considered.

5 Proposed control system of the CFC

One of the features of the CFC is the ability to balance currents in the transmission cables or cables. Currents one or more can be relatively high and with the balancing control all currents can be maintained within the acceptable limits and redistributed among all branches in order to prevent overloading of cables. Furthermore, the proposed CFC can set the current flow of one cable to a desired value either to limit the current or damp it to zero. This feature may help in cases of maintenance of the cables as only off load dis-connector switches are required to isolate the cable eliminating the need for a DC circuit breaker or interrupting the whole transmission by opening the AC side circuit breaker.

A controller is designed to implement the CFC operation explained in the previous section. For currents balancing, the sum of currents in the three branches is measured and then divided by the number of branches to obtain the average value of the desired current, i^*. This value is considered the reference value to be compared with the measured value of the current(s) that need to be redistributed. The user can assign a value directly to i^* to achieve the other desired functions of current nulling or limiting. The error signal is processed using a proportional–integral (PI) controller which produces the gating signals to the relevant switches as shown in Fig. 5*a*. Similarly, any desired cable current can be limited to any chosen value. This value is set as the reference value for the controller and switches are controlled to let the capacitor charge from the chosen cable and discharge in the other two cables. If the reference value is set to zero, the capacitor will charge from the desired cable until it is fully charged to stop the current flow in this cable. As there are theoretically no power losses, except for the switching losses of IGBTs, when the current is decreased in any cable by a certain amount it will increase by the same amount in the remaining cables. It is important to check the capacity of these cables to prevent overloading problems.

Furthermore, Fig. 5*b* illustrates another proposed controller for the CFC not only to control the current flow, but also to regulate the capacitor voltage. The outer controller, which is the current control loop, is realised by a simple PI controller, similar to that of

IET Power Electron., 2016, Vol. 9, Iss. 2, pp. 305–315

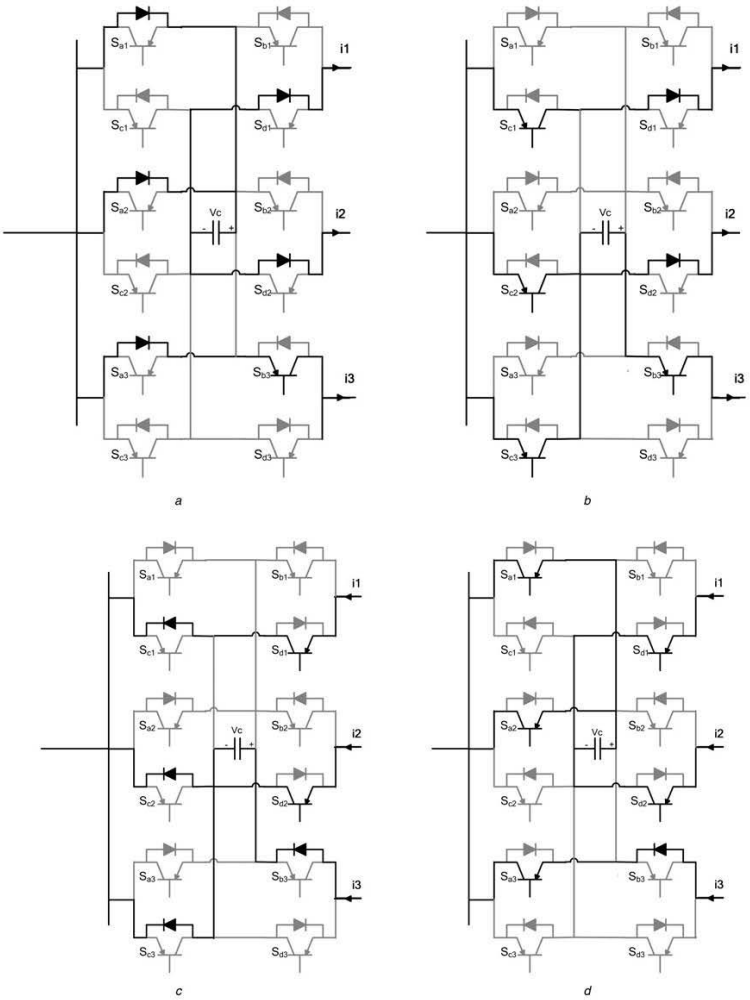


Fig. 4 *CFC conduction states*

a Charging the capacitor from cables 1 and 2 (mode 4 – forward operation)
b Discharging the capacitor in cable 3 (mode 4 – forward operation)
c Charging the capacitor from cable 3 (mode 9 – reverse operation)
d Discharging the capacitor in cables 1 and 2 (mode 9 – reverse operation)

Fig. 5*a*, to process the error between the reference value i^* and the actual current i_x, determined from the mode detector, to set the required setting of the capacitor voltage v_c^*. A limiter can be used to prevent exceeding the rated capacitor voltage. The inner control loop is dictated to regulate the capacitor voltage at its estimated value from the outer one using another PI controller. The output of this controller is the duty cycle of the modulating switches.

With the aid of Table 1, a generic control algorithm, shown in Fig. 5*c*, is designed to automatically select the relevant switches to be controlled based on the required operation mode. First, the controller acquires the measured currents and determines the operating mode. If the currents flows are changed in the grid during balancing current operation, the line currents are no longer balanced. This fact is employed to detect the mode of operation. Simply, the operating mode must be changed if any current hits a hysteresis window centred around the average value. Consequently, the CFC controller is deactivated, for a short time, to identify the new mode precisely before reactivating once again

Table 1 Switches conduction states

Mode	Currents	Direction	Switching states											
			S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	S_{c1}	S_{c2}	S_{c3}	S_{d1}	S_{d2}	S_{d3}
1	i_1	forward	off	off	off	off	on	on	pulsed	pulsed	pulsed	off	off	off
2	i_2	forward	off	off	off	on	off	on	pulsed	pulsed	pulsed	off	off	off
3	i_3	forward	off	off	off	on	on	off	pulsed	pulsed	pulsed	off	off	off
4	i_1 and i_2	forward	off	off	off	off	off	on	pulsed	pulsed	pulsed	off	off	off
5	i_2 and i_3	forward	off	off	off	on	off	off	pulsed	pulsed	pulsed	off	off	off
6	i_1 and i_3	forward	off	off	off	off	on	off	pulsed	pulsed	pulsed	off	off	off
7	i_1	reverse	pulsed	pulsed	pulsed	off	off	off	off	off	off	off	on	on
8	i_2	reverse	pulsed	pulsed	pulsed	off	off	off	off	off	off	on	off	on
9	i_3	reverse	pulsed	pulsed	pulsed	off	off	off	off	off	off	on	on	off
10	i_1 and i_2	reverse	pulsed	pulsed	pulsed	off	off	off	off	off	off	off	off	on
11	i_2 and i_3	reverse	pulsed	pulsed	pulsed	off	off	off	off	off	off	on	off	off
12	i_1 and i_3	reverse	pulsed	pulsed	pulsed	off	off	off	off	off	off	off	on	off

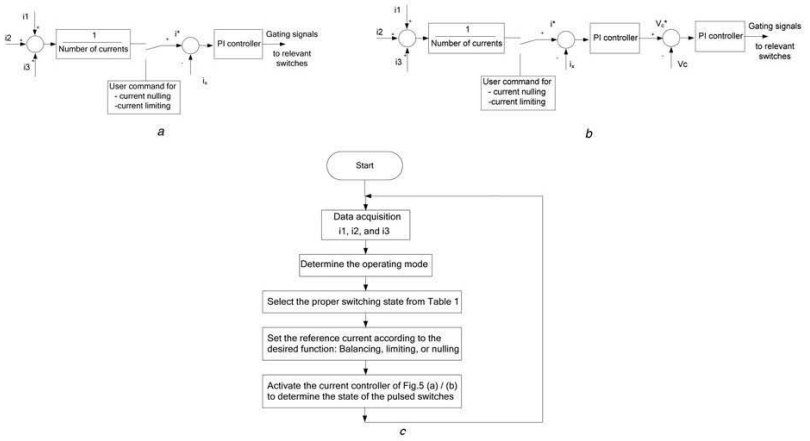


Fig. 5 *Proposed control for the three-port CFC*

a Current controller for the CFC switches
b Cascaded controller-based capacitor voltage regulation
c Flowchart of the proposed control algorithm

with the new mode settings. After checking the user-defined set point, the controller decides which switches are involved to operate the current controller as discussed earlier.

6 Simulation results

Simulation study is carried out using PSCAD/EMTDC software package in this section. A four terminals DC grid, shown in Fig. 1, is simulated to evaluate the dynamic and steady-state performance of the proposed three-port CFC. The system parameters are obtained from [38] where a multi-terminal HVDC grid is presented to set a base for research studies. The simulation parameters are shown in Table 2. Three case studies are presented in the following sections to evaluate the different features and operation modes of the proposed CFC.

Table 2 Simulation parameters

	Cable length, km	Value
grid voltage rating	–	400 kV
capacitor	–	4.7 mF
switching frequency	–	1 kHz
cable 1–2	142	1.35 Ω
cable 1–3	273	2.6 Ω
cable 1–4	263	2.5 Ω
cable 2–3	178	1.7 Ω
cable 3–4	85	0.8 Ω

6.1 Case 1: charging from cable 1 and discharging in cables 2 and 3

In this case study, currents i_1, i_2 and i_3 are equal to 1.1, 0.79 and 0.81 kA, respectively. It is required to redistribute the currents to achieve a balanced operation by decreasing the current flow in cable 1 and increase the currents flow in cables 2 and 3. The proposed control selects mode one of operation for the CFC which is programmed to activate at $t = 1.5$ s. Fig. 6*a* demonstrates that the proposed three-port CFC succeeds to balance the three cable currents with fast dynamics and without overshoot. Fig. 6*b* illustrates the capacitor voltage which is <600 V. This result proves one of the advantages of the proposed CFC that is the capacitor and switches voltage rating is very small when compared with the grid voltage 400 kV. The series voltage introduced by the CFC to each cable is shown in Fig. 6*c*. Note that series voltages of cables 2 and 3 are the same.

IET Power Electron., 2016, Vol. 9, Iss. 2, pp. 305–315

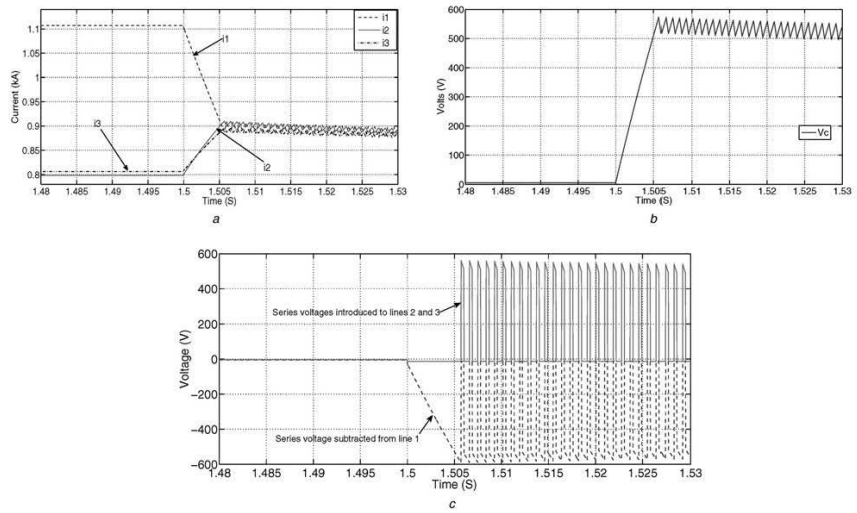


Fig. 6 *Charging the capacitor from cable 1 and discharging in cables 2 and 3*

a Cable currents
b Capacitor voltage
c Series voltages

6.2 Case 2: charging from cables 1 and 3 and discharging in cable 2

In this case study, currents i_1 and i_3 are higher than i_2 and the average value. Mode 2 is activated to redistribute the currents among the cables at $t = 1.5$ s. Fig. 7*a* indicates the successful action of the proposed CFC to decrease both i_1 and i_3 from 1.1 and 1 kA, and simultaneously increasing $i2$ from 0.8 kA to achieve a balanced operation at ~0.95 kA. Fig. 7*b* displays the capacitor voltage at this case.

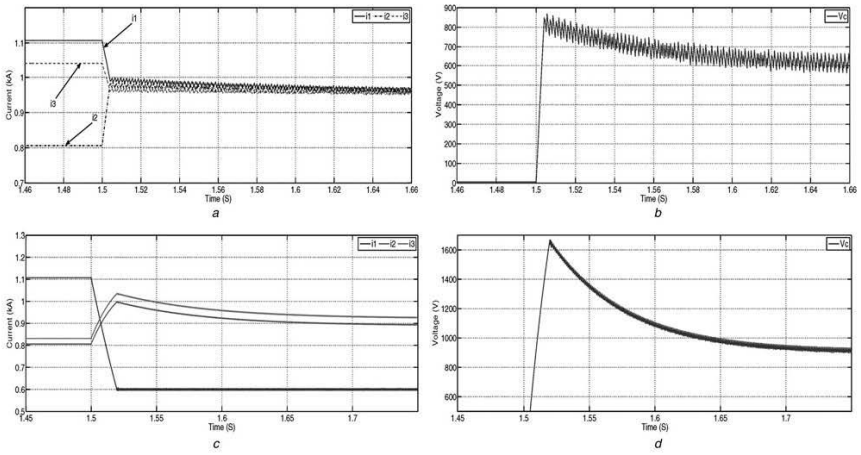


Fig. 7 *Simulation results*

a Cable currents during balancing
b Capacitor voltage during balancing
c Cable currents during current setting
d Capacitor voltage during current setting

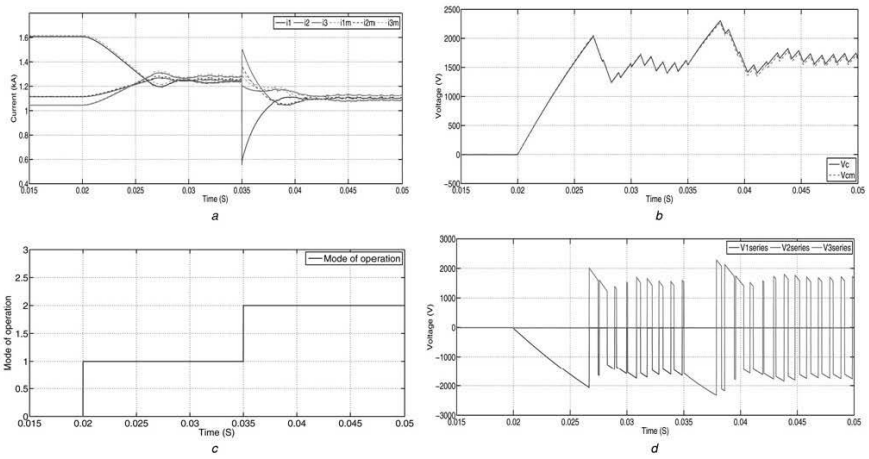


Fig. 8 *Comparison between the average model and detailed circuit simulation*

a Cable currents
b Capacitor voltage
c Mode of operation
d Series voltage introduced to each cable

6.3 Case 3: current set point

The final simulation case study is dedicated to test the feature of the proposed CFC to set any cable current to a desired value. In this case, current i_1 is equal to 1.1 kA, initially, and is required to reduce it to 0.6 kA. The CFC controller is enabled at $t = 1.5$ s. It can be noted from Fig. 7*c* that the CFC succeeds in achieving this target smoothly. The capacitor voltage at this case is shown in Fig. 7*d*. It is worth mentioning that the capacitor voltage for this case is higher than the previous cases. This action is expected as to achieve the required 46% reduction in one cable current, the capacitor should be charged to a higher level of voltage compared with the current balancing cases. As explained in Section 3.1, the capacitor is inserted to the other two cables to transfer the energy from cable 1.

6.4 Case 4: evaluating the average model and mode detection algorithm

To evaluate the accuracy of the average model, three cable inductances of values 2, 3.8 and 3.5 mH are added in simulation to cables 1, 2 and 3, respectively. Fig. 8 illustrates the currents and the capacitor voltage obtained from the detailed circuit simulations, i_1, i_2, i_3 and v_c, and the average models, i_{1m}, i_{2m}, i_{3m} and v_{cm}, presented earlier in Section 4. The CFC is enabled at $t = 0.02$ s to balance the line currents. To evaluate the mode detection algorithm, a sudden load change is programmed to occur at $t = 0.035$ s where i_2 becomes the highest current instead of i_1 as indicated in Fig. 8*a*. The CFC succeeded to detect the mode change from mode 1 to mode 2 as displayed in Fig. 8*c*. As a result, the switching algorithm is automatically changed to

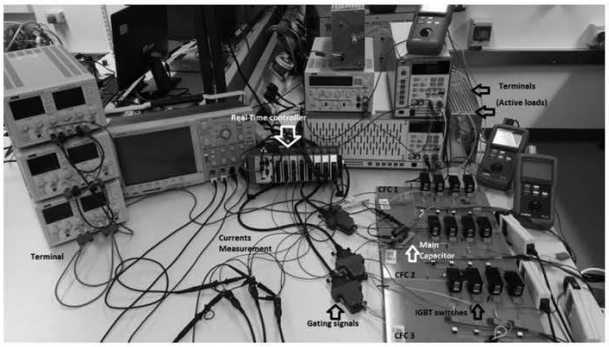


Fig. 9 *Experimental prototype setup*

maintain the currents balancing operation. Fig. 8*d* shows the series voltage introduced to each cable throughout the simulation process. Moreover, it can be noted that the traces obtained from the average model and the detailed circuit simulation are inline. Furthermore, the steady-state value of the capacitor voltage is calculated from (11) and it is coinciding with the result of Fig. 8*b*. In addition, the measured capacitor voltage ripple is very close to the value calculated from (13), 184 V. Therefore, the average model is validated.

7 Experimental validation

A low-power prototype of the CFC is implemented in the laboratory based on IGBT switches. The DC grid is built with one terminal DC supply and the rest of terminals are connected to active loads. National Instruments (NI) Compact Rio 9024 field programmable gate array real-time controller is used to realise the proposed control of the CFC, measuring the cable currents and outputting gating signals to the IGBTs. First, a two-port CFC is built which has been expanded to a three-port CFC. Fig. 9 displays the complete laboratory setup. The experimental system parameters are shown in Table 3.

Fig. 10*a* illustrates the balancing currents operation using two-port CFC prototype where initially i_1 is 2.3 A and i_2 is 1.1 A. The proposed control of the CFC succeeds to balance the two cable currents at about 1.75 A with very fast dynamic response. To examine the proposed mode change detection algorithm, currents are suddenly changed such that if the CFC is disabled, i_1 and i_2 become 1.1 and 1.9 A, respectively. The CFC succeeded in detecting the mode change and corrects the switching algorithm to maintain the currents balancing operation smoothly. The change of the capacitor voltage at moment of mode change is illustrated at the lower plot of Fig. 10*a*. Fig. 10*b* evaluates the dynamic performance of the proposed CFC where a sudden load change is applied and the mode is not changed as i_1 remains higher than i_2. It can be noted that the CFC keeps the balancing of the currents. Figs. 10*c* and *d* investigate the nulling operation of current i_1 from 1.2 A to zero and the corresponding capacitor voltage, respectively. Fast acting without overshoot dynamic performance of the proposed CFC is obvious from these results.

Table 3 Experimental prototype parameters

	Value
terminal 1	150 V DC power supply
terminal 2	prodigit 3261 300 V/18 A active load
terminal 3	prodigit 3251 150 V/8 A active load
cables resistance	1.2 Ω
CFC capacitor	4.7 mF
N-channel IGBT	HGTG10N60A4D – 70 A – 600 V
proportional gain	25
integral gain	0.01
controller time cycle	25 nS
maximum allowed switching frequency	2 kHz

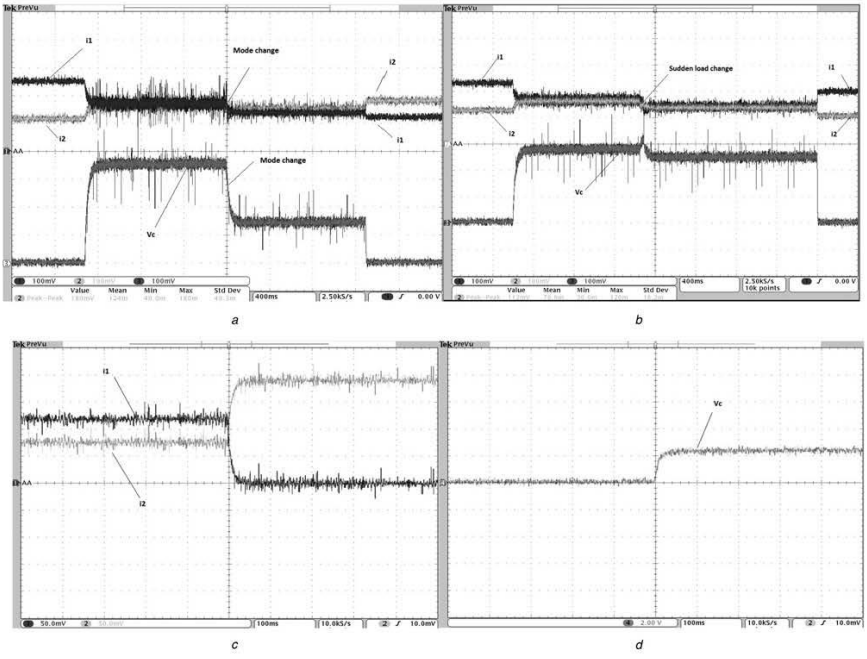


Fig. 10 *Experimental results from two-port CFC*

a Balancing currents i_1 and i_2 with sudden mode change. *X*-axis: 400 ms/Div and *Y*-axis: 1A/Div, 1 V/Div
b Balancing currents i1 and i2 with sudden load change. *X*-axis: 400 ms/Div and *Y*-axis: 1A/Div, 1 V/Div
c Current nulling. *X*-axis: 100 ms/Div and *Y*-axis 0.5A/Div at 70 V DC
d Capacitor voltage in case of current nulling. *X*-axis: 100 ms/Div and *Y*-axis: 2 V/Div

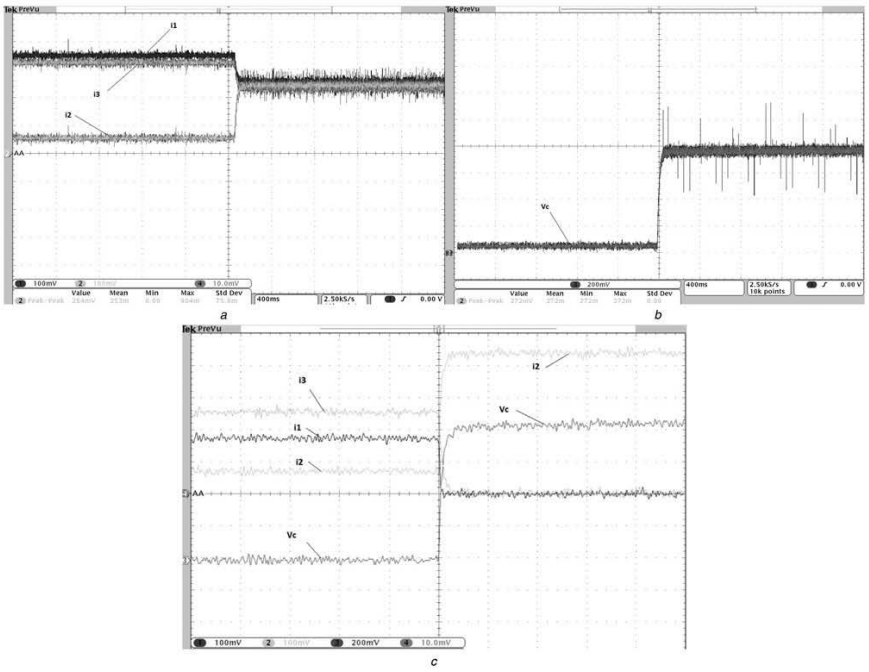


Fig. 11 *Experimental results*

a Balancing currents in three-port CFC. *X*-axis 400 ms/Div and *Y*-axis 1 A/Div
b Capacitor voltage of three-port CFC during balancing currents. *X*-axis 400 ms/Div and *Y*-axis 2 V/Div
c i_1 and i_3 currents nulling in three-port CFC. *X*-axis 40 ms/Div and *Y*-axis 1 A/Div, 2 V/Div

Furthermore, the experimental setup is expanded to three-port CFC by adding one more port with its corresponding load to act as a fourth terminal. Currents i_1, i_2 and i_3 are initially equal to 3.55, 0.5, and 3.1 A, respectively, as indicated in Fig. 11*a*. The proposed controller is set to redistribute the currents equally to ~2.4 A. The CFC capacitor is charged from cables 1 and 3 and discharged into cable 2. The relevant capacitor voltage is shown in Fig. 11*b*.

Moreover, Fig. 11*c* investigates a current nulling operation for i_1 and i_3, where it is ramped to zero. As a result, cable 2 carries the current of cables 1 and 3; therefore, i_2 is increased. This particular case is useful in cases of cable maintenance as it eases the isolation of any cable online, as explained previously. Similarly, the current can be set to any desired value as shown in Section 6. Fast response of the proposed three-port CFC is revealed from these results.

8 Conclusion

This paper presents the operation and control of an IGBT-based current flow controller. The proposed CFC can be utilised for the power flow control applications in DC grids including multi-terminal HVDC systems. A number of functionalities such as current balancing, current limiting and current nulling of the proposed three-port CFC are discussed and evaluated. Fast dynamic response and accurate performance of the proposed system are investigated using both computer software and experimental prototyping. Results show that the proposed CFC offers solutions for next generations DC grids power flow control problems.

9 Acknowledgments

The authors would like to thank Arab Academy for Science, Technology and Maritime Transport, Cairo, Egypt, and Staffordshire University, Staffordshire, UK, for funding Mr Hatem Yassin Diab PhD.

10 References

1 Toonen, H.M., Lindeboom, H.J.: 'Dark green electricity comes from the sea: capitalizing on ecological merits of offshore wind power?', *Renew. Sustain. Energy Rev.*, 2015, **42**, pp. 1023–1033
2 Yang, X., Bai, K.: 'Development and prospects of offshore wind power'. Proc. IEEE WNWEC, Nanjing, China, 2010, pp. 1–4
3 Higgins, P., Foley, A.: 'The evolution of offshore wind power in the United Kingdom', *Renew. Sustain. Energy Rev.*, 2014, **37**, pp. 599–612
4 Perveen, R., Kishor, N., Mohanty, S.R.: 'Off-shore wind farm development: present status and challenges', *Renew. Sustain. Energy Rev.*, 2014, **29**, pp. 780–792
5 Gordon, S.: 'Supergrid to the rescue', *Power Eng.*, 2006, **20**, (5), pp. 30–33
6 Hertem, D.V., Ghandhari, M.: 'Multi-terminal VSC HVDC for the European supergrid: obstacles', *Renew. Sustain. Energy Rev.*, 2010, **14**, (9), pp. 3156–3163
7 F.O.S.G work group: 'Roadmap to the supergrid technologies'. Available at http://www.friendsofthesupergrid.eu/wp-content/uploads/2014/06/WG2_Supergrid-Technological-Roadmap_20140622_final.pdf, accessed 1 January 2015

8 Vrana, T.K., Torres-Olguin, R.E., Liu, B., *et al.*: 'The north sea super grid-a technical perspective'. Ninth IET Int. Conf. AC and DC Power Transmission, London, UK, October 2010, pp 1–5
9 Decker, J.D., Woyte, A.: 'Review of the various proposals for the European offshore grid', *Renew. Energy*, 2013, **49**, pp. 58–62
10 Foerst, R., Heyner, G., Kanngiesser, K.W., *et al.*: 'Multiterminal operation of HVDC converter stations', *IEEE Trans. Power Appl. Syst.*, 1969, **88**, (7), pp. 1042–1052
11 Hertem, D.V., Ghandhari, M., Delimar, M.: 'Technical limitations towards a supergrid – a European prospective'. Proc. IEEE Int. Energy Conf. Exhibition, Manama, Bahrain, December 2010, pp. 302–309
12 Koldby, E., Hyttinen, M.: 'Challenges on the road to an offshore HVDC grid'. Nordic Wind Power Conf., Bornholm, Denmark, 2009, pp. 1–8
13 Shukla, A., Demetriades, G.D.: 'A survey on hybrid circuit-breaker topologies', *IEEE Trans. Power Deliv.*, 2015, **30**, (2), pp. 627–641
14 Barker, C.D., Whitehouse, R.S.: 'An alternative approach to HVDC grid protection'. Ninth IET Int. Conf. on AC and DC Power Transmission, Birmingham, UK, December 2012, pp. 1–6
15 Sneath, J., Rajapakse, A.D.: 'Fault detection and interruption in an earthed HVDC grid using ROCOV and hybrid DC breakers', *IEEE Trans. Power Deliv.*, 2014, **PP**, (99), pp. 1–8
16 Jovcic, D.: 'Bidirectional, high-power dc transformer', *IEEE Trans. Power Deliv.*, 2009, **24**, (4), pp. 2276–2283
17 Jovcic, D., Ooi, B.T.: 'Developing DC transmission networks using DC transformers', *IEEE Trans. Power Deliv.*, 2010, **25**, (4), pp. 2535–2543
18 Barker, C.D., Davidson, C.C., Trainer, D.R., *et al.*: 'Requirements of DC–DC converters to facilitate large DC grids'. Proc. CIGRE Symp., Paris, France, August 2012, pp. 1–10
19 Luth, T., Merlin, M.M.C., Green, T.C., *et al.*: 'High frequency operation of a DC/AC/DC system for HVDC applications', *IEEE Trans. Power Electron.*, 2014, **29**, (8), pp. 4107–4115
20 Carrizosa, M.J., Navas, F.D., Damm, G., *et al.*: 'Optimal power flow in multi-terminal HVDC grids with offshore wind farms and storage devices', *Int. J. Electr. Power Energy Syst.*, 2015, **65**, pp. 291–298
21 Rodrigues, S., Pinto, R.T., Bauer, P., *et al.*: 'Optimal power flow control of VSC-based multiterminal DC network for offshore wind integration in the north sea', *IEEE J. Emerg. Sel. Top. Power Electron.*, 2013, **1**, (4), pp. 260–268
22 Pinto, R.T., Rodrigues, S.F., Wiggelinkhuizen, E., *et al.*: 'Operation and power flow control of multi-terminal DC networks for grid integration of offshore wind farms using genetic algorithms', *Energies*, 2013, **6**, pp. 1–26
23 Haileselassie, T.M., Uhlen, K.: 'Impact of dc line voltage drops on power flow of MTDC using droop control', *IEEE Trans. Power Syst.*, 2012, **27**, (3), pp. 1441–1449
24 Wang, W., Barnes, M.: 'Power flow algorithms for multi-terminal VSCHVDC with droop control', *IEEE Trans. Power Syst.*, 2014, **29**, (4), pp. 1721–1730
25 Gavriluta, C., Candela, I., Luna, A., *et al.*: 'Hierarchical control of HV-MTDC systems with droop-based primary and OPF-based secondary', *IEEE Trans. Smart Grid*, 2015, **6**, (3), pp. 1502–1510
26 Dierckxsens, C., Srivastava, K., Reza, M., *et al.*: 'A distributed DC voltage control method for VSC MTDC system', *Electr. Power Syst. Res.*, 2012, **82**, (1), pp. 54–58
27 Rouzbehi, K., Miranian, A., Luna, A., *et al.*: 'DC voltage control and power sharing in multiterminal DC grids based on optimal DC power flow and voltage-droop strategy', *IEEE J. Emerg. Sel. Top. Power Electron.*, 2014, **2**, (4), pp. 1171–1180
28 Rouzbehi, K., Miranian, A., Candela, J.I., *et al.*: 'A generalized voltage droop strategy for control of multi-terminal DC grids', *IEEE Trans. Ind. Appl.*, 2014, **51**, (1), pp. 607–618
29 Jovcic, D., Hajian, M., Zhang, H., *et al.*: 'Power flow control in DC transmission grids using mechanical and semiconductor based DC/DC devices'. Tenth IET Int. Conf. AC DC Power Transmission, Birmingham, UK, 2012, pp. 1–6
30 Mu, Q., Liang, J., Yalou, L., *et al.*: 'Power flow control devices in DC grids'. IEEE Power and Energy Society General Meeting, San Diego, USA, 2012, pp. 1–7
31 Rouzbehi, K., Miranian, A., Candela, J.I., *et al.*: 'Proposals for flexible operation of multi-terminal DC grids: introducing flexible DC transmission system (FDCTS)'. IEEE Int. Conf. Renewable Energy Research and Applications, Milwaukee, USA, 2014, pp. 180–184
32 Veilleux, E., Ooi, B.: 'Multiterminal HVDC with thyristor power-flow controller', *IEEE Trans. Power Deliv.*, 2012, **27**, (3), pp. 1205–1212
33 Chen, W., Zhu, X., Yao, L., *et al.*: 'An interline DC power flow controller (IDCPFC) for multi-terminal HVDC system', *IEEE Trans. Power Deliv.*, 2015, **30**, (99), pp. 1–9
34 Balasubramaniam, S., Liang, J., Ugalde-Loo, C.E.: 'An IGBT based series power flow controller for multi-terminal HVDC transmission'. 49th IEEE Int. Universities Power Engineering Conf., Cluj-Napoca, Romania, 2014
35 Barker, C.D., Whitehouse, R.S.: 'A current flow controller for use in HVDC grids'. Tenth IET Int. Conf. on AC and DC Power Transmission, Birmingham, UK, 2012, pp. 1–6
36 Taranto, G.N., Pinto, L.M.V.G., Pereira, M.V.F.: 'Representation of FACTS devices in power system economic dispatch', *IEEE Trans. Power Syst.*, 1992, **7**, (2), pp. 572–576
37 Helbing, S.G., Karady, G.G.: 'Investigations of an advanced form of series compensation', *IEEE Trans. Power Deliv.*, 1994, **9**, (2), pp. 939–947
38 Vrana, T.K., Yang, Y., Jovcic, D., *et al.*: 'The CIGRE B4 DC grid test system'. CIGRE Electra Magazine, 2013

JPE 16-5-

http://dx.doi.org/10.6113/JPE.2016.16.5.????
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Reduced Switch Count Topology of Current Flow Control Apparatus for MTDC Grids

Hatem Yassin Diab†, Mostafa Ibrahim Marei*, and Sarath Tennakoon**

†Dept. of Electrical and Control Engineering, Arab Academy for Science, Technology and Maritime Transport (AASTMT), Cairo, Egypt
*Dept. of Electrical Power and Machines, Faculty of Engineering, Ain Shams University, Cairo, Egypt
**Faculty of Computing, Engineering and Sciences, Staffordshire University, Stoke on Trent, United Kingdom

Abstract

The increasing demand for high voltage DC grids resulting from the continuous installation of offshore wind farms in the North Sea has led to the concept of multi-terminal direct current (MTDC) grids, which face some challenges. Power (current) flow control is a challenge that must be addressed to realize a reliable operation of MTDC grids. This paper presents a reduced switch count topology of a current flow controller (CFC) for power flow and current limiting applications in MTDC grids. A simple control system based on hysteresis band current control is proposed for the CFC. The theory of operation and control of the CFC are demonstrated. The key features of the proposed controller, including cable current balancing, cable current limiting, and current nulling, are illustrated. An MTDC grid is simulated using MATLAB/SIMULINK software to evaluate the steady state and dynamic performance of the proposed CFC topology. Furthermore, a low power prototype is built for a CFC to experimentally validate its performance using rapid control prototyping. Simulation and experimental studies indicate the fast dynamic response and precise results of the proposed topology. Furthermore, the proposed controller offers a real solution for power flow challenges in MTDC grids.

Key words: Current control, CFC, DC grids, MTDC, power control, RCP

I. INTRODUCTION

Unlike in AC grids, power flow in any DC grid is determined mainly by grid cable resistances. A reliable and safe operation, in which cables are guaranteed to carry currents below their thermal limit even under sudden load changes, is difficult to achieve. Cables carrying currents over their limit for long periods may fail. Therefore, power (current) flow controllers are needed in DC grids. Currently, researchers and industry leaders are urged to focus on multi-terminal direct current (MTDC) grids as a solution to establish an interconnection among European grids [1]-[5]. Power flow control is one of the several major challenges that prevent the realization of MTDC grids [6], [7]. Other challenges include the absence of high voltage DC (HVDC) circuit breakers, protection schemes, and algorithms [8]-[10]; and HVDC DC to DC converters (DC transformers) [11]-[14]. The lack of practical, reliable and accurate current (power) flow control is a critical challenge for industry practitioners and researchers. Current approaches to achieving power flow control in MTDC are based on either modifying the control of the voltage source converters [15]-[24] or adding additional devices to the grid itself [25]-[30]. The insulated gate bipolar transistor (IGBT)-based current flow controller (CFC) concept presented in [29], [30] is adopted because it offers a promising solution to the power flow control problem. The present work presents a reduced switch count topology of the CFC to achieve accurate current flow control in MTDC grids with similar voltage stresses while cutting the cost and footprint in half. The CFC is connected in series to transmission cables to achieve functionalities such as balancing cable currents and current nulling in numerous cables and thereby ease the maintenance process. The main

Manuscript received Mar. 22, 2016; accepted Jun. 7, 2016
Recommended for publication by Associate Editor Liqiang Yuan.
†Corresponding Author: hatem.diab@research.staffs.ac.uk
Tel: +202-22685616, Fax: +202-22685892, AASTMT
*Department of Electrical Power and Machines Engineering, Ain Shams University, Egypt
**Faculty of Computing, Engineering and Sciences, Staffordshire University, United Kingdom

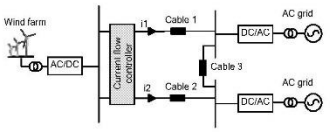


Fig. 1. A three terminal MTDC grid with CFC inserted in series.

advantage of the proposed CFC is its installation in series with the grid cables and isolation from the system ground (Fig. 1). Moreover, the voltage ratings of the capacitor and IGBT switches are relatively low in comparison with the grid voltage. This characteristic, in addition to the proposed reduced topology, leads to low manufacturing cost and footprint.

A simple control system based on the hysteresis band current control (HCC) technique is proposed for the CFC. HCC offers precise control and accurate results without the complexity of implementation or tuning. The complete operation and control of the proposed CFC are presented to balance the currents, set a current to a desired reference point, or null a current in a chosen cable. Simulation results illustrate the precise performance of the proposed CFC system. Moreover, experimental validation is carried out using advanced rapid control prototyping (RCP) by building a three-terminal DC grid with the CFC prototype to evaluate its functionality in different cases.

This paper is organized as follows. The theory of operation of the proposed reduced switch count topology for the CFC is discussed in Section II. The discussion includes possible operating modes with their switching states and mathematical modeling. The proposed control system is detailed in Section III. Computer simulations are carried out using the MATLAB/SIMULINK software package, and the results are demonstrated and analyzed in Section IV. The experimental validation of the proposed CFC system using the RCP technique is presented in Section V. Selected operating modes and functionalities are illustrated as well. Conclusions are provided in Section VI.

II. THEORY OF OPERATION

A. Operation of Current Flow Controller

The CFC consists of IGBT switches with parallel freewheeling diodes and capacitors, as shown in Fig. 2(a). Four IGBTs are inserted in series with each cable, and a capacitor is connected between both cables. The goal is to switch the capacitor in series such that it charges from the cable carrying a higher current and discharges from the other cable. This process can be controlled to achieve the desired operation, which could be balancing the currents in both cables, setting a current to a desired value, or nulling a current to zero. The speed and duration of switching the capacitor to charge/discharge from a cable depends on the set reference value, which is determined by the controller. Fig. 2(b) illustrates the proposed reduced switch count topology for the CFC, in which the numbers of switches and diodes are reduced by half. Two modes of operation are available for the CFC. In the first mode, i1 is the higher current, and Sa2 is switched on to allow current i2 to flow in cable 2 while connecting the capacitor in series to cable 1 to charge from it (Fig. 3(a)). This phase is followed by the switching on of Sb1 and Sb2 to allow the current i1 to flow in cable 1 and to connect the capacitor in series in cable 2 for discharging (Fig. 3(b)). In mode 2, when i2 is higher than i1, the operation is identical, except Sa1 is switched on instead of Sa2 (Figs. 4(a) (b)). The switching states of different IGBTs for the two modes of operation of the CFC are summarized in Table I.

B. Mathematical Modeling

To dynamically model a CFC using an averaging technique, we consider operation mode 1 illustrated in Fig. 3. As shown in this figure, i1 is higher than i2. The following equations describe the circuit of Fig. 3(a), in which the capacitor is charging from the line carrying the higher current, i1.

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + v_c + V_1 \quad (1)$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + V_2 \quad (2)$$

$$i_1 = C \frac{dv_c}{dt} \quad (3)$$

where r_1 and L_1 are the resistance and inductance of the first line, respectively; r_2 and L_2 are the resistance and inductance of the second line, respectively; v_c is the capacitor voltage; V is the voltage at the bus to which CFC is connected; and V_1 and V_2 are the voltages at the end terminals of the first and second lines, respectively. By defining $x^T = [i_1 \quad i_2 \quad v_c]$ as a state vector, where T refers to the transpose operation, equations (1), (2), and (3) can be arranged in a matrix form as

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & -1 \\ 0 & -r_2 & 0 \\ 1 & 0 & 0 \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B_1} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \quad (4)$$

Similarly, the state equations of Fig. 3(b), in which the capacitor is discharging into the line carrying the lower current i2, are written as follows:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 \\ 0 & -r_2 & 1 \\ 0 & -1 & 0 \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B_2} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \quad (5)$$

Assume that the duty ratio of the charging mode of the operation is D. Multiplying (4) and (5) by D and (1-D), respectively, and adding the results to obtain the average model for the CFC when i1 >i2 yields the following:

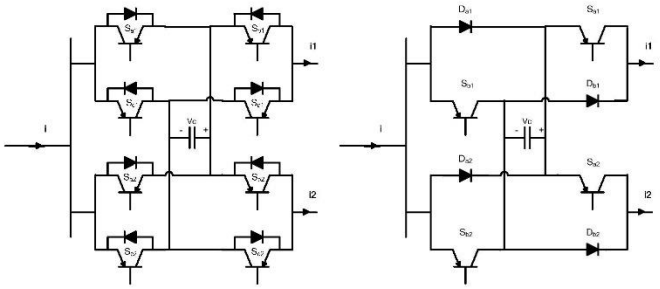


Fig. 2. (a) CFC circuit topology [29]–[30], (b) proposed CFC reduced circuit topology.

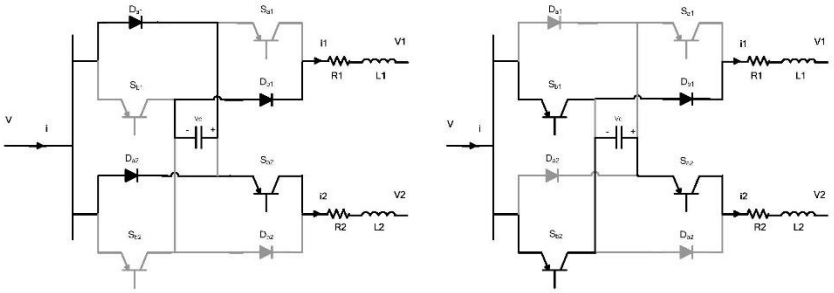


Fig. 3. (a) CFC operating in mode 1: charging from cable 1, (b) CFC discharging in cable 2.

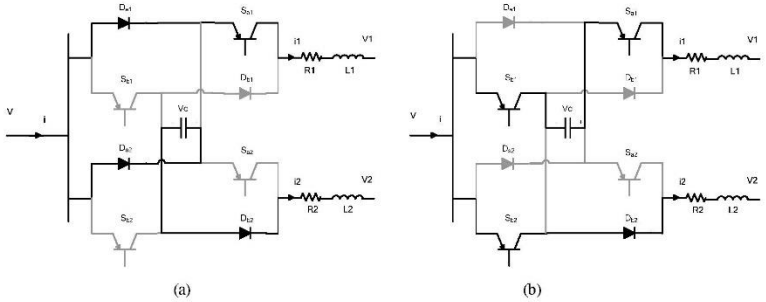


Fig. 4. (a) CFC operating in mode 2: charging from cable 2, (b) CFC discharging in cable 1.

TABLE I
SWITCHING STATES FOR CFC MODES OF OPERATION

Mode	Higher Current	Switching states			
		S_{a1}	S_{a2}	S_{b1}	S_{b2}
1	i_1	off	on	PWM	PWM
2	i_2	on	off	PWM	PWM

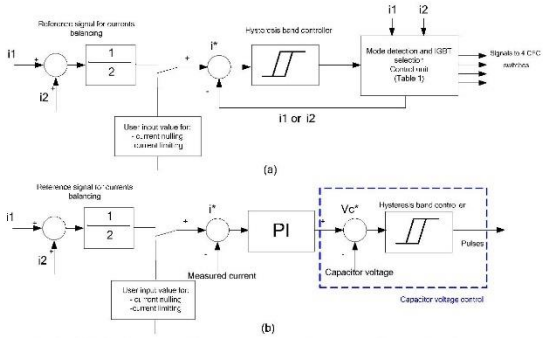


Fig. 5. (a) Proposed HCC control for the CFC, (b) proposed instantaneous voltage controller for CFC.

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & -D \\ 0 & -r_2 & 1-D \\ D & -1+D & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix}}_{U} \tag{6}$$

where A=DA1+(1-D)A2 and B=DB1+(1-D)B2. At steady state, (6) is written as

$$\begin{bmatrix} -r_1 & 0 & -1 \\ 0 & -r_2 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ V_c \end{bmatrix} + \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V \\ V_1 \\ V_2 \end{bmatrix} = 0 \tag{7}$$

Solving (9), the DC steady-state value of the capacitor voltage can be expressed as

$$V_c = \frac{\frac{r_2}{r_1} D(V-V_1)+(V_2-V)(1-D)}{\frac{r_2}{r_1} D^2+(1-D)^2} \tag{8}$$

Equation (8) expresses the capacitor voltage as a function of network parameters and voltage drops across the cables connected to the CFC; this function represents the loading condition of the grid. The rated voltage of the CFC switches, which is equal to the rated capacitor voltage, can be estimated from (8).

To calculate the capacitor voltage ripple, (3) is integrated over the charging period as follows:

$$\int_0^{DT} i_1 \, dt = C \int_{V_{cmin}}^{V_{cmax}} v_c \tag{9}$$

where T refers to the switching period, which is the reciprocal of the switching frequency fs. Disregarding the current ripples compared with the average value, I1, results in the linear charging of the capacitor from the initial minimum voltage Vcmin to the maximum voltage Vcmax. The capacitor voltage ripple ΔV_c can be estimated from (9).

$$\Delta V_c = V_{cmax} - V_{cmin} = \frac{D\, i_1}{C\, f_s} \tag{10}$$

Equation (10) shows that increasing the capacitance reduces the capacitor voltage ripple. Equation (7) shows that the parameters of the DC grid and loading condition influence

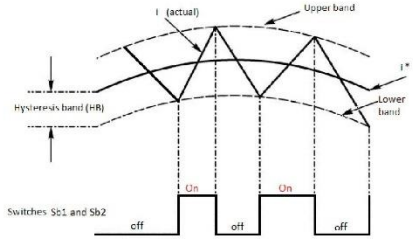


Fig. 6. Hysteresis band current control.

the line current, thus affecting the capacitor voltage ripple. The capacitor voltage ripple depends on the mode of operation as the charging current, which is I1 for mode 1, changes from mode 1 to mode 2. For mode 1, the capacitance can be roughly estimated from (8) and (10) to meet a required percentage voltage ripple, $\Delta V_{c\,pu} = \Delta V_c / V_c$, at the extreme deviations of the line currents. Similarly, the capacitance can be calculated for each mode of operation of the CFC. Finally, maximum capacitance is considered to meet the desired voltage ripple for all modes of operation. In the present study, the capacitance of the CFC is selected using trial and error, and, as implied by (10), higher capacitors produce smoother CFC performance and lower operating switching frequency.

III. Proposed Control of CFC Switches

Fig. 5(a) illustrates the proposed control system. It is based on the HCC technique to derive the PWM switches of the proposed CFC. In case of current balancing, the average value of both currents is calculated, and the result is set as a reference value for the controller, i*. The calculated reference value is compared with the measured actual value of the current that must be decreased, i1 or i2, which is set by the selection control unit. The error signal is considered as the

TABLE II
SIMULATION PARAMETERS

Parameter	Value
Grid voltage rating	320 kV
Capacitor 1	1 mF
Cable 1	1.5 Ω
	0.8 mH
Cable 2	2.35 Ω
	1.1 mH
Cable 3	2.42 Ω
	1.1 mH
Hysteresis band	5 A

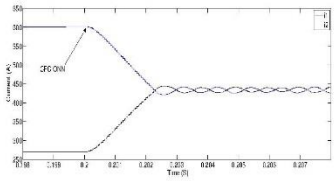


Fig. 7. Balancing currents i1 and i2 (mode 1).

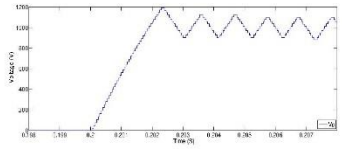


Fig. 8. CFC capacitor voltage.

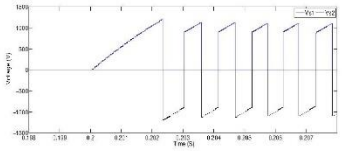


Fig. 9. Series voltages introduced by the CFC to both cables.

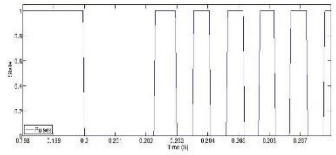


Fig. 10. HCC generated pulses.

input of the HCC (Fig. 5(a)). The on/off states determined by the HCC are assigned to the switches chosen by the IGBT selection control unit on the basis of the detected mode of operation (Table I). The HCC initially deactivates switches Sa to charge the capacitor from the cable carrying the highest current. When the actual current exceeds the reference current with the predefined hysteresis band (HB), the HCC activates switches Sa to disconnect the capacitor and allow it to discharge in the other cable. As a result, the actual current falls below the reference current based on the HB. The process is then repeated. Fig. 5(b) shows another control circuit that enables the application of capacitor voltage regulation. The error signal is passed through a proportional integral (PI) controller, and its output is considered as the reference capacitor voltage Vc*, which is compared with the measured value and passed through an HB controller that produces the switching signals. This step is important in cases in which capacitor voltage must be limited to ensure that it does not exceed its rated value during operation. The principle of HCC is also illustrated in Fig. 6, which shows that the effects of varying the width of the HB on the switching frequency are noticeable. Switching frequency and accuracy depend mainly on the set value of the HB. The HB is inversely proportional to the switching frequency and accuracy. HCC offers many advantages, such as simplicity and ease of implementation. Moreover, its tuning and parameter settings are not as complicated as those of PI controllers. Similarly, external reference values can be applied directly to the proposed control system for current nulling and current setting. These two functions are useful in cases in which the current in the cable must be limited to a desired value or lowered to zero to disconnect the cable and facilitate maintenance.

IV. SIMULATION RESULTS

A simulation is carried out using the MATLAB/SIMULINK software package, and the results are presented in this section. An MTDC grid, similar to that in Fig. 1, is simulated to evaluate the dynamic and steady-state performance of the proposed control system of the CFC. The main simulation parameters are shown in Table II. As shown in this table, cables 1 and 2 carry currents i1 and i2, respectively. Two case studies are presented to evaluate the different features and operation modes of the proposed CFC.

A. *Case 1: Balancing i1 and i2*

This case study demonstrates a current balancing operation using the proposed CFC. Currents i1 and i2 are initially 0.6 and 0.27 kA, respectively. The CFC is set to operate at t = 0.2 s to charge the capacitor from cable 1 and discharge it in cable 2 to achieve the balanced operation. Currents i1 and i2 reach an average of 0.43 kA (Fig. 7), which indicates a fast performance without any overshoot. The capacitor voltage Vc and series voltages Vs introduced by the CFC to both cables are shown in Figs. 8 and 9, respectively. Fig. 9 shows that both series voltages Vs1 and Vs2 are equal but opposite in terms of direction as the capacitor charges from cable 1 and starts immediately discharging in cable 2. The gating signals generated by the HCC are presented in Fig. 10. As shown in

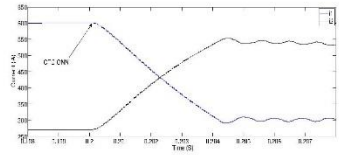


Fig. 11. Setting current i1 to 300 A.

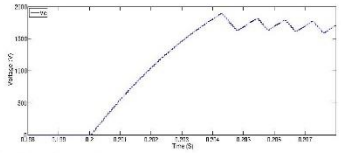


Fig. 12. Capacitor voltage.

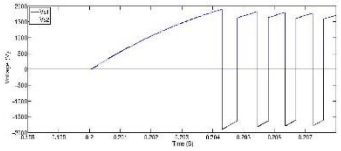


Fig. 13. Series voltages introduced by the CFC to both cables.

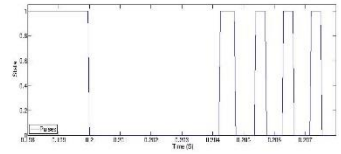


Fig. 14. HCC output pulses.

this figure, HCC produces an off gating signal from t = 0.2 s until the current i1 reaches the lower HB at t = 0.202 s. The results demonstrate one of the advantages of the CFC, that is, the capacitor and switches are subjected to an extremely small voltage (approximately 1 kV) relative to the grid voltage of 320 kV. The result is a low production cost and footprint for the CFC.

B. Case 2: Setting i1 to 0.3 kA

This case study limits the current i1 to 0.3 kA. As explained earlier, the user defines the reference value, which is 0.3 kA, and a similar control process is conducted. Currents i1 and i2 are shown in Fig. 11. The proposed control system of the CFC successfully performs the task, and current i1 is limited. Current i2 is increased to balance the sudden decrease in i1. The capacitor voltage and series cable voltages are shown in Figs. 12 and 13, respectively. The capacitor and series voltages are higher than those in case 1, as the capacitor must charge more in case 2 to achieve the reference

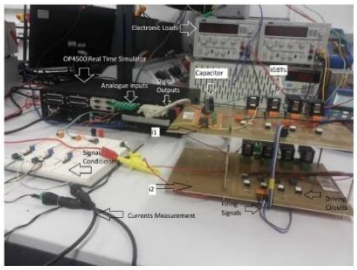


Fig. 15. Experimental RCP setup of the CFC.

TABLE III
EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	Value
Terminal 1	150 V DC power supply
Terminal 2	Electronic load
Terminal 3	Electronic load
Capacitor 1	1 mF
N-channel IGBT	70 A–600 V
Hysteresis band	5 mA

point. The capacitor and series voltage are approximately 2 kV, which is relatively low. Fig. 14 presents the gating signals produced by HCC in this case.

V. EXPERIMENTAL VALIDATION

A low power prototype of the CFC is built in the laboratory using low rating IGBT switches (Fig. 15). A three-terminal DC grid is constructed, with one terminal supplying DC and the other two connected to electronic (active) loads. The RCP technique is implemented using an OPAL RT OP4500 real-time simulator to control the CFC circuits in real time with the proposed control system. All cable currents are measured and connected as inputs to the OP4500 that outputs all gating signals to the CFC IGBT switches. The experimental prototype system parameters are shown in Table III.

A. Case 1: Balancing i1 and i2

To validate case 1, as explained earlier in the simulation results section, we present a similar case, in which i1 and i2 are balanced from the initial values of 1.8 and 1 A, respectively. The HB is set to 50 mA to demonstrate the operation of HCC (Fig. 6). The results in this case are shown in Fig. 16, which shows a clear gap between currents i1 and i2 after the balancing as they are oscillating around the average value 1.4 A as a result of the high HB set. This HB is then decreased to 5 mA in Fig. 17, which shows that the accuracy increases, and the switching frequency of the pulses increase significantly from 0.5 kHz to 4 kHz. The capacitor voltage Vc is also shown in both figures. Decreasing the HB

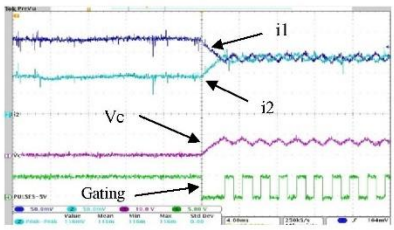


Fig. 16. Balancing i1 and i2 with HB=50 mA. X axis: 4 ms/Div and Y axis: 0.5 A/Div, 10 V/Div, 5 V/Div.

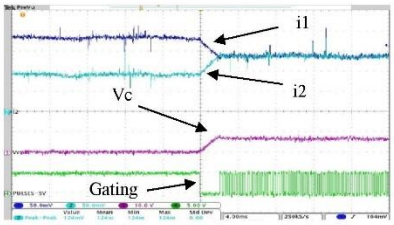


Fig. 17. Balancing i1 and i2 with HB = 5 mA. X axis: 4 ms/div and Y axis: 0.5 A/div, 10 V/div, 5 V/div.

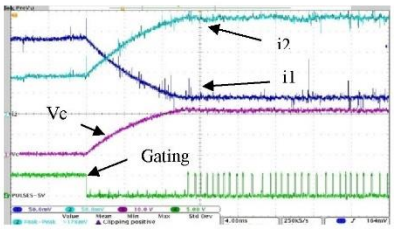


Fig. 18. Setting i1 to 400 mA. X axis: 4 ms/div and Y axis: 0.5 A/div, 10 V/div, 5 V/div.

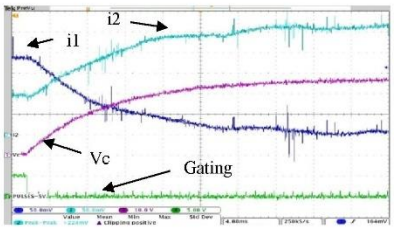


Fig. 19. Nulling current i1. X axis: 4 ms/div. and Y axis: 0.5 A/div, 10 V/div, 5 V/div.

results in a smooth balancing of the currents, but a higher switching frequency is incurred.

B. Case 2: Setting i1 to 0.4 and 0 A

The reference value is set to 0.4 A to validate the results obtained from case 2 of the simulation. i1 is successfully limited to 0.4 A, and i2 increases significantly to cover the decrease in i1 (Fig. 18). The capacitor voltage Vc is higher than that in case 1, as i1 decreases at a higher amount, in which case the capacitor has to charge more. The gating signals in this case are shown in Fig. 18. Another option is to set the reference value to zero to null the current flowing in the cable. The results of this case are shown in Fig 19, in which the capacitor is fully charged to block the current i1 and the gating signal is equal to zero to keep the capacitor connected. The success of the experimental operation demonstrates the validity of the proposed CFC and control strategy.

VI. DISCUSSION

The simulated and experimental results validate the proposed topology and control strategy. They also show that reducing the HB results in increased switching frequency. A common practice is to set the HB in the range of 3% to 5% of the current magnitude. The performance improves as the ripples decrease; however, the switching losses increase, as expected for any power electronics converter. Hence, a CFC capacitor with high capacitance should be chosen because its application ensures a smooth operation with low voltage and current ripples while minimizing switching frequency and losses.

VII. CONCLUSIONS

This paper presents a reduced switch count topology for a CFC to achieve current limiting applications in DC grids, including multi-terminal HVDC systems. A simple control system based on the HCC technique is proposed for the CFC. The detailed operating modes and mathematical modeling are illustrated. Functionalities such as current balancing, current limiting, and current nulling of the proposed HCC-based CFC are discussed and evaluated accordingly. The fast dynamic response and accurate performance of the proposed system are investigated using computer software and experimental validation. As indicated in the results, the proposed CFC incurs low costs and a small footprint and thus serves as a promising solution for power flow control problems in next-generation DC grids.

ACKNOWLEDGMENT

The authors would like to thank the Arab Academy for Science, Technology and Maritime Transport, Cairo, Egypt; and the Staffordshire University, Staffordshire, UK, for funding Mr. Hatem Yassin Diab's PhD research project.

REFERENCES

[1] D. Ebehard and E. Voges, "Digital single sideband detection for S. Gordon, "Supergrid to the rescue," *Power Engineer*, Vol. 20, No. 5, pp. 30-33, Oct. 2006.

[2] D. V. Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," *Renewable and Sustainable Energy Reviews*, Vol. 14, No. 9, pp. 3156-3163, Dec. 2010.

[3] F. O. S. G work group.: 'Roadmap to the supergrid technologies', http://www.friendsofthesupergrid.eu/wp-content/uploads/2014/06/WG2_Supergrid-Technological-Roadmap_20140622_final.pdf, accessed 1 Jun. 2016.

[4] T. K. Vrana, R. E. Torres-Olguin, B. Liu, and T. M. Haileselassie, "The north sea super grid-a technical perspective," in *AC and DC Power Trans., (ABCD 2010), 9th IET International Conference on*, pp. 1-5, 2010.

[5] J. De Decker and A. Woyte. "Review of the various proposals for the European offshore grid," *Renewable Energy*, Vol. 49, pp. 58-62, Jan. 2013.

[6] D. V. Hertem, M. Ghandhari, and M. Delimar, "Technical limitations towards a SuperGrid – A European prospective," In *Energy Conference and Exhibition (EnergyCon), 2010 IEEE International*, pp. 302-309, 2010.

[7] E. Koldby and M. Hyttinen, "Challenges on the road to an offshore HVDC grid," in *Nordic Wind Power Conference*, pp. 1-8, 2009.

[8] A. Shukla and G. D. Demetriades, "A Survey on hybrid circuit-breaker topologies," *IEEE Trans. Power Del., Vol.* 30, No. 2, pp. 627-641, Apr. 2015.

[9] C. D Barker and R. S. Whitehouse, "An alternative approach to HVDC grid protection," in *AC and DC Power Trans. (ACDC 2012), 10th IET International Conference on*, pp. 1-6, 2012.

[10] J. Sneath and A. D. Rajapakse, "Fault detection and interruption in an earthed hvdc grid using rocov and hybrid dc breakers," *IEEE Trans. Power Del.*, Vol. 31, No. 3, pp. 1-8, Jun. 2014.

[11] D. Jovcic, "Bidirectional, high-power DC transformer," *IEEE Transactions Power Delivery*, Vol. 24, No. 4, pp. 2276-2283, Oct. 2009.

[12] D. Jovcic and B. T. Ooi. "Developing DC transmission networks using DC transformers," *IEEE Trans. Power Del.*, Vol. 25, No. 4, pp. 2535-2543, Oct. 2010.

[13] C. D. Barker, C. C. Davidson, and D. R. Trainer, and R. S. Whitehouse, "Requirements of DC-DC Converters to facilitate large DC Grids," *Cigre Session 2012*, pp. 1-10, 2012.

[14] T. Luth, M. Merlin and T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a DC/AC/DC system for HVDC applications," *IEEE Transactions Power Electronics*, Vol. 29, No. 8, pp. 4107-4115, Aug. 2014.

[15] M. J. Carrizosa, F. D. Navas and G. Damm, and F. Lamnabhi-Lagarrigue, "Optimal power flow in multi-terminal HVDC grids with offshore wind farms and storage devices," *International Journal of Electrical Power & Energy Systems*, Vol. 65, pp. 291-298, Feb. 2015.

[16] S. Rodrigues, R. T. Pinto and P. Bauer, et al. "Optimal power flow control of VSC-based multiterminal DC network for offshore wind integration in the north sea," *IEEE J. Emerg. Sel. Topics Power Electron.*, Vol. 1, No. 4, pp. 260-268, Dec. 2013.

[17] K. Rouzbehi, A. Miranian and A. Luna, and P. Rodrigues, "DC voltage control and power sharing in multiterminal DC grids based on optimal DC power flow and voltage-droop strategy," *IEEE J. Emerg. Sel. Topics Power Electron.*, Vol. 2, No. 4, pp. 1171-1180, Dec. 2014.

[18] R. T. Pinto, S. F. Rodrigues and, E. Wiggelinkhuizen, R. Scherrer, P. Bauer, and J. Pierik, "Operation and power flow control of multi-terminal DC networks for grid integration of offshore wind farms using genetic algorithms," *Energies*, Vol. 6, No. 1, pp. 1-26, Dec. 2012.

[19] T. M. Haileselassie and K. Uhlen, "Impact of DC line voltage drops on power flow of MTDC using droop control," *IEEE Trans. Power Syst.*, Vol. 27, No. 3, pp. 1441-1449, Aug. 2012.

[20] W. Wang and M. Barnes, "Power flow algorithms for multi-terminal VSC-HVDC with droop control," *IEEE Trans. Power Syst.*, Vol. 29, No. 4, pp. 1721-1730, Jul. 2014.

[21] C. Gavriluta, I. Candela, A. Luna, A. Gomez-Exposito, and P. Rodriguez, "Hierarchical control of HV-MTDC systems with droop-based primary and OPF-based secondary," *IEEE Trans. Smart Grid*, Vol. 6, No. 3, pp. 1502-1510, May 2015.

[22] C. Dierckxsens, K. Srivastava, M. Reza and S. Cole, J. Beertena, and R. Belmansa, "A distributed DC voltage control method for VSC MTDC systems," *Electric Power Systems Research*, Vol. 82, No. 1, pp. 54-58, Jan. 2012.

[23] K. Rouzbehi, A. Miranian, A. Luna, and P. Rodriguez, "DC voltage control and power sharing in multiterminal DC grids based on optimal DC power flow and voltage-droop strategy," *IEEE J. Emerg. Sel. Topics Power Electron.*, Vol. 2, No. 4, pp. 1171-1180, Dec. 2014.

[24] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, P. Rodriguez, "A generalized voltage droop strategy for control of multiterminal DC grids," *IEEE Trans. Ind. Appl.*, Vol. 51, No. 1, pp. 607-618, Jan. 2015.

[25] Q. Mu, J. Liang, Y. Li, and X. Zhou, "Power flow control devices in DC grids," *Power and Energy Society General Meeting, 2012 IEEE*. 2012.

[26] E. Veilleux and B. T. Ooi, "Multiterminal HVDC with thyristor power-flow controller," *IEEE Trans. Power Del.*, Vol. 27, No. 3, pp. 1205-1212, Jul. 2013.

[27] S. Balasubramaniam, J. Liang and C. E. Ugalde-Loo, "An IGBT based series power flow controller for multi-terminal HVDC transmission," *Power Engineering Conference (UPEC), 2014 49th International Universities*, 2014.

[28] T. Zhang, L. Chuanyue, and J. Liang, "A thyristor based series power flow control device for multi-terminal HVDC transmission," *Power Engineering Conference (UPEC), 2014 49th International Universities*, 2014.

[29] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in HVDC grids," *AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on.*, 2012.

[30] F. Hassan, R. King and R. Whitehouse, and C. Barker, "Double modulation control (DMC) for dual full bridge current flow controller (2FB-CFC)," *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, 2015.

Hatem Yassin Diab received his B.Sc. (Hons.) and M.Sc. degrees from the Arab Academy for Science and Technology, Cairo, Egypt, in 2009 and 2012, respectively. He is currently working on his Ph.D. degree at Staffordshire University, Stoke-on-Trent, U.K. From 2009 to 2013,

he worked as an Assistant Lecturer in the Department of Electrical and Control Engineering, College of Engineering and Technology, Arab Academy for Science and Technology, Cairo, Egypt. His research interests include power systems, control systems, automation, renewable energy technologies, HVDC, DC grids and application of power electronics in power systems.

Mostafa Ibrahim Marei received his B.Sc. (Hons.) and M.Sc. degrees in Electrical Engineering from Ain Shams University, Cairo, Egypt, in 1997 and 2000, respectively, and his Ph.D. degree in Electrical Engineering from the University of Waterloo, Waterloo, ON, Canada, in 2004. From 2004 to 2006, he was a Postdoctoral Fellow with the University of Waterloo. Currently, he is an Associate Professor with the Department of Electrical Power and Machines, Ain Shams University. His research interests include power electronics, distributed and renewable generation, microgrids, power quality, custom power, electrical drives, and artificial intelligent applications in power systems. Dr. Marei holds the State Incentive Award in Engineering Sciences, Academy of Scientific Research and Technology, Egypt. His biography is listed in Marquis Who's Who in the World.

Sarath B. Tennakoon received his B.Sc. degree in Electrical Engineering from the University of Moratuwa, Moratuwa, Sri Lanka; his M.Sc. degree in Electrical Engineering from the University of Aston, Birmingham, U.K.; and his Ph.D. degree in Electrical Engineering and Electronics from the University of Central Lancashire, Lancashire, U.K. He is a Professor of power electronic systems and the Director of the Centre for Energy Efficient Systems, Staffordshire University, Stoke-on-Trent, U.K. His research interests include DC grids and HVDC, power system protection, and power electronics and harmonics.

A Generalized Topology of a Modular Current Flow Controlling Device for Multi-terminal DC Grid Applications

Abstract—The recent increase in installations of offshore windfarms in the North Sea area produced the idea of forming Multi-Terminal Direct Current (MTDC) grids. Power flow control is one of few challenges that need to be solved to allow reliable operation of the MTDC grids. This paper presents a generalized topology of an IGBT based modular current flow controlling device (MCFC), that can be utilized in MTDC power flow and current limiting applications. The proposed topology allows practical implementation of CFC where it can be connected to several cables at each given terminal. Theory of operation, key features, modelling, and control of the proposed MCFC are demonstrated. The different functionalities of the proposed controller including the balancing, limiting, and nulling of cable currents are illustrated. A three-port MCFC is simulated using PSCAD/EMTDC software to assess its dynamic performance. Moreover, a low power prototype is built for a three-port MCFC to experimentally validate its operations at different modes using Rapid Control Prototyping technique (RCP). Fast dynamic response and accurate performance are revealed from simulation and experimental results. Furthermore, the promising features of the proposed MCFC render it able to play an important role in power flow control of MTDC grids.

Index Terms—Current limiting, HVDC, MTDC, Power converters, Power flow control.

I. Introduction

Multi Terminal Direct Current (MTDC) grids are considered by researchers and industry to be the future solution for interconnecting offshore wind farms to one or more onshore points. As more offshore wind farms are being installed in the North Sea area by surrounding countries in the recent few years [1], the MTDC concept may play an important role in interconnecting the wind farms owned by European countries has emerged as well [2]-[3]. The concept of forming a MTDC grid has been highlighted since the early use of High-Voltage Direct Current (HVDC) transmission systems [4], but it was not possible to develop this idea into practice until the recent emergence of high Voltage Source Converters (VSCs) which have more flexibility when it comes to inverting the power direction. Major challenges preventing realization of MTDC grids are investigated by researchers and industry such as the absence of HVDC circuit breakers, protection schemes and algorithms [5]-[7], and high voltage dc to dc converters (dc transformers) [8]-[9]. The lack of practical, reliable and accurate current (power) flow control method is considered one of the critical challenges, as the power flow through the grid conductors is generally determined by the conductor's impedances leading to overloading in some of the conductors thus exceeding their thermal ratings. Efforts are done to achieve the dc power flow control via controlling the converter connected at different terminals of the MTDC grid [10]-[13]. several methods are proposed in literature to achieve current flow control in dc grids. The first method is based on inserting a voltage source in series with the line using three-phase converter coupled with a transformer [14], [15], while the second method proposed using dc transformers [16], [17]. The main disadvantage of these methods is the high cost and large size of the transformer [15]. The use of dc/dc converters have been also proposed [18]-[20] but still the utilization of series inductor with kA rated grid currents and high voltage switches increase the cost and complexity [18], [20]. Moreover, a single dc/dc converter is needed to control the current in each cable at a given node, making it a hard solution for offshore wind generation where platforms sizes should be minimal.

To overcome this problem, an apparatus called Current Flow Controller (CFC) is proposed in [15], [21], [22]. However, the available CFC topology is based on one capacitor which limits its application to control the current flow between two cables at any given time, and there is no information available on how this topology can be expanded. For realistic integration with MTDC grids, which may require the ability of controlling the currents at several cables simultaneously, the CFC topology must be modified to offer independent current flow paths between the cables.

This paper presents generalized topology for a Modular Current Flow Controller (MCFC) based on Insulated Gate Bipolar Transistor (IGBT) for precise current flow control in MTDC grids. The proposed MCFC consists of a number of Sub-Modules (SM) and capacitors that can be connected to any number of cables to achieve different functionalities such as balancing cable currents, limiting currents and currents nulling in a number of cables to ease the maintenance process. The main advantage of the MCFC is that it is installed in series with the cables of the dc grid and isolated from the system ground, as shown in Fig. 1. This action results in reducing the voltage rating of the IGBT switches to a small fraction of the grid voltage leading to low cost and small footprint in comparison with series dc/dc converters needed to perform similar action, and giving MCFC superiority when it comes to offshore platforms installations. Furthermore, MCFC is able to redistribute high currents that may result from cable disconnection during faults, preventing cables overloading.

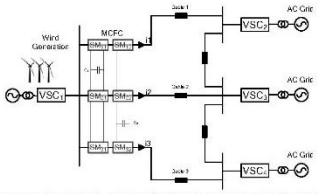


Fig. 1. A 4 terminals DC grid with 6 sub modules MCFC inserted in series.

The circuit topology of the proposed MCFC is determined by the number of cables that it is connected to. Complete analysis, operation and control of a three-port MCFC is presented in this paper to balance the three currents, set a current to desired reference point or even null a current in any chosen cable. The new generalized topology sets basis for designing MCFC to control the current flow in any number of cables and offers additional degrees of control when compared to the available topology in [21] which uses single capacitor, where functions such as nulling current in one cable and balancing the two remaining currents can be now carried out with the MCFC. Simulation results demonstrate the accurate dynamic performance of the proposed MCFC. Furthermore, experimental validation is carried out using the Rapid Control Prototyping (RCP) advanced technique by building a four terminals dc grid with a three-port MCFC prototype to test different cases.

This paper is organized as follows: In section II, generalized MCFC topology and principle of operation are introduced. The detailed explanations of operating modes of three- port MCFC, mathematical modelling and the proposed control strategy for the MCFC are presented in section III. Computer simulation is carried out using PSCAD/EMTDC software package and results are discussed in section IV. In section V, experimental validation is presented using the RCP technique and different operating modes are tested. Finally, section VI concludes the paper.

II. THE PROPOSED GENERALIZED CURRENT FLOW CONTROLLER

The proposed modular topology consists of IGBT switches integrated with parallel freewheeling diodes and capacitors. The building block of the MCFC is a sub-module containing four IGBT switches as shown in Fig. 2. The number of cables (ports) connected to the MCFC determines its topology as shown in Fig. 3 for two, three, four, and n ports. The number of sub-modules required can be calculated from the following equation:

$$n_s = n(n-1) \tag{1}$$

where n_s is the total number of submodules and n is the number of cables to be controlled by the MCFC. In addition, the number of the involved capacitors can be obtained from:

$$n_c = (n-1) \tag{2}$$

The principle of operation of the MCFC is based on switching capacitors in series with cables carrying higher currents, one capacitor to one cable. This action allows each capacitor to charge independently from its connected cable and hence reducing the current flow.

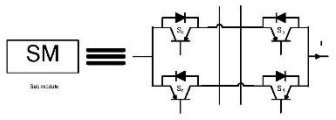


Fig. 2. Building block of the MCFC

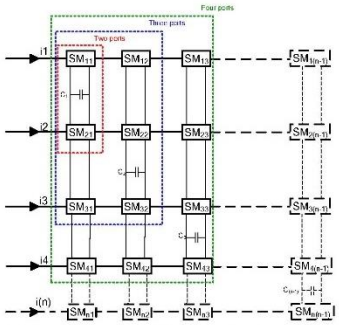


Fig. 3. Proposed Generalized MCFC topology for n cables.

For each capacitor, this period is followed by a discharging period, where the capacitor is switched to a low current carrying cable with reversed polarity. As a result, a series voltage is inserted with the low current carrying cable allowing it's current to increase. Consequently, the proposed MCFC controls the current flow in the MTDC grid. The duration of the charging/discharging periods are determined by the control algorithm based on the requested set point. The MCFC is able to operate independently from the VSCs control modes as its control unit depends mainly on the cable currents, giving it another advantage as no communication is needed even when more than MCFC is installed in a complex MTDC grid. In the following section the operation, dynamic modelling and control strategy of the MCFC are discussed in details.

III. THREE-PORTS MCFC

A. Modes of operation

As discussed earlier, the MCFC operates to decrease desired currents by switching the capacitor(s) in series with the cables carrying high currents to charge them, and then switched to cables carrying lower currents to discharge into. This action indicates that for every MCFC topology different modes of operation may appear. Three-ports MCFC, with six submodules (24 switches) and two capacitors is chosen to explain different

possible modes of operation and demonstrate the MCFC capabilities. Fig. 4 illustrates the three-port MCFC circuit topology operating in mode 1, where currents flowing in cables one and two are assumed higher than the average value of the three line currents, *i1*, *i2*, and *i3*. It is required to decrease the highest currents to achieve different functionalities such as balancing them with i3, setting them to any desired value or even nulling them. In this mode, switches S_{b12}, S_{b21}, S_{b31}, and S_{b32} are switched-on to allow capacitor C_1 to charge from cable 1 and capacitor C_2 to charge from cable 2, as shown in Fig. 4, leading to decrease their currents. Two different PWM signals, P_1 and P_2, are delivered to switches S_{c11}, S_{c22}, S_{c31} and S_{c32} to allow both capacitors to discharge in cable 3 (see Fig. 5). Similarly, the switching states for modes 2 and 3 can be derived as shown in Table 1.

Another scenario, where only one of the three line currents is higher than the average value and needs to be decreased, which gives three modes of operation, modes 4 to 6, in the forward (positive) direction as indicated in Table 1. In the cases where currents flowing in the reverse (negative) direction, modes 7 to 12, the MCFC operates in a similar way but using switches S_a and S_d instead of S_c and S_b, respectively. All the possible modes along with their corresponding state of each of the 24 switches are presented in Table 1. The proposed control of the MCFC that generates the PWM signals is discussed in details in sub-section C.

B. Dynamic Modelling

In this subsection, the averaging technique is used to derive a dynamic model for the three-port MCFC. Considering mode 1 of operation, $i_1 > i_2$ and both currents are greater than the average current flowing in the three cables. The proposed MCFC transfer currents from cable 1 and cable 2 through C1 and C2, respectively, to cable 3. The MCFC charges C1 from cable 1 for a time interval of D_1T, while it charges C2 from cable 2 for a time interval of D_2T, where D_1 and D_2 are duty ratios for charging periods of C1 and C2, respectively, and T is the switching period. Since i_1 is considered greater than i_2, consequently, D_1 becomes greater than D_2. Therefore, the operation of the proposed MCFC in mode 1 can be divided into three consecutive intervals of periods D_2T, $(D_1\text{-}D_2)T$, and $(1\text{-}D_1)T$. Fig. 4(a) presents the operating devices of the MCFC during the first interval where both C1 and C2 are charging from cable 1 and cable 2, respectively. The circuit equations that describe the MCFC during this interval, D_2T, can be written as:

$$V = r_1 i_1 + L_1 \frac{di_1}{dt} + v_{c1} + V_1 \quad (3)$$

$$V = r_2 i_2 + L_2 \frac{di_2}{dt} + v_{c2} + V_2 \quad (4)$$

$$V = r_3 i_3 + L_3 \frac{di_3}{dt} + V_3 \quad (5)$$

$$i_1 = C \frac{dv_{c1}}{dt} \quad (6)$$

$$i_2 = C \frac{dv_{c2}}{dt} \quad (7)$$

where r_1 and L_1 are the resistance and the inductance of the first line, r_2 and L_2 are the resistance and the inductance of the second line, r_3 and L_3 are the resistance and the inductance of the third line, v_{c1} and v_{c2} are the capacitors voltages of the three-port MCFC capacitors, V is the bus voltage where the MCFC is connected, V_1, V_2 and V_3 are the voltages at the end terminals of the first, second, and third lines, respectively. The state-space model representation of (3)-(7) is given by:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -1 & 0 \\ 0 & -r_2 & 0 & 0 & -1 \\ 0 & 0 & -r_3 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \quad (8)$$

In the second interval, C_2 is switched to discharge in cable 3 while C_1 remains charging from cable 1. The duration of this interval is $(D_1\text{-}D_2)T$. In a similar way, the state equations representing the second interval are written as follows:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -1 & 0 \\ 0 & -r_2 & 0 & 0 & 0 \\ 0 & 0 & -r_3 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \quad (9)$$

During the third interval, $(1\text{-}D_1)T$, C1 is switched to cable 3. Hence, both C1 and C2 are discharging into cable 3, as indicated in Fig. 4(b). The mathematical representation of the MCFC during this interval is given by:

$$\underbrace{\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}}_{K} \underbrace{\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & 0 & 0 \\ 0 & -r_2 & 0 & 0 & 0 \\ 0 & 0 & -r_3 & 1 & 1 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix}}_{A_3} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{U} \quad (10)$$

Multiplying (8), (9) and (10) by their duty ratios, D_2, $D_1\text{-}D_2$, and $1\text{-}D_1$, respectively, and summing the result to get the average model for the MCFC for mode 1 when i1>i2, as follows:

$$K\dot{X} = \underbrace{\begin{bmatrix} -r_1 & 0 & 0 & -D_1 & 0 \\ 0 & -r_2 & 0 & 0 & -D_2 \\ 0 & 0 & -r_3 & 1-D_1 & 1-D_2 \\ D_1 & 0 & -(1-D_1) & 0 & 0 \\ 0 & D_2 & -(1-D_2) & 0 & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{c1} \\ v_{c2} \end{bmatrix}}_{X} + BU \quad (11)$$

where $A = D_2 A_1 + (D_1\text{-}D_2) A_2 + (1\text{-}D_1) A_3$. At steady state, (11) is written as:

$$AX + BU = 0 \quad (12)$$

Rearranging (12), the capacitors' voltages can be expressed as:

$$V_{c1} = \frac{((1-D_2)^2+r_3D_2^2/r_2)a-b/(1-D_1)(1-D_2)}{1-((1-D_2)^2+r_3D_2^2/r_2)((1-D_1)^2+r_3D_1^2/r_1)} \quad (13)$$

$$V_{c2} = \frac{(1-D_1)(1-D_2)a-\left((1-D_1)^2+\frac{r_3}{r_1}D_1^2\right)b}{\frac{r_3}{r_1r_2}((D_1D_2)^2+(1-D_1)^2(r_1D_2^2+r_2D_1^2))} \quad (14)$$

where $a = (1-D_1)(V-V_3) - r_3D_1(V-V_1)/r_1$ and $b = (1-D_2)(V-V_3) - r_3D_2(V-V_2)/r_2$. The rated voltage of the capacitors and hence voltage stresses on the MCFC switches can be calculated from the maximum of (13) and (14). It is obvious that the capacitor voltage depends on of the network parameters and the voltage drops across the cables connected to the MCFC which are related to the loading condition of the grid. In order to calculate the first capacitor's voltage ripple, (6) is integrated over the charging period as follows:

$$\int_0^{DT} i_1\, dt = C \int_{V_{cmin}}^{V_{cmax}} v_{c1} \quad (15)$$

where T refers to the switching period which is the reciprocal of the switching frequency fs. Neglecting the current ripples compared to the average value, i_1, results in linear charging of the capacitor from initial minimum voltage V_{cmin} to maximum voltage V_{cmax}. Therefore, the first capacitor's voltage ripple, ΔV_{c1} can be estimated from (16):

$$\Delta V_{c1} = V_{cmax} - V_{cmin} = \frac{D\, I_1}{C\, f_s} \quad (16)$$

Eq. (16) shows that increasing the capacitance reduces the capacitor voltage ripple, as expected. Similarly, voltage ripple can be calculated for the second capacitor using i_2. It is noticeable that the capacitor voltage ripple depends on the mode of operation as the charging current changes from mode to another. For mode 1, the capacitance of the first capacitor can be roughly estimated from (15) and (16) to meet a required percentage voltage ripple, $\Delta V_{c\,pu} = \Delta V_c/V_c$, at the extreme deviations of the line currents. Similarly, the second capacitor can be calculated and for mode 1 and all other operating modes. Finally, the maximum value of the capacitances is considered to meet the desired level of voltage ripples for all modes of operation.

C.Control Strategy

One of the features of the MCFC is the ability to balance currents in the transmission cables or lines. One or more currents flow in the cables can be relatively higher than the rest and with the balancing control all currents are maintained within the acceptable limits and redistributed among all branches in order to prevent overloading of cables. Furthermore, the proposed MCFC can set the current flow in one cable to a desired value either to limit the current or damp it to zero. This feature may help in the situation of cables maintenance as only off load dis-connector switches are required to isolate the cable. This action eliminates the need for a dc circuit breaker or interrupting the whole transmission by opening the ac side circuit breaker. Fig.5 presents the proposed control system of the MCFC to control the current flow and simultaneously regulating the capacitor voltage. Two cascaded controllers are designed for each capacitor to realize the PWM signals needed for the MCFC. Two selector switches are utilized to determine the function of the MCFC. For currents balancing, the sum of currents in the three branches is measured and then divided by the number of branches to obtain the average value of the desired current, i^*. This value is considered the reference value to be compared with the measured value of the current(s) i_x that needs to be redistributed. The error signal is processed using a PI controller, where the output of this outer current control loop is considered the reference value of the capacitor voltage v_c^*. A limiter is used to prevent exceeding the rated capacitor voltage. The inner control loop is dictated to regulate the capacitor voltage at its estimated value from the outer one using another PI controller. The output of this controller is the duty cycle of the modulating switches. A mode detection unit measures the three cable currents to determine the operating mode and assign the two PWM signals (P_1 and P_2) and the on/off states to all relevant IGBT switches based on Table 1. Similarly, any desired cable current can be limited to any chosen value. This value is set as the reference value for the controller and switches are controlled to let the capacitor charge from the chosen cable and discharge in the other cable(s) carrying lower currents. If the reference value is set to zero, the capacitor will charge from the desired cable until it is fully charged to null the current flow in this cable. When the current is decreased in any cable by a certain amount it will increase in the remaining cables. It is important to check the capacity of these cables to prevent overloading problems.

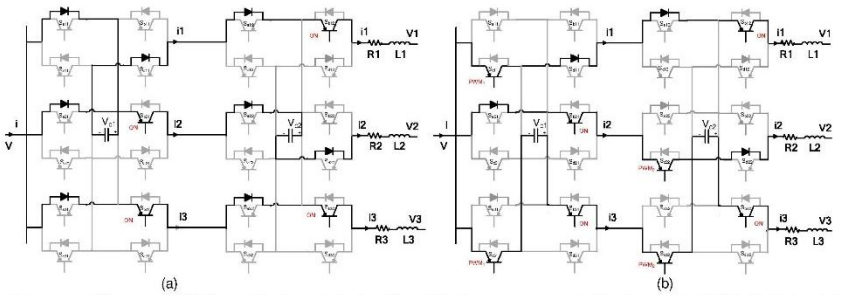


Fig. 4. The proposed Three-ports MCFC operating in mode 1 where i1 and i2 > the average current of the three cables (a) The first interval where the capacitors are charging from cable 1 and 2, (b) The second interval where the capacitors are discharging in cable 3.

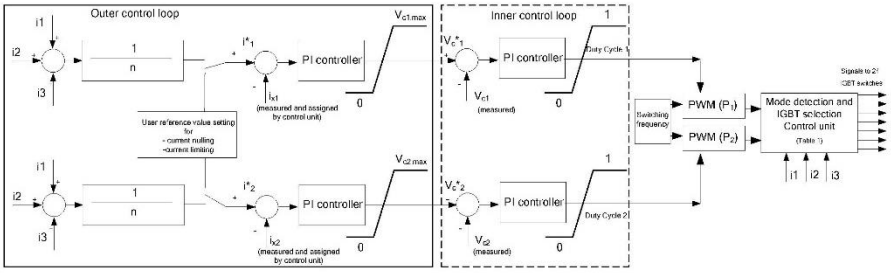


Fig. 5. The proposed control system for the three-port MCFC.

TABLE I
Switches Conduction States

Operation modes													
Direction:	----------Forward----------						----------Reverse----------						
Highest currents:	$i_1\&i_2$	$i_2\&i_3$	$i_1\&i_3$	i_1	i_2	i_3	$i_1\&i_2$	$i_2\&i_3$	$i_1\&i_3$	i_1	i_2	i_3	-
Mode:	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**Bypass**
S_{a11}	0	0	0	0	0	0	P_1	P_1	P_1	P_1	P_1	P_1	1
S_{a21}	0	0	0	0	0	0	0	P_1	P_1	P_1	P_1	0	1
S_{a31}	0	0	0	0	0	0	P_1	0	0	0	0	P_1	1
S_{b11}	0	1	0	0	1	1	0	0	0	0	0	0	1
S_{b21}	1	0	1	1	0	1	0	0	0	0	0	0	1
S_{b31}	1	1	1	1	1	0	0	0	0	0	0	0	1
S_{c11}	P_1	P_1	P_1	P_1	P_1	P_1	0	0	0	0	0	0	1
S_{c21}	0	P_1	P_1	P_1	P_1	0	0	0	0	0	0	0	1
S_{c31}	P_1	0	0	0	0	P_1	0	0	0	0	0	0	1
S_{d11}	0	0	0	0	0	0	0	1	0	0	1	1	1
S_{d21}	0	0	0	0	0	0	1	0	1	1	0	1	1
S_{d31}	0	0	0	0	0	0	1	1	1	1	1	0	1
S_{a12}	0	0	0	0	0	0	0	P_2	0	P_2	0	0	1
S_{a22}	0	0	0	0	0	0	P_2	0	P_2	0	P_2	P_2	1
S_{a32}	0	0	0	0	0	0	P_2	P_2	P_2	P_2	P_2	P_2	1
S_{b12}	1	1	1	0	1	1	0	0	0	0	0	0	1
S_{b22}	0	1	1	1	0	1	0	0	0	0	0	0	1
S_{b32}	1	0	0	1	1	0	0	0	0	0	0	0	1
S_{c12}	0	P_2	0	P_2	0	0	0	0	0	0	0	0	1
S_{c22}	P_2	0	P_2	0	P_2	P_2	0	0	0	0	0	0	1
S_{c32}	P_2	P_2	P_2	P_2	P_2	P_2	0	0	0	0	0	0	1
S_{d12}	0	0	0	0	0	0	1	1	1	0	1	1	1
S_{d22}	0	0	0	0	0	0	0	1	1	1	0	1	1
S_{d32}	0	0	0	0	0	0	1	0	0	1	1	0	1

IV. SIMULATION RESULTS

Simulation study is carried out using PSCAD/EMTDC software package where a multi-terminal MTDC grid, similar to that shown in Fig.1, is simulated. The main simulation parameters are shown in Table 2, where cables 1, 2 and 3 are carrying currents *i1*, *i2* and *i3*, respectively. VSC1 is operating in dc voltage regulating mode and the remaining three VSCs are operating in power control mode. Two case studies are presented to evaluate the different features and operation modes of the proposed MCFC.

TABLE II
Simulation parameters

Parameter	Value
Grid voltage rating	400kV
Capacitor 1	1mF
Capacitor 2	1mF
Switching frequency 1	1kHz
Switching frequency 2	1kHz
Cable 1	1.25Ω 10 mH
Cable 2	2.5Ω 10 mH
Cable 3	0.5Ω 10 mH

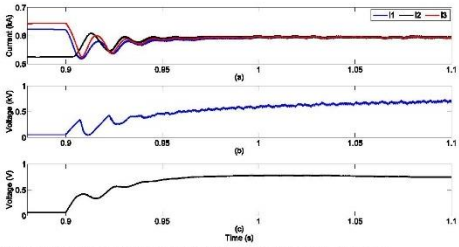


Fig.6. MCFC performing currents balancing: mode 3. a) Cable currents, b) Capacitor voltage Vc1, c) Capacitor voltage Vc2

A. Case 1: Currents Balancing

In this case study, currents *i1*, *i2* and *i3* are initially equal to 0.62kA, 0.52kA and 0.65kA, respectively. It is required to redistribute the currents to get a balanced operation by decreasing the currents flowing in both cables 1 and 3, and increase the current flowing in cable 2. The proposed control selects mode three of operation for the MCFC as shown in Table 1. The proposed control system of the MCFC is enabled at $t = 0.9\ s$. Fig. 6(a) demonstrates that the proposed three-port MCFC succeeds to balance the three cable currents to approximately 0.59kA with fast dynamics and without overshoot. Figs. 6(b) and (c) illustrate the capacitor voltages *Vc1 and Vc2* for this case respectively with steady state value of 0.75kV. These results demonstrate one of the advantages of the proposed CFC that is the capacitor and switches voltage rating is very small when compared to the grid voltage 400kV, resulting in low cost and small footprint for the MCFC. In addition, the superiority of the proposed MCFC topology over three-ports CFC topology with single capacitor proposed in [21] is presented where accurate currents balancing is achieved despite the remarkable differences in cable currents magnitudes.

To evaluate the viability of the proposed MCFC in realistic operating conditions, the same case study where the MCFC is enabled at t= 0.9 s to balance the currents is repeated under dynamic changes of the MTDC grid. The power references for terminals 2,3 and 4 are ramped up at t= 1.1 s to withdraw a total of 1500MW from the generating terminal 1. The system is set to return to the original reference value at t=1.4 s.

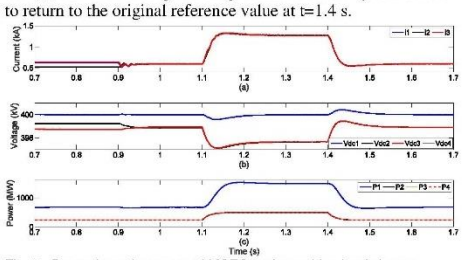


Fig. 7. Dynamic performance of MCFC under sudden load change. (a) Cable currents, (b) Terminal voltages, (c) Active powers

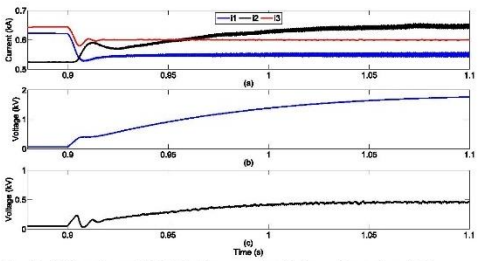


Fig. 8. Setting i1 and i3. (a) Cable currents. (b) Capacitor voltage Vc1, (c) Capacitor voltage Vc2.

Fig. 7(a) indicates that the MCFC performs the currents balancing operation smoothly even under sudden load changes. Moreover, the dc voltages are shown in Fig. 7(b) where it is noticed that the voltage regulating terminal 1 successfully maintain its voltage at 400kV. Finally, Fig.7(c) portrays the active power delivered at each terminal where *P2*, *P3* and *P4* are overlapping.

B. Case 2: Currents setting and nulling

In this case study, it is required to validate the ability of the proposed MCFC topology to perform tasks simultaneously by utilizing both capacitors. Currents *i1*, *i2* and *i3* are initially equal to 0.62kA, 0.52kA and 0.65kA, respectively. The MCFC is enabled at t=0.9 s to set both currents *i1* and *i3* to 0.55 kA and 0.6 kA respectively. Fig 8(a) indicates that the MCFC successfully performed the setting operation for both currents and current i2 has increased to achieve the balance in the grid. The capacitor voltages *Vc1* and *Vc2* are demonstrated in Figs. 8(b) and (c), respectively. It is noticed that *Vc1* is slightly higher than *Vc2* as *i1* is set to a lower value than *i3* and hence the capacitor C1 needs to charge more.

Similarly, the MCFC is controlled to set one current and balance the other two as illustrated in Fig. 9(a), where current *i3* is set to 0.375kA and currents i1 and i2 are balanced. Another function is to ramp down current *i3* to zero, and at the same time to set current i1 at 0.6kA as demonstrated in Fig. 9(b).

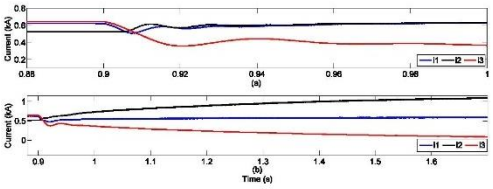


Fig. 9. MCFC performing simultaneous tasks. (a) Setting i3 to 0.375kA and balancing i1 and i2, (b) Nulling i3 and setting i1 to 0.6kA.

As explained earlier, this particular case is beneficial in cases of maintenance where cables can be disconnected easily using offload switches. Another advantage is that in cases of faults, a cable may be disconnected due to circuit breaker action and this will result in higher currents flowing in the remaining cables. The MCFC can be utilized to redistribute the currents flow in the remaining cables to prevent cable overloading and heating problems.

V. EXPERIMENTAL VALIDATION

A low power three-ports prototype of the proposed MCFC is implemented in the laboratory based on 24 IGBT switches with 70A – 600V rating each. A four terminals dc grid is formed with one terminal dc supply and the rest of terminals are connected to electronic (active) loads. Rapid Control Prototyping technique (RCP) is carried out by using OPAL RT OP4500 real time simulator to implement the proposed control system of Fig. 5 and acts as real time controller for the MCFC circuits. Grid cable currents are measured and delivered to the OP4500 that generates gating signals to the MCFC IGBT switches. The experimental system parameters are shown in Table 3 and a photograph of the setup is shown in Fig.10.

TABLE III
Experimental prototype parameters

	Value
Terminal 1	150V dc Power supply
Terminal 2	Active load
Terminal 3	Active load
Terminal 4	Active load
Capacitor 1	1mF
Capacitor 2	1mF
N-channel IGBT	70A – 600V
Proportional gain	100
Integral Gain	0.01
switching frequency	1000Hz

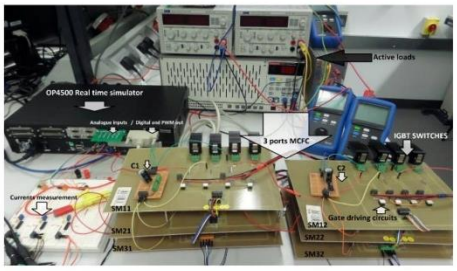


Fig. 10. Photograph of the MCFC experimental setup.

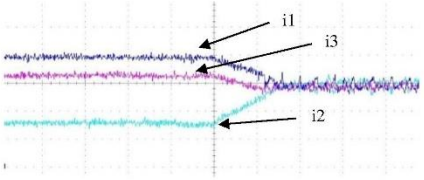


Fig. 11. Balancing i1 and i3 into i2. X axis: 1ms/Div and Y axis: 0.5A/Div.

A. Case 1: Balancing i1 and i3 into i2

Similar to case 1 presented earlier in the previous section of simulation results, mode three is tested practically using the experimental setup, where currents *i1*, *i2* and *i3* are initially equal to 2A, 0.75A and 1.75A, respectively. The MCFC is turned-on to perform the currents balancing operation as illustrated in Fig.11. The currents are balanced successfully to a value of 1.5A, approximately. Capacitor voltages in this case *Vc1* and *Vc2* are portrayed in Fig. 12(a) and 12(b), respectively. It can be noticed that *Vc1* is higher than Vc2 as current *i1* is relatively higher than current *i3*. Finally, the two PWM signals *P1* and *P2* are shown in Fig.13.

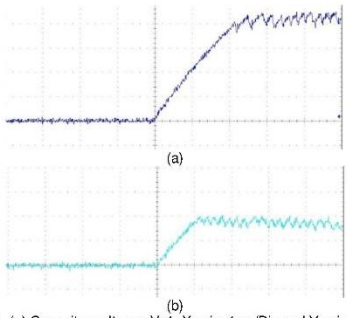


Fig. 12. (a) Capacitor voltages Vc1. X axis: 1ms/Div and Y axis: 1V/Div, (b) Capacitor voltages Vc2. X axis: 1ms/Div and Y axis: 1V/Div

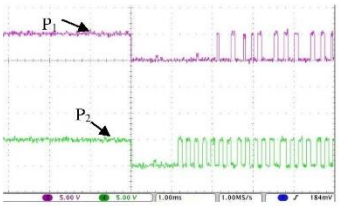


Fig. 13. PWM signals. X axis: 1ms/Div and Y axis: 5V/Div.

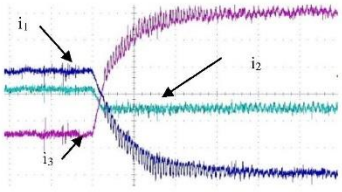


Fig. 14. Nulling i1 and setting i2. X axis: 10ms/Div and Y axis: 0.5A/Div.

B. Case 2: Nulling i1 and setting i2

Currents *i1*, *i2* and *i3* are initially equal to 2A, 1.5A and 0.75A. The reference values of the controllers are set as zero for *i1* and 1.25A for *i2*. The proposed MCFC succeeds in nulling current *i1* and setting current *i2* at the desired value as demonstrated in Fig.14. It is noticed that *i3* is decreased to a value that keep the energy balance in the grid. The corresponding capacitor voltages are presented in Fig.15 (a) and 15(b). Notice that the capacitor *C1* is charged to block current *i1* as indicated in Fig. 15(a). The relevant PWM signals are shown in Fig 16, where *P1* remains zero to allow *C1* to charge from cable 1 and *P2* is pulse width modulated to let *i2* achieve the required set point value. Fluent operation of the MCFC can be noticed and the topology is experimentally proven.

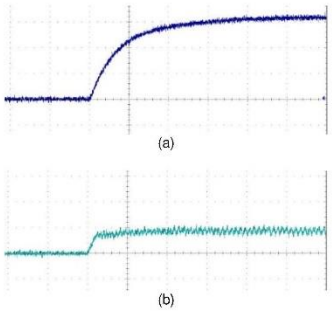


Fig. 15. (a) Capacitor voltage Vc1. X axis: 10ms/Div and Y axis: 5V/Div, (b) Capacitor voltage Vc2. X axis: 10ms/Div and Y axis: 1V/Div

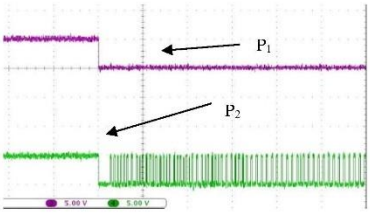


Fig. 16. PWM signals. X axis: 10ms/Div and Y axis: 5V/Div.

VI. Conclusion

This paper presents a generalized topology for a modular current flow controlling device. The proposed MCFC can be practical solution for power flow control applications in multi-terminal dc grids. The detailed analysis and operation of the proposed MCFC for bidirectional current flow are discussed. Simulation results are presented to evaluate the dynamic performance of the proposed three-port MCFC for various functionalities such as current balancing, current limiting, and current nulling during different modes of operation. Moreover, a scaled laboratory setup based on rapid control prototyping technique is built up and the experimental results validate the dynamic performance of the proposed control system of the MCFC. Fast dynamic response and accurate performance of the proposed control system for the MCFC are demonstrated using both computer software and rapid control prototyping. Results revealed that the proposed MCFC offers promising solutions for power flow control problems in specially in offshore MTDC grids where the cost and size can be significantly minimized.

References

[1] Higgins, P., Foley, A.: 'The evolution of offshore wind power in the United Kingdom', Renew. Sust. Energ. Rev. , no. 37, pp. 599-612, 2014.
[2] M. Aredes, R. Dias, A. F. Da Cunha De Aquino, C. Portela, and E. Watanabe, "Going the distance," IEEE Ind. Electron. Mag., vol. 5, no. 1, pp. 36–48, Mar. 2011.
[3] Gordon, S.: 'Supergrid to the rescue', Power Engineer, vol. 20, no.5, pp. 30-33, 2006.
[4] Foerst, R., Heyner, G., Kanngiesser, K.W., et al.: 'Multiterminal operation of hvdc converter stations', IEEE Trans. Power App. Syst., vol. 88, no.7, pp. 1042–1052, 1969.
[5] Shukla, A., Demetriades, G.D.: 'A Survey on hybrid circuit-breaker topologies', IEEE Trans. On Power Deliv., vol. 30, no. 2, pp. 627-641, 2015.
[6] Barker, C.D., Whitehouse, R.S.: 'An alternative approach to HVDC grid protection', 9th IET Int. Conf. on AC and DC Pow. Transm., Birmingham, UK, pp. 1-6, Dec. 2012.
[7] Sneath, J., Rajapakse, A.D.: 'fault detection and interruption in an earthed HVDC grid using ROCOV and hybrid DC breakers', IEEE Trans. Power Del., PP, (99) pp. 1-8, 2014.
[8] Jovcic, D.: 'Bidirectional, high-power dc transformer', IEEE Trans. on Power Deliv., vol. 24, no.4, pp. 2276-2283, 2009.
[9] Luth, T., Merlin, M.M.C., Green, T.C., et al.: 'High frequency operation of a DC/AC/DC system for HVDC applications', IEEE Trans. On power electronics, vol. 29, no.8, pp.4107-4115, 2014.
[10] Pinto, R. Teixeira, et al. "A novel distributed direct-voltage control strategy for grid integration of offshore wind energy systems through MTDC network." IEEE Trans. On Ind. Electron., vol. 60, no. 6, pp. 2429-2441, 2013
[11] Wang, W., Barnes, M.: 'Power flow algorithms for multi-terminal VSCHVDC with droop control', IEEE Trans. Power Syst., vol. 29, no.4, pp. 1721–1730, 2014.
[12] Rouzbehi, K., Miranian, A., Candela, J.I., et al.: 'A generalized voltage droop strategy for control of multi-terminal DC grids' IEEE Trans. on Indust. App., vol. 51, no.1, pp.607-618, 2014.
[13] J. C. Vasquez, J. M. Guerrero, A. Luna, P. Rodriguez, and R. Teodorescu, "Adaptive droop control applied to voltage-source inverters operating in grid-connected and islanded modes," IEEE Trans. Ind. Electron., vol. 56, no. 10, pp. 4088–4096, Oct. 2009.
[14] Veilleux, E., Ooi, B.: 'Multiterminal HVDC with thyristor power-flow controller', IEEE Trans. Power Del., vol. 27, no.3, pp. 1205– 1212, 2012.
[15] Barker, C.D., Whitehouse, R.S.: 'A current flow controller for use in HVDC grids', 10th IET international Conf. on AC and DC Pow. Transm., Birmingham, UK, pp. 1-6, 2012
[16] Mu, Q., Liang, J., Yalou, L., et al.: 'Power flow control devices in DC grids ', IEEE Power and Energy Society General Meeting, San Diego, USA, pp.1-7, 2012.

[17] Feng, C., Wang, S., & Mu, Q. "DC grid power flow control devices" in HVDC Grids: For Offshore and Supergrid of the Future, Wiley, 2016, pp. 429-450.

[18] Jovcic, D., et al. "Power flow control in DC transmission grids using mechanical and semiconductor based DC/DC devices." 10th IET International Conference on. IET, 2012.

[19] K. Rouzbehi; J. I. Candela; A. Luna; G. Gharehpetian; P. Rodriguez, "Flexible Control of Power Flow in Multi-Terminal DC Grids Using DC-DC Converter," in IEEE Journal of Emerg, and Select, Topics in Pow. Electron., vol.PP, no.99, pp.1-1.

[20] Jovcic, D., "Bidirectional, high-power DC transformer." IEEE Trans. on Power. Del., vol. 24, no. 4, pp.2276-2283, 2009

[21] H. Y. Diab, M. I. Marei & S. B. Tennakoon 'Operation and control of an insulated gate bipolar transistor-based current controlling device for power flow applications in multi-terminal high-voltage direct current grids.' IET Power Electronics, vol. 9, issue 2, pp. 305-315, 2016

[22] S.Bassols, Joan, E. Prieto-Araujo, and O. Gomis-Bellmunt. "Modelling and control of an interline Current Flow Controller for meshed HVDC grids." IEEE Trans. Power. Del., vol. PP, no. 99, pp.1-9, 2016.

An Investigation of Power Flow Control Methods in Multi Terminal High Voltage DC Grids

Hatem Diab
Staffordshire University
United Kingdom
Hatem.diab@research.staffs.ac.uk

Sarath Tennakoon
Staffordshire University
United Kingdom
s.b.tennakoon@staffs.ac.uk

Christopher Gould
Staffordshire University
United Kingdom
C.A.Gould@staffs.ac.uk

Mostafa Marei
Ain Shams University
Egypt
mostafamarei@yahoo.ca

***Abstract*- Some significant problems prevent the formation of multi terminal high voltage DC grids until now. Absence of power flow control is considered one of the main challenges that have to be solved in the near future to allow building of an efficient DC grid. This paper investigates different power flow control methods. Simulation of series insertion of AC/DC converters is carried out using MATLAB/SIMULINK software package and results are discussed.**

***Index Terms*— HVDC, MTDC grids, Power flow control**

I. Introduction

Offshore wind energy is growing every day in Europe and is expected to play an increasingly important role in the coming few years [1], particularly to meet the goal of establishing a European DC super grid to interconnect conventional AC grids along with offshore wind farms in the north sea area (Fig.1) [2,3].

As distances between offshore wind farms and on shore AC grids grew longer, DC transmission became the economical and efficient option to transmit the generated power to the shore when compared to AC, as the breakeven distance at which DC is more economical than AC for submarine cable transmission is around 100 km [4,5].

Major problems facing the development of MTDC networks are absence of DC circuit breakers, protection algorithms and power flow controllers. The inability to control the power flow or more particularly the current flow through the network branches is due to the simple nature and characteristics of DC power which is different from AC power that can be controlled through different methods such as FACTS [6]. Power flow control is needed to allow distribution of the power according to the dispatch center orders and to protect cables from getting overloaded by high currents. Recent research has focused on achieving power flow control through the control of voltage source converters and a few methods can be found in literature [7-10]. In this paper three methods of power flow control namely, insertion of series resistors, insertion of DC voltage sources and utilizing IGBT based AC/DC are studied. The study is carried out through computer simulation using MATLAB/SIMULINK software package.

This paper is organized as follows: section II discusses the feasibility of using series resistors for power flow control, section III illustrates the use of controlled DC voltage sources and section IV shows how AC/DC converters can be utilized as power flow controllers. Finally, sections V, VI and VII show description of the current flow controller device, simulation results and conclusion respectively.

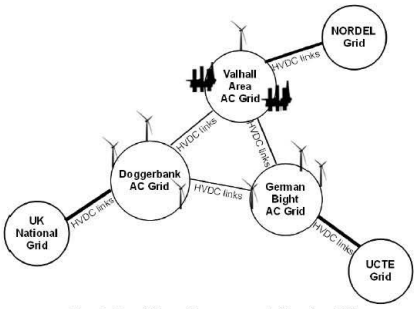


Fig. 1. Possible north sea super grid topology [3].

II. Insertion of Series Resistors

The first approach proposed is to change the series resistance in a certain branch by switching series resistors in or out of the branch as shown in Fig.2. The total resistance of cable 1 would change and thus current can be decreased or increased to the desired value. Switches can be either mechanical or electronic IGBTs. Mechanical switches would offer slow switching operation with low switching losses while electronic switches would offer very fast switching with high switching losses. Resistors can be set into a configuration similar to the binary configuration to achieve more flexible values of resistances with fewer resistors. The main drawback of this method is that the Power loss in DC which is directly proportional to the square of the current passing through the resistor as shown in equation (1).

$$P_L = I^2 . R \quad (1)$$

This means that for each additional 1 ohm resistor inserted in a cable carrying 1kA current, an additional power loss of 1 MW will occur, and this is relatively high compared to the overall power losses in any DC grid.

978-1-4673-9682-0/15/$31.00 ©2015 IEEE

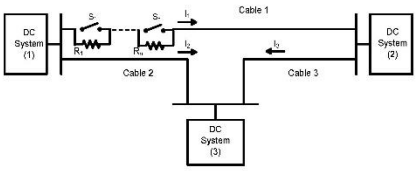


Fig. 2. Switching of series resistors.

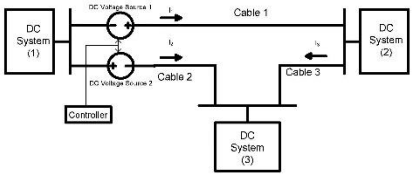


Fig. 3. Inserting two controlled DC voltage sources in series.

III. Insertion of Series Voltage Sources

The second approach would be to vary the voltage in a certain branch, which can be achieved by inserting a controlled voltage source in series that would be either acting as additional positive resistance or negative resistance based upon the voltage source polarity (See Fig. 3). This method is ideal in low voltage applications, where controlled DC voltages can easily be implemented. However investigation is carried out to clarify the advantages of this concept and in the following section similar, more practical solution is proposed.

It is assumed that cables 1 and 2 (Fig. 3)are carrying two different currents, and it is required to equally distribute both currents to prevent one of the cables from overheating. A proportional – integral (PI) controller is designed to fulfill this purpose. Currents I1 and I2 are compared together and the output error signal is inserted to the PI controller, the PI controller provides the two voltage sources with the required voltage set point for the balancing operation as shown in Fig.4.

IV. AC/DC Converters Utilized as Power Flow Controllers

The third method is a more practical implementation of the second approach mentioned earlier in section III. The absence of high voltage DC voltage source is solved by injecting the required DC voltage to the grid through AC/DC converters. (see Fig.5). Converters can be supplied by three phase AC voltage through the nearest terminal by stepping down the voltage to the desired level. An IGBT based three level PWM voltage source converter [11] shown in Fig.6 is used as a power flow controller in this paper. Two converters are inserted in the two cables as a similar example of the one shown earlier in Fig.3. The controller of the converter is supplied with reference DC voltage; this set point is determined by a PI controller that minimizes the error signal of both currents (Fig.7).

This power flow control method offers a very good solution as AC/DC converters are very common in power

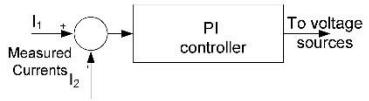


Fig. 4. PI controller to balance currents I1 and I2.

industry and the required additional controller is not complicated. Converters can be set to limit the current to a required value or to balance the currents as mentioned earlier. The noticeable disadvantage is that stepping the HVAC down from hundreds of kVs to few kVs to supply the converter will require a relatively bulky, high cost three phase AC transformer. The option of supplying the converter from the same nearest main transformer can be also considered. A full bridge can be added to give bi directional functionality to the controller.

V. Current Flow Controller

The current flow controller proposed in [12] is one of the recent inventions dedicated for DC power flow control problem. It consists of eight IGBT switches (four for each cable) and two capacitors (one for each cable) as shown in Fig.8. The current flow controller interchanges amount of voltage between the two cables in order to balance the currents. The current flow controller can also be set to keep the current at any desired value or even ramp the current to zero which is useful in maintenance purposes. One of its numerous advantages is that the IGBT valves can be of a few kV rating resulting in small footprint and low cost.

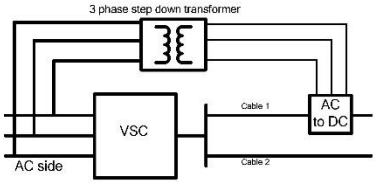


Fig. 5. AC/DC converter as a power flow controller.

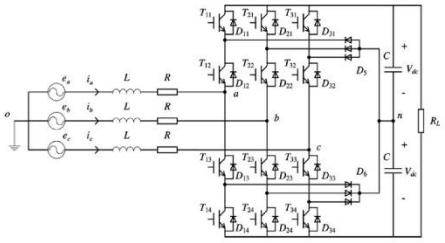


Fig. 6. Typical 3 level AC/DC converter circuit topology [11].

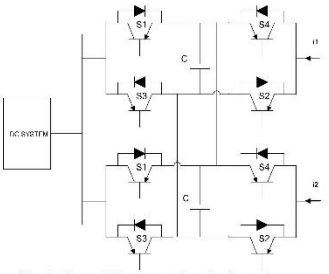


Fig. 8. Current flow controller circuit topology.

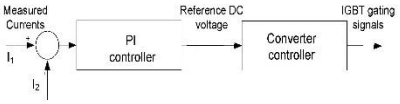


Fig. 7. Currents balancing through AC/DC converter's control loop.

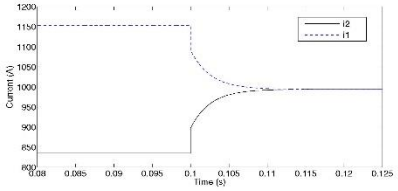


Fig. 9. Balancing I1 and I2 using DC voltage sources.

VI. Simulation Results

A. Case I: Balancing Currents Using Voltage Sources

A three terminal test system is used as a multi terminal DC grid in all simulation cases (Fig.3). The parameters of the test system are given in Table I. Cable inductances are neglected in case I only. In normal operation, currents I1 and I2 are 1.18 and 0.84 kA respectively. The target of this simulation is to distribute both currents evenly on both cables 1 and 2. Ideal DC voltage sources with a PI controller are used in series with both cables. Fig. 9 shows the fast dynamic response of when the controller is switched on at 0.1 seconds and succeeds to balance the currents in less than 0.02 seconds. However as mentioned before this method is investigated for illustration only and it is not practical in multi terminal HVDC applications.

B. Case II: Balancing Currents Using AC/DC Converters

For the same grid simulated in case I, two IGBT based three level PWM voltage source converters are to replace the voltage sources in case I, and inserted in series in cables 1 and 2 as shown in Fig. 10. Currents I1 and I2 are given to the PI controller as inputs and the PI controller generate the DC voltage set point for both converters. One converter adds the amount of voltage decided by the PI controller in one cable and the other converter subtracts the same amount from the other cable in order to achieve the balanced currents as shown in Fig. 11. The DC voltage injected and subtracted to both cables by the converter is shown in Fig.12.

TABLE I
TEST GRID PARAMETERS

Parameter	Value
DC Voltage rating	320 kV
Cable 1 – 131km	1.25 Ohm & 276 mH
Cable 2 – 255 km	2.42 Ohm & 538 mH
Cable 3 – 255 km	2.42 Ohm & 538 mH
Converter's AC voltage	400V peak

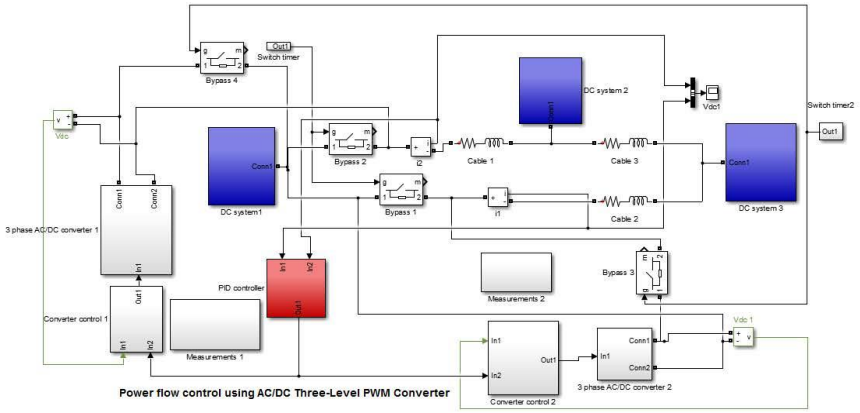


Fig. 10. MATLAB/Simulink model showing three terminals DC grid with two series AC/DC converters and PI controller

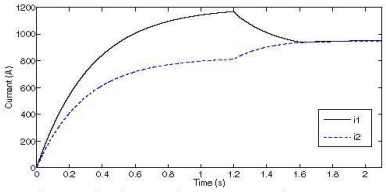


Fig. 11. Balancing I1 and I2 using two AC/DC converters.

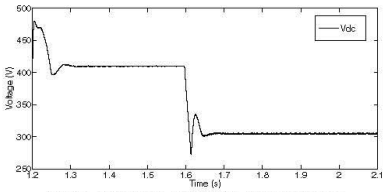


Fig. 12. DC voltage added to the grid by converter.

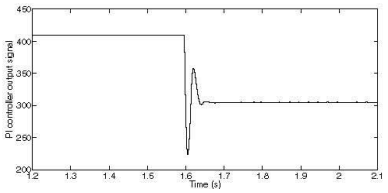


Fig. 13 PI controller output signal.

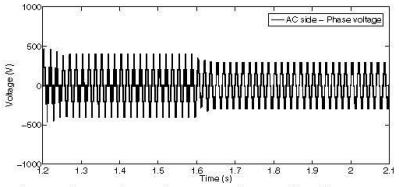


Fig. 14 Phase to Phase voltage V_{AB} at the AC side of the converter.

Fig. 13 and Fig.14 show the PI controller output signal and the converter's AC side phase to phase voltage respectively.

C. Case III: Current Set Point Using Single AC/DC Converter

Similarly, one converter only can be used to decrease the current within a cable to any desired value. Fig. 15 shows the operation of one converter only applied into cable one to set the current I1from 1200A to 900A at 2 seconds and 950 at 3 seconds, while current I2 remains uncontrolled. Fig.16 shows the applied DC voltage of the converter to the grid.

We can observe from the simulation results that power flow control using AC/DC converters is possible and accurate results can be achieved if proper control is applied. Controlled voltage source method shows very fast response and accurate results although it can be used only in low voltage DC power flow applications.

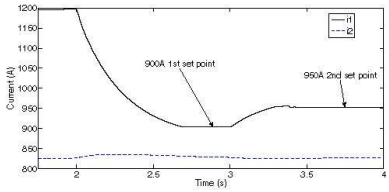


Fig. 15. I1 is set to 900A and 950A using single AC/DC converter.

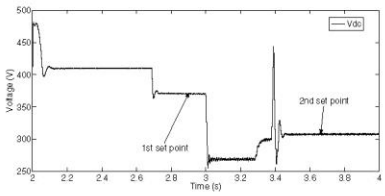


Fig. 16. DC voltage added to the grid by converter.

VII. Conclusion

This paper investigates the power flow control problem in multi terminal HVDC grids. Three different power flow control methods are investigated. Series resistors method cause high power losses despite its simplicity. Two methods usage of AC/DC converters and DC voltage sources are simulated using MATLAB/SIMULINK software package and tested on a three terminal HVDC grid. AC/DC shows the ability of playing the HVDC power flow controller role in the future as it can fluently add or subtract voltage from any desired cable and thus control the flowing current. Results show fast dynamic response and accurate performance in balancing and limiting DC currents.

References

[1] E. W. E. A. (EWEA). (2013) - Communication from the commission to the European parliament, the council, the European economic and social committee and the committee of the regions. Availble: http://ec.europa.eu/maritimeaffairs/policy/blue_growth/documents/com_2012_494_en.pdf

[2] F.O.S.G. Working group 2 Technological -Roadmap to the Supergrid Technologies Revision 2014. Available: http://www.friendsofthesupergrid.eu/wp-content/uploads/2014/06/WG2_Supergrid-Technological-Roadmap_20140622_final.pdf

[3] Vrana, T. K., et al. "The North Sea super grid-a technical perspective." . 9th IET International Conference on AC and DC Power Transmission, 2010. ACDC. London, Oct. 2010.

[4] Colla, Luigi, et al. "Mediterranean high voltage submarine cable links technology and system challenges." AEIT Annual Conference, IEEE, Mondello, Oct. 2013.

[5] Meah, Kala, and Sadrul Ula. "Comparative evaluation of HVDC and HVAC transmission systems." Power Engineering Society General Meeting, IEEE, Tampa 2007.

[6] Hingorani, Narain G., and Laszlo Gyugyi. "Understanding FACTS: concepts and technology of flexible AC transmission systems". Ed. Mohamed El-Hawary. Vol. 1. New York: IEEE press, 2000.

[7] Haileselassie, Temesgen M., and Kjetil Uhlen. "Impact of DC line voltage drops on power flow of MTDC using droop control." IEEE Transactions on Power Systems, 27.3 pp 1441-1449. Aug. 2012.

[8] Johnson, Brian K., et al. "Expandable multiterminal DC systems based on voltage droop." , IEEE Transactions on Power Delivery 8.4 .1993.

[9] Dierckxsens, Carlos, et al. "A distributed DC voltage control method for VSC MTDC systems." Electric Power Systems Research 82.1 pp 54-58, 2012.

[10] Beerten, Jef, Dirk Van Hertem, and Ronnie Belmans. "VSC MTDC systems with a distributed DC voltage control-A power flow approach." PowerTech, IEEE Trondheim, 2011.

[11] Lou, H., et al. "Pulse width modulation AC/DC converters with line current harmonics minimisation and high power factor using hybrid particle swarm optimisation." IET Power Electronics 2.6. pp 686-696. 2009.

[12] Barker, C. D., and R. S. Whitehouse. "A current flow controller for use in HVDC grids." 10th IET conference on AC and DC power transmission .Birmingham, 2012.

Appendix

E.

Lists of Figures and Tables

E.1 List of Figures

E.2 List of Tables