Inter-tier crosstalk noise on power delivery networks for 3-D ICs with inductively-coupled interconnects

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Inter-Tier Crosstalk Noise on Power Delivery Networks for 3-D ICs with Inductively-Coupled Interconnects

Ioannis A. Papistas and Vasilis F. Pavlidis
Advanced Processor Technologies Group
School of Computer Science, The University of Manchester
{papistai, pavlidis}@cs.man.ac.uk

ABSTRACT

Inductive links have been proposed as an inter-tier interconnect solution for three-dimensional (3-D) integrated systems. Combined with signal multiplexing, inductive links achieve high communication bandwidth comparable to that of through silicon vias. However, being a wireless medium, electromagnetic coupling between the inductive link and nearby on-chip interconnects can cause voltage fluctuations affecting interconnect performance. Although the interference of interconnects on the operation of inductive links has been investigated, the inverse problem has yet to be explored. Consequently, this paper performs an investigation on the effect of electromagnetic coupling on different topologies of power delivery networks (PDNs) in the vicinity of on-chip inductors. Results indicate that the interdigitated PDN topology suffers from the induced noise due to the inductive links of the neighbouring tiers exhibiting a minimum aggregate noise of 131.3 mV. Alternatively, the paired topologies exhibit a superior noise behaviour, achieving a 39.4% and 35.4% decrease in noise level for paired type I and paired type II topologies, respectively, compared to the interdigitated topology.

Keywords

Inductive Links; Crosstalk Noise; Power Delivery Networks; Wireless 3-D Systems

1. INTRODUCTION

Heterogeneous three-dimensional integration is an emerging technology that provides a platform for multifunctional, high performance, and low power electronics [1], by vertically stacking ICs of disparate technologies. Through silicon vias (TSVs) and inductive links provide low latency and low power interconnections [2] for inter-tier communication, exhibiting comparable performance, when signal multiplexing is employed for inductive links [3].

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TSVs, however, can be an expensive means due to manufacturing complexity and possibly low yield [4]. Alternatively, inductive links comply with standard (2-D) CMOS processes. Furthermore, inductive links provide unique advantages to heterogeneous integration, such as die detachability [5], and although the transceiver can be designed with different nominal voltage supplies there is no need for level shifters [6].

High performance inductive links have been developed recently [7, 8]. In addition to design methods, the crosstalk between inductive links [5, 9] and the interference of interconnects on inductive links have both been explored [10]. Nevertheless, the effect of inductive links on global interconnects has yet to be investigated. Due to the magnetic flux, on-chip wireless communication leads to parasitic coupling with nearby conductors, such as power delivery interconnects, which operate as accidental antennas [11]. Consequently, undesirable voltage fluctuations are induced on the power delivery network, that can limit the performance of the system and increase power consumption.

This work focuses on the noise caused by electromagnetic coupling between the inductive link interface and different topologies of power delivery networks (PDN). This crosstalk noise is added to the other components of noise experienced by a power delivery network topology. Power/ground (P/G) wires suffer from static IR-drop noise due to the wire resistance and transient, high frequency voltage drop, $L\frac{di}{dt}$ due to device switching [12]. In 3-D systems with inductive links, voltage fluctuations are induced on the P/G wires adjacent to the inductive link array, deteriorating system robustness.

Standard design methodologies provision for the static and dynamic noise on PDNs. However, traditional PDN design can not cope with the additional noise, originating from the on-chip inductors in contactless 3-D systems. Consequently, the combined effect of noise onto PDNs is addressed in this paper, including the induced noise by multiple inductors and the resistive IR-drop noise[1]. Interconnect structures are simulated, considering the spatial alignment of power and ground loops to the inductive link and the area of the PDN topology that couples with the inductor.

An expression to determine the impact of an inductive link array onto a P/G grid is also provided. Analysis indicates that crosstalk coupling between inductors and P/G wires can lead to harmful levels of power supply noise. The susceptibility of a PDN to this type of noise is shown to

[1]The spatial behaviour of power supply noise is considered in this work, while the temporal component is left as future work and is therefore beyond the scope of this paper.

strongly depend on the inductance and placement of the P/G wires with respect to the inductive links. Considering these important dependencies, measures to diminish the induced noise are proposed.

The remainder of this paper is organised as follows. In Section 2, physical models are utilised to describe crosstalk noise between an inductive link and various topologies of power delivery networks. Moreover, the behaviour of the induced noise is presented for each topology, as a function of the area and spatial position of the PDN with respect to the inductive link. A practical scenario is investigated in Section 3 where an array of inductive links couples with a portion of the power network and the location of P/G wires is adapted to satisfy both the induced noise and IR-drop constraints. Some conclusions are drawn in the last section.

2. SIMULATION ANALYSIS AND RESULTS

The coupling between an inductive link and different PDN topologies is presented in this section. This coupling is analysed as a function of the area of a PDN loop and as a function of the spatial position with respect to the inductive link in subsections 2.1 and 2.2, respectively. The combined effect of these (physical) parameters is investigated in Section 2.3.

The investigated PDN topologies are depicted in Fig. 1. The chosen PDN topologies include the interdigitated P/G, shown in Fig. 1(a), and paired P/G type I and II illustrated in Figs. 1(b) and 1(c), respectively [12]. The power and ground wires are denoted with grey and white colours, respectively. Those topologies are chosen for being commonly used, while also presenting different physical traits. An analysis of the non-interdigitated topology is omitted, as it can be devised from the interdigitated topology.

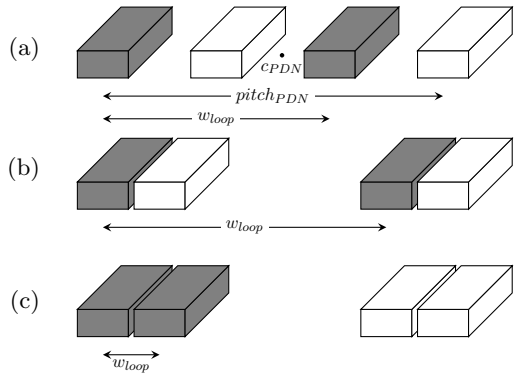

Figure 1: PDN topologies, where (a) is an interdigitated P/G-P/G topology, (b) is a paired type I P/G-P/G topology, and (c) is a type II P/P-G/G topology.

The centre and pitch of an elemental PDN segment, c_{PDN} and $pitch_{PDN}$, respectively, are depicted in Fig. 1. As the width of the loop, w_{loop}, between the power or ground wires is different for each topology, $pitch_{PDN}$ is used for all topologies to provide a fair comparison. The centre of the PDN segment, c_{PDN} is used to define the relative spatial position of the PDN with respect to the inductive link.

The simulated structure is based on a flip-chip and face-to-back 3-D integration approach consisting of an inductive link and one interconnection loop. The cross-section of the structure is depicted in Fig. 2(a), showing the communication distance X between the inductors of the link. The top view of this structure is seen in Fig. 2(b). Distance δ_c denotes the spatial separation between the geometric centre of the inductor, c_I and the geometric centre of the interconnect loop, c_{PDN}.

Each closed path formed within the PDN is susceptible to eddy currents and, consequently, voltage fluctuations induced by the inductor. Closed paths are formed between two or more power or ground wires. The amplitude of the induced voltage on the PDN depends on the geometric and electrical characteristics of the closed path that alter the coupling between the inductor and the PDN loop. Furthermore, the induced voltage depends upon the magnetic flux density, that changes according to the spatial position of the PDN with respect to the inductor. As shown in Section 2.2 this spatial dependency is the primary factor that contributes to the induced noise for all of the investigated topologies.

Voltage fluctuations $V_{noise,P}$ induced by the inductor to the power loop are extracted by the S-parameters of the simulated structure. As the transmission coefficient S_{ij} describes the transmitted voltage ratio between the respective structures [13], $V_{noise,P}$ is given by

$$V_{noise,P} = (S_{31} + S_{21}S_{32})V_{dd}, \tag{1}$$

where S_{31} is the transmission coefficient from the transmitter inductor to the PDN wire. S_{21} describes the transmission coefficient from the transmitter inductor to the receiver inductor and S_{32} the transmission coefficient from the receiver inductor to the PDN wire, modelling the impact of both inductors. Note that both inductors induce some voltage on the power wire, yet the level of noise from the receiver is significantly lower. A similar analysis also applies to ground wires. The accumulated noise induced by the inductive link on the PDN is given by

$$V_{noise,acc} = V_{noise,P} + V_{noise,G}, \tag{2}$$

where $V_{noise,P}$ is the noise induced on power loops and $V_{noise,G}$ is the noise induced on ground loops, respectively.

To quantify this noise, the structure in Fig. 2 is simulated for a 65 nm technology [14]. A width and spacing of 0.45 μm are used for the windings of the inductive link, while a width of 4.5 μm is used for the power loop. The structure is assumed to occupy the three topmost interconnect layers, with a thickness of 1.2 μm each and the inductor is laid out on the uppermost metal layer. The inductive link model is based on [6], where an inductor with an outer diameter of $d_{out} = 79$ μm and $n = 8$ turns is implemented. Due to the symmetry of the structure, each inductor can transmit or receive data, and therefore, there is no need to add another wire beneath the inductor in the lower tier (see Fig. 2(a)). With this approach the electromagnetic simulation is simplified, without sacrificing accuracy.

2.1 Effect of the Pitch of the PDN Topology on the Induced Noise

The results concerning the pitch of the PDN topology and the respective accumulated induced noise are presented in this subsection. To investigate the effect of the PDN pitch, the PDN loop and the inductive link are considered centred, $\delta_c = 0$ μm, while the pitch of the PDN is swept across a range of typical values, $pitch_{PDN} = [45\ \mu m, 105\ \mu m]$ [12].

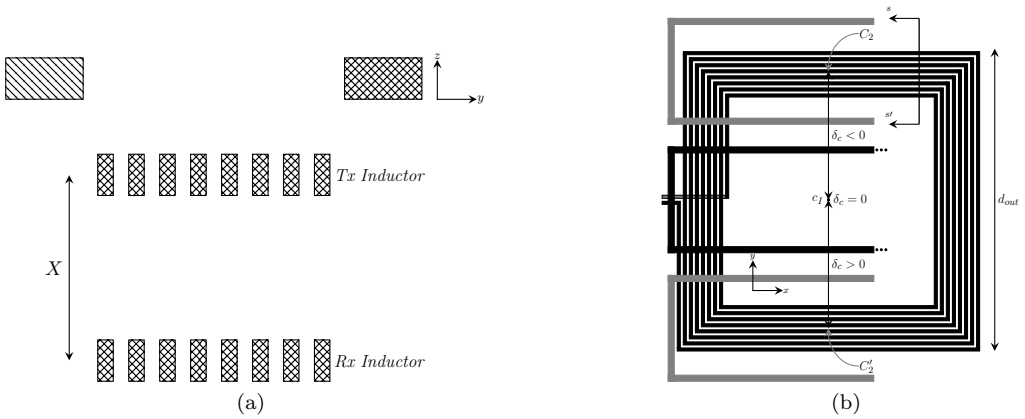

Figure 2: Inductive link with adjacent P/G loop, (a) cross-section of the structure along $s - s\prime$ in Fig 2(b) and (b) top view of the structure with the loop placed in different locations.

The susceptibility of the PDN topologies to the induced noise with respect to the PDN pitch is illustrated in Fig. 3. Solid lines denote the noise induced on the interdigitated PDN topology, while dotted and dashdotted lines indicate the noise on the paired type I and type II topologies, respectively. As the PDN is symmetric and centred to the inductive link, noise induced on the power loop can be considered equal to the noise induced on the ground loop with negligible error.

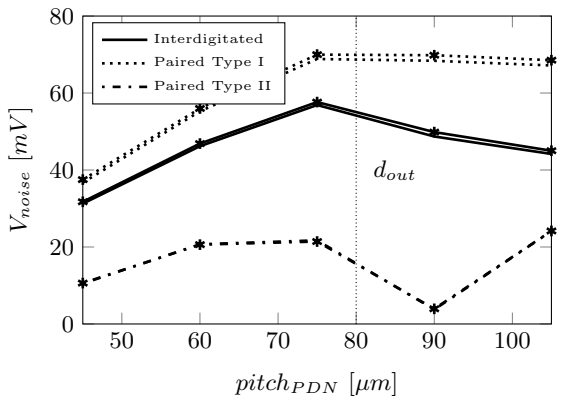

Figure 3: Induced noise by the inductive link depending on the pitch $pitch_{PDN}$ of the PDN topology. Lines marked with asterisks indicate ground loops, whereas unmarked lines label the power loops.

For pitches $pitch_{PDN} \leq d_{out}$, the induced noise worsens with increasing pitch for all three topologies. This outcome can be attributed to two factors. An increasing PDN pitch leads to higher inductance for the PDN loop and consequently increased coupling. Moreover, by increasing the PDN pitch, the conductors of the PDN shift closer to the windings of the inductor. The shortened horizontal distance between the PDN segments and the inductor windings leads to increased coupling, resulting in higher levels of induced noise. Nevertheless, the behaviour is different for $pitch_{PDN} > d_{out}$. For the interdigitated and paired type I topologies, increasing the pitch of the PDN more than the outer diameter of the inductor leads to a slight decrease in the induced noise, since the PDN conductors are shifted away from the inductor windings. Between these two topologies, the interdigitated topology exhibits a larger drop in the induced noise, as the curve in Fig. 3 suggests, implying a lower susceptibility to induced noise.

Alternatively, the paired type II topology exhibits a significant decrease in induced noise, before increasing again for larger pitches. For $pitch_{PDN} = 90\ \mu m$, the topology resembles the structure shown in Fig. 2, with C_2 the geometric centre of the power loop and C_2' the geometric centre of the ground loop, respectively. This placement results in a minimum induced noise, due to the opposite polarity of the accrued magnetic flux that couples with the conductors of the PDN loops. The magnetic flux coupled with the conductor of the wire loop lying on the inner side of the inductor $(y_{C_2'} - w_{loop}/2)$ presents an opposite polarity compared to the conductor lying on the outer side of the inductor $(y_{C_2'} + w_{loop}/2)$. Thus, induced currents flow in opposite directions, effectively minimising the induced noise. Nevertheless, increasing the pitch further, the power and ground loops lie completely outside the inductor and the currents induced by the magnetic flux present the same polarity, leading to higher levels of noise. Beyond this point nevertheless, the noise amplitude steadily decreases, due to the reduced magnetic flux for those distances.

2.2 Effect of Spatial Position of the PDN Topology on the Induced Noise

In this subsection, the induced noise due to the spatial position of the PDN with respect to the inductive link is presented. To this end, the pitch of the PDN is kept constant to $pitch_{PDN} = 60\ \mu m$. Alternatively, the distance δ_c between the geometric centres of the PDN and the inductive link is swept across a range of values, $\delta_c = [0, d_{out}]$.

Results relating to the spatial position of the PDN are shown in Fig. 4. The depicted accumulated noise includes the impact of both the power and ground loops according to (2). The solid line denotes the induced noise on the interdigitated topology, while the dotted and dashdotted lines the noise on the paired type I and paired type II topologies, respectively.

Since the pitch of the PDN is constant in this analysis, the loop inductance for each topology remains constant throughout the experiment. Due to the smaller loop size (see w_{loop} in Fig. 1) of the paired type II compared to the other topologies, the coupling between the PDN and the in-

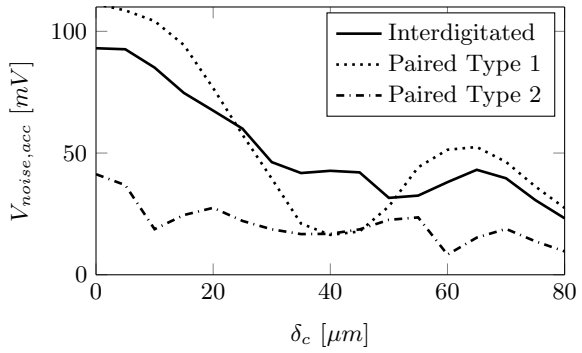

Figure 4: Noise induced by the inductive link for increasing distance δ_c.

ductive link is weaker, thus being less susceptible to noise. Differently, the interdigitated and paired type I topologies exhibit stronger coupling with the inductor, due to their higher inductances caused by the increased distance between the power (or ground) wires forming a power (ground) loop. Consequently, these topologies exhibit a stronger coupling with the inductive link and, therefore, higher levels of noise are induced.

Nevertheless, as the noise is also a funtion of the magnetic flux density, all of the PDN topologies exhibit positions where the induced noise is reduced, exploiting the opposite polarity of the magnetic flux, as mentioned in subsection 2.1. The density of the magnetic flux is spatially dependent, thus, placing the PDN in different positions leads to a different amount of magnetic flux coupled with the PDN. As a result, even the paired type I topology, which due to the wider P/G loops (see Fig. 1) exhibits increased noise susceptibility, presents a minimum noise level for $\delta_c = 40\ \mu m$. This behaviour indicates that proper placement of the PDN is more important than the pitch of the PDN, when aiming to mitigate the effect of induced noise.

2.3 PDN Susceptibility to Induced Noise

The results relating to both the PDN pitch and the spatial positioning with respect to the inductive link are collectively compiled in this subsection. The pitch, $pitch_{PDN}$ and spatial distance, δ_c vary as in subsections 2.1 and 2.2, respectively.

A 3-D plot is produced for each topology, illustrating the induced noise behaviour against both the pitch and spatial position. The 3-D surface plots are illustrated in Fig. 5, where results relating to the interdigitated topology are presented in Fig. 5(a). The outcome for the paired type I and paired type II topologies are depicted in Figs. 5(b) and 5(c), respectively. The results are symmetric for negative values of the spatial distance, $\delta_c = [-d_{out}, 0]$.

For the interdigitated PDN topology, the induced noise amplitude significantly increases as the structure shifts closer to the centre of the inductor. For a distance of $\delta_c < 50\ \mu m$, the amplitude of the induced noise becomes prohibitive for typical power supply noise constraints. As the pitch of the PDN, $pitch_{PDN}$ increases, the spatial distance where a minimum induced noise is observed also increases.

Similar results are produced for the paired type I PDN topology. The induced noise levels for $\delta_c < 50\ \mu m$ render this topology unusable for typical power supply noise constraints, even for small widths, that lower the inductance of the PDN loop. Minimum noise can be observed for the full range of $pitch_{PDN}$, when the PDN is placed in such a position that the magnetic flux that couples with each PDN conductor has opposite polarities.

For the paired type II PDN topology, the overall noise behaviour is improved as the accumulated noise is below $V_{noise,acc} = 40\ mV$ for most of the simulated range of δ_c. As the pitch of the PDN increases, a rise in the induced noise amplitude is incurred, due to the increased inductance of the PDN loops. Nevertheless, there exist positions that minimise the induced noise, independently of the pitch size, such as for $pitch_{PDN} = 30\ \mu m$ and $\delta_c = 0\ \mu m$.

3. CASE STUDY: INDUCTIVE LINK ARRAY

Although the structure implemented so far is sufficient to demonstrate the harmful effects that an inductive link can have on P/G lines, a 3-D system that employs wireless inter-tier communication will utilise an array of inductors as in [7, 8] to support sufficient inter-tier bandwidth. Consequently, more than one inductor can couple with the long P/G wires, further aggravating the crosstalk noise.

3.1 Simulation Setup for Inductive Links

In the case of a high performance communication link, N inductors are assumed to be placed along the length of the power (or ground) loop and are simulated with HFSS [15] to model the induced noise. However, this approach significantly increases the simulation time particularly as noise for varying frequencies and δ_c or $pitch_{PDN}$ must be determined. To address this problem, the noise from a single inductor is determined where this inductor is placed successively at the location of N inductors. Using superposition, the noise from N inductors along the length of the loop can be described as

$$V_{n,array} = 2V_{noise,l} + (N-2)V_{noise,m}, \qquad (3)$$

where $V_{noise,l}$ is the noise due to the inductors placed at the edges of the loop and $V_{noise,m}$ is the noise produced by the remaining $N-2$ inductors coupled to the loop.

To verify the accuracy and simulation time gains of this approximation using (3), four inductors ($N = 4$) are assumed to couple to a power loop along the x-axis. The distance between subsequent inductors is given by $pitch = d_{out} + 30\ \mu m$, with the added space used to reduce crosstalk between the inductors during simultaneous operation. The noise due to a single inductor placed at specific locations along the x-axis is listed in column 2 of Table 1. This noise is compared with the noise reported in column 3 resulting by each of the four inductors where all four inductors are simulated. The low error of $\sim$2% and the reduced simulation time reported in the last row of Table 1 show that superposing the noise due to a single inductor which is successively placed along the power loop is a computationally effective approach.

Table 1: Noise Induced by Four Inductive Links

x-distance, 6 GHz	V_{noise} [mV]		Error [%]
	Single	Multiple	
$x = 0$	17.7	17.4	1.6
$x = pitch$	15.1	15.1	0
$x = 2 \times pitch$	15.0	15.0	0
$x = 3 \times pitch$	18.0	17.9	0.5
Simulation Time	$4 \times 1'\ 37''$	$16'$	—

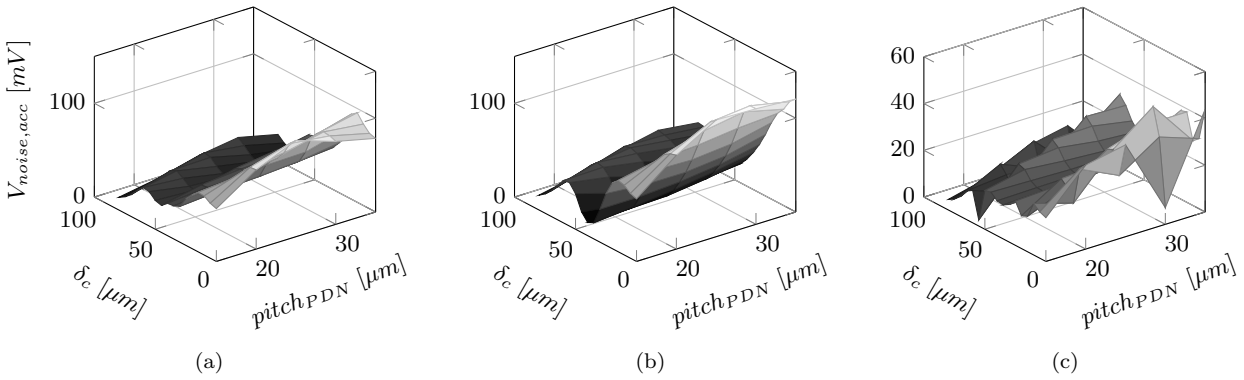

Figure 5: Noise induced by the inductive link for varying PDN physical parameters ($pitch_{PDN}$, δ_c), (a) interdigitated topology, (b) paired type I, and (c) type II topology, respectively.

3.2 Induced Noise by Inductive Link Arrays

The induced voltage due to the presence of inductive links on the power grid in the neighbouring tier appears as another component of power supply noise for contactless 3-D systems. To limit this noise a ground shield between the inductor and the PDN could be a valid approach, which would also improve the quality factor of the inductor and reduce the coupling with the substrate for the implemented frequency [16]. Nevertheless, a ground shield between the inductors of the inductive link would be detrimental for inter-tier coupling, as it would absorb the magnetic flux that forms the inter-tier link. Consequently, this approach is only applicable to face-to-face bonding. Alternatively, relocation of the P/G wires in a great distance from the inductors is another straightforward approach to avoid coupling. However, an increase in the IR-drop is inevitable. The tradeoff between these two different noise components (i.e., the crosstalk noise and IR-drop) is considered in this section to determine suitable locations for the P/G lines so that the overall power supply noise is restricted within acceptable limits.

An array of 4×4 inductive links is assumed, with a spacing of 30 μm between each link to reduce crosstalk during simultaneous transmission. The area of the array is 436 $\mu m \times$ 436 μm. Each inductive link consists of the transceiver and multiplexing circuits consuming a current of $I = 7.1\ mA$ [7], and are modelled as uniformly distributed current sources across the area of each inductor. The array is supplied by a power grid that utilizes the global and intermediate metal layers of a 65 nm technology node. The power loops on the topmost global layer are illustrated in Fig. 6 as solid lines. The power loops span the entire array connecting to $C4$ bumps placed symmetrically at the periphery of the array. A spacing of $s_{C4} = 150\ \mu m$ and diameter of $d_{C4} = 75\ \mu m$ are assumed for the bumps, satisfying the minimum size requirements for $C4$ pad placement [17]. The surrounding C4 bumps are assumed to supply the total current drawn by the array of inductors at nominal $V_{dd} = 1.1\ V$. The design of the grid results in a worst case IR-drop of 20 mV to 39 mV, depending on the PDN topology and geometry, which satisfies a 10% V_{dd} power supply noise constraint assumed in this case study.

The power loops are connected to each of the supply pads through a global wire, modelled by the resistance R_{dist}. This resistance is used to capture the added IR-drop as the power lines are shifted away from the pads, also changing the overall magnetic flux that couples with the PDN. To include both the inductive link noise from (3) and the additional IR-drop due to relocation of the P/G wires, R_{dist} is also described as a function of δ_c, yielding a sheet resistance of $R_{dist,pm} = 23.7\ m\Omega/\mu m$. For $\delta_c = -77\ \mu m$ (or -($d_{out}/2 + d_{C4}/2$)) the power lines are aligned with the pads at the top of the array and there is no added resistance ($R_{dist} = 0$). As the wires are shifted away from the pads, R_{dist} increases, reaching a maximum of 3.8 Ω for $\delta_c = d_{out}/2 + d_{C4}/2$. Note that increasing the fineness of the grid to mitigate the added IR-drop due to R_{dist} results in a grid with prohibitively high induced noise levels due to the inappropriate positions of specific P/G wires.

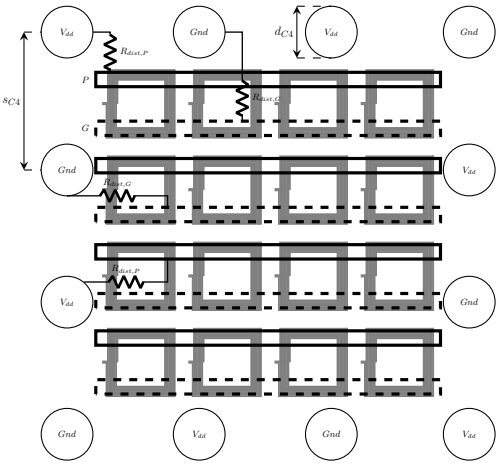

Figure 6: Inductive link array and P/G loops connected to $C4$ supply and ground pads. Power and ground wires are depicted by solid and dashed lines, respectively. Not all of the metal layers are shown for the sake of clarity.

Results for an array of the 4×4 grid of inductive links are reported in Table 2. Several cases are listed for each PDN topology, for pairs of ($pitch_{PDN}$, δ_c) that can provide acceptable noise levels for a constraint of 10%. The induced noise $V_{n,array}$ is given by (3), considering the induced noise both on the power and ground loops.

Concerning the interdigitated PDN topology, results indicate a higher sensitivity to induced noise compared to the paired topologies. Even in the spatial positions where the induced noise is minimum, the added IR-drop noise due to R_{dist} for the power and ground loops increases the total noise to prohibitive amplitudes. Overall, a minimum noise of 13.9% V_{dd} is noted, surpassing the 10% noise constraint.

Alternatively, both paired topologies present pairs of

Table 2: Total Accumulated Noise for Different PDN Geometries

Topology	Geometry		$V_{noise,acc}$ $[mV]$	IR-Drop $[mV]$		Total $[mV]$	Overall Noise
	$pitch_{PDN}$ $[\mu m]$	δ_c $[\mu m]$		Power Loop	Ground Loop		
Interdigitated	45	-45	108	5.25	18.1	131.3	13.9% (Fail)
	45	70	92	52.8	61.3	153.8	18.1% (Fail)
Paired Type I	45	-40	56.1	11.1	14.1	81.3	*7.3% (Pass)*
	60	-40	59.2	14.2	6.1	79.5	*7.2% (Pass)*
	105	-50	69.2	35.2	27.7	132.1	12% (Fail)
	105	50	69.2	56.2	63.7	189.1	17.1% (Fail)
Paired Type II	45	-35	58.1	9.7	27.2	95	*8.6% (Pass)*
	75	-45	65.3	16.7	26.3	108.3	*9.8% (Pass)*
	90	0	28.5	10.8	45.5	84.8	*7.7% (Pass)*

($pitch_{PDN}$, δ_c), where the overall noise is below the specified limit. For the type I topology, a noise level of 7.1% is achieved, well below the specified limit. The overall noise mainly occurs due to the induced noise, while the added IR-drop is relatively small for the accepted spatial positions. For the type II topology, the ground loop IR-drop significantly increases the overall noise, due to the larger distance from the pads. Nevertheless, locations exist where the overall noise level is tolerable, such as the positions shown in Fig. 6, with an overall noise of 7.7%.

4. CONCLUSION

The impact of inductive link interfaces on different power delivery networks is investigated. Noise induced by the inductive link and the IR-drop on the P/G wires, for interdigitated, paired type I and paired type II PDN topologies is explored based on the area that couples with the inductor and the spatial position. Results indicate that the increased inductance of specific topologies leads to higher levels of noise, due to the increased coupling. However, the spatial position is the primary factor affecting the induced noise amplitude. Analysis suggests that the interdigitated topology is the most susceptible to induced noise, as the lowest induced noise amplitude is 92 mV. Alternatively, paired topologies exhibit placement locations where the induced noise is considerably lower, and consequently are better candidates for power delivery in 3-D systems that employ inductive links.

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