Enhanced Average-Value Modelling of Interleaved DC-DC Converters Using Sampler Decomposition

DOI:
10.1109/TPEL.2016.2559449

Document Version
Accepted author manuscript

Enhanced Average-Value Modelling of Interleaved DC-DC Converters Using Sampler Decomposition

Alejandro Villarruel-Parra, *Member, IEEE,* and Andrew J. Forsyth, *Senior Member, IEEE*

***Abstract*—To provide a basis for controller design in interleaved dc-dc converters, an improved small-signal averaged model is presented. Sampler decomposition techniques are used to represent the interleaved operation of the individual control loops within the converter. The resultant model reveals interaction effects and instability phenomena that are not predicted by a simple non-interleaved model, and which impose significant restrictions on the selection of control parameters. The model is validated by detailed simulations and experimental results from a digitally controlled, dual-interleaved boost converter.**

***Index Terms*—Average current, control, DC-DC converters, interleaved converters, modelling, small-signal.**

I. Introduction

Interleaved DC-DC converters have been widely adopted in power supplies for microprocessors and communication systems, high-power-factor rectifiers, and more recently in the power-train of electric vehicles. The parallel-connected channels of an interleaved converter, Fig. 1, use the same topology, component values and switching frequency, but their switching cycles are mutually delayed, providing ripple cancellation at input and output. With two interleaved channels, the switching delay is half the switching period, the input and output ripple frequency is doubled and the ripple-current amplitude is reduced, allowing smaller filter capacitors to be used. Also, the current is distributed across multiple devices and components, reducing thermal load. For instance, the dual-interleaved boost converter, Fig. 2, is one of the topologies that has been proposed to interface fuel-cells, super-capacitors, battery banks and traction drives within the power train of an electric vehicle [1-3], where power levels could be up to 100 kW. The circuit in Fig. 2 uses an inter-phase transformer to combine the voltages of the two switching legs and a single inductor, and is considered to offer a reduced magnetic component weight compared with a two-inductor alternative [4].

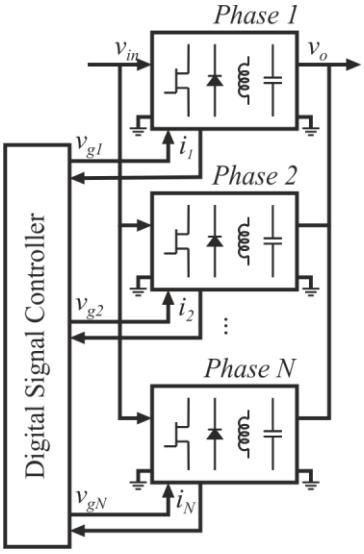

Fig. 1. Interleaved DC-DC converter.

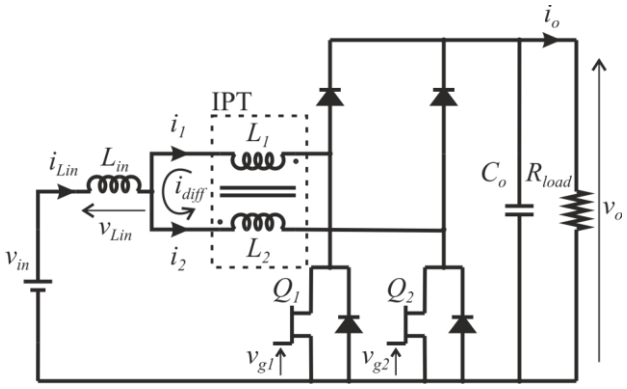

Fig. 2. Dual-interleaved boost converter with inter-phase transformer.

To prevent current imbalances between parallel phases, for example due to second-order effects such as mismatches in switching times and circuit impedances, some form of current-control is normally required in interleaved converters. With a small number of phases, peak or averaged current-mode control can be used for each phase, with a common current reference formed by the output voltage control loop. Some of the solutions to balance the phase-currents for systems with a high number of phases include: operating the parallel converters in discontinuous conduction mode, [3]; balancing the phase-currents using digital algorithms, [5, 6]; and non-linear control methodologies [7].

Manuscript received on November 29, 2015; revised January 6, 2016 and February 29, 2016; accepted April 11, 2016. Date of current version April 17, 2016.

A. Villarruel-Parra, was with the School of Electrical and Electronic Engineering, The University of Manchester, Manchester, M13 9PL, U.K. He is now with the School of Mechanical and Electrical Engineering, IPN, Mexico City, 04430, Mexico (e-mail: vipaal.22@gmail.com)

A. J. Forsyth is with the School of Electrical and Electronic Engineering, The University of Manchester, Manchester, M13 9PL, U.K. (e-mail: andrew.forsyth@manchester.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier

Averaging techniques have been used by several authors for the dynamic analysis and control design of interleaved converters, for example state-space averaging and circuit averaging [8-12], however, these approaches do not account for the interleaved operation of the converter phases, creating the possibility that unexpected interactions and instability phenomena could occur. For instance, the stability analysis carried out in [13] for a dual interleaved buck converter demonstrated using non-linear maps that slow-scale instabilities arise in the system due to the interaction of the converter phases, which are not predicted by an averaged model. Sampled-data techniques provide an alternative to averaged models, they incorporate both slow-scale and switching-frequency related fast-scale effects and can include interleaved operation [14], however the analysis complexity makes these models very difficult to use in many cases.

In this paper, multi-rate data-sampled theory is used to enhance the small-signal averaged model of interleaved converters to include the interactions of the converter phases, and provide a theoretical basis for the direct digital design of the current control-loops. The modelling technique is initially presented in a general fashion for an *N*-phase, average current-mode controlled converter. Based on this theory, a modelling example is presented for a dual-interleaved boost converter with inter-phase transformer. The model is validated using time-domain simulations and practical results from a multi-kW prototype, showing how the interleaved operation introduces instability regions that are not predicted by a non-interleaved averaged model.

II. SMALL-SIGNAL MODELLING OF INTERLEAVED CONVERTERS WITH AVERAGE-CURRENT MODE CONTROL

A. Operation of interleaved converters using digital average-current mode control

To ensure an equal distribution of the current amongst the converter phases, a separate current feedback loop per converter is typically used as illustrated in Fig. 1. A number of digital current control methods for single-phase DC-DC converters have been proposed in the literature, showing that by strategic synchronization of the current sampling instants with specific events of the digital Pulse Width Modulator (PWM) it is possible to acquire the peak-current, valley-current or the average-current in each feedback loop [15]. Fig. 3 shows waveforms to illustrate the sampling of the average-current. The digital PWM counter is configured in count up-down mode, generating a triangular waveform. The digital modulator output is turned-on when the counter crosses the modulating signal during the count down. In contrast, when the counter crosses the modulating waveforms during the count up the output signal is turned-off. The modulating signal is updated once per cycle when the counter reaches its maximum value, therefore the switching instants of the PWM output waveforms are symmetrical with respect to the minimum-value of the digital triangular waveform. From this symmetry it follows that if the feedback current sampling occurs when the counters are at their minimum value, the current sample will be located in the middle of the transistor conducting periods and will be the local-average value of the phase current. This method is termed triangular-carrier modulation with symmetric on-time [15, 16]. To achieve the interleaving of the PWM waveforms for each converter, the digital counters of the feedback-loops are delayed with respect to each other by *T/N*, where *T* is the switching period and *N* the number of phases.

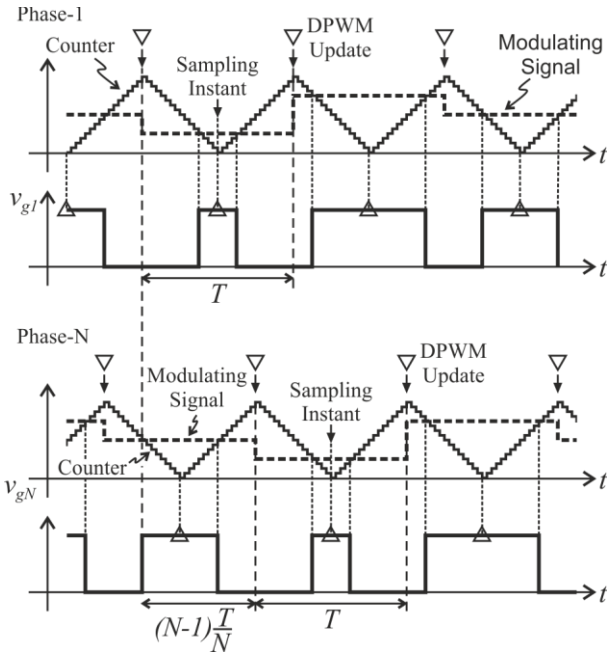

Fig. 3. Control waveforms of an interleaved DC-DC converter with digital average-current control.

B. Closed-loop, small-signal model of the system

Fig. 4 shows the block diagram of an average current-mode controlled, interleaved converter, assuming that the converter and controller can be represented by linear transfer-functions. Each converter phase is represented by an averaged, linearized transfer function which relates small changes in the transistor duty-ratios $\tilde{d}_1(s)$, $\tilde{d}_2(s)$, …, $\tilde{d}_N(s)$ to the small changes in the phase-currents $\tilde{i}_1(s)$, $\tilde{i}_2(s)$, …, $\tilde{i}_N(s)$. The analog-to-digital conversion of the phase currents is modelled by the sampler devices S_1, S_2, …, S_N which operate in an interleaved manner. Since both the reference and phase currents in each feedback loop are sampled synchronously, a single sampler located after the summing junctions is used. The quantization non-linearity of the ADC and the measurement and conditioning delays are disregarded. The digital compensators on each phase, $C(z)$, are represented in the Laplace-domain using the transfer function $C(s)$ followed by the corresponding phase sampler. The delay associated with the digital compensator, $e^{-\tau s}$, is identical for each control loop. Finally, the digital modulator operation is represented by the zero-order-hold extrapolator transfer function, [15, 17]:

$$G_{h0}(s) = \frac{\left(1 - e^{-sT}\right)}{s} \tag{1}$$

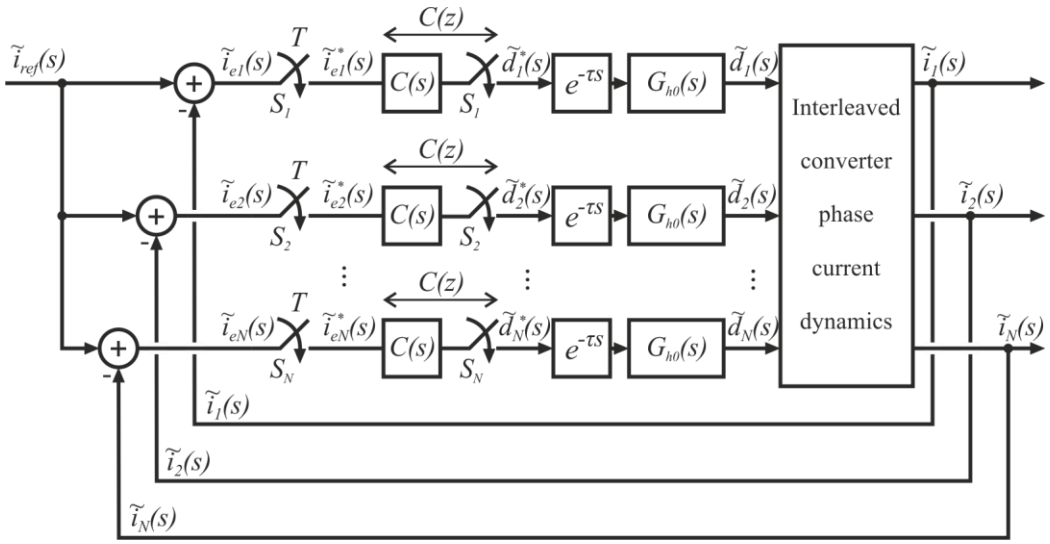

Fig. 4. Block diagram of a digital average-current mode controlled interleaved DC-DC converter.

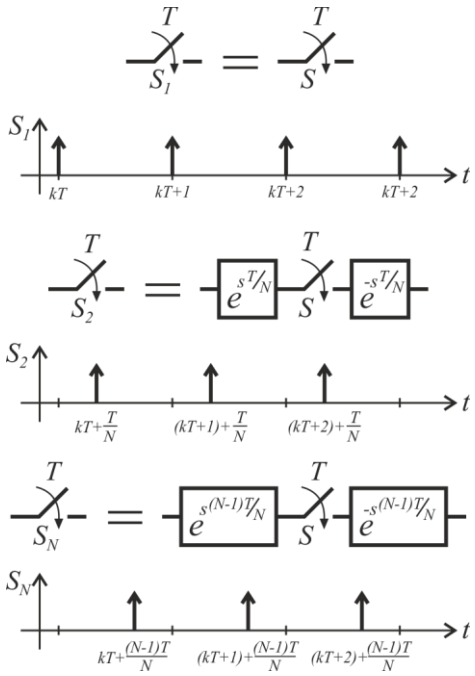

Fig. 5. Equivalent sampler representation using the sampler decomposition technique.

This representation may be replaced by more elaborated small-signal models such as that introduced in [15].

C. Modelling of the interleaved operation of the feedback loops

Assuming the sampler S_1 in Fig. 4 as the reference, the delayed samplers S_2 to S_N may be represented in terms of S_1 preceded by a time-advance unit of $+n(T/N)$ and followed by a time-delay unit of $-n(T/N)$, where $n = 1,2,\ldots,(N-1)$, as illustrated in Fig. 5. This technique is known as the sampler decomposition method [17, 18]. Upon substitution of the equivalent samplers in Fig. 4, the system may be analysed using z-transforms.

III. Modelling Example: Dual Interleaved Boost Converter with Inter-Phase Transformer

A. Small-signal averaged model of the power stage

Fig. 2 shows the schematic diagram of the dual interleaved boost converter with IPT. By substitution of the converter switch networks with the averaged PWM switch model, the DC and averaged small-signal model of the converter shown in Fig. 6 is obtained, where the IPT has been modelled using self and mutual inductances. Using Fig. 6, the small-signal model of the converter can be represented in the state-space form as:

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A_{av}}\tilde{\mathbf{x}} + \mathbf{B_{av}}\tilde{\mathbf{u}} \tag{2}$$

where the state vector, $\tilde{\mathbf{x}}$, comprises the small-signal components of the phase currents in the IPT windings and the voltage across the output capacitor: $\tilde{\mathbf{x}} = [\tilde{i}_1 \;\; \tilde{i}_2 \;\; \tilde{v}_o \;]^T$; and the input vector, $\tilde{\mathbf{u}}$, contains the control inputs for each phase and the load disturbance current: $\tilde{\mathbf{u}} = [\;\tilde{d}_1 \;\; \tilde{d}_2 \;\; \tilde{i}_z \;]^T$. The matrices $\mathbf{A_{av}}$ and $\mathbf{B_{av}}$ in (2) may be expressed as:

$$\mathbf{A_{av}} = \begin{bmatrix} -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{(1-D)(L_c+L_m)}{L_{Tot}} \\ -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{(1-D)(L_c+L_m)}{L_{Tot}} \\ \dfrac{(1-D)}{C_o} & \dfrac{(1-D)}{C_o} & -\dfrac{1}{R_{load}C_o} \end{bmatrix} \tag{3}$$

$$\mathbf{B_{av}} = \begin{bmatrix} \dfrac{V_{in}(L_{in}+L_c)}{L_{Tot}(1-D)} & -\dfrac{V_{in}(L_{in}-L_m)}{L_{Tot}(1-D)} & 0 \\ -\dfrac{V_{in}(L_{in}-L_m)}{L_{Tot}(1-D)} & \dfrac{V_{in}(L_{in}+L_c)}{L_{Tot}(1-D)} & 0 \\ -\dfrac{V_{in}}{2R_{load}C_o(1-D)^2} & -\dfrac{V_{in}}{2R_{load}C_o(1-D)^2} & \dfrac{1}{C_o} \end{bmatrix} \tag{4}$$

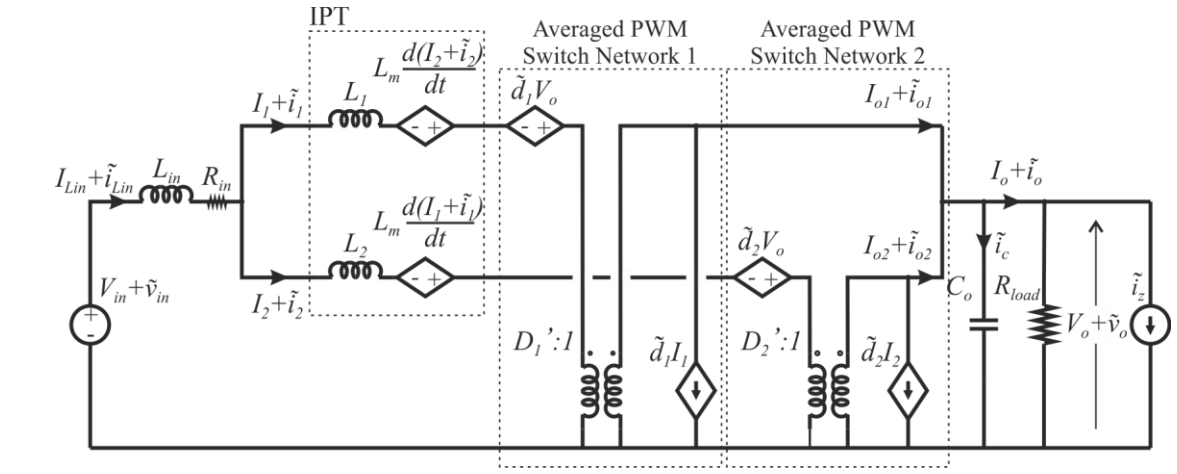

Fig. 6. DC and small-signal model of the dual-interleaved boost converter with IPT.

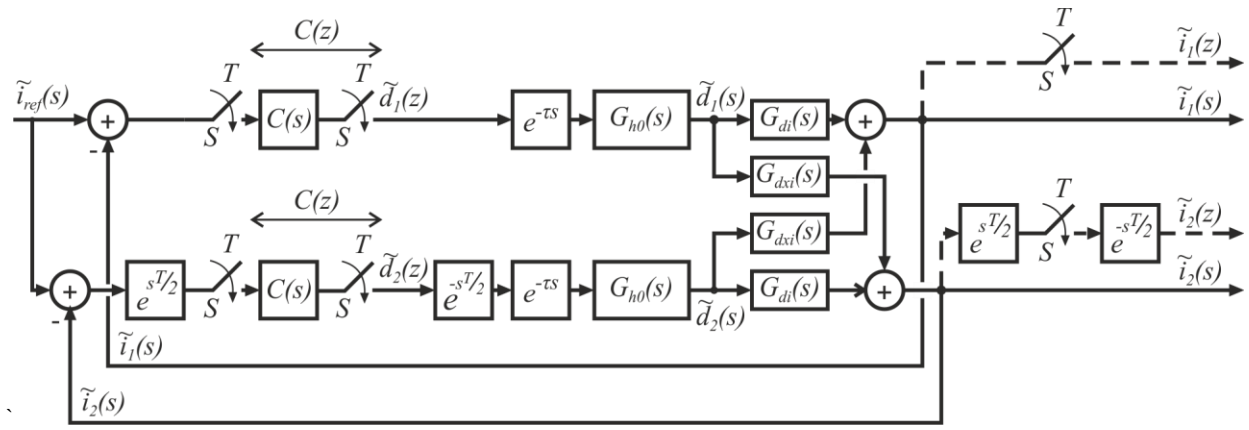

Fig. 7. Block diagram of the dual-interleaved boost converter with IPT with digital average-current control.

where $L_c = L_1 = L_2$, L_m is the mutual inductance between L_1 and L_2, and $L_{Tot} = 2L_{in}(L_c+L_m)+(L_c^2-L_m^2)$. By transforming into the Laplace-domain, the small-signal transfer functions between $\tilde{d}_1(s)$ and $\tilde{d}_2(s)$, and the converter phase-currents, $\tilde{i}_1(s)$ and $\tilde{i}_2(s)$, may be determined in the form:

$$\tilde{i}_1(s) = G_{d1i1}(s)\tilde{d}_1(s) + G_{d2i1}(s)\tilde{d}_2(s) \quad (5)$$

$$\tilde{i}_2(s) = G_{d1i2}(s)\tilde{d}_1(s) + G_{d2i2}(s)\tilde{d}_2(s) \quad (6)$$

where $G_{d1i1}(s) = G_{d2i2}(s)$ and $G_{d1i2}(s) = G_{d2i1}(s)$ since the components that comprise the converter phases are assumed identical. The transfer functions $G_{d1i1}(s)$ and $G_{d1i2}(s)$ can be found in the Appendix.

B. Small-signal averaged model of the converter with current feedback control

The closed-loop, small-signal model of the dual-interleaved boost converter may be derived from the generalized system diagram in Fig. 3 by substitution of the duty-ratio to phase-current transfer functions, (5) and (6), as shown in Fig. 7, where $G_{d1i1}(s) = G_{d2i2}(s) = G_{di}(s)$ and $G_{d1i2}(s) = G_{d2i1}(s) = G_{dxi}(s)$. Furthermore, the sampler S_2 has been replaced by its equivalent representation in terms of S_1 using time advance and time delay units equal to $e^{+sT/2}$ and $e^{-sT/2}$, as described in Section II. Closed-loop transfer functions for the phase currents $\tilde{i}_1(z)/\tilde{i}_{ref}(z)$ and $\tilde{i}_2(z)/\tilde{i}_{ref}(z)$, may be determined by analysis of Fig. 7. First, considering the two feedback loops, expressions may be written for $\tilde{d}_1(z)$ and $\tilde{d}_2(z)$:

$$\tilde{d}_1(z) = C(z)\Big[\mathrm{Z}\left\{\tilde{i}_{ref}(s)\right\} - \tilde{d}_1(z)\mathrm{Z}\left\{e^{-\tau_s}G_{h0}(s)\mathrm{G}_{di}(s)\right\} - \tilde{d}_2(z)\mathrm{Z}\left\{e^{-sT/2}e^{-\tau_s}G_{h0}(s)\mathrm{G}_{dxi}(s)\right\}\Big] \quad (7)$$

$$\tilde{d}_2(z) = C(z)\Big[\mathrm{Z}\left\{e^{sT/2}\tilde{i}_{ref}(s)\right\} - \tilde{d}_1(z)\mathrm{Z}\left\{e^{sT/2}e^{-\tau_s}G_{h0}(s)\mathrm{G}_{dxi}(s)\right\} - \tilde{d}_2(z)\mathrm{Z}\left\{e^{-\tau_s}G_{h0}(s)\mathrm{G}_{di}(s)\right\}\Big] \quad (8)$$

where Z{F(s)} denotes the z-transform of F(s). Considering the fictious-sampler outputs in Fig. 7:

$$\tilde{i}_1(z) = \tilde{d}_1(z)\mathrm{Z}\left\{e^{-\tau_s}G_{h0}(s)\mathrm{G}_{di}(s)\right\} + \tilde{d}_2(z)\mathrm{Z}\left\{e^{-sT/2}e^{-\tau_s}G_{h0}(s)\mathrm{G}_{dxi}(s)\right\} \quad (9)$$

$$\tilde{i}_2(z) = \tilde{d}_1(z)\mathrm{Z}\left\{e^{sT/2}e^{-\tau_s}G_{h0}(s)\mathrm{G}_{dxi}(s)\right\} + \tilde{d}_2(z)\mathrm{Z}\left\{e^{-\tau_s}G_{h0}(s)\mathrm{G}_{di}(s)\right\} \quad (10)$$

Eliminating $\tilde{d}_1(z)$ and $\tilde{d}_2(z)$ from (7) and (8) using (9) and (10), the closed-loop transfer functions of the system are obtained:

$$G_{i1iref}(z) = \frac{\tilde{i}_1(z)}{\tilde{i}_{ref}(z)} =$$

$$\frac{C(z)G_{di}(z) + C(z)G_{dxi\phi}(z) + C^2(z)\left[G_{di}{}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2C(z)G_{di}(z) + C^2(z)\left[G_{di}{}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]} \tag{11}$$

$$G_{i2iref}(z) = \frac{\tilde{i}_2(z)}{\tilde{i}_{ref}(z)} =$$

$$\frac{C(z)G_{di}(z) + C(z)G_{dxi\theta}(z) + C^2(z)\left[G_{di}{}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2C(z)G_{di}(z) + C^2(z)\left[G_{di}{}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]} \tag{12}$$

The z-transforms of the constituent transfer functions of (11) and (12) are defined as:

$$G_{di}(z) = \mathrm{Z}\left\{e^{-\tau s}G_{h0}(s)\mathrm{G}_{di}(s)\right\} = \mathrm{Z}_m\left\{G_{h0}(s)\mathrm{G}_{di}(s)\right\}\Big|_{m=1-(\tau/T)} \tag{13}$$

$$G_{dxi\phi}(z) = \mathrm{Z}\left\{e^{-sT/2}e^{-\tau s}G_{h0}(s)\mathrm{G}_{dxi}(s)\right\} = \mathrm{Z}_m\left\{G_{h0}(s)\mathrm{G}_{dxi}(s)\right\}\Big|_{m=1-(1/2+(\tau/T))} \tag{14}$$

$$G_{dxi\theta}(z) = \mathrm{Z}\left\{e^{sT/2}e^{-\tau s}G_{h0}(s)\mathrm{G}_{dxi}(s)\right\} = z\,\mathrm{Z}_m\left\{G_{h0}(s)\mathrm{G}_{dxi}(s)\right\}\Big|_{m=(1/2-(\tau/T))} \tag{15}$$

where the z-transform of the transfer functions multiplied by fractional time-delay and time-advance units are evaluated using the modified z-transform method [17].

Inspection of (11) and (12) reveals that an open-loop transfer function is not immediately identifiable, complicating the use of traditional compensator design procedures such as Bode-plots. Following a similar method, the closed-loop transfer functions may also be derived assuming synchronous operation of the samplers S_1 and S_2 in Fig. 7, resulting in:

$$G_{i1iref}(z) = G_{i2iref}(z) = \frac{C(z)\left[G_{di}(z) + \mathrm{G}_{dxi}(z)\right]}{1 + C(z)\left[G_{di}(z) + \mathrm{G}_{dxi}(z)\right]} \tag{16}$$

where:

$$G_{dxi}(z) = \mathrm{Z}\left\{e^{-\tau s}G_{h0}(s)\mathrm{G}_{dxi}(s)\right\} = \mathrm{Z}_m\left\{G_{h0}(s)\mathrm{G}_{dxi}(s)\right\}\Big|_{m=\tau} \tag{17}$$

In contrast with the interleaved transfer functions (11) and (12), (16) is greatly simplified and also an open-loop transfer function is easily identifiable.

TABLE I
CONVERTER COMPONENTS AND PARAMETERS

Component	Symbol	Value
Input Inductance	L_{in}	5.12 µH
Input inductor stray resistance	R_{in}	0.029 Ω
IPT self-inductance	L_1, L_2	75.14 µH
IPT mutual inductance	L_m	74.9 µH
IPT coupling coefficient	k	0.997
Output capacitance	C_o	45 µF
Switching frequency	f	30 kHz
Switching/sampling period	T	33.33 µs
Computational delay	τ	T/2

IV. COMPARISON BETWEEN INTERLEAVED AND NON-INTERLEAVED MODELS

A. Performance of the phase-current to step changes

To illustrate the improved accuracy of the interleaved model a set of small step responses is presented in Fig. 8 for one of the phase currents in a dual-interleaved boost converter. SABER simulation results, using a detailed switched model that includes the interleaved sampling of the phase currents in the digital controller, are shown in the first column, whilst the second and third columns show the transfer function predictions (11) and (16) from the interleaved and the non-interleaved models respectively. The SABER and small-signal models exclude all losses except R_{in}, the series resistance of the input inductor. The converter parameters are listed in Table I and the same values are used for the practical validation in Section V. In the first row in Fig. 8, the PI compensator integral gain is varied from 1 to 20, in the second row, the steady-state phase-current is increased from 40 A to 120 A, finally, in the last row, the input voltage is varied from 40 V to 150 V.

The results from the transfer functions show a close correspondence with the simulation results with virtually-identical rise-time, natural frequency (5 kHz) and damping ratio. However, a lower, lightly-damped natural frequency (approximately 850 Hz) is evident in many of the responses from the interleaved model, but is completely absent in the non-interleaved model results. The same natural frequency is also observable in the SABER results. The top set of responses in Fig. 8 with integral gain $K_i = 20$, show unstable behaviour in the SABER simulation and interleaved model, whilst the non-interleaved model is completely stable. The lower frequency natural mode in the i_1 phase current was found to occur in anti-phase in the i_2 phase current, but was unobservable in the input inductor current. The additional high-frequency oscillations that occur in the SABER simulation results were attributed to PWM quantization and current-sampling effects.

B. Pole-zero maps and frequency response

To compare the transfer functions obtained from the proposed interleaved model and the standard non-interleaved model, z-domain pole-zero maps are shown in Fig. 9 for the closed-loop, reference-to-phase-1 current transfer function for

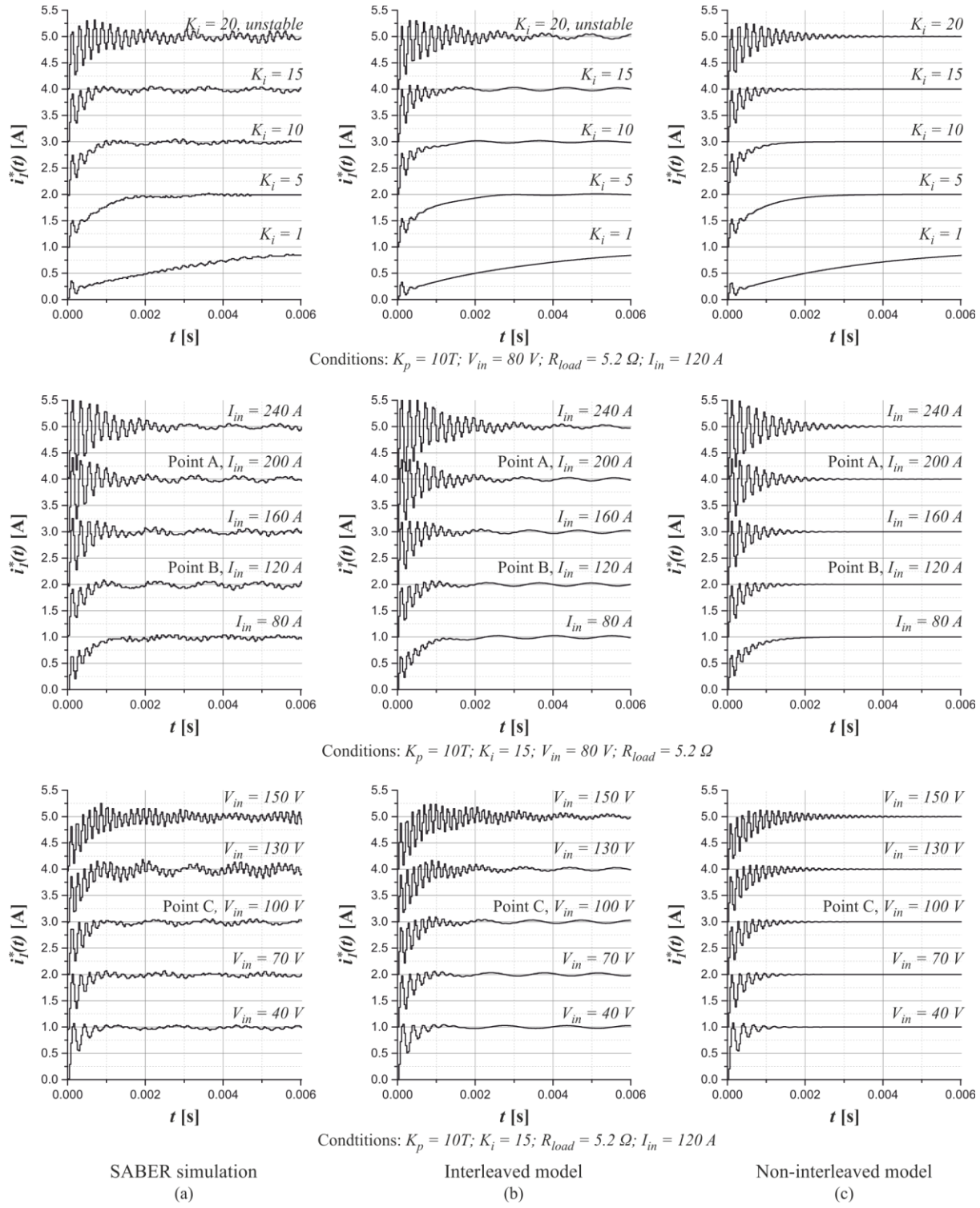

Fig. 8. Time-domain response of the phase-*1* current of the (a) SABER switched model, (b) the interleaved small-signal model and (c) the non-interleaved/conventional small-signal model to small step-increments in the reference input.

the operating condition of V_{in} = 80 V, I_{in} = 200 A, and R_{load} = 5.2 Ω with PI controller gains K_p = 10(T) and K_i = 15. This operating condition corresponds with the plot labelled Point A in Fig. 8. The main difference between the plots is that the interleaved model contains an additional pair complex poles, which are just inside the unit circle and cancelled by complex zeros, indicating a natural mode that is unobservable in the phase-current transfer function. The natural frequency of the poles is around 850 Hz and they are responsible for the lightly-damped oscillation in the transient responses in Fig. 8

Finally, Fig. 10 shows the closed-loop, reference-to-phase-1 current frequency response from the interleaved model compared with the result from a SABER switched simulation obtained using the SABER Time Domain System Analyser

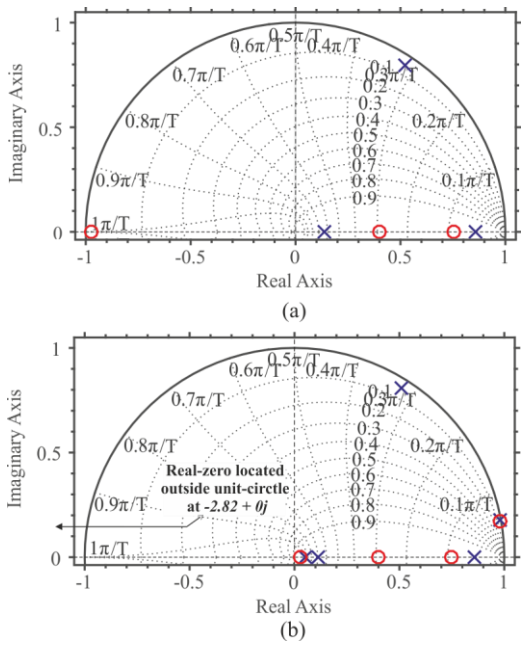

Fig. 9. Pole-zero maps from the closed-loop, reference-to-phase-*1* current transfer function, $G_{i1iref}(z)$, from (a) the non-interleaved small-signal model, and (b) the interleaved small-signal model. V_{in} = 80 V, I_{in} = 200 A and R_{load} = 5.2 Ω corresponding to Point A, Fig. 8. $K_p = 10(T)$ and K_i = 15.

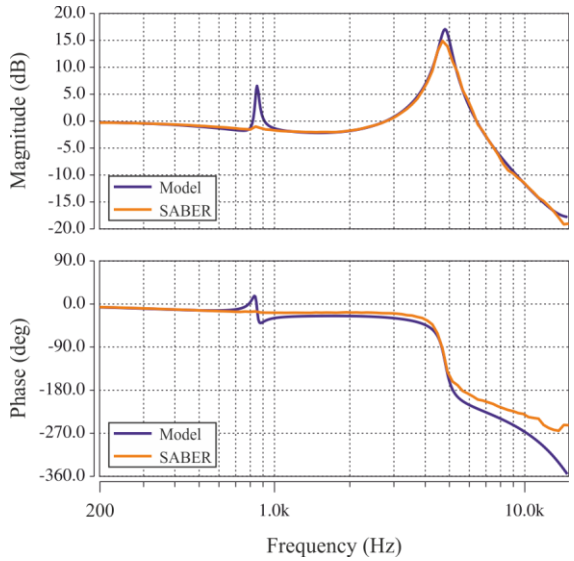

Fig. 10. Comparison of the frequency response of the closed-loop, reference-to-phase-*1* current transfer function, $G_{i1iref}(z)$, obtained from the interleaved small-signal model and the switched simulation. V_{in} = 80 V, I_{in} = 200 A and R_{load} = 5.2 Ω corresponding to Point A, Fig. 8. $K_p = 10(T)$ and K_i = 15.

tool. The same parameters were used for the pole-zero maps in Fig 9. In general the two sets of data correspond closely, providing further validation of the model, however, the cancelled complex poles are much less evident in the SABER results.

C. Root-loci of the system and stability maps

To provide further insight into the system dynamics and stability, the sensitivity of the system poles to parameter variations was examined using (11) and (12). The parameters included the input-voltage, load-resistance and PI compensator gains.

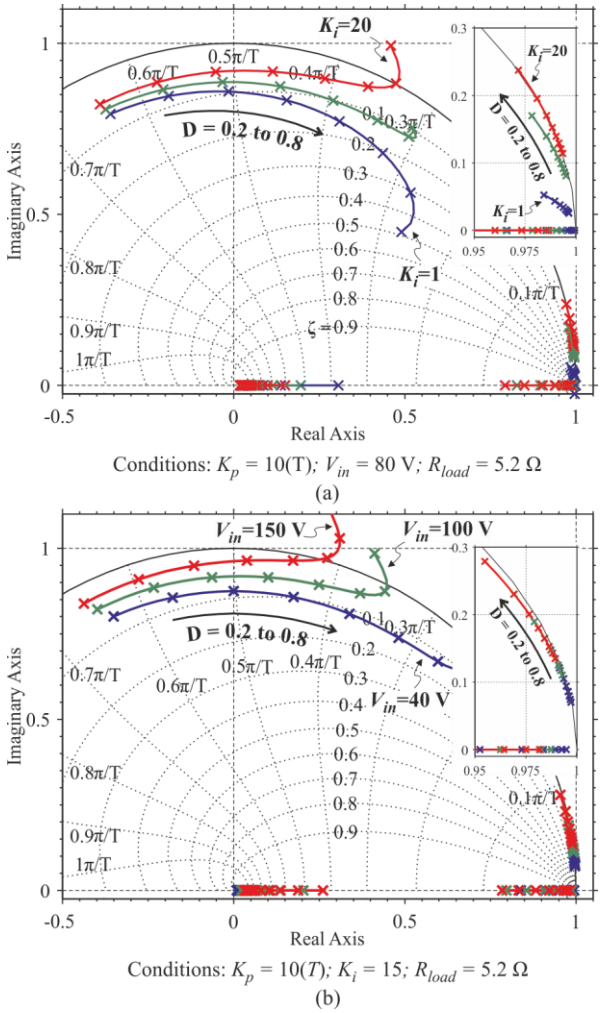

Fig. 11. Sensitivity of the pole trajectories from the interleaved model to variations in (a) the integral gain, K_i = 1, 10 and 20; and (b) the input-voltage, V_{in} = 40 V, 100 V and 150 V.

Fig. 11(a) shows the trajectories of the system poles when D is varied from 0.2 to 0.8 for values of K_i of 1, 10 and 20 whilst the proportional gain is fixed at $K_p = 10(T)$. The plot shows a pair of low-frequency complex poles located in the vicinity of the +1 point, which are not present in the non-interleaved model of the system, (16), and are attributed to the squared term of the compensator transfer-function found in the denominator of (11) and (12). Also, a pair of high-frequency complex poles can be identified in the root-locus, which were also observed in the root-locus of the non-interleaved model. As the duty-ratio is increased the high-frequency poles tend to move around the unit circle, with K_i = 1 the poles move towards the real axis, but with higher values of K_i, for example K_i = 20, the poles turn back on themselves and move outside the unit circle. The low-frequency complex poles, on the other hand, tend to move around the unit circle and away from the real-axis, in the case of K_i = 20 the poles lie on the unit circle, but are inside the unit circle with lower values of K_i. Fig 11(b) shows a similar pattern in the pole trajectories for different input voltages. The high-frequency poles tend to become unstable for higher input-voltages and higher duty-ratios, whilst the low-frequency poles remain close to the unit circle.

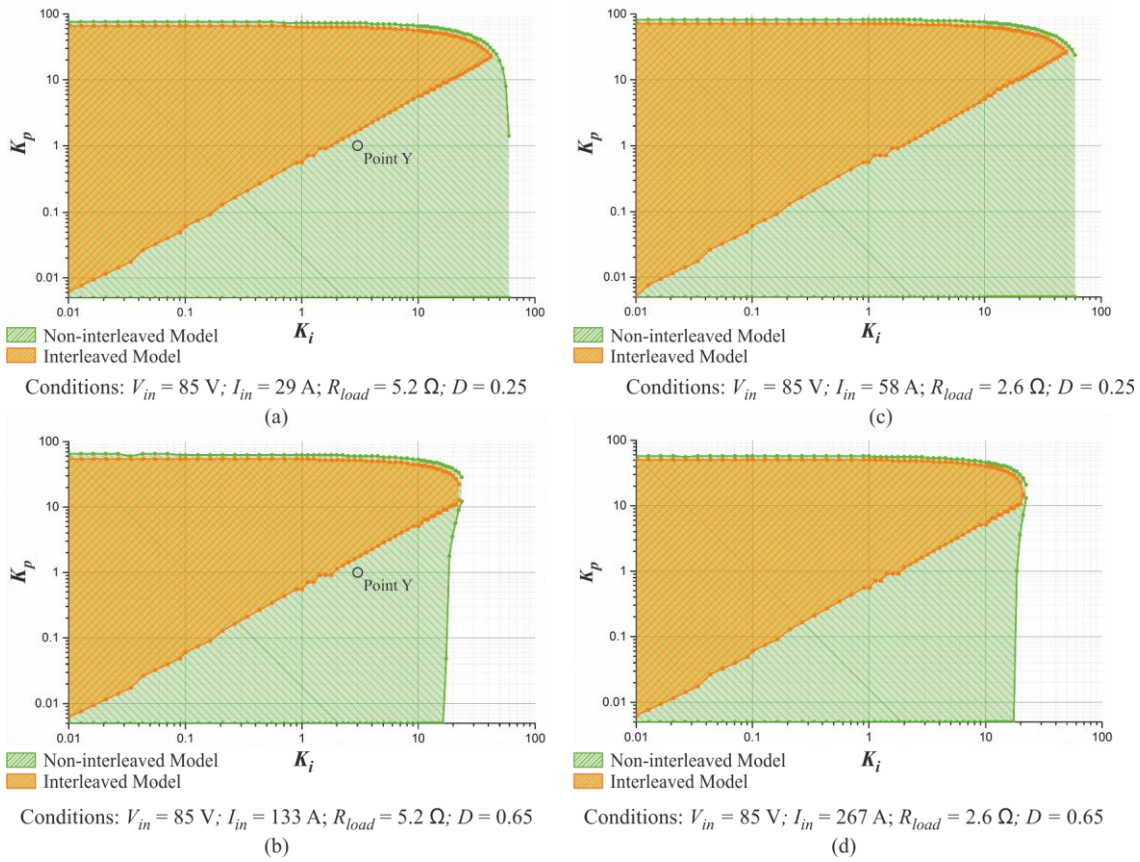

Fig. 12. Comparison of the stability-range predicted by the interleaved and the conventional/non-interleaved model when a digital PI compensator is used to regulate the current-feedback control-loops at different points of operation.

The significant difference in the converter stability range predicted by the interleaved and non-interleaved models is illustrated by the shaded regions in the K_p/K_i controller design space, Fig. 12. The dark shaded regions indicate the stable combinations of K_p and K_i predicted by the interleaved model, whilst the lighter shaded areas are the additional regions where the non-interleaved/conventional model suggests that the system operation will be stable. The regions were generated numerically by calculation of the system poles over a systematic sweep of the controller parameters using (11) and (16). The plots indicate that the conventional model seriously over predicts the converter stability limits, particularly for higher values of K_i and lower values of K_p.

V. Experimental Prototype and Model Validation

Experimental validation of the interleaved converter model was undertaken using a multi-kW dual-interleaved boost converter with IPT, Fig. 2, which had been developed for an electric vehicle application. The IGBT-based converter operated at 30 kHz with output-voltages up to 250 V. A Texas Instruments TMS320F28335 was used to implement the digital, interleaved, phase current control and PWM generation. The phase currents were measured using Hall-effect sensors, and the system operated without an output voltage control loop. The converter parameters are listed in Table I, and are identical to the values used in the simulations and predictions in Section IV. Fig. 13 shows a comparison of

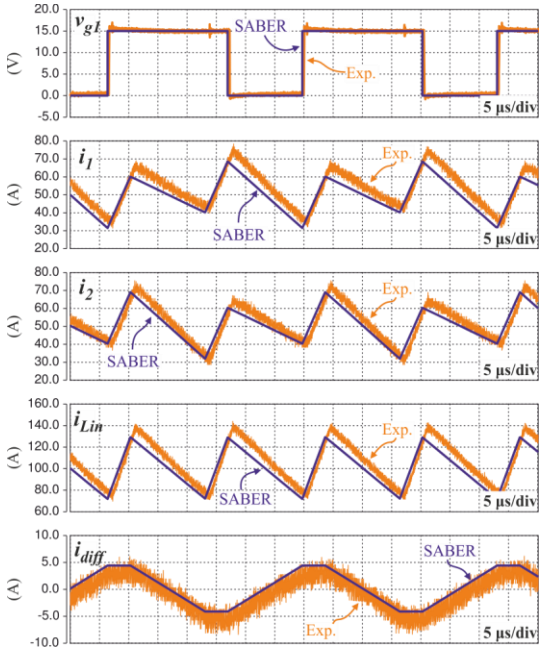

Fig. 13. Simulated and experimental waveforms of the DIBC with IPT under steady-state conditions. V_{in} = 80 V, R_{load} = 5.2 Ω, I_{in} = 100 A, D = 0.61, V_o = 205 V and P_o = 8 kW.

the steady-state waveforms v_{g1}, i_1, i_2, i_L and i_{diff} (calculated as $(i_2 - i_1)/2$) obtained from the simulation and the experimental test-rig which confirm the accuracy of the simulation results. Small signal step responses (15 %) in the current reference,

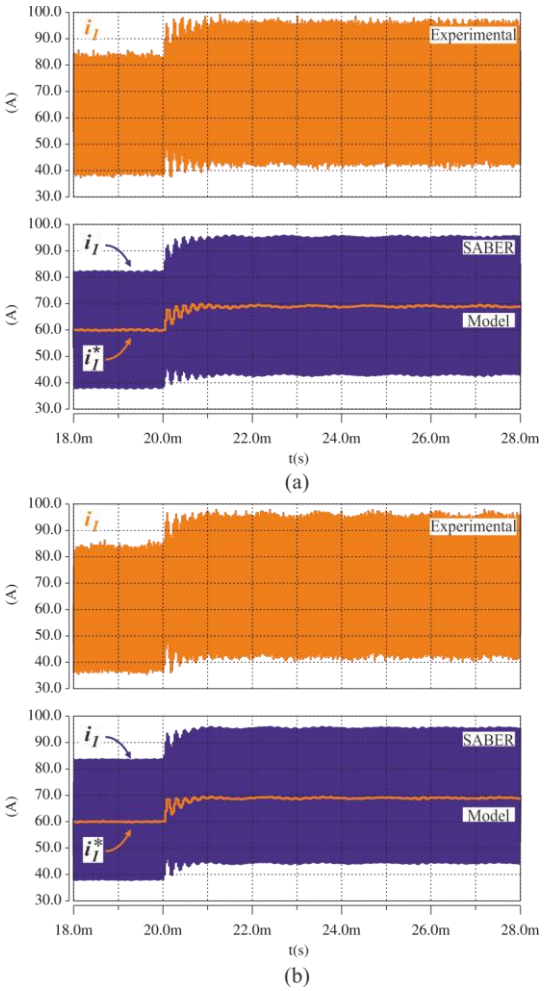

Fig. 14. Experimental and simulated response of i_1 to a 15 % step-increase in I_{ref} going from 60 A to 69 A for (a) V_{in} = 100 V corresponding to Point C, Fig. 8; and (b) V_{in} = 80 V corresponding to Point B, Fig. 8. R_{load} = 5.2 Ω, I_{in} = 120 A, K_p = 10(T) and K_i = 15.

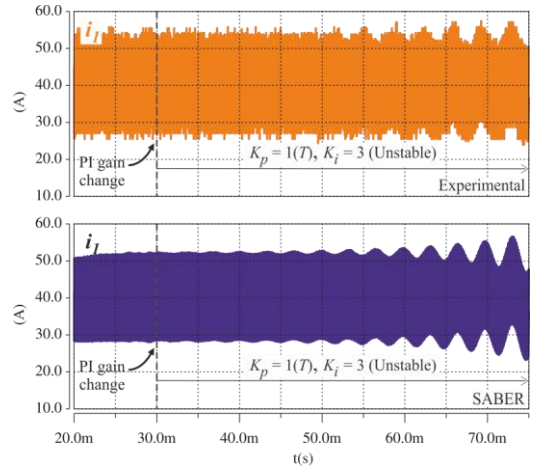

Fig. 15. Experimental and simulated response of i_1 to an unstable set of K_p and K_i gains predicted by the interleaved model. V_{in} = 85 V, R_{load} = 5.2 Ω, I_{in} = 80 A corresponding to Point Y, Fig. 10. Initial PI gains: K_p = 10(T) and K_i = 3.

i_{ref}, were used to examine the transient behaviour of the prototype and to compare with SABER simulations and predictions from the interleaved model. Fig. 14 shows results

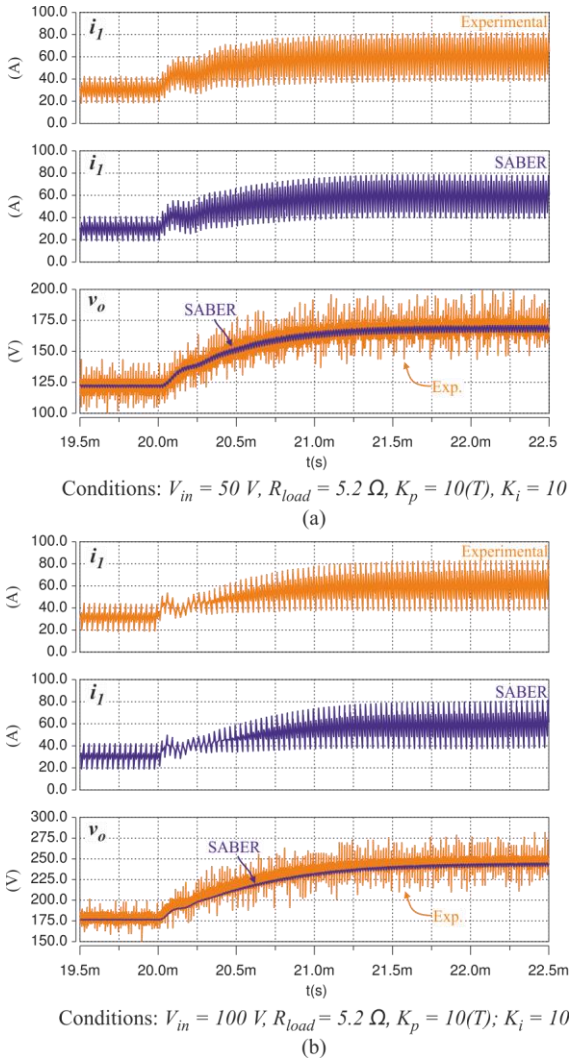

Figure 16. Simulated and experimental response of i_1 and v_o to a step-increase in I_{ref} going from 30 A to 60 A for (a) V_{in} = 50 V and (b) V_{in} = 100 V.

for two operating conditions with experimental data in the upper plots and SABER simulations and model predictions in the lower plots. The two operating conditions correspond with the plots labelled Point B and Point C in Fig. 8. The three sets of data correspond closely for both operating points. The high frequency natural mode (5 kHz) is clearly visible and its damping is accurately predicted, furthermore the lightly-damped low frequency natural mode (880 Hz approximately) is clearly evident in all the data sets, confirming the accuracy of the interleaved model.

Fig. 15 shows the experimental and simulation results of switching the converter into an unstable operating condition. Initially in Fig. 15 a stable combination of K_p and K_i was used, then at t = 30 ms the gains were changed to K_p =1(T) and K_i = 3. The values are marked as Point Y in Fig. 12 and are predicted to be unstable by the interleaved model but should be stable according to the non-interleaved analysis. The results show that the phase current becomes unstable after the change of gains and validates the prediction of the interleaved model.

Finally, Fig. 16 shows large-signal reference current step

responses from the converter along with SABER simulations. The digital phase current controllers were designed using the interleaved model, root-locus plots and stability maps to ensure well-damped responses over the converter operating range. The selected control parameters were K_p = 10(T) and K_i = 10. Apart from confirming the effectiveness of the model, the results also confirmed that the phase currents are well-balanced throughout the transient preventing any possibility of IPT saturation. Whilst the response times of the phase currents (around 1 ms) are much slower than could be achieved with an analogue current mode controller, these could be improved throughout optimisation of the digital implementation, in particular by reducing the processing delay in the update of the PWM signals.

VI. Conclusion

Using the sampler decomposition technique, a small-signal averaged model for average current-mode controlled, interleaved converters that accounts for the interleaved interaction of the phases has been developed. The method was applied to a dual-interleaved boost converter with inter-phase transformer and the closed-loop transfer functions were validated using time-domain step responses from a SABER simulation and experimental prototype. The model revealed an instability region that is not predicted by a non-interleaved model and which restricts the combinations of controller gains that may be used. The instability was attributed to the presence of a low-frequency natural mode that is virtually unobservable in the phase current transfer functions. The model was successfully used in the design of the phase current controllers for the interleaved boost converter, the large-signal response times of the currents being around 1 ms. Furthermore, the phase currents remained well-balanced at all times.

The analysis and design approach is based on well-known averaged converter models and may be readily applied to other circuit topologies such as dual-interleaved converters with separate inductors and no interphase transformer, and to systems with a greater number of phases. Whilst sampled-data techniques could be used to analyse interleaved sampling effects in these converters, [14], the comparative simplicity of the proposed modelling method is seen as a great advantage, however, as it is based on averaging, the model is limited to the prediction slow-scale dynamics.

Appendix. Small-signal, control-to-phase current transfer functions of the DIBC with IPT

$$G_{d1i1}(\mathrm{s}) = G_{d2i2}(\mathrm{s}) =$$

$$G_{di}(\mathrm{s}) = \left[\frac{(L_c + L_{\mathrm{in}})V_{\mathrm{in}}}{(1-\mathrm{D})L_{\mathrm{Tot}}}\right]\frac{\left(s^2 - a_{di1}s + a_{di0}\right)}{s\left(s^2 + b_1 s + b_0\right)} \qquad (A.1)$$

$$a_{di1} =$$

$$\frac{\left(\left(3L_c + 2L_{\mathrm{in}} + L_m\right)L_{\mathrm{Tot}} + 2C_o\left(L_c + 2L_{\mathrm{in}} - L_m\right)\left(L_c + L_m\right)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{2C_o\ \ L_{\mathrm{Tot}}R_{\mathrm{load}}\left(L_c + L_{\mathrm{in}}\right)} \qquad (A.2)$$

$$a_{di0} = \frac{\left(L_c + 2L_{\mathrm{in}} - L_m\right)\left(L_c + L_m\right)\left(R_{\mathrm{in}} + (1-\mathrm{D})^2 R_{\mathrm{load}}\right)}{C_o\ \ L_{\mathrm{Tot}}R_{\mathrm{load}}\left(L_c + L_{\mathrm{in}}\right)} \qquad (A.3)$$

$$G_{d1i2}(\mathrm{s}) = G_{d2i1}(\mathrm{s}) =$$

$$G_{dxi}(\mathrm{s}) = \left[-\frac{(L_{\mathrm{in}} - L_m)V_{\mathrm{in}}}{(1-\mathrm{D})L_{\mathrm{Tot}}}\right]\frac{\left(s^2 - a_{dxi1}s + a_{dxi0}\right)}{s\left(s^2 + b_1 s + b_0\right)} \qquad (A.4)$$

$$a_{dxi1} =$$

$$\frac{\left(\left(L_c - 2L_{\mathrm{in}} + 3L_m\right)L_{\mathrm{Tot}} - 2C_o\left(L_c + 2L_{\mathrm{in}} - L_m\right)\left(L_c + L_m\right)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{2C_o L_{\mathrm{Tot}}R_{\mathrm{load}}\left(L_{\mathrm{in}} - L_m\right)} \qquad (A.5)$$

$$a_{dxi0} = \frac{\left(L_c + 2L_{\mathrm{in}} - L_m\right)\left(L_c + L_m\right)\left(R_{\mathrm{in}} + (1-\mathrm{D})^2 R_{\mathrm{load}}\right)}{C_o\ \ L_{\mathrm{Tot}}R_{\mathrm{load}}\left(L_{\mathrm{in}} - L_m\right)} \qquad (A.6)$$

$$b_1 = \frac{\left(L_{\mathrm{Tot}} + 2C_o\left(L_c + L_m\right)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{C_o L_{\mathrm{Tot}}R_{\mathrm{load}}} \qquad (A.7)$$

$$b_0 = \frac{2\left(L_c + L_m\right)\left(R_{\mathrm{in}} + (1-\mathrm{D})^2 R_{\mathrm{load}}\right)}{C_o L_{\mathrm{Tot}}R_{\mathrm{load}}} \qquad (A.8)$$

VII. References

[1] O. Garcia, P. Zumel, A. de Castro, and J. A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, vol. 21, pp. 578-586, May 2006.

[2] G. Calderon-Lopez and A. J. Forsyth, "High power density DC-DC converter with SiC MOSFETs for electric vehicles," in *Proc. IET PEMD*, 2014, pp. 1-6.

[3] N. Liqin, D. J. Patterson, and J. L. Hudgins, "High Power Current Sensorless Bidirectional 16-Phase Interleaved DC-DC Converter for Hybrid Vehicle Application," *in IEEE Trans. Power Electron.*, vol. 27, pp. 1141-1151, Feb. 2012.

[4] G. Calderon-Lopez, A. J. Forsyth, and D. R. Nuttall, "Design and Performance Evaluation of a 10-kW Interleaved Boost Converter for a Fuel Cell Electric Vehicle," in *Power Electronics and Motion Control Conference, 2006. IPEMC 2006. CES/IEEE 5th International*, 2006, pp. 1-5.

[5] K. Hongrae, M. Falahi, T. M. Jahns, and M. Degner, "Inductor Current Measurement and Regulation Using a Single DC Link Current Sensor for Interleaved DC-DC Converters," in *IEEE Trans. Power Electron.*, vol. 26, pp. 1503-1510, Jun. 2011.

[6] J. Abu-Qahouq, M. Hong, and I. Batarseh, "Multiphase voltage-mode hysteretic controlled DC-DC converter with novel current sharing," in *IEEE Trans. Power Electron.*, vol. 19, pp. 1397-1407, Nov. 2004.

[7] J. Cabiles-Magsino, R. C. Guevara, and M. Escoto, "Implementation of sliding mode control for current sharing in fixed frequency voltage regulator modules," in *Proc. IEEE TENCON*, 2012, pp. 1-6.

[8] H. Xudong, W. Xiaoyan, T. Nergaard, L. Jih-Sheng, X. Xingyi, and L. Zhu, "Parasitic ringing and design issues of digitally controlled high power interleaved boost converters," in *IEEE Trans. Power Electron.*, vol. 19, pp. 1341-1352, Sept. 2004.

[9] O. Hegazy, J. Van Mierlo, and P. Lataire, "Analysis, Modeling, and Implementation of a Multidevice Interleaved DC/DC Converter for Fuel Cell Hybrid Electric Vehicles," in *IEEE Trans. Power Electron.*, vol. 27, pp. 4445-4458, Jun. 2012.

[10] D. De, C. Klumpner, C. Patel, K. Ponggorn, M. Rashed, and G. Asher, "Modelling and control of a multi-stage interleaved DC-DC converter

with coupled inductors for super-capacitor energy storage system," in *IET Power Electron.*, vol. 6, pp. 1360-1375, Sept. 2013.
[11] L. Yean-Kuo, S. Yi-Ping, H. Yu-Ping, L. Yu-Huei, C. Ke-Horng, and H. Wei-Chou, "Time-Multiplexing Current Balance Interleaved Current-Mode Boost DC-DC Converter for Alleviating the Effects of Right-half-plane Zero," in *IEEE Trans. Power Electron.*, vol. 27, pp. 4098-4112, May 2012.
[12] H. B. Shin, E. S. Jang, J. G. Park, H. W. Lee, and T. A. Lipo, "Small-signal analysis of multiphase interleaved boost converter with coupled inductors," in *IEE Proc. Electric Power App.*, vol. 152, pp. 1161-1170, Oct. 2005.
[13] S. K. Mazumder, "Stability analysis of parallel DC-DC converters," in *IEEE Trans. Aerospace and Electronic Systems.*, vol. 42, pp. 50-69, Mar. 2006.
[14] A. J. Forsyth and G. Calderon-Lopez, "Sampled-Data Analysis of the Dual-Interleaved Boost Converter With Interphase Transformer," in *IEEE Trans. Power Electron.*, vol. 27, pp. 1338-1346, Feb. 2012.
[15] D. M. VandeSype, K. DeGusseme, F. M. L. L. DeBelie, A. P. VandenBossche, and J. A. Melkebeek, "Small-Signal z-Domain Analysis of Digitally Controlled Converters," in *IEEE Trans. Power Electron.*, vol. 21, pp. 470-478, Mar. 2006.
[16] S. Buso and P. Mattavavelli, *Digital Control in Power Electronics*, USA: Morgan & Claypool, 2006.
[17] B. C. Kuo, "Transfer Functions, Block Diagrams and Signal Flow Graphs," in *Digital control systems*, 2nd ed. USA: Oxford University Press, Inc., 1992, ch. 4, sec. 7, pp. 149-167.
[18] J. T. Tou, *Digital and sampled-data control systems*. USA: McGraw-Hill, 1959.