Phase-Locked Loops for Grid-Tied Inverters: Comparison and Testing,

Phase-Locked Loops for Grid-Tied Inverters: Comparison and Testing

Siyu Gao*, M. Barnes[+]

*Elia Grid International, Belgium
[+]School of Electrical and Electronic Engineering, The University of Manchester, UK

Keywords: Phase-locked loops, inverters, AC-DC dynamics, VSC control.

Abstract

The increasing number of power electronic inverters connected to the utility grid means their synchronization to the utility grid plays an increasingly key role. Typically a phase-locked loop (PLL) is used, however limited information is still only available on PLLs in the public domain comparing them for power system applications. This paper presents quantified analyses and comparisons of the main PLL techniques based on different structures for both single phase and 3-phase systems. A more comprehensive comparison than previous work is made by introducing the robustness to geomagnetically induced current effects and islanding.

1 Introduction

Synchronization with the utility grid voltage is an important matter for a variety grid-connected power electronic converters, be they in the form of distributed power generation systems (DPGS), High Voltage DC transmission (HVDC), Flexible AC Transmission Systems (FACTS) or Custom Power units. Power flow is controlled by adjusting the voltage phase and magnitude between the inverter and the network to control current flow. Acquiring the correct phase and frequency information of the utility grid voltage is thus crucial for executing normal operation and control of the converters, especially when the utility grid is subjected to unbalanced faults. For example consider the operation of a vector controller grid-tied 3-phase inverter: phase information is used to converter abc phase information into the dq domain for both voltage and current, then frequency information is used to decouple d and q control loops, before control is undertaken and phase information is again used to convert dq signals to abc voltages.

Typically a Phase-Locked-Loop (PLL) [1]. Figure 1(a), is used to derive the network frequency and phase. The most basic PLL structure [2] consists of a phase detector (PD) block for generating a phase error signal between the input signal and the output signal of the PLL; a loop filter (LF) to reduce input phase error AC components; a voltage controlled oscillator (VCO) to generate the frequency and phase outputs from the output of LF. The drawback of using a simple multiplier as the PD block is that it introduces oscillations at

twice the frequency of the input signal. Removing these double frequency oscillations, is a key driver behind more advanced PLLs. Figure 1(b) shows a PLL with a more-advanced PD using a quadrature signal generator (QSG). When the PLL is locked to the input signal, θ'=θ, and thus e=0, which indicates no oscillatory term will be present once the PLL is synchronized with the input signal and reaches steady state. An alternative method uses adaptive filtering structures. Two examples are shown in Figure 1: the second order generalized integrator (SOGI), Figure 1(c), and the enhanced phase-locked loop (EPLL) based on the adaptive notch filter, Figure 1(d).
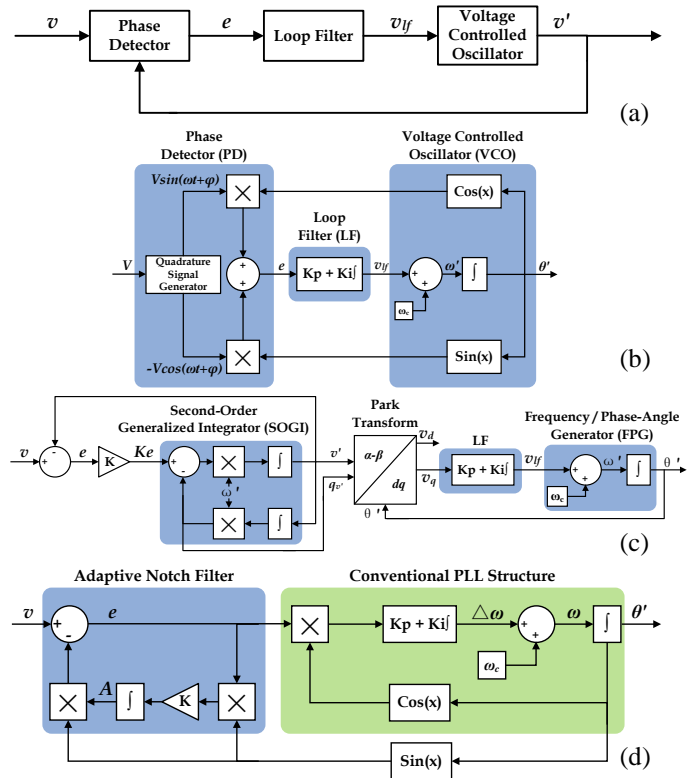

Figure 1 Overview of PLL Types (a) Basic structure of a PLL; (b) A PLL using an in-quadrature PD; (c) Structure of the SOGI-PLL; (d) Structure of the EPLL

2 PLL Overview

A more comprehensive introduction to PLLs is given in [14]. This paper takes this previous comparison and adds measures which particularly apply to three-phase voltage-source

converter grid-tied inverter systems: the impact of geomagnetically induced currents and islanding.

Generally, there are two ways to implement a PLL for a 3-phase system. The first one is to use 3 single phase PLLs for each phase to extract the phase angles independently. The transformation from 3-phase *abc* to *dq* space is not necessary for this structure [5]. A positive sequence extractor can be added to this structure to improve the performance when the system is subjected to unbalanced distortions, e.g. the 3-phase EPLL. The other implementation is to use a 3-phase PLL, which does involve the transformation from 3-phase *abc* to *dq*. The usage of this transformation is effectively a "down-dimensioning" process, i.e., translating the 3-phase system into an equivalent 2-phase system, which can be seen as the opposite of the advanced single phase PLLs. These two different structures will result in different reference quantities, and thus different control strategies [5].

The Synchronous Reference Frame (SRF) PLL is a classic example of 3-phase PLL based on in-quadrature signals. The structure is shown in Figure 2(a). The SRF-PLL structure can be found even within some advanced 3-phase PLLs, located at the output stage to generate the frequency and phase outputs, such as the DSOGI-PLL and the DDSRF-PLL.

The structure of the 3-phase 'Enhanced'-PLL (EPLL) is shown in Figure 2 (b). Three sets of in-quadrature signals are generated from 3 single phase EPLLs and then passed to the positive sequence extractor (PSE) followed by another single phase EPLL to generate the estimated frequency and phase outputs. Two extra single phase EPLLs can be added to lock on to the positive components of phase B and phase C [6].

The SRF-PLL with lead compensation is proposed in [7]. Its structure is shown in Figure 2 (c). This PLL is effectively a modified SRF-PLL with a filter located in front of the PI controller. The lead compensator has one notch peak at ω_Z and one resonant peak at ω_P in the magnitude response. Therefore, the lead compensator will remove the harmonic content around ω_Z frequency while amplifying the harmonic content around the ω_P frequency.

The "Windowed" SRF-PLL is proposed in [8]. Its structure is shown in Figure 2 (d). Similar to the idea of the SRF-PLL with lead compensation, this method also uses a nonconventional filter in front of the PI controller to improve the performance of the SRF-PLL. The rectangular window filter does not have any resonant peaks, and thus will not amplify the harmonic components. This filter can also be used in other PLLs to improve performance.

The structure of the Double Second-Order Generalised Integrator (DSOGI) PLL is shown in Figure 2(e). The principle of the DSOGI-PLL is to use a pair of SOGI based adaptive filters to generate the in-quadrature signals of the $\alpha\beta$ stationary reference frame voltages. These in-quadrature signals are then passed to the PSE to provide the positive sequence components for frequency and phase estimations.

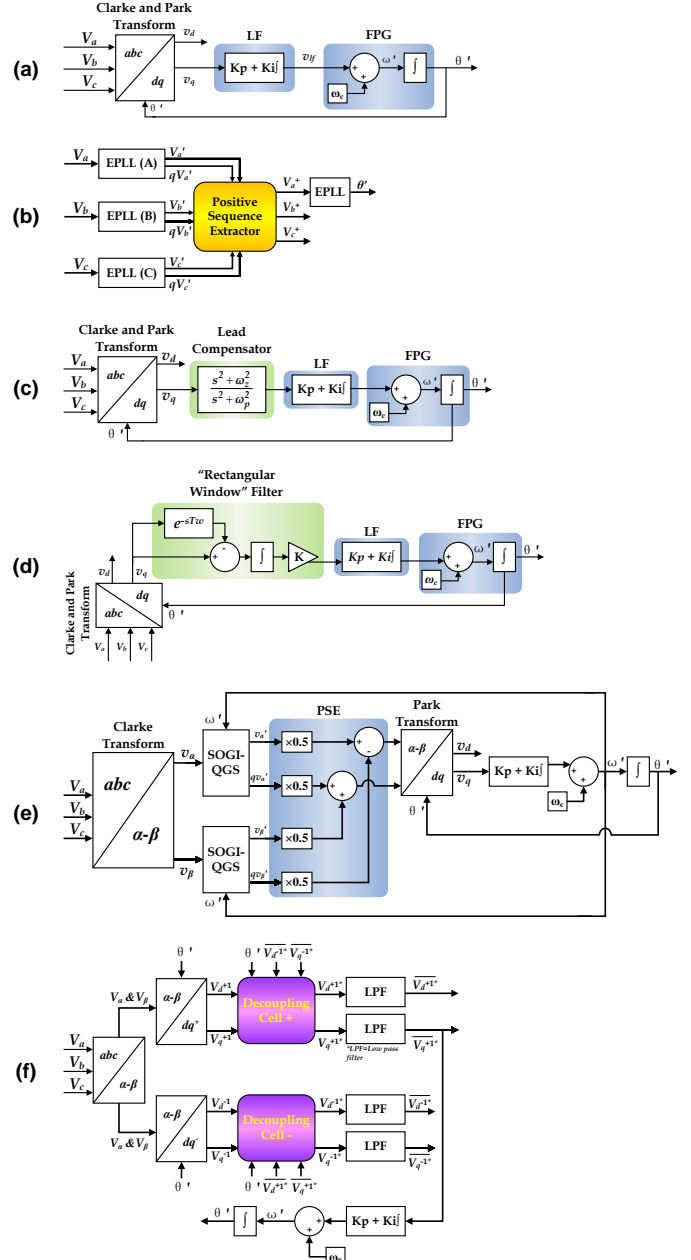The DSOGI-PLL is fundamentally different from the 3-phase EPLL and does provide extra filtering.

Figure 2 (a) Structure of the SRF-PLL; (b) Structure of the 3-phase EPLL; (c) Structure of the SRF-PLL with lead compensator; (d) Structure of the "windowed" SRF-PLL; (e) Structure of the DSOGI-PLL; (f) Structure of the DDSRF-PLL

The structure of the Decoupled Double Synchronous Reference Frame (DDSRF) PLL is shown in Figure 2(f). The concept of the DDSRF-PLL is that the rotating dq reference frame can be separated into positively rotating components and negatively rotating components. If the positively rotating components are decoupled and extracted from the negatively rotating components, then the performance of the traditional SRF-PLL can be improved based on the decoupled positive components. This idea is discussed in detail in [2] and [9].

3 Core Simulations of 3-Phase PLLs

In [14] the six 3-phase PLLs and the built-in PLL module of the PSCAD/EMTDC software package were subjected various distortions in order to evaluate their performance and response characteristics. The configuration of the PSCAD PLL module was included as a benchmark, and has been kept as its default. Other PLLs have been tuned to minimize the steady state error and to achieve a settling time of 0.1s when subjected to a 1Hz frequency drop. The observations are focused on the frequency outputs of the PLLs, since they are more visible than their integrated counterpart (the angle outputs). The phase outputs have also been examined during simulations. The low pass filters used in the DDSRF-PLL are rectangular window filters with T_w of 0.02s (50Hz).
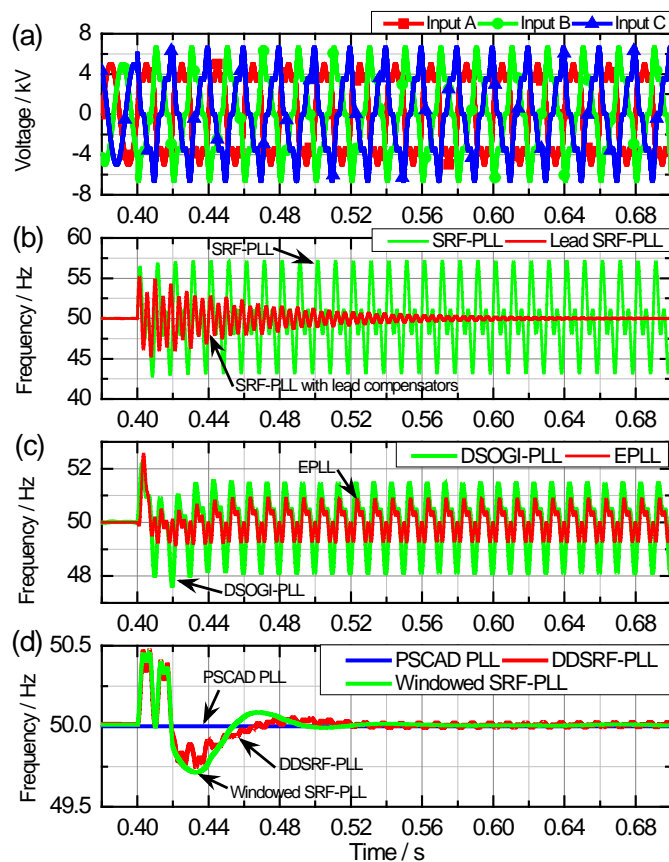

Figure 3 Harmonic Test. (a) 3-Phase inputs, 20% of 3rd and 5th harmonic injections at 0.4s, (b) Output frequencies of SRF-PLL and SRF-PLL with lead compensators, (c) Output frequencies of 3-phase EPLL and DSOGI-PLL, (d) Output frequencies of PSCAD PLL, DDSRF-PLL and the windowed SRF-PLL

Further tests applied in [14] were:
- A the frequency drop test. The 3-phase input frequency drops from 50Hz to 45Hz at 0.4s. T SRF-PLL, DSOGI-PLL, windowed SRF-PLL and the PSCAD PLL were able to generate smooth responses in a frequency drop situation. The responses of the EPLL, DDSRF-PLL and the SRF-PLL with lead compensators contain oscillations.

- A phase jump test where a phase jump of -45˚ is introduced at 0.4s. Similar to the frequency drop test, the SRF-PLL, DSOGI-PLL, windowed SRF-PLL and the PSCAD PLL are able to generate smooth responses, while the responses of the EPLL, DDSRF-PLL and the SRF-PLL with lead compensators contain oscillations.
- An amplitude drop test. The amplitudes of the 3-phase inputs drop by 80% at 0.4s. The SRF-PLL, SRF-PLL with lead compensators, the windowed SRF-PLL and the PSCAD PLL are not sensitive to input amplitude drop. On the other hand, the responses of the EPLL, DDSRF-PLL and the DSOGI-PLL do contain transients, though all except the EPLL are small.
- An unbalanced input test where the 3-phase inputs become unbalanced at 0.4s. The negative sequence to positive sequence ratio during the unbalanced event is about 18.4%. All PLLs have a transient component. The DDSRF-PLL and the windowed SRF-PLL are able to generate the best responses whose transients are the smallest.

In summary:
- The response of the EPLL is the most oscillatory and contains high transient overshoots.
- The SRF-PLL and the PSCAD PLL have some similar responses. Whereas the other PLLs recover quickly from the onset of unbalanced input conditions, these do not. The PSCAD PLL does not response to harmonic content.
- The DSOGI-PLL is able to generate smooth responses, however the transient overshoots can be significant.
- The DDSRF-PLL and the windowed SRF-PLL perform well under various distortions.
- The SRF-PLL with lead compensators, DDSRF-PLL and the windowed SRF-PLL are able to remove nearly all the harmonic contents in the test, however, the lead compensators require careful tuning or the harmonics will be amplified instead of reduced.

For grid-tied inverters, additional factors become important. Here the impact of system disturbances in the form of islanding are added and the effect of external system wide effects, in this case geomagnetically induced currents.

4. PLL Behaviours in an Islanding Case

Renewable energy generation and micro-grids will see more use of inverters in harmonic rich systems which are also capable of islanded operation. PLLs must be able to cope in such situations, even if they are only used to detect islanding and respond accordingly. In [10, 11] a positive frequency feedback model was proposed to predict the frequency behaviours grid-connected voltage source inverters (VSI). [10, 11] have demonstrated the correlations between different load types (inductive or capacitive) and the different frequency behaviours of inverters during islanded conditions. [10, 11] have also proposed an anti-islanding method utilizing the changes in the output frequencies of PLLs. The proposed relations between load type and frequency behaviours in [10, 11] can be further extended to the view of power balance at the point of common coupling (PCC). The model of the test

circuit is shown in Figure 4. The parallel RLC load is chosen according to the IEEE Standard 929-2000 [12] with a quality factor of 2.5. The line impedance of the VSI is 20 mΩ with an X to R ratio of 20. The RLC load and the VSI are connected to the 11 kV infinite bus model through a grid impedance of 0.1 mΩ with an X to R ratio of 6. An average model of the VSI is used for ease of identification of the oscillations in the outputs of the PLLs. In order to show how the theory proposed in [10, 11] can be extended to the power balance point of view, the VSI is set in constant power mode. The 11 kV grid contains 1% of 2nd harmonic, 2.5% of 3rd harmonic, 3% of 5th harmonic, 2.5% of 7th harmonic, 1.5% of 13th harmonic, 0.25% of 15th harmonic and 0.25% of 24th harmonic. The total harmonic distortion is 5%. The harmonic contents are chosen according to the British standard BS EN 50160:2007 [13]. Simulation results of test 1 are shown in Figure 5. Breaker 1-1 was opened at 0.4s. The VSI was set to consume reactive power. The RLC load was set to be capacitive.
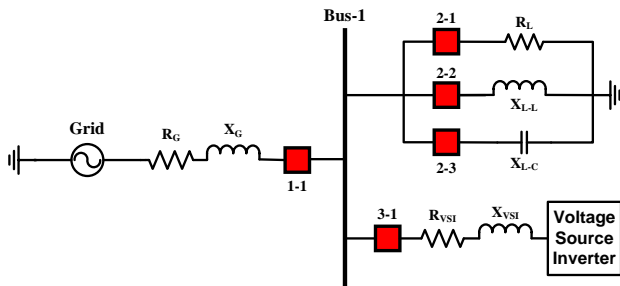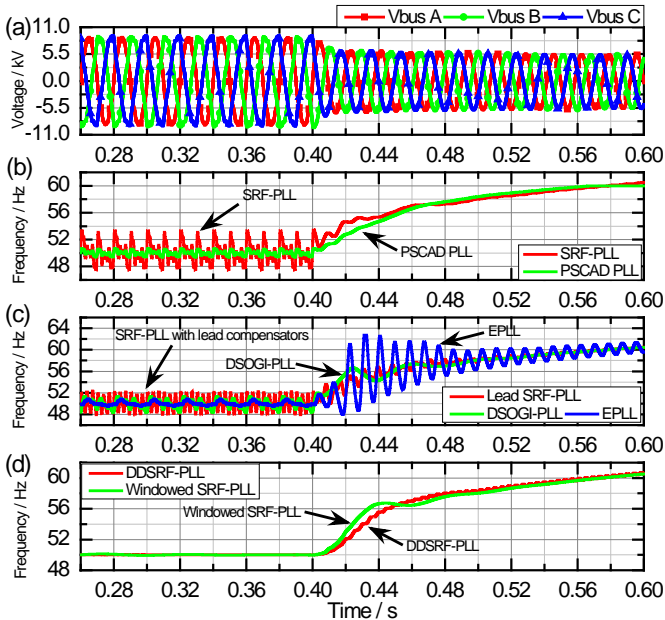

Figure 4 Model of islanding test circuit

Figure 5 Simulation results of islanding test 1. (a) Output frequency of SRF-PLL and PSCAD PLL, (b) Output frequency of SRF-PLL with lead compensators, DSOGI-PLL and EPLL, (c) Output frequency of DDSRF-PLL and windowed SRF-PLL

As shown in Figure 5, the bus voltages decrease after the opening of breaker 1-1, while the frequency is increased.

Results of test 2 are shown in Figure 6. In this test, breaker 1-1 was opened at 0.4s. The VSI was set to generate reactive power. The RLC load was set to be capacitive. This time, the frequency is decreased. It can be seen in Figure 6(b) that, there is a limiter on the output of the PSCAD PLL.
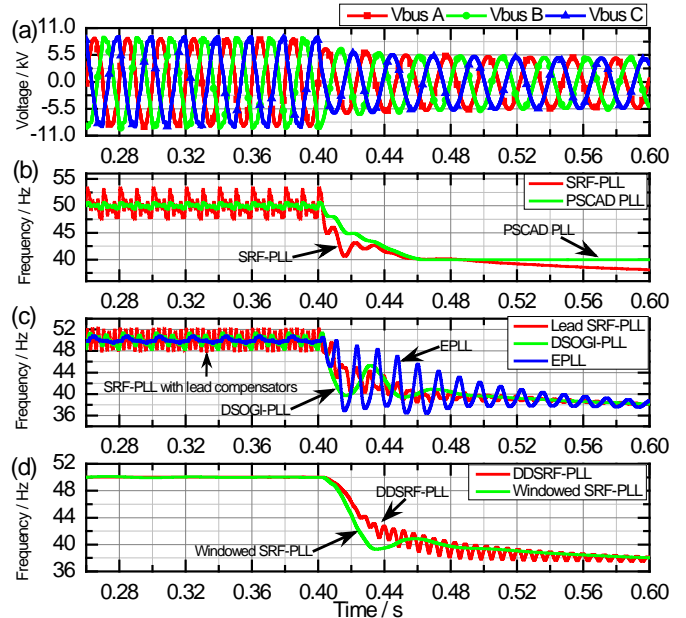

Figure 6 Simulation results of islanding test 2. (a) Output frequency of SRF-PLL and PSCAD PLL, (b) Output frequency of SRF-PLL with lead compensators, DSOGI-PLL and EPLL, (c) Output frequency of DDSRF-PLL and windowed SRF-PLL

As shown in Figure 5, the response of the EPLL is the most oscillatory. The output of the DDSRF-PLL contains a lot of small oscillations after the fault was introduced. Other PLLs are able to generate relatively smooth outputs.

In Figure 6, the oscillations in the output of the DDSRF-PLL are more visible than the previous test. The SRF-PLL and the windowed SRF-PLL are able to generate comparatively smoother response within the PLLs tested.

Due to the differing nature of responses, providing a single quantity to define the behaviour of the PLLs in this situation was regarded as being unhelpful.

5. Assessment of Geomagnetically Induced Current Impact on PLLs

A type of event which may cause severe unbalanced disturbance to the three-phase voltage, but yet to be studied comprehensively in the context of PLLs, is known as Geomagnetically Induced Current (GIC) These are caused by solar space weather, injecting, in effect a DC potential between any two earth connections in a power system. Generally small, when these earths are widely spaced (for example the earths between transformers on a long transmission line), significant potentials can result. An example for an HVDC lines is shown in Fig. 7
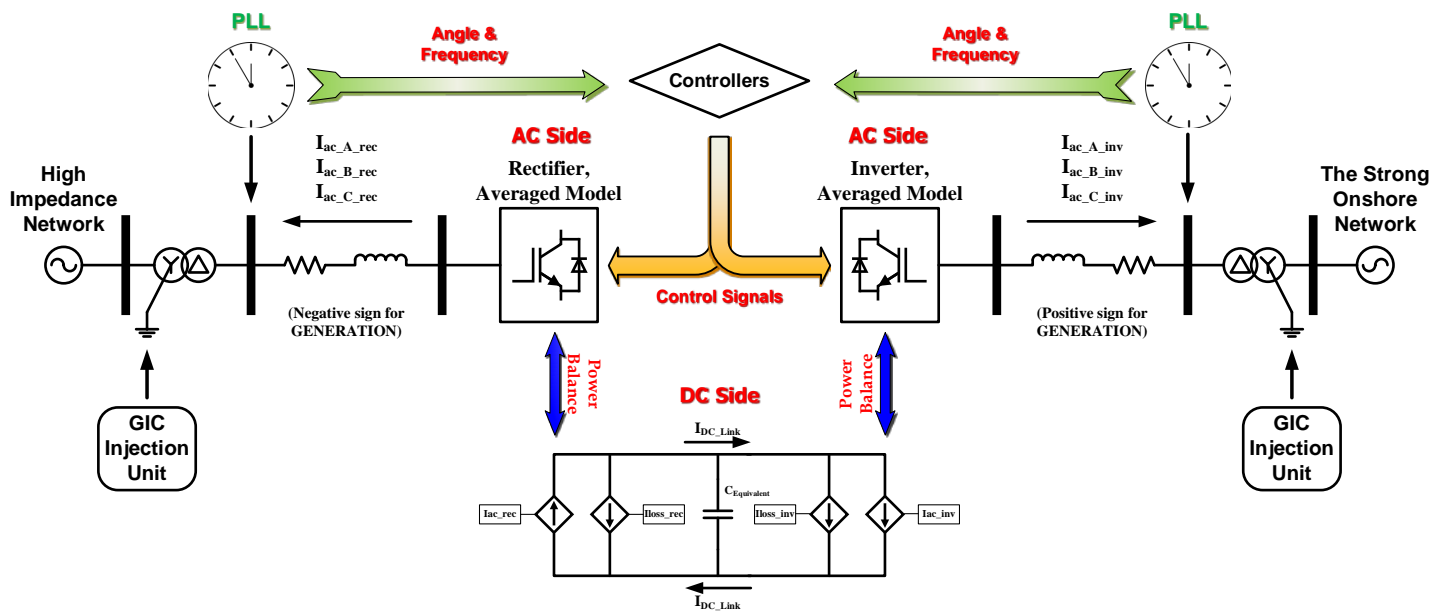
Figure 7 Schematic of the test model

As shown in Figure 7, the test model comprises of a high impedance network (e.g. a weak isolated onshore network), transformers, the GIC injection units, the voltage-source High Voltage DC Modular Multilevel Converter (MMC) converters, the PLLs, controllers and the strong larger network.

The narrow bandwidth of GIC events (from milli Hz to about 1 Hz), means a suitable fidelity model can be chosen to simplify computation. The high impedance network is modelled as a three-phase voltage source. The transformer model used is the UMEC transformer model with three single-phase transformers used to form a three-phase transformer. The MMC model used in the GIC tests is the industry standard 'average value model' (AVM), which models the terminal characteristics of the MMC since the bandwidth of GIC events is much slower than the inner dynamics of the MMC converter. DQ current control is used for the MMC, since real power and reactive power can then be controlled separately. Constant power control is used on the high impedance network side. The HV side AC voltage in the model is 400 kV line-to-line, while the LV side AC voltage is 333 kV line-to-line. The DC link voltage is ±320 kV with capacity of 1000 MW. These ratings are selected according to [15]. Fault introduction facilities are implemented after the transformer in order to test the fault ride through ability of the MMC model. GIC is modelled with a constant DC current injection as recommended in [16].

To examine the performance of the PLLs under GIC conditions, a GIC of 224A (74.67A per phase) was injected into the grounded transformer neutral on the rectifier side. This particular amount of GIC is chosen because it was the estimated total amount of GIC during the 1989 Québec event [17]. The rectifier is set to delivery 900MW constant power (0.9 p.u.) while the inverter is set to V_{dc} control.

Figure 8 shows the harmonic analysis of the transformer primary currents after 15s of GIC injection. A DC component is clearly visible in the primary currents, indicating that the GIC injected is passed into the three-phase currents. Other even and odd harmonics can also be observed in the harmonic analysis, noticeably the second, fourth, seventh and tenth harmonics. DC currents and triplen harmonics will be blocked other harmonics are not blocked.
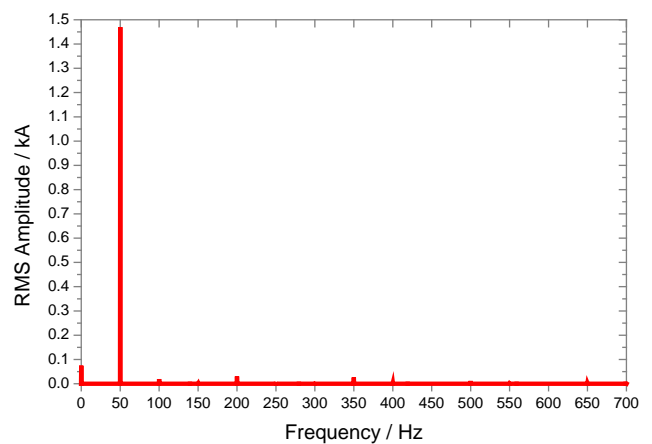

Figure 8 Harmonic analysis of the primary currents after 15s of GIC injection

These components will disturb the PLLs. The SRF-PLL with lead compensation is the most oscillatory PLL during this test. The PSCAD PLL and the SRF-PLL are less oscillatory than the SRF-PLL with lead compensation, but the patterns of oscillations are similar. This indicates that the lead compensators used can have the potential to amplify certain harmonics, therefore, notch peaks and the resonant peaks of the compensators have to be selected carefully. The DSOGI-PLL and the three-phase EPLL show much lower degree of frequency oscillations, while the DDSRF-PLL and the

"Windowed" SRF-PLL appear to be able to achieve fairly accurate frequency outputs.

To quantify the performance of the PLLs in this test, the absolute frequency errors of the PLLs from time 9.7s to 10.0s are summed up, averaged and then converted into percentages of the 50Hz frequency. Figure 9 shows a compensate of PLL performance.
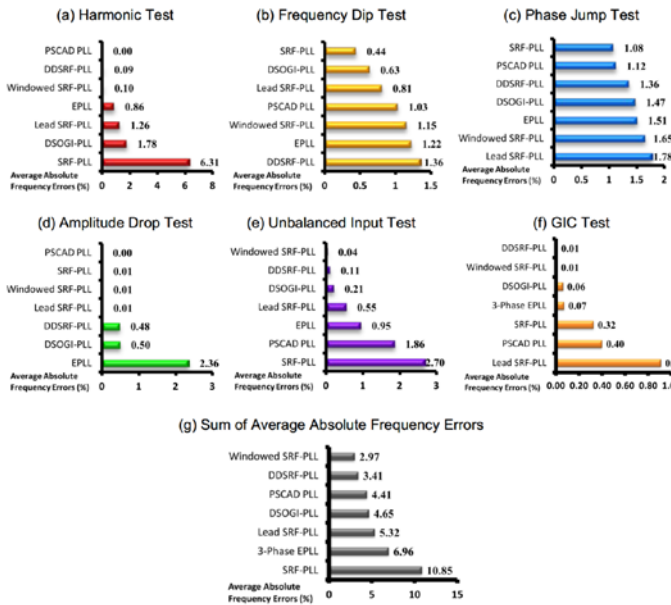

Figure 9 Updated results of PLL quantification

6. Conclusions

The study and results in this paper summarize the two widely used techniques in phase detection: in-quadrature signal generation and adaptive filtering. Three-phase PLLs have been assessed for a variety of power system disturbances. According to the methodology used the windowed SRF-PLL and DDSRF-PLL are able to deliver the best overall performance.

7. Acknowledgements

8. References

1. Guan-Chyun, H. and J.C. Hung, *Phase-locked loop techniques. A survey.* Industrial Electronics, IEEE Transactions on, 1996. **43**(6): p. 609-615.
2. Teodorescu, R., Liserre, M., Rodríguez, P., *Grid Converters for Photovoltaic and Wind Power Systems.* 2011: John Wiley & Sons, Ltd.
3. Jovcic, D., *Phase locked loop system for FACTS.* Power Systems, IEEE Transactions on, 2003. **18**(3): p. 1116-1124.
4. Karimi-Ghartemani, M. and M.R. Iravani, *A method for synchronization of power electronic converters in polluted and variable-frequency environments.* Power

5. Blaabjerg, F., et al., *Overview of Control and Grid Synchronization for Distributed Power Generation Systems.* Industrial Electronics, IEEE Transactions on, 2006. **53**(5): p. 1398-1409.
6. Nicastri, A. and A. Nagliero. *Comparison and evaluation of the PLL techniques for the design of the grid-connected inverter systems.* in *Industrial Electronics (ISIE), 2010 IEEE International Symposium on.* 2010.
7. Freijedo, F.D., et al., *Three-Phase PLLs With Fast Postfault Retracking and Steady-State Rejection of Voltage Unbalance and Harmonics by Means of Lead Compensation.* Power Electronics, IEEE Transactions on, 2011. **26**(1): p. 85-97.
8. Karimi-Ghartemani, M., et al., *Derivation and Design of In-Loop Filters in Phase-Locked Loop Systems.* Instrumentation and Measurement, IEEE Transactions on, 2012. **61**(4): p. 930-940.
9. Rodriguez, P., et al., *Decoupled Double Synchronous Reference Frame PLL for Power Converters Control.* Power Electronics, IEEE Transactions on, 2007. **22**(2): p. 584-592.
10. Dong, D., et al. *Frequency behavior and its stability of grid-interface converter in distributed generation systems.* in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE.* 2012.
11. Dong, D., et al. *A novel anti-islanding detection algorithm for three-phase distributed generation systems.* in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE.* 2012.
12. *IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems.* IEEE Std 929-2000, 2000.
13. *BRITISH STANDARD; Voltage characteristics of electricity supplied by public distribution networks* BS EN 50160:2007.
14. Siyu Gao and Mike Barnes, *Phase-locked Loop for AC systems: Analyses and Comparisons*, IET Power Eectronics Machines and Drives Conference 2014
15. Peralta, J., Saad, H., Dennetiere, S., Mahseredjian, J., and Nguefeu, S. *Detailed and averaged models for a 401-level MMC-HVDC system.* in *Power and Energy Society General Meeting (PES), IEEE.* 2013
16. Manitoba HVDC Research Centre Inc., *Application of PSCAD/EMTDC.* Manitoba HVDC Research Centre Inc., 2008.
17. North America Electric Reliability Corporation, *March 13, 1989 Geomagnetic Disturbance.* NERC, 1990.

Systems, IEEE Transactions on, 2004. **19**(3): p. 1263-1270.