Fabrication of Submicrometer InGaAs/AlAs Resonant Tunneling Diode Using a Tri-layer Soft Reflow Technique with Excellent Scalability

M. A. Md Zawawi, KaWa Ian, J. Sexton and M. Missous, *Senior Member, IEEE*

***Abstract*—A tri-layer soft reflow fabrication method using solvent vapour that resulted in a sub-micrometer resonant tunneling diode is reported in details. The processing steps are simple, time efficient and are all based on conventional i-line photolithography. The tri-layer soft reflow technique is able to shrink the emitter lateral width from 1µm down to 0.35µm (65% reduction) using a solvent at a very low temperature (<50 ˚C). Studies of device's peak current density (J_P) suggests that excellent scalability is achieved as the emitter area reduces from ~29µm^2 down to ~0.5µm^2 with no significant increase in peak voltage (V_P) due to high series resistance normally associated with sub-micrometer dimensions. The valley current (I_V) however increases due to side-wall damage introduced by the reactive ion etching (RIE) process. As a result, the peak-to-valley-current ratio (PVCR) decreases from 5.0 (6.3) to 3.8 (4.1) in forward (reverse) direction as the emitter area decreases. We therefore successfully demonstrated the fabrication of a sub-micrometer RTD by using a tri-layer soft reflow technique that has the benefit of excellent scalability, high throughput, repeatable and a reliable low cost process.**

***Index Terms*—InGaAs-AlAs, resonant tunneling diode, soft reflow, submicrometer processing.**

I. INTRODUCTION

AMONGST all high frequency electron devices, the resonant tunneling diode (RTD) receives a lot of attention due to its simple structure and ultra high frequency capability. The growing interest in RTD, due to its ability to generate continuous wave (CW) at terahertz frequencies, has seen many breakthroughs in this fields with excellent results [1-3]. To date, the highest room temperature fundamental oscillation of up to 1.31 THz is achieved in thin-well (3.9 nm) resonant tunneling diodes based on strained InGaAs-AlAs [3]. Currently, the terahertz and sub-terahertz frequency proves its usefulness in various applications such as radio astronomy, medical imaging, surveillance and security, atmospheric and environmental monitoring as well as holding great promises for gigabit per second (Gb/s) wireless communication [4].

As a rule of thumb, any semiconductor device which operates at very high frequency needs to have very small lateral dimension (to minimise capacitance) and the RTD is no exception [5]. Therefore the need to process down to sub-micrometer RTD mesa area is a must.

Several works have been done related to sub-micrometer RTD, in order to realise a one-dimensional (1-D) devices. These one-dimensional RTDs have typical diameter of 100 nm. The first attempt was pioneered by Reed et.al [6] from Texas Instrument back in late 80's. In Reed's work, the RTD had a diameter of 100 nm to 200 nm patterned by electron-beam lithography (EB) and reactive ion etching (RIE) for side-wall formation. The material used was GaAs/AlGaAs/InGaAs (contacts/barriers/well). However, the resulting DC characteristics were rather disappointing with peak-to-valley-current ratio of 1.1 [7].

Further work on sub-micrometer RTDs was then carried out using focussed ion beams in order to achieve ~ 100 nm diameter as demonstrated by Tarucha [8]. There are also sub-micrometer RTD fabricated by

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photolithography with selective wet etching, however the metal contact was not put directly on top of the device in these studies [9]. The most recent and complex method of creating sub-micrometer RTD is by using nanowire or nanowhiskers using chemical beam epitaxy [7].

All the techniques mentioned above are rather complicated and expensive, and fairly time consuming with slow through-put especially when using electron-beam (EB) lithography. The method proposed in this work is simple, reproducible and provides an economical solution in order to obtain sub-micrometer feature sizes. This new process was first introduced for application in pHEMTs [10]. The technique, termed low temperature soft reflow, uses conventional i-line photolithography to define the lateral structure and solvent vapour to achieve sub-micrometer features.

However, in this work, the original technique with bi-layer lift-off has been modified and extended to suit the processing of an RTD by employing a tri-layer lift-off technique. Since the RTD does not require a T-gate shape as in the case of a pHEMT, therefore to create a sub-micrometer RTD, the soft-reflow technique is combined with a trilayer lift-off technique that results in a straight top metal contact.

II. SOFT REFLOW PRINCIPLE

The main principle involves the absorption of vapour by the photoresist to expand its volume. The soft reflow process is done in a purpose –built closed chamber with a sample being placed at some distance above the solvent. The entire process is controllable through these parameters: solvent temperature, duration of reflow and thickness of the photoresist. While the solvent temperature and photoresist thickness are kept constant, the shrinking of the initial opening (L) is inversely related to reflow duration (time in seconds). In another word, as the reflow duration increases, more vapour will be absorbed by the photoresist on both sides of the opening, hence a smaller opening (L') is obtained. The amount of shrinkage is given by parameter ΔL. This soft reflow process is quick to perform and most beneficial especially in the absence of electron beam (EB) lithography to define the sub-micrometer lateral dimensions. Fig. 1 illustrates the principle of the soft reflow technique.

The photoresist that is readily coated onto the sample absorbs the vapour by a method of condensation. An isotropic expansion in terms of photoresist volume occurs on both sides of the opening and results in a reduced final dimension.

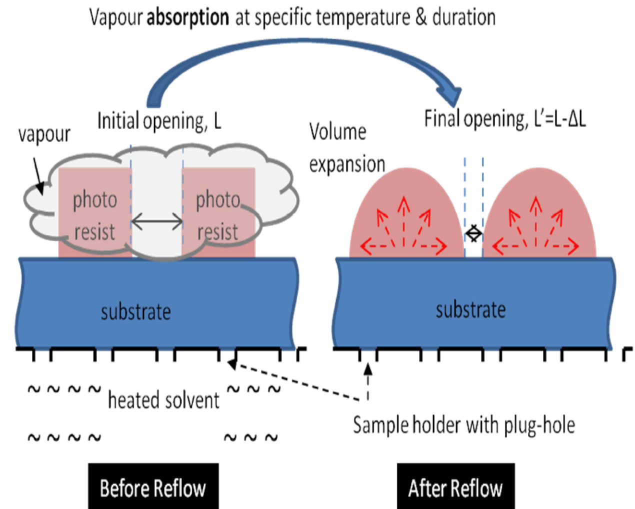

Fig. 1. Illustration of the soft reflow principle.

This work is an extension to the previously reported bi-layer soft reflow technique successfully performed on pHEMTs by K. W. Ian *et al* [11]. The trend of the feature size reduction against reflow time is almost similar for both bi-layer and tri-layer techniques as shown in Fig. 2. Slight differences between the two curves could be attributed to differences in ambient conditions, namely the temperature and humidity. Any changes in either one or both of these external parameters would cause changes in the solvent evaporation rate and vapour absorption rate.

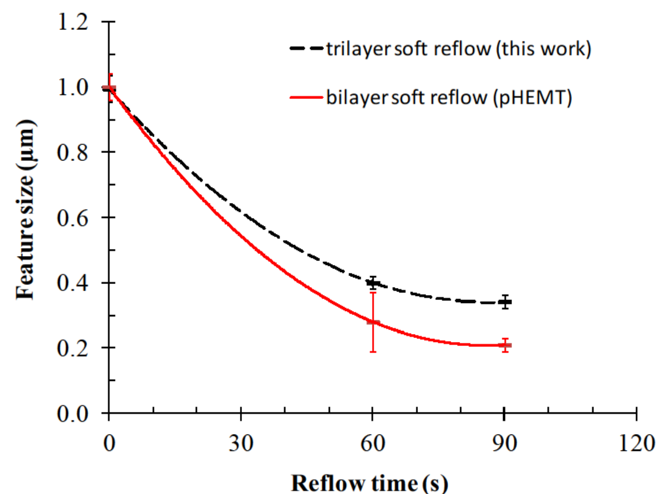

Fig. 2. Relationship between feature size and reflow time in this study in comparison to bi-layer soft reflow process for pHEMT [11].

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III. SAMPLE PREPARATION AND PROCESSING

The sample used in this study, denoted as XMBE277 was grown in house using a RIBER V100 molecular beam epitaxy (MBE) system on a (100) semi-insulating InP substrate. Table I shows the epitaxial structures which consist of a 400 nm highly doped n^+ - $In_{0.53}Ga_{0.47}As$ collector-contact layer on top of an InP substrate. This was followed by a 25 nm n -$In_{0.53}Ga_{0.47}As$ collector layer. Then, a 20 nm undoped $In_{0.53}Ga_{0.47}As$ spacer layer was grown. This spacer layer also prevents the diffusion of dopants into subsequent layers during growth. A 1.3 nm undoped AlAs barrier, a 4.5 nm undoped highly-strained $In_{0.8}Ga_{0.2}As$ well, and another 1.3 nm undoped AlAs barrier formed the double barrier quantum well (DBQW) structure. A further 20 nm undoped $In_{0.53}Ga_{0.47}As$ spacer layer and a 25 nm n - $In_{0.53}Ga_{0.47}As$ emitter were grown on top of the DBQW structure. Finally a 45 nm highly doped n^+ -$In_{0.53}Ga_{0.47}As$ emitter-contact layer was grown to facilitate good ohmic-contacts. In order to characterise and optimise the growth conditions especially for the thin highly-strained $In_{0.8}Ga_{0.2}As$/AlAs DBQW structure, a double crystal x-ray diffraction (DCXRD) method was used to estimate the various epitaxial layer thicknesses.

TABLE I. The epitaxial structure for sample XMBE277.

Layer	Thickness (nm)	Doping Concentration (cm^{-3})
n^+- $In_{0.53}Ga_{0.47}As$	45	2.00×10^{19}
n- $In_{0.53}Ga_{0.47}As$	25	3.00×10^{18}
$In_{0.53}Ga_{0.47}As$	20	undoped
AlAs	1.3	undoped
$In_{0.8}Ga_{0.2}As$	4.5	undoped
AlAs	1.3	undoped
$In_{0.53}Ga_{0.47}As$	20	undoped
n- $In_{0.53}Ga_{0.47}As$	25	3.00×10^{18}
n^+- $In_{0.53}Ga_{0.47}As$	400	1.00×10^{19}
Semi-insulating InP		

The RTD emitter lateral dimensions as defined by mask patterns are 1x1 μm^2, 1.5x1 μm^2, 2x1 μm^2, 3x1 μm^2 and 4x1 μm^2 . However, when subjected to the soft-reflow technique, the final emitter areas become 1x0.35μm^2, 1.5x0.35μm^2, 2.0x0.35 μm^2, 3.0x0.35 μm^2 and 4x0.35μm^2respectively. These 5 sub-micrometer dimensions are incorporated in order to determine the dependency of oscillation frequency on mesa area at a later stage of this study. Reducing mesa area is a geometrical way of reducing the RTD capacitance to improve frequency performance. It is also important to observe if there is no degradation in DC performance within the sub-micrometer areas.

It may be worthwhile to mention that the length (1.0 µm, 1.5 µm, 2.0 µm, 3.0 µm and 4.0 µm) of the emitter is defined by the mask. However, the width of the emitter although initially defined by the mask (1.0 µm) during photolithography, its final width is determined after the soft-reflow technique is completed. There was no process induced bias to the fabricated dimensions.

The processing begins with an LOR 3A resist being spin-coated onto the surface of the semiconductor to produce a 300 nm thick film. This is then followed by the deposition of 200 nm Si_3N_4 on top of the LOR 3A. LOR 3A lift-off resist is based on polydimethylglutarimide. It is used as an undercut layer underneath the Si_3N_4 and S1805 photoresist. While having an excellent adhesion to InGaAs, the processing is easy without the need for extra UV exposure. The third layer, Shipley S1805 positive photoresist of about 420 nm thick is then spin-coated on top of the Si_3N_4. Shipley S1805 belongs to Microposit S1800 series positive photoresist. It is compatible with LOR 3A resist and i-line photolithography. The tri-layer technique is useful for a clean and easy metal lift-off. To define the 1 µm emitter opening, an i-line optical lithography is used to transfer the pattern onto the positive photoresist. The sample is then subjected to the soft-reflow process until the opening shrinks from 1 µm down to 350 nm. This sub-micrometer feature is transferred to the Si_3N_4 by CF_4 reactive ion-etching, followed by O_2 reactive ion-etching (RIE) to strip the LOR 3A resist in order to expose the semiconductor surface. An undercut profile is created by using an MF319 solution to facilitate a clean metal lift-off. Microposit MF-319 is a metal-ion-free developer dedicated for S1800 series positive photoresists, thus the best candidate for S1805 development. Using an immersion technique, excellent resist profile can be obtained.

The sample is then dipped into a diluted Hydrochloric acid solution, $HCl:H_2O$ = 1:1 for the de-oxidation process before metal deposition by thermal evaporation takes place. This is to ensure a good contact between metal and semiconductor surfaces with minimum oxide formation. An emitter metal consisting of Ti/Au (50 nm / 200 nm) is deposited onto the surface of a highly doped $In_{0.53}Ga_{0.47}As$ emitter by thermal evaporation and subsequent lift off in hot N-methyl-2-pyrrolidone (NMP) solvent. Fig. 3 describes the first processing step (tri-layer soft-reflow) for the sub-micrometer RTD.

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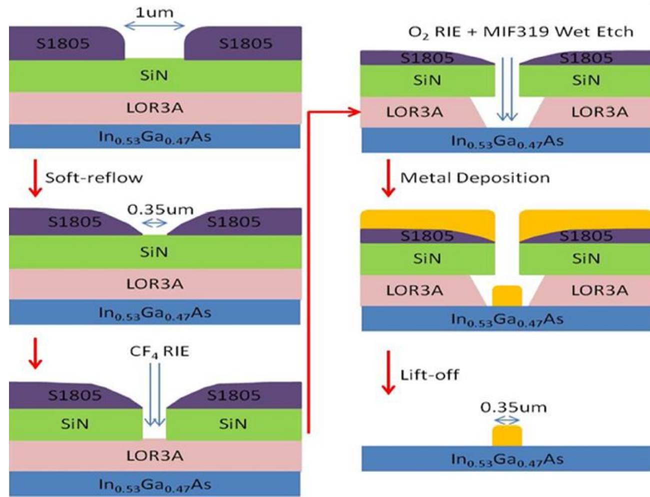

Fig. 3. Illustration of the first processing steps for the sub-micrometer RTDs.

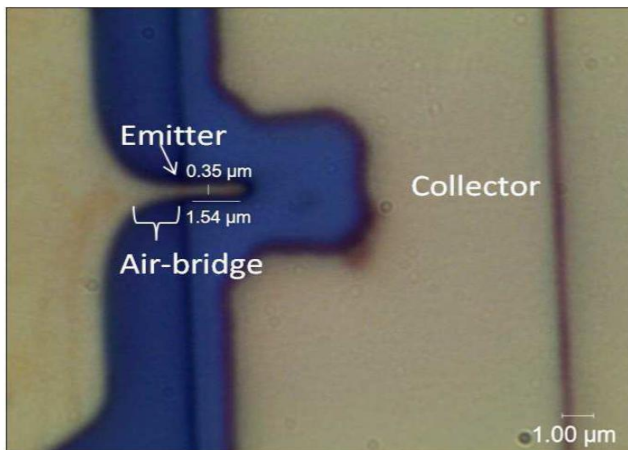

Fig. 4. The completed sub-micrometer RTD with emitter lateral dimension of ~ 1.54 µm (length) and ~ 0.35 µm (width) resulting in a mesa area of ~ 0.54 µm^2.

Using the emitter metal as an etch mask, the sample is put into CH_4:H_2 (1:8) reactive-ion-etching for 20 minutes. The chamber pressure is kept at 40 mTorr at a power of 150W. This resulted in an anisotropic sidewall 210 nm down to the collector layer.

Subsequently, wet-etching is performed by applying a positive photoresist and UV-photolithography to define the areas. An Ortho-phosphoric etchant (H_2O:H_3PO_4:H_2O_2 = 50:3:1), with an etch rate of 90 nm per minute is used to etch away about 300 nm of epilayer materials down to the surface of InP, which acts as an etch-stop layer. The 5 minutes wet-etch will simultaneously provide the necessary undercut through lateral etching for the air-bridge formation. The air-bridge structure (1 µm x 3 µm) must be fully opened to avoid high parasitic (parallel) resistance. Both the sub-micron area and large-area processing used identical process flow during the formation of the air-bridge structures.

Finally, the collector contact is formed by thermal evaporation of Ti/Au (50 nm / 500 nm). The bottom (collector) contact is also ohmic, similar to the top emitter contact. A typically completed sub-micrometer RTD is shown in Fig. 4. The schematic cross-section of the RTD is illustrated in Fig. 5, showing two distinct regions of passive and active mesas connected through an air-bridge structure.

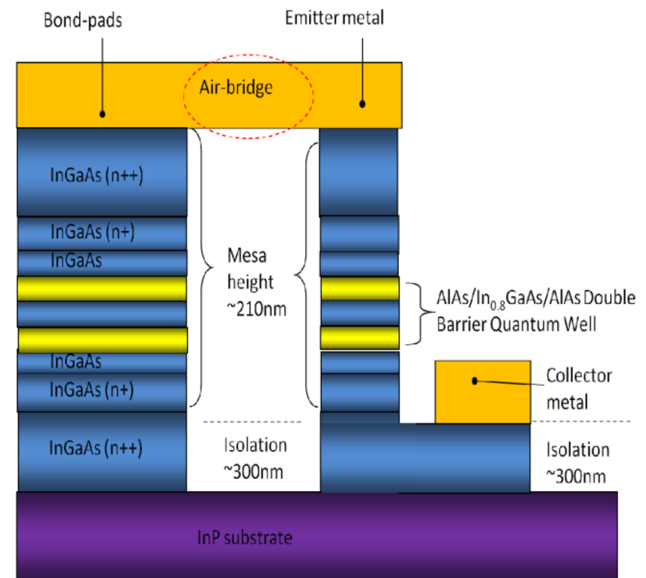

Fig. 5. Schematic illustration of the cross-sectional view of the sub-micrometer RTDs.

IV. RESULTS AND DISCUSSIONS

Upon completion of the sub-micrometer RTD, room temperature DC characteristics were measured using an HP 4142 DC parameter analyser. The success of the sub-micrometer processing can be quantitatively determined by device scalability in terms of their peak current densities. For this purpose, large areas RTDs are fabricated together with the sub-micrometer RTDs on the same sample as to minimise process-related errors. Fig. 6 below depicts measured current-voltage characteristics of a large area RTD (28.6 µm^2) and a sub-micrometer RTD (0.54 µm^2), a nearly 60:1 reduction in active area.

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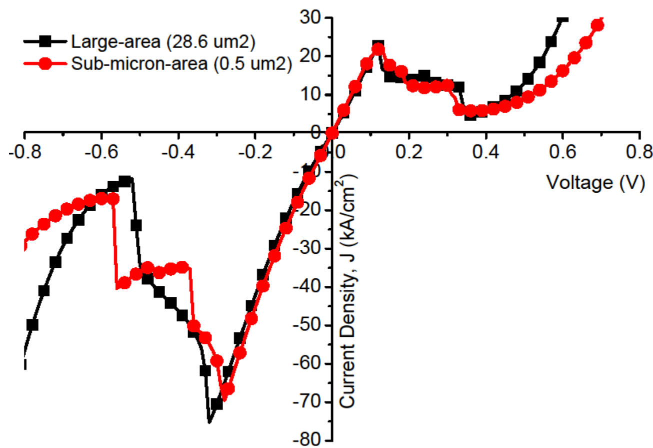

Fig. 6. Measured current-voltage characteristics for sample XMBE277 at room temperature for different mesa sizes. Note the very low value of peak voltage.

In forward bias, the large area RTD has a peak current density of 23 kA/cm^2 which occurs at a peak voltage of 120 mV. The sub-micrometer RTD has similar peak current density of 22 kA/cm^2 at a peak voltage of 130 mV. The 10 mV difference in peak voltage is due to the resolution of the step-size in this measurement. In the negative polarity, the large area RTD has a peak current density of 75 kA/cm^2 which occurs at a peak voltage of 320 mV, and the sub-micrometer RTD has a peak current density of 69 kA/cm^2 which occurs at peak voltage of 280 mV.

Evidently, as the emitter area is scaled down to 0.525 µm^2 from 28.62 µm^2, the peak voltage (V_P) between these two RTDs are almost the same at ~ 120 mV in forward bias and ~ 300 mV in reverse direction. This implies that the RTDs are not depleted by the CH_4 reactive-ion-etching (RIE) process. Otherwise, the peak voltage for sub-micrometer RTD would have drifted to higher value due to series resistance effects associated with side-wall damage.

Noticeably, the fabricated RTDs have a very low value of peak voltage, V_p and in particular in the forward direction, the peak current occurs at a voltage as low as 120 mV. Notice that even though too large a peak current, I_P may be undesirable due to the issue of high power dissipation during circuit implementation, this can be compensated by designing RTD with very low peak voltage, V_P.

The fact that both peak current densities between these two devices are similar, serves as an indicator towards excellent device scalability. A full overview of peak current density as a function of device area is plotted in Fig. 7.

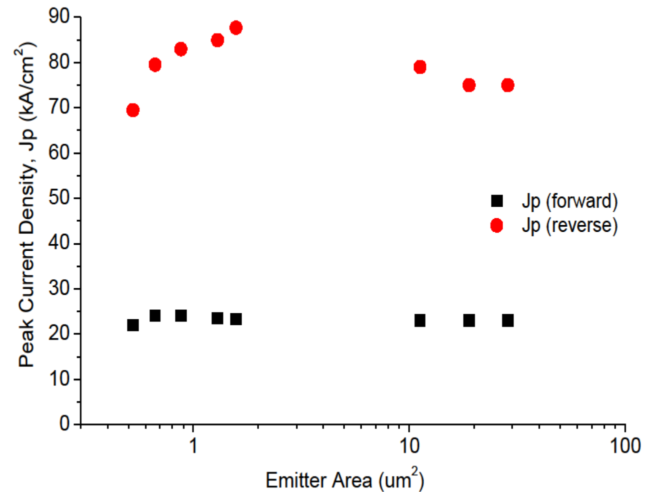

Fig. 7. Measured peak current density against emitter area for sample XMBE277.

Clearly, in the sub-micrometer areas (0.35µm^2, 0.54µm^2 and 0.7µm^2), the RTDs are still able to maintain peak current densities similar to those of the large-areas RTDs (beyond 10 µm^2) at roughly 23 kA/cm^2 in the forward direction and around 80 kA/cm^2 when negatively biased. This excellent scalability reveals at least two important aspects for this work. Firstly, the new sub-micrometer process is indeed robust, considering there is no degradation in the value of peak current density. This simply means the current adjusts its value corresponding to the changes in the device mesa area.

Secondly the reactive-ion-etching (RIE) process, using (CH_4:H_2) is working as intended. The importance of using RIE, as opposed to wet-etch at sub-micrometer lateral dimension has been discussed extensively by Tchego *et.al* [12]. Small area devices usually suffer from high series resistance due to undercut effect known to be caused by lateral etching for emitter size < 10 µm^2. Since the effective emitter area is reduced, this significantly decreases nominal peak current density, J_p.

By introducing a sub-micrometer processing for the RTDs, the CH_4 RIE process to obtain an almost vertical or anisotropic side-wall for the device, becomes mandatory. Reactive-ion-etching using ionised gas is beneficial in terms of having an anisotropic side-wall. But this is at the expense of damaging both the side-wall and semiconductor surface [13]. The latter is not a

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problem in this case since the damaged surface is beneficial to ensure good metal adhesion to the semiconductor during metal contact formation using thermal evaporation.

However, we did find that the side-wall damage degrades the DC performance in terms of lowering the peak-to-valley-current ratio (PVCR) due to increased leakage current through the side-wall [14]. Fig. 8 shows that the experimental PVCR is reduced from 5.0 to 3.8 and 6.3 to 4.1 as the emitter area shrinks from 28.62 μm^2 to 0.54 μm^2 in both forward and reverse direction respectively. Even though the side-wall damage can be controlled and minimised, this has not implemented in this work, at least at this stage. Nevertheless there is also a tendency for the peak to valley current ration to decrease as the lateral sizes decrease, as seen in other work [15] thus the reduction cannot be solely be attributed to the reactive-ion-etching process.

An interesting development in sub-micrometer III-V Esaki Tunnel Diode (ETD) fabrication was reported by Pawlik *et.al* [16]. Their sub-micrometer radius of 350nm is patterned by electron beam lithography but the final radius is reduced to sub-100nm by undercut due to mesa wet-etching. Similar work has been carried out by Romancyzk *et.al* [17] with modified doping level of ETD layers. Both authors reported no significant degradation in peak-to-valley-current ratio with respect to scaling down of the junction area.

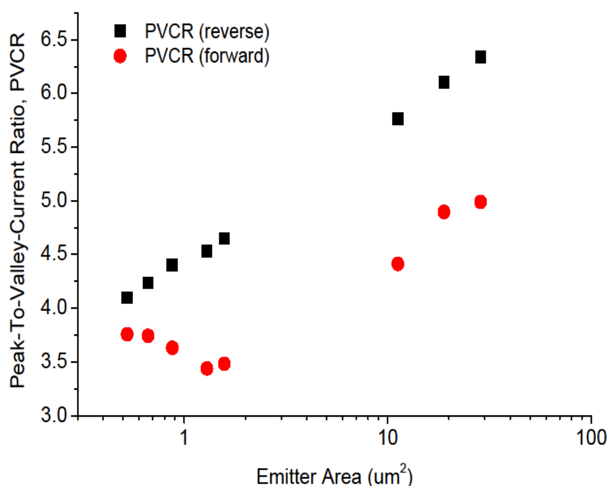

Fig. 8. Measured peak-to-valley-current ratio against emitter area for sample XMBE277.

V. CONCLUSION

We have developed an alternative processing technique to obtain sub-micrometer resonant tunnelling diodes without the need for electron beam (EB) lithography or any other complicated techniques. The feature size shrinkage is controllable through parameters such as initial feature size opening, temperature and reflow time.

In our studies, the values of peak current densities, J_P were uniform throughout the entire range of emitter areas. This technique evidently produced excellent device scalability, good repeatability and a simple process. Most importantly, this new method provides an economical solution to produce resonant tunnelling diodes with sub-micrometer lateral dimensions.

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