Design, Construction and Evaluation of a Power-Dense 12 V to 48 V Bidirectional DC-DC converter for Automotive Applications

DESIGN, CONSTRUCTION AND EVALUATION OF A POWER-DENSE 12 V TO 48 V BIDIRECTIONAL DC-DC CONVERTER FOR AUTOMOTIVE APPLICATIONS

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List of Abbreviations

3D	Three dimensional
AC	Alternating current
AlN	Aluminium nitride
ANSI	American National Standards Institute
APU	Auxiliary power unit
CCM	Continuous current mode
Cu	Copper
DBC	Direct bond copper
DC	Direct current
DCM	Discontinuous current mode
EV	Electric vehicle
EMI	Electromagnetic interference
ESR	Equivalent series resistance
GaN	Gallium nitride
HEV	Hybrid electric vehicle
IPT	Interphase transformer
kW	Kilowatts
MLCC	Multilayer ceramic capacitor
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
Oz.	Ounce
PCB	Printed circuit board
PFC	Power factor corrected
PHEV	Plugin hybrid electric vehicle
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
T-Clad	Thermal clad
TIM	Thermal interphase material
ZVS	Zero voltage switching
µm	Micro meter
µF	Micro farad

List of Symbols

A	Cross-sectional area	ILmax	Maximum of input inductor current
Ae	Effective cross-sectional area of a magnetic core	ILmin	Minimum of input inductor current
A_L	Inductance factor	I_{L11}	Current in IPT winding one
Aw	Window area of a magnetic core	I_{L22}	Current in IPT winding two
ΔB	Peak to peak AC flux ripple	I_{peak}	Peak current in IPT winding
B	Flux density	Io	Average output current
Bac	AC flux density	It	MOSFET current
Bac_{peak}	Peak of AC flux density	It_{RMS}	RMS MOSFET current
B_{max}	Maximum flux density limit for core saturation	k	Thermal conductively
C	Capacitance	l	Length
D	Duty ratio	lg	Air gap in magnetic cores
E	Air gap width in a magnetic core	L	Inductance of input inductor
f	Frequency of flux density inside of a magnetic core	L_{diff}	IPT differential inductance
F	Fringing flux factor	Lin	Input inductor
fsw	Switching frequency	L11	IPT winding one
h	Height	L22	IPT winding two
H	Magnetic field intensity	N	Turn number in a magnetic winding
ΔI_{diff}	Peak to peak ripple in IPT differential current	Pc	MOSFET conduction loss
ΔI	Peak to peak ripple in input current	Pcr	Magnetic Core loss
ΔI_L	Peak to peak ripple in input inductor current	P_{cu}	Copper loss
ΔI_{peak}	Peak of inductor current ripple	P_{dcon}	MOSFET body diode conduction loss
Ic	Output capacitor current	P_{drr}	MOSFET body diode reverse recovery loss
I_{cin}	Input capacitor current	Pg	Magnetic Gap loss
Id	Diode current	Psw	MOSFET switching loos
I_{diff}	IPT differential current	Prr	Loss in MOSFET due to diode reverse recovery
ig	MOSFET gate current	Pt,Ptt	Total loss in MOSFET
Iin	Input current	Pdt	Total loss in MOSFET body diode
I_L , I_{Lin}	Input inductor current	P_{Lin}	Total loss in input inductor
I_{Lav}	Average input inductor current	P_{IPT}	Total loss in IPT

Q_{plt}	MOSFET gate to drain Miller Plateau charge	ΔVo	Peak to peak ripple in output voltage
Qrr	MOSFET reverse recovery charge	Vcom	Voltage of the centre-tap of IPT
Q_{th-p}	MOSFET threshold to plateau gate charge	Vdiff	Voltage across IPT output terminals (Differential voltage)
R	Electrical Resistance	V_{FM}	MOSFET body diode forward voltage drop
R_{ds}	MOSFET drain to source resistance	Vg, V_{gs}	Gate to source voltage for MOSFET
R_g	MOSFET internal gate resistance	$V_{gs(th)}$	Threshold gate to source voltage for MOSFET
R_{thj-c}	MOSFET junction of case thermal resistance	Vin	Input voltage
R_θ	Thermal resistance	V_{Lin}	Voltage across input inductor
SA	Convective surface area	Vo	Output voltage
ΔT	Change in temperature	V_{plt}	MOSFET plateau voltage
t	Thickness	W	Width
trr	MOSFET reverse recovery time	Z_{drv}	Gate drive impedance
Tc	MOSFET case temperature	δ	Ratio of the inductor current fall time to switching period in DCM operation
Th	Heat sink temperature	μ_o	Permeability of air
Tj	MOSFET junction temperature	μ_e	Relative permeability
T	Switching period	ρ	Resistively of copper
Ts	Substrate temperature		

Abstract

Power dense and highly efficient converters are becoming very important in the electric vehicle industry. They have the capability of reducing the power consumption of an electric vehicle by reducing the overall weight of the vehicle. This dissertation report introduces a 1.5kW power dense and highly efficient DC-DC bidirectional converter (12V to 48V). Planar magnetics, thermally conducting substrate, and double-sided cooling semiconductor devices were used to design this converter. Interphase transformer based dual interleaved boost topology was chosen for the converter. A full bridge configuration was selected to ensure bidirectional power flow in the circuit. Semiconductor devices, magnetic cores, capacitors, heat sink, and connectors were selected based on the electrical, mechanical, and thermal optimization of each component. The power circuit layout was done on a thermal clad board in a careful manner to ensure symmetry and low parasitic impedance. After testing the converter, the results were analysed based on the steady state and dynamic operation of an interphase transformer based dual interleaved boost converter. All the waveforms were found to be in close proximity with the theory and specifications. The planar interphase transformer showed a high coupling and good current sharing between its windings. The power loss and temperature of different components were found closely matched with design predictions. An efficiency of around 94% was found in both boost and buck mode of operation at the rated condition. With the heat sink and without the heat sink, the power densities were found 1.8 kW/litre and 5.1 kW/litre, respectively. The designed converter showed that a high efficiency and a high power density can be achieved with off-the-shelf components. This converter can be used in an electric vehicle to interface auxiliary loads with the 12V battery. It can also be used in an aircraft or in an electric ship for the same purpose.

Declaration

No portion of the work referred to in the dissertation has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning

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Chapter1: Introduction and Literature Review

1.1 Introduction

One of the major limiting factors for widespread take-up of electric vehicles (EV) in the current automotive market is the size, efficiency and cost of power electronic converters. These converters are used to interface energy sources like batteries, fuel cells, and super capacitors with electrical loads such as motors, actuators, and other electrical appliances. Usually they convert power from a low DC voltage to a high DC voltage and then to an AC voltage. Similar arrangement can also be found in electric aircrafts, electric ships, and solar photovoltaic systems. A power dense and highly efficient converter can reduce the overall system mass; thereby fuel and energy consumption in EV, aircraft, or ship can be reduced, making them greener. A power dense system will process higher power than the conventional system in per unit volume or mass of that system. However, electrical, mechanical, and thermal stress on the system will be increased. Therefore, increasing the power density of these converters while maintaining a decent efficiency is one of the main challenges for the green initiative in transportation sectors.

Several types of electric vehicles have been introduced in the past two decades in the automotive industry. Hybrid EV (HEV), fuel cell EV, and plug-in hybrid EV (PHEV) are the three major types, which became popular in the market. Though pure electric vehicle (no combustion engine) is the most efficient and cleanest technology it has not got the support as much as other three types because of its higher production cost, greater dependence on grid power, longer battery charging time, and smaller range of operation [1]. In HEV a combustion engine's output is combined with an electrical motor's output to run the vehicle. A rechargeable battery is an essential component in HEV. HEV has transitioned from micro hybrid to mild hybrid and then to full hybrid where the electrification has increased gradually. The electric component of full HEVs like Toyota Prius, Lexus, BMW X6, Mercedes M-Class Hybrid, and Volkswagen Touareg TSI Hybrid not only supply power to all electrically driven accessories and the traction motor but also has the capability to operate the vehicle in electric mode alone [2]. In a fuel cell EV, the combustion engine is replaced by the hydrogen fuel cell, which ensures zero emission. However because of the poorly regulated output voltage a battery or a super-capacitor is essential in the power train. Again with the high cost and other unresolved technical issues such as hydrogen storage technology, natural gas reformers and bi-product water treatment, this technology still remains in the research and development phase [3]. PHEV has additional advantage over HEV because of its ability to recharge the battery from any suitable electrical socket. PHEVs like Toyota Prius Plug-in, Chevrolet Volt and Mercedes Vision S500 Plug-in Hybrid have the capacity of all-electric driving for a distance equivalent to the daily average urban driving, i.e. from approximately 15 to above 100 km [2]. Also with respect to the source to wheel efficiency they are considered as the most viable solution for the present day EV market [1].

The electrical network inside EVs is diverse and there is no specific standard at present. With respect to driving the main traction motor, there are series (engine and battery in series), parallel (engine and battery in parallel) and series-parallel configuration. In each case a high power DC-DC converter (several kilowatts range) interfaces the battery with the traction motor drive by converting 200-300V at the battery end to 500-700V at the drive inverter end. Sometimes super capacitor or flywheel is used as peak power buffer. A lower power DC-DC converter interfaces them with the high voltage DC link. Now another essential part of the EV power train is Auxiliary Power Unit (APU). This is a system with DC-DC converts, 12V and 42V batteries, and auxiliary loads such as head lamps, horn, wiper blade motor, power steering (EPS), navigation system, radio, air-conditioner etc. The low power DC-DC converter connects auxiliary loads to the main power train through a 12V or 42V battery [4]. Another similar type of DC-DC converter used in Toyota Lexus, General Motors' GMC Yukon, and Chevrolet Tahoe hybrid converts 300V at the battery end to 42V at the higher power electronic steering end [5].

Apart from configurations described above some HEVs use integrated starter alternator system where the main engine is coupled with a belt-driven starter alternator to power up the APU [3]. Fuel cell or battery based APU is also considered to generate power at 42V with higher efficiency [3]. Whichever configuration is used, the 42V/12V dual voltage architecture has been considered most viable for the APU because of the ever increasing power demand in EV. So one of the opportunities of research in the development of APU in EV is to couple these two buses in a way that the most efficient and stable arrangement can be achieved. Another option is to use the single 12V or 14V conventional architecture and to use separate DC-DC converters for higher power loads (42V or 48V). In either case development of a power dense and highly efficient bidirectional DC-DC converter is crucial for future APUs in electric vehicles.

A 12V to 48V power dense bidirectional DC-DC converter was constructed in this project using some cutting edge technologies like high power planar magnetics, thermally conducting substrate and double-sided cooling semiconductor switches. Surface mount components were used throughout the whole circuit. All the components were chosen by considering electrical, mechanical and thermal optimization of the converter circuit. A high efficiency of around 94% was found at the rated power of 1.5 kW. Although the chosen voltage conversion level was 12V to 48V, changing the duty cycle of switches, other voltage conversion levels, i.e. 12V to 42V or 14V to 42V can be achieved easily.

1.2 Aim and Objectives

The aim of this dissertation project was to design, construct and evaluate a 12V to 48V power dense and highly efficient bidirectional DC-DC converter for the auxiliary power unit of an electric vehicle. A number of objectives were selected: i) selecting a suitable topology for the converter, ii) selecting a suitable substrate, iii) selecting suitable semiconductor device, iv) identifying

fabrication methodology for magnetic components, v) selecting appropriate cores for magnetic components, vi) selecting suitable capacitor, vii) identifying the loss and calculating temperature in different components, viii) building the 1.5 kW converter, ix) testing the converter, x) verifying loss calculation by measuring temperature in different components, xi) achieving a target efficiency of 92% at rated condition, and xii) identifying achievable power density for 1.5 kW DC-DC bidirectional converter with commercially available materials.

1.3 Literature Review

Several publications during last five decades have showed the development of power dense converters for different applications. Yet few publications have been found proposing the design of a power dense converter for the auxiliary power unit of an electric vehicle. This section presents a review of literatures on power net architectures in EV, power dense DC-DC converters, power MOSFETs, magnetic components, converter circuit construction methods and thermal management techniques.

1.3.1 Power Net Architectures in Electric Vehicles

Several powertrain structures were considered for electric vehicles in past two decades. All major structures are illustrated in Appendix A1. Reference [3] and [6]-[8] gave a summary of most popular powertrain configurations such as series, parallel, series-parallel, series with peak power buffer, fuel cell, and plug-in system. Reference [2] demonstrated the usage of these configurations in recent electric vehicle models. Figure A1.1 of Appendix A1 shows typical powertrain configuration of series, parallel, and series-parallel hybrid electric vehicles. In the series configuration, engine and battery are connected in series through an alternator and rectifier. The alternator is usually a three phase permanent magnet machine or an induction machine and the rectifier is a three-phase controlled rectifier [3]. The engine only supplies power to the battery to uphold its state of charge to a desired level [7]. A high power bidirectional DC-DC converter interfaces the high voltage battery to the traction motor drive (three phase inverter), which also helps the battery to get charged during regeneration. A smaller power unidirectional DC-DC converter charges the 12V battery through which power is supplied to auxiliary loads. Sometimes the inverter of the air-conditioner is coupled with the 12V battery. Though the series hybrid has the advantage of low fuel consumption, the two energy conversion stages between the ICE and wheels decrease its efficiency [7].

In parallel configuration both the engine and traction motor are connected to the vehicle transmission through a torque coupler (example Toyota Prius) [6]. Other parts of the power train remain almost same as series HEV. There is also an alternative configuration without any alternator between the engine and the coupler [7]. Engine operates alone during high speed operation and the motor operates alone during low speed operation [7]. Its continuously variable

transmission system helps to choose the most efficient operating points for the engine for a specific torque demand [7]. So the overall drivetrain efficiency is higher than the series HEV. Yet, parallel HEV needs a complex control system [6]. In series-parallel hybrid there is an additional mechanical link between the alternator and the motor. The power split determines the operational strategy such as engine intensive or motor intensive operation. It has some combined advantages of series HEV and parallel HEV, but the control system is more complicated and more expensive [7].

Sometimes high voltage super-capacitors (SC) are used instead of battery in the main power train or they can be used as peak power buffer. Super-capacitor or flywheel based energy storage ensures improved vehicle performance by decoupling its energy and power requirements [9]. It ensures extended lifetime of the primary source, which is now independent from high power demand. Also the vehicle can give consistent response independent of status of the primary energy source [9]. A bidirectional DC-DC converter is used for capturing energy during regenerative breaking. This converter has complex control as super-capacitor voltage varies with respect to its state of charge [8].

In a fuel cell based HEV, depending on the load condition, fuel cell's output voltage varies. So a unidirectional DC-DC converter is required in the main power train to interface it with the battery or super-capacitor. In an alternative case (Toyota Fuel Cell Vehicle) where the battery or super-capacitor's voltage is less than the main powertrain voltage, another bidirectional DC-DC converter is used to interface the fuel cell stack with the traction drive inverter [3].

In a plugin hybrid, a high energy density battery pack can be charged from an external socket [6]. Because of its similarity with the HEV, auto manufacturers have converted old models to this new configuration by adding new high energy density battery packs in it [6]. The battery charger (AC-DC converter) has to be a power factor corrected (PFC) converter because of grid regulations.

In all configurations above, auxiliary loads in connection with the 12V auxiliary battery forms the auxiliary power unit (APU). However, there are alternative configurations with a 42V battery or a fuel cell or a belt driven starter alternator system [3]. Reference [7] proposes different structures for the powertrain of APU using 42V or 12V or dual bus system. In all the cases a low power DC-DC converter is required to interface auxiliary loads to the energy source.

In summary the powertrain configuration in EV has not been standardised yet not only because there are several components in it but also there are several possibilities for combining them within an integrated system. On one hand, the auxiliary loads are increasing continuously and different new configurations are showing new advantages, on the other hand, each configuration has its own disadvantages and a superior system has not found yet for a specific electric vehicle. Nevertheless, plugin electric vehicles are getting the most attention at the moment and the newly

released American National Standards Institute (ANSI) standardization roadmap for U.S. electric vehicle deployment also shows its main focus on plugin EV [10]. However, in all the configurations, high power or low power bidirectional or unidirectional DC-DC converters are essential in both main and auxiliary power trains.

1.3.2 Development of Power Dense Converters

Figure 1.1 shows the basic circuit diagram of unidirectional and bidirectional DC-DC boost converters. In figure 1.1a, only basic components of a boost converter such as inductor, switch and capacitor are shown. In figure 1.1b switches are modelled in detail with their body diodes and intrinsic capacitors, where bidirectional operation can be done by switching one of the switches and by using alternative switch's body diode. Both circuits can operate in two modes: continuous inductor current mode (CCM) and discontinuous inductor current mode (DCM). In both cases the inductor stores energy when a switch is on and then transfers it to the load when the switch is off. The choice of operating mode affects the choice of inductor and semiconductor switch in a specific design. DCM mode operation increases the conduction loss in switches and it also creates electromagnetic interference (EMI) problem. However, DCM mode operation can be advantageous for the bidirectional circuit as zero voltage switching (ZVS) can be done in this case. As the switching loss is very low for ZVS, high frequency operation is possible for this case. [11]

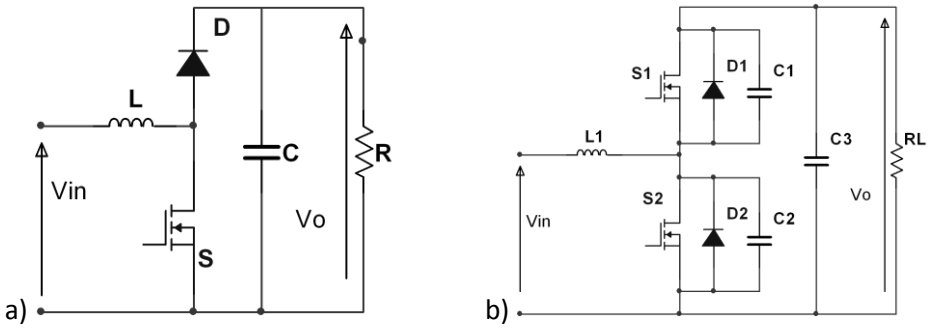

Figure 1.1: a) Unidirectional and b) bidirectional boost converter

In Cuk converter the input current is always continuous in both CCM and DCM mode [11]. However, it is based on the capacitive energy transfer. Reference [12] showed that by using multiple-output and multiple-gap coupled inductors structure for its two inductors, it is possible to get ripple free input current and output current simultaneously. This converter ensures efficient use of magnetic materials and as a result its power density is increased. But the capacitor is stressed as it has to carry large ripple current with a DC voltage across it [11]. The voltage stress across the transistor and diode is higher than the boost converter. The peak current in the switch is also very high as it has to carry both inductors' current.

As the power handling capability of a single boost cell is limited, sometimes they are paralleled for high power operation. Reference [13] showed the design of a 1.5 kW PFC AC-DC converter with eight boost cells operating in an interleaving fashion at DCM mode. The paper showed that

interleaving can increase the power density and power conversion efficiency of a converter by reducing the input current ripple magnitude. Also an optimized design for a converter can be found by predicting appropriate ripple magnitude reduction.

Figure 1.2a and 1.2b show two-phase unidirectional and bidirectional interleaved boost converter respectively. The phases are switched alternatively. As a result the input current ripple is reduced as shown in figure 1.2c. In case of gate pulses with 50% duty ratio, the input current becomes ripple free. The frequency of the input current and the output filter capacitor current also increases without increasing the switching loss [14]. So input and output capacitors sizes are reduced. However, because of high magnitude phase current ripple, inductor's size remains high. The input current remains continuous because of interleaving even in the DCM operation [14]. Nevertheless, the drawbacks of this type of converter are limited voltage conversion ratio, un-equal current sharing between the phases, enhanced complexity in control and the presence of input current ripple [8].

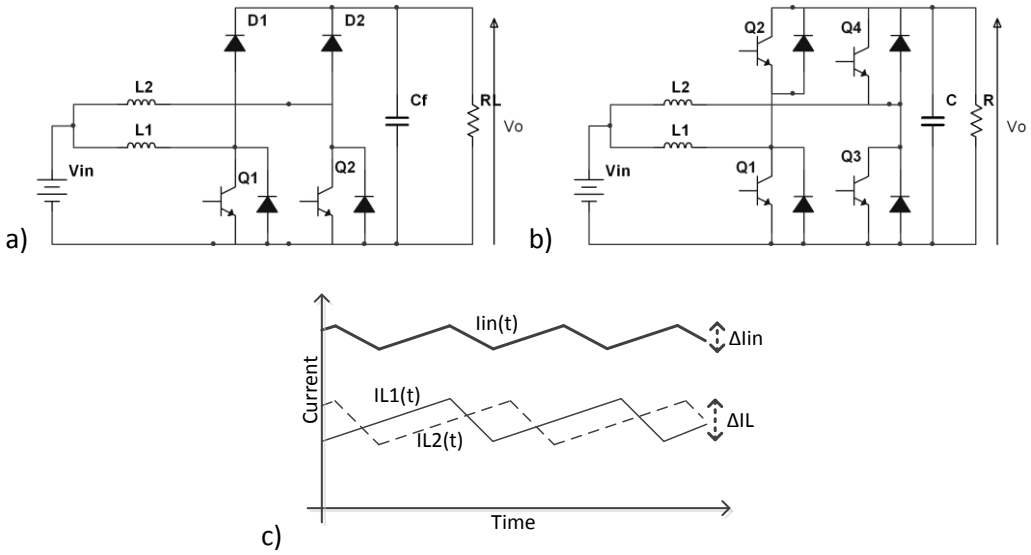

Figure 1.2: a) Unidirectional, b) bidirectional dual interleaved boost converter, and c) ideal input current waveforms

A multi-device interleaved DC-DC boost converter for EV application was shown in [15] where each transistor in figure 1.2a was replaced by a pair of parallel transistors. Although it shows a better performance than the usual interleaved boost converter with respect to efficiency and power density, the technique utilizes semiconductor switches poorly, as the maximum duty ratio for gate pulses in this operation was less than 50%.

Now in figure 1.2a and 1.2b if the two input inductors are coupled in a single core, further size reduction and better current sharing can be found. Reference [16] showed that the closely coupled inductors provided good current sharing between phases even in the presence of large duty cycle mismatch. A steady state analysis was done by modelling the two coupled inductors as a series-parallel combination of three uncoupled inductors. Again drawbacks of this design were

high leakage inductance and high AC ripple current in coupled inductors' windings, which eventually increased the loss.

Reference [17] showed the control of a dual interleaved DC-DC buck converter where the two inductors were inversely coupled to make an interphase transformer (IPT). Because of the inverse coupling in IPT, the DC flux became zero in its core. Using a closed loop proportional integral (PI) controller the volt second imbalance across IPT terminals was compensated. This technique ensured accurate current sharing between IPT windings.

Figure 1.3a and 1.3b show IPT based unidirectional and bidirectional dual interleaved boost converters respectively. References [8], [18-21] showed the design of automotive DC-DC converters using either of these topologies. All of them demonstrated high efficiency and high power density. Using a small valued input inductor, Lin, and closely coupled inductors L11 and L22, it is possible to achieve smaller size and lower loss for magnetic components than loosely coupled inductors in an interleaved boost converter [18]. Using an analytical comparison between circuits in figure 1.2a and figure 1.3a, the following two conclusions were made: i) for the same amount of DC inductive stored energy and same input current ripple, the inductance (L) of Lin in the second circuit was half of the inductance of individual branch inductor in the first circuit and ii) peak flux density was lower in Lin of the second circuit than the first circuit's individual inductors because of lower LΔI value (ΔI is the input ripple current) [19]. So the size and weight of magnetics were lower in the IPT based converter. However, a large DC current was flowing in Lin, so a core with high saturation flux limit was used. Again current ripples in L11 and L22 were high, but that does not hamper the power density as high frequency ferrite cores (low saturation flux and low core loss) were used to design the IPT.

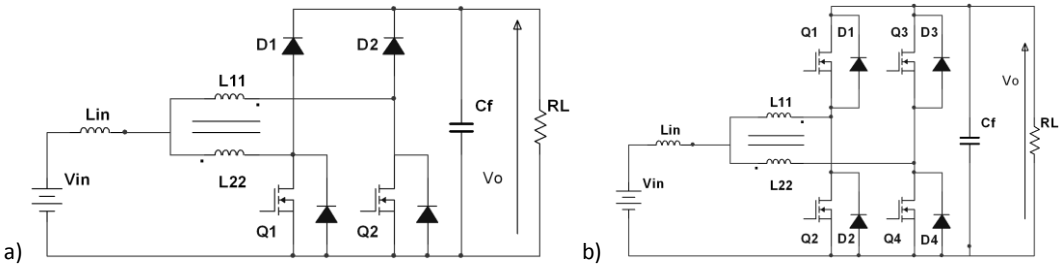

Figure 1.3: IPT based dual interleaved boost converter a) unidirectional and b) bidirectional

ZVS operation is possible by using the bidirectional circuit in figure 1.3b. Analytical calculations in [21] showed that if the ratio between the IPT inductance and the input inductance was low (<0.7), then for a large range of duty ratio and load conditions the circuit remained in DCM, and ZVS operation was achieved with a constant switching frequency.

1.3.3 Low Power Isolated DC-DC Bidirectional Converters for Electric Vehicles

References [4], [22], and [23] showed three designs of highly efficient isolated ZVS DC-DC bidirectional converter for the APU of an EV. A 2.2 kW full bridge DC-DC resonant converter was

demonstrated in [4], which achieved an efficiency of 90% in both buck and boost mode for more than 50% of the rated load condition. In [22] again a full bridge configuration was used along with a control technique which reduced the circulating current in the auxiliary ZVS circuit and thus gave an improved efficiency at even very low load condition. Using controlled duty cycle the 2 kW prototype showed an efficiency of around 93% for 15% to 100% load condition. In [23] a 1.6 kW power dense configuration was shown using a dual half bridge topology and a unified zero voltage switching technique. However the voltage conversion level in all those converters was 12V at the low voltage end and 300V-415 V at the high voltage end.

1.3.4 Semiconductor Devices

The use of silicon (Si) based Power MOSFET for medium power (few kilowatts) DC-DC converters up to 300V, is very common now-a-days [8]. IGBTs are normally chosen for designs where device breakdown voltage is above 1000V [24]. Reference [24] also showed that for operation of above 250V voltage International Rectifier MOSFETs and IGBTs models showed almost equal loss during 50 kHz hard switched and soft switched operation (as of 1997 models).

At present, new advanced packages from the key players of the semiconductor device market are ensuring not only higher thermal capability but also better reliability and power density. Also new technologies such as silicon carbide (SiC) and gallium nitride (GaN) devices have started to enter the market. High frequency and high voltage operation of SiC switches promises lower conduction loss and switching loss and eventually increases the power density of the circuit. SiC JFET based current source back to back converter obtained a power density of 2.4 kW/l [25]. SiC BJT and SiC Schottky diode based 50 kW-70 kHz dual interleaved boost converter showed a power density of 10.5k W/kg [26]. However, major entrepreneur of SiC and GaN devices like Microsemi is still considering SiC devices for high power or high voltage switching applications, and GaN devices for lower power and lower voltage applications [27]. Furthermore, GaN devices are still in the research and development phase and they do not offer the possibility of producing MOSFET [27].

International Rectifier is one of the market leaders in Si based MOSFET and they are offering several packages for various applications up to 250 V range. Their Power QFN package gives a very low on state resistance. Their HEXFET MOSFETs have been used in several automotive applications in past years. The recent advancement is the introduction of DirectFet package which has a 40% smaller footprint than the standard SO-8 package, and an equal footprint with the standard DPak package (around 55 mm^2) [28]. Its 0.77mm surface mounted profile along with the efficient top and bottom side cooling has made it an ideal device for power dense systems [28]. The combination of latest HEXFET Power MOSFET technology with DirectFet package achieves very low on-state resistance for several models with a voltage rating between 40V to 250V [28]. These MOSFETs can be considered ideal for low power low voltage DC-DC automotive converters.

1.3.5 Magnetic Components

Usually the input inductor of a DC-DC converter has to be rated to the converter power. The major factors of designing this type of power inductor are the selection of a suitable core, distribution of core and copper losses, and consideration for the temperature rise and regulation requirements [29]. Reference [8] gave a list of core materials along with their compositions and brief characteristics (table 1.1). The detailed information such as core loss data and core material characteristics can be found in reference [30]. The molybdenum-nickel-iron high permeability magnetic alloys (Mollypermalloy) and High-flux Permalloy cores made its greatest impact in the switching power supply because of its high frequency low loss operation. Iron powder cores (material mix-2,26,52) have high saturation flux density, but they have low permeability, which means they require relatively large number of turns for a specific inductance value. For this reason they were typically used in differential-mode input and output power inductors of power electronic circuits. Thin tape Ni-Fe alloys were used in high frequency power conversion of aerospace for its square or round B-H loop characteristics. Metallic Glass (Metglas) materials are also being used in high frequency applications because of their high induction, high permeability and low core loss. Metglas 2605SC or 2650SA is an appropriate choice for high frequency DC inductors as it has a unique combination of high resistivity, high saturation flux density, and low core loss. For instance, the input inductor of the power dense dual interleaved boost converter in [8] used Metglas 2650SA core. [30]

Recently developed Nanocrystalline soft magnetic cores (Finemet) showed ultra-low power loss and high flux density comparable to amorphous materials. The material composition is 82% iron and the remaining balance is composed of silicon, boron, niobium, copper, carbon, molybdenum, and nickel. The raw material is produced in amorphous state and then it is recrystallized. The annealing process comprises of a precise mixture of amorphous and Nanocrystalline phases, giving the material its unique magnetic properties. This core can be considered ideal for inductors in high power converters or for pulse transformers. For instance, the input inductor of the 18 kW power dense dual interleaved boost converter in [20] used Hitachi Finemet C cores. [31]

Ferrites are homogeneous ceramic materials with a composition of MeF_2O_3. Iron oxide is the main constituent and 'Me' mostly represents manganese and zinc (Mn-Zn) or nickel and zinc (Ni-Zn) [32]. From table 1.1, it is clear that they have the lowest saturation flux density limit. So for very high DC current they are not suitable for use, as they will require a large air-gap between the cores to avoid saturation, which in turn will increase the power loss. However ferrite cores have very low core loss and have been widely used in switched mode power supply (SMPS) circuits [32]. Depending on the SMPS converter type a core is selected based on the switching frequency, operating flux density, the resulting core loss, and ambient temperature [32]. Sometimes

distributed gap structure is used in the ferrite cores to reduce the eddy current loss in the winding as shown in reference [21].

Material	Manufacturer	Composition	B_{max} (T)	μ_e
Mollypermalloy	Magnetics Inc.	Powder core (79% Ni, 17% Fe, 4% Mo)	0.7	14-550
High-flux	Magnetics Inc.	Powder core (50% Ni, 50% Fe)	1.5	14-160
Kool Mμ	Magnetics Inc.	Powder core	1	26-125
Mollypermalloy	Arnold	Powder core (81% Ni, 17% Fe, 2% Mo)	0.7	14-350
High-flux	Arnold	Powder core (50% Ni, 50% Fe)	1.4	14-200
Material mix-26,52	Micrometals	Iron powder	1.4	75
Material mix-8	Micrometals	Iron powder	1.2	35
Supermalloy	Magnetics Inc.	Thin tape 80% Ni-Fe alloy	0.65-0.82	22,000
Square Permalloy	Magnetics Inc.	Thin tape 80% Ni-Fe alloy	0.66-0.82	
Orthonol	Magnetics Inc.	Thin tape 50% Ni-Fe alloy	1.42-1.58	
Metglas Amorphus Alloy 2605SC	Allied Signal Inc.	Tape-wound amorphous metal	1.61	300,000 (max)
Metglas Amorphus Alloy 2605SA	Metglas	Tape-wound amorphous metal	1.56	45000 (as cast)
Ferrites	Ferroxcube, Epcos, TDK	Mn-Zn, Ni-Zn	0.3	2400
Finemet	Hitachi metals, Metglas, MK Magnetics	Tape-wound Nanocrystalline	1.23	30000

Table 1.1: Magnetic core materials and their characteristics [8][18]

Another advantage of ferrite core is its availability in different sizes and shapes; especially in case of planar magnetic design ferrite planar core is the only option. Planar magnetics have become very popular in automotive, aerospace, renewable energy, telecommunication, defence, healthcare, and other industrial applications because of its compact design. Normally a planar winding is formed using flat copper foils or printed circuit board (PCB) tracks and they are sandwiched between the planar ferrite cores to make an inductor or transformer. Proper lamination has to be used between winding layers. The flat package provides a larger surface area which ensures the best heat transfer condition and also helps to maintain a low hot spot temperature [33]. Reference [33-36] showed the design procedure of planar magnetics which was based on PCB layers and planer E cores. Reference [33] illustrated different connections between multilayer PCB windings and investigated the parasitic and thermal behaviour of different prototypes of high frequency planar transformer, based on those connections. The prototypes showed low leakage inductances and very high magnetizing inductances. Also considering both double sided and single sided heat transfer, a moderate temperature rise was found in both cases. References [34] and [35] explained the design calculations for planar magnetic components using PCB layers. Reference [36] showed a design of a 25W DC-DC forward converter using only planer magnetics. The transformer and the output inductor were integrated in six PCB layers for a compact converter design.

Several publications also investigated the design of core structures to reduce the size and weight of the magnetic components. The core of the integrated three inductors of a three-phase interleaved boost converter in [37] had 4 legs (E and I side by side connected with a plate on the top). One common leg (I) was shared by three outer legs corresponding to three phases. The current ripple magnitude reduced in each of the inductors, which was dependent on the reluctance ratio between the outer leg and common leg. As lower reluctance ratio ensured lower current ripple, so two different materials, i.e. ferrite and powdered iron were proposed for the outer legs and common leg respectively [37]. Though the design showed power dense magnetics, the custom core design poses a problem to its practical implementation. The 500W converter in [38] had the same circuit configuration as in figure 1.3a. It demonstrated an integrated design of three of windings within an EI core. The central leg did not have any AC flux as the windings in outer two legs were inversely coupled [38]. The inductors had smaller values and the design showed high efficiency. However, as the windings were loosely coupled, the DC flux was not cancelled in the core, so it can only be useful for low power design. Also leakage inductances were large, which means the core required higher volume to contain residual flux [18].

1.3.6 Converter Circuit Construction

For power electronic converter circuit construction, different approaches have been taken based on their power levels and circuit complexity. For low power converters (less than 300W) where thermal management is not so important, printed circuit board (PCB) has been used widely. Reference [39] showed a 180W prototype of a single stage single switch power factor corrected circuit construction on a single PCB board. The power circuit and the control circuit were closely arranged on the board for compact design. The maximum current of the circuit was 12.8A, so only single sided 1 oz. PCB board (35 µm copper layer) was used for the circuit.

For higher power converter design using PCB there are two options, one is to increase the copper thickness on the PCB board and second is to use the multilayer PCB boards. However, increased copper thickness means fabrication complexity and also widely available commercial PCB boards have highest 2 oz. (70 µm) of copper layer. In reference [25] the SiC based converter used multiple layers of PCB for power circuit, gate-driver, control and measurement circuit, and EMI filter circuit. This compact arrangement was one of the reasons for its high power density.

Again, in higher power application where thermal management is important, insulated metal substrate (IMS) is used. Though aluminium based IMS is the most common type its high thermal expansion rate sometimes make the solder joints unreliable [40]. Therefore, recently aluminium silicon carbide (AlSiC) and copper (Cu) are being used, as they have lower rates of thermal expansion [40]. However, they are expensive. Reference [41] shows a matrix converter where power stage is constructed on an IMS board.

Direct bond copper (DBC) substrate is another suitable option for high power electronics. It consists of thick copper foil cladded to ceramic isolators, alumina (Al_2O_3) or aluminium nitride (AlN). Because of the high heat conductivity of Al_2O_3 (24 W/mK) and AlN (130-180 W/mK), and high heat capacity of copper, this substrate has a very good heat spreading and heat dissipating capability. Its matched temperature co-efficient of expansion with silicon ensures minimum mechanical stress on the silicon die. Also the thick copper coating (200-600 μm) ensures high current carrying capability [42]. In reference [26], all-SiC based converter's power modules were constructed on an AlN based DBC.

Planar bus bar is another alternative for power rails in high power electronics. Because of the small gap between the conductors, planar bus bars pose very low inductance. As they have low characteristics impedance, the noise attenuation also becomes better [43]. Reference [43] showed the design of a bus bar for power electronic circuit with very low stray inductance. EMI was significantly reduced in an inverter with the proposed bus bar. In [8] [19-21], the dual interleaved converters used planar bus bars for their power rails to avoid the overvoltage transient across transistor during commutation period.

Reference [44] demonstrated the volume reduction capability in integrated power electronic modules by using planar substrates and optimized three-dimensional (3D) design. The interesting technique was the design of 3D passive integrated power electronic modules using special bare-unpacked components and electromagnetically integrated components. Though the power density increased by some folds, unconventional component topologies and packages are a challenge for this design.

1.3.7 Thermal Management

Thermal management is an essential criterion for designing high efficiency and high power dense automotive DC-DC converter. Different converters as well as the engine in a HEV need a proper cooling circuit within the vehicle. Based on the position of the circuit in the vehicle and the loss in the circuit, the cooling arrangement is fixed. Quite often, the DC-DC converter of the auxiliary power module is mounted together with the inverter of traction motor to simplify the water cooling circuit (example: Saturn Vue Green Line) [5]. Again, Honda chose to mount the converter close to battery and used air cooling for them together in their Civic Hybrid model [5]. The following table 1.2 gives a list of APU converters in modern HEVs and their cooling arrangements.

Again with respect to cooling loops, many HEVs include one 65°C coolant loop for the power electronic converters and electric motor, and another 105°C loop for the engine [8]. Research has been going on to combine them into a single loop (105° C). The potential problem is the junction temperature of the semiconductor devices, which is limited to around 175° C even with the double sided cooling of an advanced package like DirecFet [45]. This temperature is again limited

to 125°C to increase the lifetime of devices; thus maximum coolant temperature increase is limited to 20°C, hence power dissipation in the device became restricted [8]. New SiC devices have similar junction temperature limit, but they have lower operating loss [25][26][44]. Replacing Si devices with SiC devices showed significant loss reduction (30-40%) in the corresponding circuits, which reduced the thermal management complexity [25][26][44].

Vehicle	Voltage range (V)	Power (kW)	Cooling Arrangement
Honda Civic hybrid	158-13.9	1.3	Forced Air
Toyota Prius THSII	202-500	50	Water
Toyota Prius THSII	202-14		Water
Lexus ES400h	288-650		Water
Lexus ES400h	288-14		Water
Lexus GS450h	288-14	1.8	Air
Ford Escape Hybrid	330-14	1.5	Water
Saturn Vue Green Line	36-14	2	Water

Table 1.2: Cooling arrangement of HEV auxiliary power module converters [5]

1.4 Summary of Literature Review

In this chapter main power train architectures of present-day electric vehicles have been demonstrated. It is clear from the review that no fixed configuration is dominating the current market. Also voltage levels inside an electric vehicle are not standardised and different manufacturers are using different strategies for their power trains. The development of power dense converter topologies in the past five decades has been discussed and it is found that compact magnetics is the key to achieve high power density, as inductors or transformers are responsible for 20-30% of the total converter weight [37]. New emerging magnetic materials with high temperature capability and high flux density limit can be considered ideal for a power dense configuration. With respect to auxiliary power unit, isolated topologies are getting some attention; still it is not a dominant topology in the EV industry. Several new semiconductor switches and new substrates have been reviewed to give the converter a high thermal capability. High power automotive MOSFETs can be considered suitable for low voltage converters in EV.

Interleaved topologies seem attractive for a 12V to 48V automotive DC-DC converter. Compact magnetic design along with proper choice of semiconductors and substrate can give these topologies higher power density and better thermal management. Therefore, it was decided to use planer magnetic components, thermally conducting substrate, and surface mount components, to make this converter compact, efficient and reliable. The next chapter discusses theory and methodology for the proposed converter design.

Chapter 2: Theory and Design of a 12V to 48V IPT based Dual Interleaved Bidirectional Boost Converter

2.1 Introduction

This chapter explains the methodology for designing a 1.5 kW bidirectional DC-DC boost converter. The considered voltage conversion ratio was four, i.e. 12V to 48 V. At first the converter topology was selected based on the loss calculation for switches. It was found that the dual interleaved boost topology with an interphase transformer was an optimum solution for this design. Then the steady state operation of the circuit was analysed and design equations were derived. Finally, different components were selected for an optimized paper design of the circuit.

2.2 Selection of the Converter Topology

The bidirectional boost converter showed in figure 1.1b was considered as the preliminary topology. The circuit operation is explained below. Considering its unidirectional operation, the upper-leg MOSFET was off all the time and the lower-leg MOSFET was doing the switching operation. Currents flowing in input inductor, MOSFET, diode, and capacitor are shown in the following figure 2.1. Figure 2.1a and 2.1b show the continuous conduction mode (CCM) operation and discontinuous conduction mode (DCM) operation respectively.

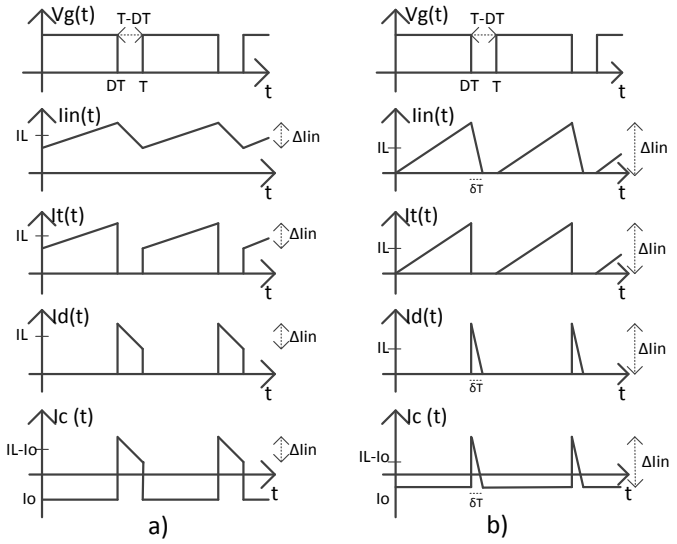

Figure 2.1: Gate voltages, input currents, MOSFET currents, diode currents and capacitor currents in a boost converter for a) continuous mode and b) discontinuous mode operation

Considering steady state operation and applying volt-second balance on inductor current (Iin in figure 2.1), the voltage conversion ratio for CCM operation is found.

$$\frac{\mathrm{Vo}}{\mathrm{Vin}} = \frac{1}{1-\mathrm{D}} \qquad (2.1)$$

Peak to peak ripple magnitude of input inductor current for CCM operation can be written:

$$\Delta I = \frac{VinDT}{L} = \frac{(Vo - Vin)(T - DT)}{L} \quad (2.2)$$

From the capacitor current waveform, the peak to peak output voltage ripple can be written:

$$\Delta Vo = \frac{DTVo}{RC} \quad (2.3)$$

Similarly for DCM operation, the respective equations are given below. Derivation of all the equations for both CCM and DCM operations is given in Appendix A2.

$\frac{Vo}{Vin} = \frac{1+\sqrt{1+\frac{4D^2}{k}}}{2}$, $\Delta I = \frac{VinDT}{L}$, and $\Delta Vo = \frac{\delta T(\Delta I - Io)^2}{2C\Delta I}$; where k= 2L/RT

Now using the MOSFET current waveform from figure 2.1a, the RMS MOSFET current for CCM operation can be written (from Appendix A2):

$$It_{RMS} = \sqrt{\frac{D(ILmax^2 + ILmax * ILmin + ILmin^2)}{3}} \quad (2.4)$$

A moderate switching frequency of 40 kHz was considered for design calculations. Higher switching frequency would have increased the MOSFET switching losses, magnetic core losses and gap losses. Lower switching frequency would have increased the size of magnetic components (from equation (2.2) if T increases then L will also increase for same current ripple). Again as the plan was to use the body diode of upper-leg MOSFET, which generally does not have a very good reverse recovery characteristics, higher switching frequency would have increased the diode reverse recovery loss.

The design specification and preliminary calculations for the converter are shown below in table 2.1. Duty ratio for gate pulse and RMS MOSFET current (It_{RMS}) were calculated from equation (2.1) and (2.4) respectively. A small input current ripple was considered to limit the conduction loss of the MOSFET (from equation (2.4), high ripple in Iin will increase It_{RMS} in the MOSFET).

Specification	Input voltage	12 V	Output voltage	48 V
	Rated power	1.5 kW	Switching frequency, fsw	40 kHz
	Input current ripple	10%	Output voltage ripple	10%
Calculations	Average input current, IL	125 A	Average output current, Io	31.25 A
	ΔIin	12.5 A	ΔVo	4.8 V
	ILmax	131.25 A	ILmin	118.75A
	Duty ratio of gate pulse, D	75%	It_{RMS}	108.3 A

Table 2.1: Design specification and preliminary calculations

A range of power MOSFETs of appropriate voltage (V≥75V) and current rating (I≥160A) were selected from [28]. Only MOSFETs with an on-state drain to source resistance (R_{ds}) less than 5mΩ were considered. For each MOSFET conduction loss, switching loss, and loss due to diode reverse recovery were calculated and from the calculated total loss, junction temperature was predicted. The following equations were used for loss calculations and junction temperature measurement.

MOSFET conduction loos, $Pc = It_{RMS}^{2} * R_{ds}$ (2.5)

MOSFET switching loos, $Psw = Vo * \frac{Io}{2} * fsw * \left(\frac{Qth-p+Qplt}{ig}\right)$, (2.6)

where gate current, $ig = \frac{Vgs-Vplt}{Zdrv+Rg}$ (2.7)

Loss in MOSFET due to diode reverse recovery, $Prr = fsw*Vo*Io*trr + fsw*Vo*Qrr$ (2.8)

Total power loss in a MOSFET, $Pt = Pc + Psw + Prr$ (2.9)

Junction temperature in the MOSFET, $Tj = Pt*R_{thj-c} + Tc$ (2.10)

Equations (2.6)-(2.8) were adapted from reference [8] and [46]. Equation (2.10) was adapted from Reference [47]. Here Q_{th-p} is the required gate charge for increasing the gate voltage from the minimum threshold ($V_{gs(th)}$) level to the plateau voltage (V_{plt}) level. Q_{plt} is the gate to drain Miller Plateau charge and R_g is the internal gate resistance. In equation (2.8), trr and Qrr are the reverse recovery time and reverse recovery charge for the MOSFET body diode, respectively. In equation (2.10), R_{thj-c} is the junction to case thermal resistance and Tc is the case temperature. Tc and Vgs were assumed 100° C and 10V respectively. All other parameters were calculated or taken from the respective datasheets of the MOSFETs considering the worst case scenario.

Model	Voltage (V)	Rds (mΩ)	Pc (W)	Vplt (V)	Rg (Ω)	ig (A)	Qth-p (nC)	Qplt (nC)	Psw (W)	trr (ns)	Qrr (nC)	Prr (W)	Pt (W)	Rthj-c (°C/W)	Tj (°C)
IRF7759L2TRPBF	75	2.3	27.0	5.0	1.1	0.8	11	75	3.1	96	225	6.2	36.3	0.25	109.1
IRFS3107-7PPBF	75	2.6	30.5	5.2	2.1	0.7	18	57	6.7	63	160	4.1	41.2	0.40	116.5
IRFS3107PBF	75	3	35.2	5.0	1.2	0.8	16	54	5.2	60	132	3.9	44.2	0.40	117.7
IRF2907ZS-7PPBF	75	3.8	44.6	7.2	2.6	0.4	30	66	15.6	53	85	3.3	63.5	0.50	131.8
IRFS3207Z-PBF	75	4.1	48.1	4.5	0.8	0.9	12	33	2.8	62	100	3.9	54.8	0.50	127.4
IRLS4030-7PPBF	100	3.9	45.7	3.4	2.0	0.9	17	43	3.8	63	155	4.1	53.6	0.40	121.5
IRFS4010-7PPBF	100	4	46.9	5.5	2.1	0.6	26	48	7.0	67	180	4.4	58.3	0.40	123.3
IRLS4030PBF	100	4.3	50.4	3.6	2.1	0.9	15	45	4.0	60	130	3.8	58.3	0.40	123.3
IRFS4010PBF	100	4.7	55.1	5.8	2.0	0.6	18	50	6.8	81	268	5.4	67.3	0.40	126.9

Table 2.2: Junction temperature calculation for different MOSFETs

In the above analysis, all the MOSFETs have the maximum junction temperature of 175° C. However, as discussed in the section 1.3.7, a maximum operating junction temperature of 125° C is preferred for the sustainability of the device. As all the MOSFETs were showing an operating temperature close to the limit, it was essential to parallel two MOSFETs for present design specification. Also as the combined switching loss and loss due to diode reverse recovery was

significantly lower than the conduction loss, it was decided to use hard switching for the converter.

From literature review it was found that interleaved boost converter with interphase transformer showed significant high power density and high efficiency in the previous models. As two parallel branches of MOSFET had to be used, it was decided to use the IPT based dual interleaved boost converter for the design. The next section describes the steady state operation of this topology.

2.3 Steady State Operation of IPT based Dual Interleaved Boost Converter

To discuss the steady state operation of the interphase transformer (IPT) based dual interleaved boost converter, the converter circuit is drawn again in the following figure 2.2. The circuit operation is adapted from [8]. An input capacitor (Cin) is added to the circuit to supply the input ripple current to the converter and thereby ensures ripple free input current from voltage source. The purpose of the input inductor (Lin) is to filter the input current. The interphase transformer is made with two inversely coupled inductors. The coupling coefficient between the identical IPT windings is very high and if perfect current sharing is assumed between them, the DC flux will be zero inside the IPT core. However, there will be a large DC flux inside the input inductor. Therefore, different core materials have to be chosen for IPT and input inductor to ensure high efficiency. There will be AC flux in both Lin and IPT whose magnitude will be dependent on the input ripple specification, voltage levels across them, and their respective inductance values.

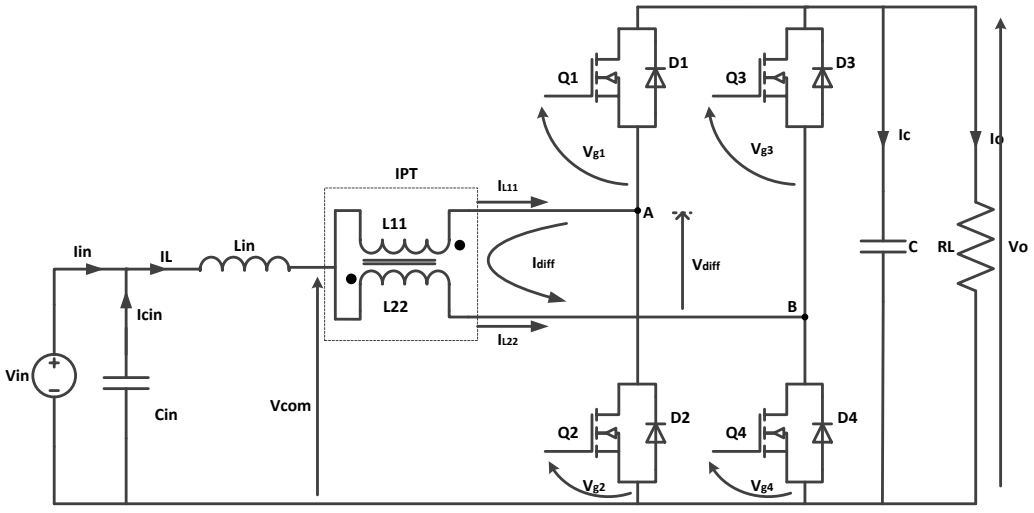

Figure 2.2: IPT based dual interleaved bidirectional boost converter

The four MOSFETs (Q1-Q4) will ensure bidirectional power flow in the converter. If Q1 and Q3 remain always off and Q2 and Q4 are switched on and off in an interleaved fashion, then the boost operation will happen. Conversely, if Q2 and Q4 remain always off and Q1 and Q3 are switched on and off in an interleaved fashion, then the buck operation will happen. Finally, an output capacitor (C) and a resistive load (RL) are considered at the output of the converter. The output capacitor filters the ripple from the converter output current. Only boost operation is

explained in this section for three operating criteria for the MOSFETs Q2 and Q4: duty ratio, D<0.5, D>0.5 and D=0.5.

Ideal steady state waveforms for D<0.5 and D>0.5 are shown in figure 2.3a and 2.3b. Vg2 and Vg4 are the gate pulses to MOSFETs Q2 and Q4. Vcom is the voltage of the centre-tap of IPT. For D<0.5, if one MOSFET is on, Vcom has a value of Vo/2, because of voltage divide across the IPT windings. Again, if both MOSFETs are off, Vcom has a value of Vo. For D>0.5, when both MOSFETs are on, the value of Vcom is zero. V_{Lin} is the voltage across input inductor, which is equal to the difference between Vin and Vcom. I_L is the input inductor current and ΔI_L is its ripple. Both Vcom and I_L have a double switching-frequency. V_{diff} is the voltage across output terminals (A and B) of IPT and I_{diff} is the differential loop current flowing inside of the IPT. It is assumed that the inductance of the IPT, L_{diff} , is very small compared with Lin and accordingly ripple in the differential loop current (ΔI_{diff}) is also very small compared with ΔI_L. I_{L11} and I_{L22} are the two IPT winding currents where $I_{L11} = I_L/2 - I_{diff}$ and $I_{L22} = I_L/2 + I_{diff}$. The averages of both of them are equal to the half of the average of input inductor current (I_{Lav}). Finally, capacitor current (Ic) is found based on the switching condition of the MOSFETs.

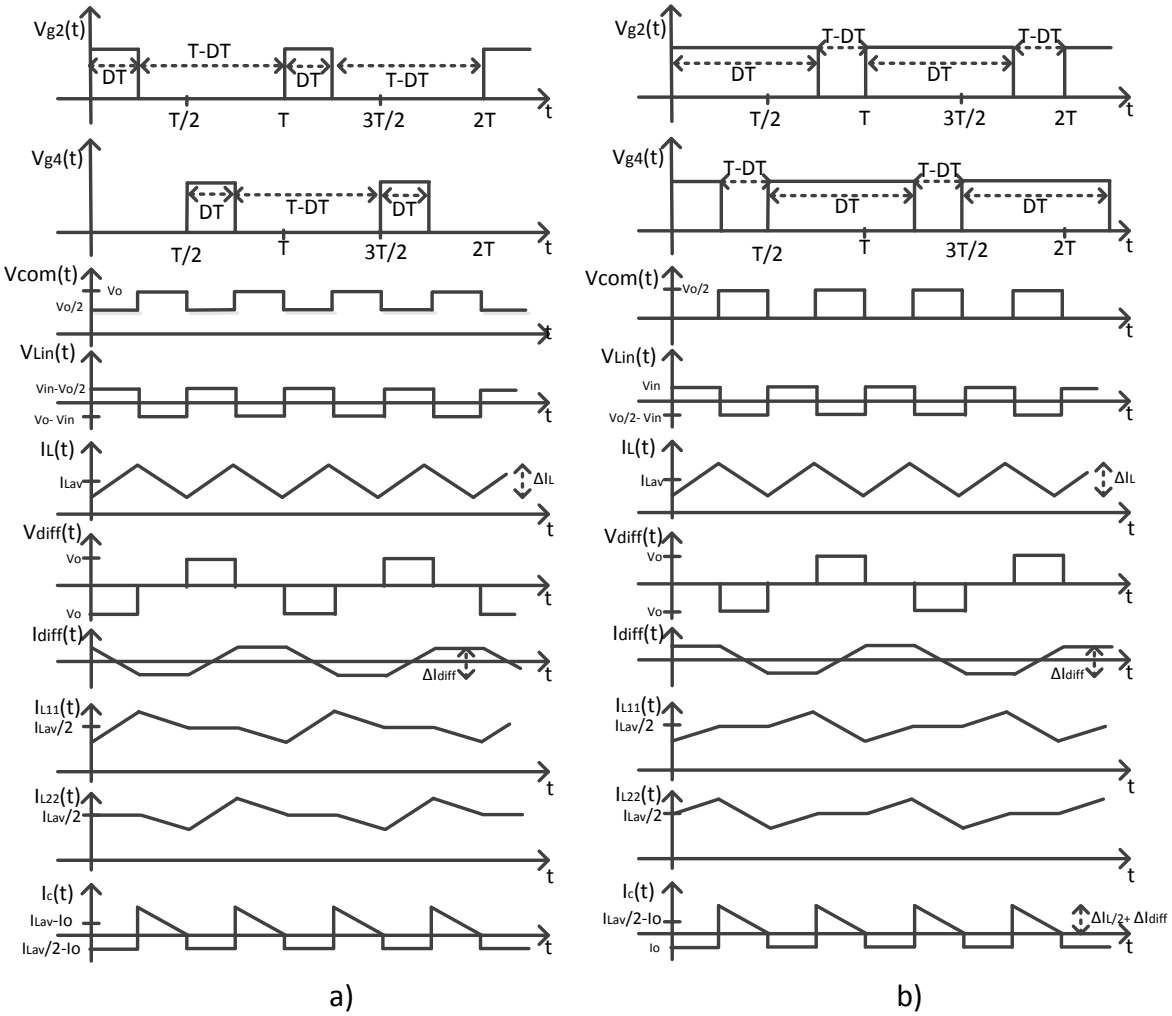

Figure 2.3: Ideal steady state waveforms in dual interleaved boost converter for a) D<0.5 and b) D>0.5

Figure 2.4 shows the respective ideal wave-shapes for D= 0.5. It is clear that V_{com} is fixed at half of the output voltage, which is also equal to the input voltage. Voltage across input inductor is zero and its current is ripple free. V_{diff} becomes a square wave of ±Vo. In a similar manner with the previous case I_{diff}, I_{L11}, I_{L22}, and Ic currents are found. Ripple in the IPT differential loop current (ΔI_{diff}) is maximum in this case because of the square wave nature of V_{diff}.

In both figure 2.3 and 2.4 it is assumed that the MOSFETs are switching instantaneously, i.e. $\Delta I_{in}/2 = \Delta I_{diff}$ and there is no stray impedance in the circuit. Now considering volt-second balance on the inductor currents for D<0.5 and D>0.5 the voltage conversion ration of the circuit is found.

From V_{Lin} waveform of figure 2.3a (D<0.5),

$(Vin - \frac{Vo}{2})*DT = (Vo - Vin)*(\frac{T}{2} - DT)$,

therefore, $\frac{Vo}{Vin} = \frac{1}{1-D}$ (2.11)

Again from V_{Lin} waveform of figure 2.3b (D>0.5),

$Vin*(DT - \frac{T}{2}) = (\frac{Vo}{2} - Vin) * (T-DT)$,

therefore, $\frac{Vo}{Vin} = \frac{1}{1-D}$

So, in both cases the voltage conversion ratio is exactly same as conventional boost converter. Also for D=0.5 the relationship holds, as Vo = 2Vin in that case.

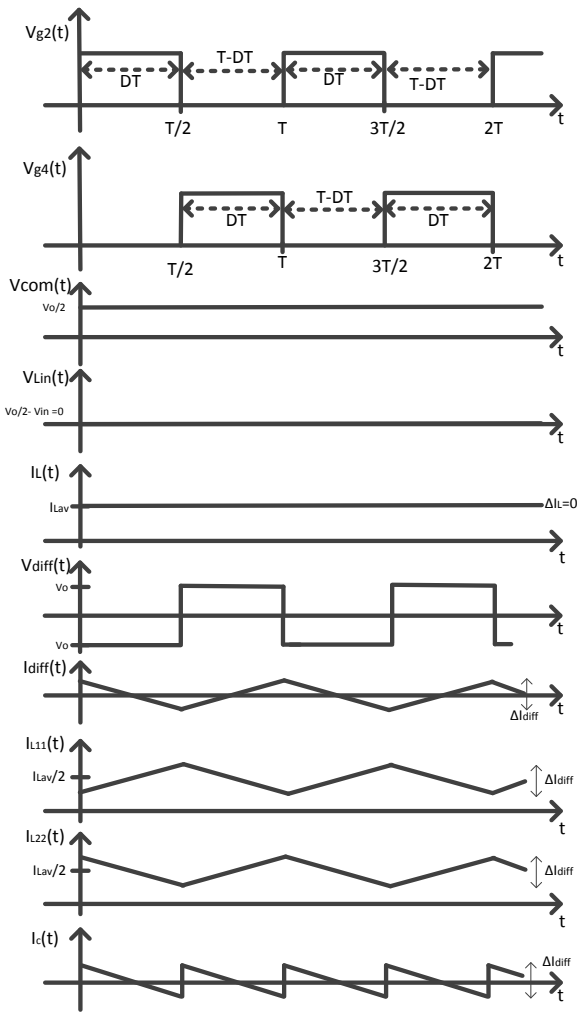

Figure 2.4: Ideal steady state waveforms in dual interleaved boost converter for D=0.5

From figure 2.4, V_{Lin}= Vin – Vcom = Vin - Vo/2 = 0, therefore, Vo= 2Vin.

Now the peak to peak ripple in the input current can be found using basic inductor voltage equation, V= L di/dt.

From I_L waveform of figure 2.3a (D<0.5),

$\Delta I_L = \frac{\left(Vin - \frac{Vo}{2}\right)DT}{Lin}$, now substituting Vo = $\frac{Vin}{1-D}$

$\Delta I_L = \frac{VinDT\,(1-2D)}{2Lin*(1-D)}$ for $0 < D \leq 0.5$ (2.12)

Again from I_L waveform of figure 2.3b (D>0.5),

$\Delta I_L = \frac{Vin(DT-\frac{T}{2})}{Lin}$,

Or, $\Delta I_L = \frac{VinT\,(2D-1)}{2Lin}$ for $0.5 \leq D < 1$ (2.13)

By comparing equations (2.12) and (2.13) with equation (2.2), it is clear that the ripple in dual interleaved boost converter is significantly reduced. For 0<D< 0.5, $\Delta I_L = \frac{\Delta I(1-2D)}{2(1-D)}$ and for 0.5≤D<1, $\Delta I_L = \frac{\Delta I(2D-1)}{2D}$ where ΔI is the ripple in the conventional boost converter.

Now again using the basic inductor voltage equation, V= L di/dt, the peak to peak ripple in the IPT differential loop current (ΔI_{diff}) can be found.

From the V_{diff} waveform of figure 2.3a (0 < D < 0.5),

$\Delta I_{diff} = \frac{VoDT}{Ldiff}$ (2.14)

From the V_{diff} waveform of figure 2.3b (0.5 < D < 1),

$\Delta I_{diff} = \frac{Vo(T-DT)}{Ldiff}$ (2.15)

Also from figure 2.4 when D=0.5, maximum ΔI_{diff} was found equal to $\frac{VoT}{2Ldiff}$, which is in accordance with equations (2.14) and (2.15).

Ripple in the output capacitor current changes with load similar to the conventional boost converter. The wave-shape of charging capacitor current in both figure 2.3a and 2.3b depends on the shape of IPT winding currents in that period. However, for discharging current the situation is different. In figure 2.3a for D<0.5 , when only one MOSFET is on ('DT' period), the capacitor current shape will be dependent on the shape of IPT winding current in that period. As it is assumed in figure 2.3 that $\Delta I_{in}/2 = \Delta I_{diff}$, the capacitor current waveform in that period has a zero gradient (fixed value of '$I_{Lav}/2$ –Io'). But in other cases it may have positive or negative slopes depending on the input current ripple and IPT differential current ripple. However, in figure 2.3b for D>0.5, this situation will never come, because during the discharging period of capacitor both MOSFETs are on. The discharge current of capacitor is always fixed to the value of output current, Io. For this reason, a generalised output voltage ripple equation can be written for D>0.5 using the area under capacitor discharging current.

$\Delta Vo = \frac{\int Iodt}{C} = \frac{Vo(DT-\frac{T}{2})}{RC}$,

Therefore, $\frac{\Delta Vo}{Vo} = \frac{(2D-1)T}{2RC}$ for $0.5 \leq D < 1$ (2.16)

Based on the above theoretical analysis of IPT based dual interleaved boost converter, the following section will describe how the most suitable components were selected for the circuit.

2.4 Selection of Components

Different components were selected based on the electrical, mechanical and thermal optimization of the proposed converter. At first a substrate was selected for the power stage where all the components would be mounted. Then a suitable MOSFET was selected based on the power loss and junction temperature calculations. After that appropriate cores for input inductor and IPT were selected based on converter design calculations. Then a proper capacitor was selected based on the output ripple voltage specification and RMS capacitor current calculation.

2.4.1 Substrate

From the literature review it was found that thermally conducting substrate and planar bus bar would be the two best options for a power dense converter. Considering the benefits of thermally conducting substrate such as better thermal performance, possibility for combined power and control circuit construction, and less complicated design process, it was selected for the design. Therefore, the options were direct bond copper (DBC) or insulated metal substrate (IMS). Finally a moderately new technology for IMS developed by Bergquist was selected for the design because of its more mechanical robustness and higher current carrying capability over DBC [48]. The product is called thermal clad insulated metal substrate or T-Clad IMS. It has three separate layers. First layer is based on copper where the components are soldered; second layer is based on a thermally conducting dielectric which isolates the circuit layer from the base metal; and third layer is the base metal which is made of aluminium and serves the purpose of efficient heat transferring from the circuit to the heat sink [49]. The reason for its high thermal performance is the technology used in the dielectric which is an exclusive blend of polymer and ceramic. The polymer has good electrical isolation properties, high bond strengths, and an ability to resist thermal aging [49]. The ceramic filler has an improved thermal conductivity and high dielectric strength [49]. Five dielectric models are available and from them Thermal Clad HR T30.20 was chosen for the design. It has a high thermal conductivity 1.1 W/m-K and a low thermal impedance of 0.9 °C/W [48]. Widths of copper, dielectric layer and Aluminium base were 70 µm, 76 µm and 1020 µm for the selected panel (2 oz. HR T30.20 panel), respectively [48]. Although there were other dielectric models with higher thermal conductivity, because of the cost and availability issue HR T30.20 was selected.

2.4.2 Power MOSFET

Because of the selection of T-Clad board for power rail and to decrease the volume of the circuit, surface-mount power-MOSFETs were considered for the design. From literature review it was found that DirectFet power MOSFETs from International Rectifier poses superior advantage over other packages such as low profile design, double-sided cooling, and low conduction loss. Also during the selection of converter topology an analytical analysis was done (section 2.2) where the DirectFet model IRF7759L2TRPBF showed the minimum loss (table 2.2). So it was decided to use the DirectFet package for the four MOSFETs in the circuit. The voltage limit for the MOSFETs was considered 75V which was more than 1.5 times of the highest voltage (48V) across them. From the International Rectifier brochure two DirectFet models, IRF7759L2TRPBF and IRF7769L2TRPBF were selected as they had very low on state drain to source resistance, R_{ds} [28]. The first one is 75V rated and the second one is 100V rated. Based on equations (2.5)-(2.9) of section 2.2 detailed power loss calculations were done for them. Because of the two phase configuration the RMS current in a single MOSFET would be half of the previous current, considering a very small ripple in IPT differential current. Also the output current in each phase was halved in calculating loss in MOSFET due to diode reverse recovery. Vgs was considered 15V in this case based on the datasheet specification. The losses in the MOSFETs, Q2 and Q4, were added to the losses in the body diodes, Q1 and Q3, to calculate the total loss. Body diode conduction loss, $P_{dcon} = V_{FM}*I_{Lav}*(1-D)/2$ [8], and reverse recovery loss, P_{drr} = fsw*Vo*Qrr [46], were calculated separately. The calculations and results are summarised in the following table 2.3.

Here, R_{ds} was calculated from the R_{ds} vs. Vgs graph of the MOSFET datasheet considering Tj=125°C. V_{plt} and Q_{plt} were calculated from the Vgs vs. total gate charge graph of the MOSFET datasheet. Rg and Q_{th-p} were given in the datasheet. Diode reverse recovery characteristics, trr and Qrr were also given in the datasheet for Tj=25°C and for a forward current of 96A. V_{FM} was calculated from the reverse drain current vs. source to drain voltage graph considering Tj=125°C.

Vgs	15	V	Zdrv	5	Ω	fsw	40	kHz	Vo	48	V					
ILav	125	A	Io	31.25	A	Itrms	54.15	A	**VFM**	0.6	V					
D	0.75															
Model	**Rds (mΩ)**	**Pc (W)**	**Vplt (V)**	**Rg (Ω)**	**ig (A)**	**Qth-p (nC)**	**Qplt (nC)**	**Psw (W)**	**trr (ns)**	**Qrr (nC)**	**Prr (W)**	**Ptt (W)**	**Pd-con (W)**	**Pdrr (W)**	**Pdt (W)**	**Ptotal (W)**
IRF7759L2TRPBF [50]	3	8.8	5.0	1.1	1.6	11	75	1.6	96	225	3.3	13.7	9.4	0.4	9.8	23.5
IRF7769L2TRPBF [51]	4.8	14.1	4.8	1.5	1.6	9	61	1.3	112	330	4.0	19.4	9.4	0.6	10.0	29.4

Table 2.3: Power loss calculation in the DirectFet MOSFETs

Clearly IRF7759L2TRPBF was better than IRF7769L2TRPBF as it has lower power loss. Therefore, IRF7759L2TRPBF was selected for the proposed design. It was assumed that both sides of the MOSFET will be connected to a heat sink. Now based on the power loss and thermal resistances of T-Clad board, thermal interfacing material, and thermal pad, the junction temperature of the MOSFET was calculated. A heat sink temperature of 60°C was assumed in this case. The detailed thermal modelling calculations are described below.

Thermal modelling strategy for DirectFet is given in reference [52]. Figure 2.5 shows the heat flow direction in a DirectFet. It is clear that the power lost inside of the device flows in three ways: i) junction-can-heat sink interface material-heat sink, ii) junction-gate pad and source pad-substrate-heat sink (if connected) and iii) junction-can-drain pad-substrate-heat sink (if connected). Based on the heat flow direction an approximate thermal equivalent circuit of the system can be drawn which is shown in figure 2.6.

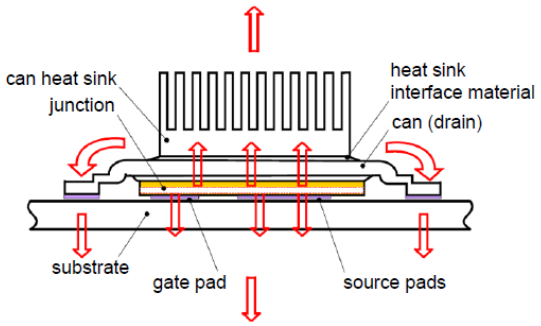

Figure 2.5: Direction of heat flow in a DirectFet [52]

In figure 2.6a all the thermal equivalent resistances are labelled. Tj, Tc, Ts and Th are temperatures in the junction, case, substrate and heat sink, respectively. Pt is the total power loss in the MOSFET. The values of R1, R2 and R3 for the IRF7759L2TRPBF (L8 package) were 0.65 °C/W, 0.25 °C/W and 0.49 °C/W respectively [52]. To calculate the value of Rc, it was assumed that a 1mm thickness (t) thermal pad was connected between heat sink and upper layer of the can. A silicone polymer thermal pad was chosen which had a thermal conductivity (k) of 4.1 W/m-K. Now using the area (A= 54.6 mm^2) of the device from the MOSFET datasheet, the value of Rc was found (4.467 °C/W) using the following equation: $R_\theta = \frac{t}{A*k}$ (2.17)

Now the thermal equivalent resistance of substrate to heat sink, Rs, was found by adding thermal resistance of T-Clad board and thermal resistance of thermal interface material (TIM), silicone heat transfer compound. The T-Clad board was comprised of three different layers. Thermal resistance of three layers were calculated separately using equation (2.17). Table 2.4 summarizes the calculation. For copper the interface area was calculated from the combined area of MOSFET pads from [53]. For both dielectric and aluminium, the area of the whole MOSFET was used as heat would spread out by the highly conductive copper. Similarly for TIM, an assumed area of the board was considered as heat would spread out by the aluminium. Finally after addition the total thermal resistance between substrate to heat sink was found 1.365 °C/W.

Now based on the rearranged thermal circuit of the device (figure 2.6b), thermal equivalent resistance between junction and heat sink was calculated, R_{eq} = 1.3 °C/W. Then using Pt = 13.7 W

and Th = 60 °C, the junction temperature for Q2 and Q4 MOSFETs was found, Tj= Pt* R_{eq} +Th = 77.81 °C. Similarly using total body diode loss, the junction temperature for Q1 and Q3 MOSFETs was found 72.74 °C.

Layers	Thickness, t	k (W/m-K)	Area, A	Thermal Resistance, R_θ	Total Thermal Resistance, Rs
Copper	70 µm	396	19.61 mm^2	0.0091 °C/W	1.365 °C/W
Dielectric	76 µm	1.1	54.6 mm^2	1.265 °C/W	
Aluminium	1.02 mm	215	54.6 mm^2	0.087 °C/W	
TIM	50 µm	0.9	150 cm^2	0.0037 °C/W	

Table 2.4: Substrate to heat sink thermal resistance calculation

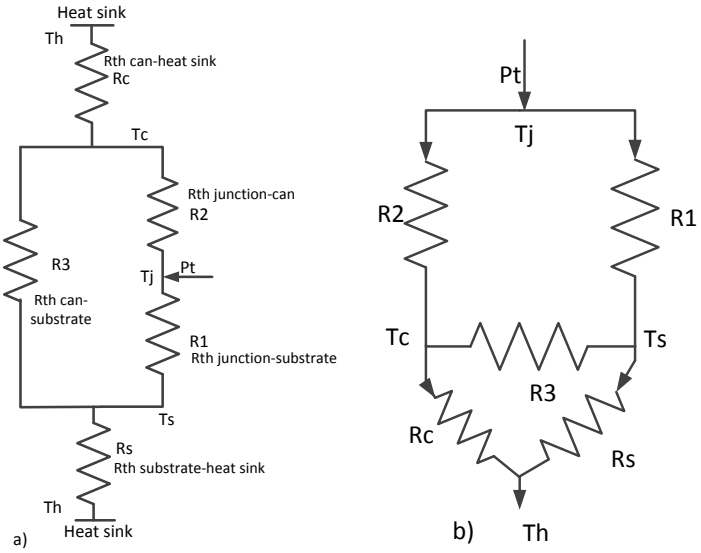

Figure 2.6: a) Approximate thermal equivalent circuit of a DirectFet [52] b) Rearranged circuit diagram

Thermal modelling calculations were verified using the online DirectFet rating calculator and also using the following equations from [52].

$$Tj = Th + \frac{\delta Pt}{\alpha+\beta-\frac{\delta*(\gamma+\zeta)}{\varphi}} \text{ where } \alpha = \frac{R3}{RsR2},\ \beta = \frac{R3}{R2R3+RcR3+RcR2},\ \gamma = \frac{R3}{RsR3+RsR1+R1R3},\ \zeta = \frac{R3}{RcR1},$$

$$\delta = \frac{\alpha}{\gamma} - \frac{R1\beta Rc}{R3} \text{ and } \varphi = \frac{\gamma RsR2}{R3} - \frac{\zeta}{\beta}$$

2.4.3 Magnetic Components

The design criteria for the two magnetic components were different. In the input inductor a large DC current would be flowing which would create a large DC flux in its core. So a core material type with high saturation flux density had to be selected. For the interphase transformer, ideally there will be no AC flux, so a core had to be selected with a minimum loss. After designing both magnetic components, power losses inside them were predicted.

2.4.3.1 Input inductor

Considering the highest saturation flux density, the highest reluctance and low loss, the Metglas Amorphous Alloy was selected for the input inductor. Different models of Metglas core from

Hitachi Metals were compared to find out the most optimized model for the design. The optimization was done based on the basic design equations of an inductor and the current density in the winding.

Design specification and preliminary calculations are listed in table 2.1 of section 2.2. From equation (2.13), input inductance was calculated using the specified values for input voltage, switching period, duty ratio, and ripple magnitude.

So, $\mathrm{Lin} = \frac{\mathrm{VinT(2D-1)}}{2\Delta \mathrm{IL}}$ = 6 µH

Two C cores from Metglas AMCC series had to be combined together to make the input inductor. The air gap, lg, between the cores and the turn number, N, for the winding are directly linked with the inductance, L, and the effective cross-sectional area of the core, Ae. Now from Appendix A3, design equations for inductor can be written:

$$N = \frac{LI}{BAe} \qquad (2.18)$$

$$lg = \frac{L*I^2*\mu o}{B^2*Ae} \qquad (2.19)$$

Now using equations (2.18) and (2.19), turn number for the winding and the air gap length for cores were calculated for different core models. Although the saturation limit of Metglas AMCC cores is 1.56T, for reliability of the design, highest flux density, B, was considered 1.2T. The current density in the winding was considered 6A/mm^2 to ensure low copper loss and good thermal management. It was decided to use copper foil as the winding because of the high current (125A). So the required area of copper for 125A current would be 20.83 mm^2. Then using the height (h) of the copper sheet available in the laboratory (0.97 mm), the width (W) of the copper foil was calculated (21.5mm). It was found from the Metglas AMCC brochure that all the core models can fit this width [54]. The results are summarised is the following table 2.5.

Design Specification	I_{Lav}	125 A	ΔI_L	12.5 A	I_{Lmax}	131.25 A
	B	1.2 T	L	6 µH	μ_o	$4\pi*10^{-7}$ H/m
	I density	6 A/mm^2	Ac	20.83 mm^2	h	0.97 mm
	W	21.5 mm				
Core Models [54]	**Ae (mm^2)**	**lg mm**	**N**	**Aw (mm^2)**	**Cu Area (mm^2)**	**Core Weight**
AMCC-63	394	0.23	2	1400	41.66	703g
AMCC- 25	267	0.34	3	840	62.5	379g
AMCC-16B	226	0.4	3	650	62.5	281g
AMCC-8	180	0.5	4	390	83.32	172g
AMCC-6.3	164	0.55	4	363	83.32	154g
AMCC-4	111	0.8	6	328	125	99g

Table 2.5: Inductor core selection

It is clear from the table that all the analysed cores can be used for the design as the required copper area for the winding is less than 50% of the core window area (Aw) even for the worst case (AMCC-4). Although the weight of the AMCC-4 core was the minimum among the models, because of the lower air gap length and lower turn number, the next model, AMCC-6.3 core was selected for the design. Its smaller air gap would ensure lower gap loss than AMCC-4. The copper area for the AMCC-6.3 was only 23% of its window area. The suitability of the selected core was also verified using the Metglas DC Reactor Core Design Software. Adhesive polyimide film 'Kapton' was selected as insulator for the winding.

Now the core loss and gap loss in the inductor were calculated from following equations (2.20) and (2.21), respectively. Peak of AC flux, Bac_{peak} , was calculated from equation (2.18) using the results from table 2.5 for Metglas AMCC-6.3 core (Ae= 164mm^2, N = 4, ΔI_{peak} = 6.25 A and L= 6 µH). Bac_{peak} was found 0.0572T.

Core loss [55], $Pcr= 6.5*f^{1.51}*Bac_{peak}^{1.74}$, (2.20)

where f is in kHz, Bac_{peak} is in tesla (T) and Pcr is in W/kg

So, $Pcr= 6.5*80^{1.51}*0.0572^{1.74} = 33.251$ W/kg

For Metglas AMCC-6.3 core (weight 154g) the core loss became 5.15 W.

Gap loss [34], $Pg= 0.0775*lg*E*f*Bac_{peak}^{2}$, (2.21)

Where air gap, lg, and tongue width of the gap, E, are in cm, f is in Hz, Bac_{peak} is in tesla (T) and Pg is in W. For Metglas AMCC-6.3 core, E = 20 mm [54]. Now by putting respective values in the equation (2.21), the gap loss was found 2.23 W. For AMCC-4, this loss would have been 2.36W.

Now to calculate the copper loss of the winding, the resistance of the coil was calculated. Only I^2R loss was considered neglecting the skin effect loss. Although the skin depth of Cu for 80kHz ripple was 0.25 mm ($2230/\sqrt{f_{kHz}}$ **)** and Cu height used in the calculation was 0.97mm, because of the very small magnitude of ripple current, the skin effect loss was not considered.

To calculate the copper loss, at first average length of a turn was calculated from the dimension of the winding bobbin. Then using the area of the copper foil and resistivity of copper at 60°C, mean resistance per turn was calculated. Finally total resistance and power loss were calculated using the total turn number.

Cu height= 0.97 mm, Cu width= 21.5 mm and Area, A= 20.855 mm^2

Average length of a turn, l = 98 mm

At 60° C, ρ = 20.136 µΩ-mm

Resistance per turn, R= ρl/A= 94.62 µΩ and total resistance = 378.5 µΩ =0.38 mΩ

Copper loss in the winding, $P_{cu}= I_{Lav}^2R$= 5.94 W and average voltage drop = 0.05V.

So the total loss in the input inductor was, **P_{Lin} = 13.32 W**

The temperature rise of the inductor due to the loss was calculated using the method described in [55]. At first considering a hypothetical box just enclosing the winding and core, the total effective convective-surface area (SA) was calculated from the dimension of the core [55]. For AMCC-6.3, it was 103.42 cm^2. Now from [55], $\Delta T=(P_{Lin} / SA)^{0.833}$= 57.2°C. Here P_{Lin} was in mW and SA was in cm^2. So a temperature change of 57.2°C would happen in the inductor over the ambient temperature.

2.4.3.2 Interphase transformer

Low cost ferrite material was selected for the interphase transformer as it has a very low core loss. To reduce the overall volume of the converter it was decided to use the planar E cores for the IPT. Because of the high current (average 62.5A at the rated condition) in the IPT winding, it was decided to use flat copper foil to make the winding. Different models of planar E cores were analysed to find out the most suitable core for the design. The analytical calculation was based on the volt-second expression across the IPT windings. Figure 2.3 showed that the voltage across IPT winding, V_{diff} , is a quasi-square wave of ±Vo for both D<0.5 and D>0.5, so it can be written using Faraday's law:

$Vo*DT = N*\Delta B*Ae$ for $(0 < D \leq 0.5)$

$Vo*(T-DT) = N*\Delta B*Ae$ for $(0.5 \leq D < 1)$ (2.22)

Here, ΔB is the peak to peak of ripple flux inside the IPT core, N is the total number turn in IPT windings and Ae is the effective cross-sectional area of the IPT core. Power ferrite material 3F3 was chosen for the design because of its low loss characteristics. At 25°C, it has a saturation flux density of 0.44T for H= 1200 A/m [32]. Considering the practical situation with current mismatch, there might be some DC flux in the core, so for design calculation maximum flux was limited to 0.12 T. For designs with higher peak flux level the IPT differential current ripple became very high depending on core models. The following table 2.6 shows all the design specifications for the interphase transformer. It was assumed that 0.1mm Kapton film would be used as winding insulator. Insulation requirements were found in [35] during the literature review of the planar magnetics.

Table 2.7 shows the result of analytical optimization. Turn number N was calculated from equation (2.22). Widths and heights of different cores were calculated from [32]. Available width for copper was found using the width of core and insulation requirement between winding and core. Then based on copper area and average winding current, the current density in the winding was calculated. It is clear from the table that only designs with E58 and E64 cores showed a sensible current density. Differential inductance, L_{diff} , was calculated based on the inductance

factor, A_L , from [32], considering the minimum air gap. Then, ΔI_{diff} was calculated using equation (2.15). Finally E58 was chosen as the ripple current is smaller than E64, which means the MOSFET conduction loss would be smaller for E58. B_{max} in the core was checked by using equation (2.18). As the height of the E58 core was sufficient for the winding, a plate core was chosen for the second part of the core. Therefore, the chosen core model was 'E+PLT58-3F3'. The gap, lg was chosen 0.2mm (corresponding to the A_L value used). As the total turn number was four (table 2.7), after centre tapping each IPT winding would have two turns.

Average IPT winding current, $I_{Lav}/2$	62.5 A	D	75%	Insulation between windings and core	0.4 mm
Peak to peak ripple flux inside IPT core, ΔB	0.24 T	T	25 µs	Insulation between copper plates	0.1 mm
Copper plate height	0.45 mm	T-DT	6.5 µs		

Table 2.6: Design specification for IPT

Model	Ae (mm^2)	N	Width of core window (mm)	Height of core window (mm)	Available width for Cu track (mm)	Current density (A/mm^2)	Required height (mm)	AL (µH/N^2)	Differential Inductance, Ldiff (µH)	Differnential ripple current, ΔIdiff (A)	Bmax from ΔIdiff (T)
E18	39.5	32	4.85	1.9	4.1	34.3	18.3	0.3	322.6	0.9	0.12
E22	78.5	16	5.65	3.1	4.9	28.6	9.5	0.6	161.3	1.9	0.12
E32	129	10	9.21	3.0	8.4	16.5	6.2	0.6	63.0	4.8	0.12
E38	194	6	11.215	4.3	10.4	13.3	4.0	1.0	36.0	8.3	0.13
E43	225	6	13.2	5.4	12.4	11.2	4.0	1.0	36.0	8.3	0.11
E58	310	4	20.85	6.5	20.1	6.9	2.9	1.6	25.6	11.7	0.12
E64	519	2	21.35	5.0	20.6	6.8	1.8	3.2	12.6	23.8	0.14

Table 2.7: IPT core selection

Similar to the input inductor there will be core loss and copper loss in the IPT. Because of the very small gap and low Bac_{peak} the gap loss was not considered in this case. Again gap loss is created by the eddy current in the core (near air gap) from the fringing flux; as ferrite cores have high resistivity, so gap loss will be the minimum for them [30]. The core loss data was taken from the datasheet [32]. At 100°C, for B=0.1T and f=100 kHz, the core loss in E+PLT58-3F3 was given 2.6 W.

Again considering a rectangular shape of winding with a width of 20 mm and using the core geometry from datasheet, the mean turn length was found 175.6mm. Then using copper area (20*0.45 =9 mm^2) and resistivity of copper at 60° C, ρ = 20.136 µΩ-mm, per turn resistance was found 0.4 mΩ. So, the total resistance of IPT windings was 1.6 mΩ, and the total resistive loss was 6.25 W. The average voltage drop in each IPT winding would be 0.05V.

Finally core and copper losses were added and a total loss of 8.85 W was found for the IPT, so **P_{IPT} = 8.85 W**. The temperature rise of IPT from the ambient was calculated in a similar fashion to the input inductor. The total effective convective-surface area (SA) was calculated from the dimension of core and winding. SA was found 111.88 cm^2, so $\Delta T = (P_{IPT} / SA)^{0.833}$ = 38.12°C. Thus a temperature rise of 38.12°C over the ambient temperature was expected.

2.4.4 Capacitor

From equation (2.16) of section 2.3, output capacitor value was calculated using 10% voltage ripple specification. The output resistor value was used 1.536 Ω, considering 48V output voltage and 31.25A output current. So the required output capacitance was found 40.7 µF. The RMS capacitor current was calculated using the capacitor current waveform in figure 2.3b by using the specified values for Io, $\Delta I_L/2$, and ΔI_{diff} (Appendix A3). This current was found 23.3 A.

It was decided to use multilayer ceramic capacitor (MLCC) with 100V rating, because of its very low profile which can effectively reduce the volume of the converter. They also have a very low equivalent series resistance (ESR). However, the problem with these surface mount components were the power loss or maximum ripple current or maximum RMS current rating were not given in datasheets for most of the models. The maximum temperature of the device is considered as the most critical criterion for an MLCC and depending on the surrounding temperature, different current rating can be found for an MLCC [56]. Sometimes experiments are made to calculate this current rating [56]. Finally a research paper was found from KEMET Electronics [57], where it showed some experimental results on MLCC. It was found that for 4.7 µF C1210 single stack MLCC, the absolute maximum temperature (125°C) was reached at 15A RMS current. Also it could take 5A RMS current for a temperature increment of 15°C over the ambient temperature of 25°C. So it was decided to use ten of C1210C475M1R2CTU (4.7µF dual MLCC stack) in parallel to ensure high reliability in the circuit (2.33A RMS current in each). Each of them had a volume of only 56mm^3 and required an area of 9.1 mm^2 on the mounting surface [58].

The current in the input capacitor (I_{cin}) would be a triangular wave with a peak equal to the peak of AC ripple of the input inductor current. Therefore, the RMS current will be 3.61 A for D=0.75 ($\Delta I_L/2\sqrt{3}$). Again integrating the I_{cin} waveform and using a 10% ripple voltage specification at the input, the required input capacitance was found 16.3 µF. The same model as output was selected for the input, but in this case only four them had to be paralleled for the required capacitance. The calculations regarding input and capacitor currents are shown in Appendix A3.

2.5 Conclusions

A detailed methodology for designing this 12V to 48V bidirectional boost converter is discussed in this chapter. The theory of the selected topology is explained, which was the basis of component selection. Analytical analysis was done for MOSFET, input inductor, and IPT to select the most suitable models. Thermal modelling of MOSFET and design procedure for magnetic components were discussed. Electrical, mechanical and thermal optimizations were done for selecting each of the components of the circuit. The next chapter will discuss about the power circuit construction as well as the construction procedure for magnetic components.

Chapter 3: Construction of the Converter

3.1 Introduction

This chapter explains the detailed construction procedure of the IPT based dual interleaved boost converter, based on the selected components in the previous chapter. The basic components selected so far were a 2 oz. panel of HR T30.20 T-Clad board as a substrate, the IRF7759L2TRPBF as the semiconductor devices, Metglas AMCC-6.3 as the input inductor core, E+PLT58-3F3 as the interphase transformer (IPT) core and KEMET C1210C475M1R2CTU as the capacitors. First the layout of the power stage was designed. Then based on the calculated specification from section 2.4.3, the magnetic components were constructed. After soldering the components on the T-Clad board and by making appropriate connections with magnetic components, the circuit became ready for testing. A suitable load was created from a variable resistor bank to test the circuit at different power conditions. The whole experimental set-up is also explained later this chapter.

3.2 Construction of the Power Circuit

The step by step construction procedure of the proposed converter's power stage is explained below. For the purpose of circuit layout design, some small bus bars were designed, through which input supply, output load, inductor, and IPT could be connected to the T-Clad board. Then the total circuit layout was done using Altium Designer 10. Then based on the losses in the components and T-Clad board a heat sink was selected.

3.2.1 Circuit Layout and Bus bar Design

The schematic of the circuit is shown in the figure 3.1a and the corresponding T-Clad layout is shown in figure 3.1b. Both of them were generated using Altium Designer 10 software. Here terminal P1 was the input connector, where the supply would be connected. After the parallel capacitors, P2 was the connector for the input inductor which would stay on top of the board. One terminal of the input inductor would be connected to P2-1 and other terminal would be connected to the centre tap of the IPT. Rest of the two terminals of the IPT would be connected to the middle points of the two phase legs through J1 and J2 connectors. IPT would also stay on top of the board. Finally at the output, the load would be connected to the P3 terminal. For each MOSFET, Zener diodes were used between gate and source to protect the gate from over voltage transients, which could be generated from the ringing between the stray inductance and the gate capacitance [59]. Also a small 1Ω resistor was included in series with the gate to prevent transient oscillations [59]. A 4X2 connector, P4, was considered for the gate drive connection.

The connectors in the circuit, P1, P2, P3, J1, and J2 had to carry very high currents (On average P1 and P2 125A, J1 and J2 62.5A and P3 31.25A) and no suitable surface mount connectors were found for them. As a result specific bus bars had to be designed for them. For high conductivity

copper (Cu) was selected as the bus bar material. Also for a compact design it was decided to use rectangular box shape bus bars for P1, P2, and P3 and cylindrical shape bus bars for J1 and J2. The dimensions of the bus bars were optimized by doing a simple resistive power loss calculation as shown in the Appendix A4. The sizes of the connecting cable-crimp and screw were also considered. The final shape and dimension of bus bars were shown in figure A4.1 of Appendix A4. Total loss for the designed bus bars was found **0.24 W** (Appendix A4).

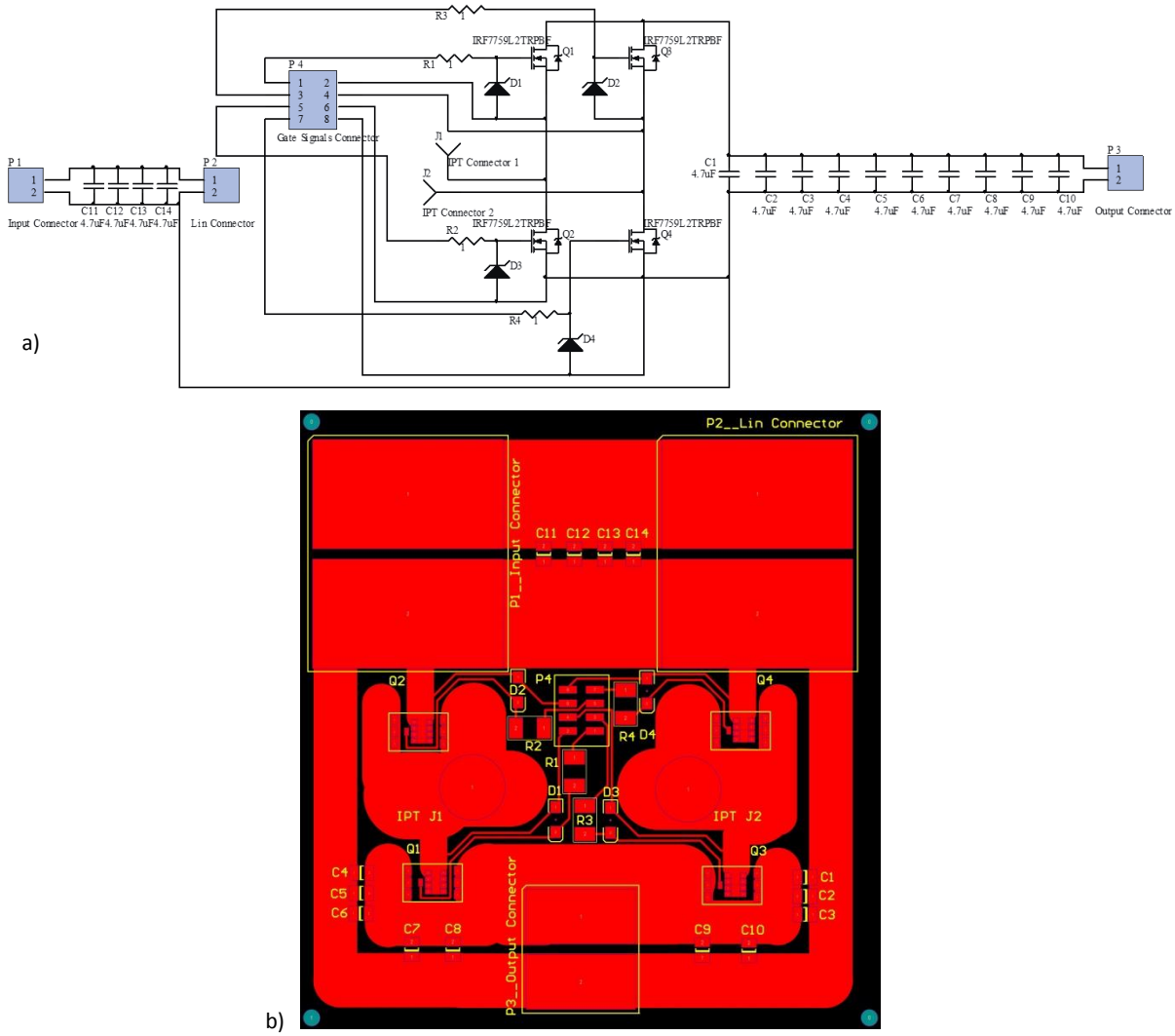

Figure 3.1: a) Schematic of the converter circuit b) T-Clad layout for the converter

Specific pads for bus bars, MOSFET, capacitor, and resistor were designed in Altium by using their footprints (respective datasheets were used when required). As the T-Clad board had Cu on only one side of the board, designing Cu tracks between the pads were challenging. Finally the circuit layout looked like figure 3.1b. A symmetrical design was done to ensure equal resistance in the two IPT winding paths, so that the current sharing between IPT windings would be perfect. Cu tracks from the gate drive connector (P4) were designed in a way that minimum loop-areas were ensured to reduce the stray inductance in the gate drive circuit. The widths of different tracks were optimized based on power loss and voltage drop calculation in them. Finally total loss in the tracks for the shown layout was found **18.16 W** and the total voltage drop was found **0.37V**. The approximate power loss calculation for the final design is shown in Appendix A5. Ripple in the

currents were not considered in this power loss calculation. Approximate current densities in different tracks were also observed and it was found as high as 140 A/mm^2 for two small tracks connected to the source pad of the lower rail MOSFETs (Q2 and Q4). However, it was considered reasonable as [49] showed that T-Clad dielectric's temperature rose only by 0.2°C for a current density of 111.61 A/mm^2. The test was done considering a 25 mm track on an HT model substrate (double thermal conductivity of the selected HR model) without a base metal [49]. Because of high current densities, in some of the tracks the loss was as high as 6.6 W. Finally, all the components were soldered on the T-Clad board using a hot plate. The temperature was fixed at 240° C in accordance with the guideline of soldering DirectFet [53] and capacitor [58].

3.2.2 Loss Audit and Heat Sink Selection

Power loss in different components was calculated considering the specification of the converter. The following table 3.1 lists the power loss in different components and the expected efficiency for the proposed design. It was clear that the proposed design would meet the target efficiency at the rated power. The capacitor power loss was not considered, because it was assumed that the input and output capacitor will be charged and discharged corresponding to each other in a loss-less manner.

Components	MOSFETs	MOSFET Body diodes	Input inductor	IPT	Bus bars	Cu tracks	Total loss (W)	Efficiency
Loss (W)	27.4	19.6	13.32	8.85	0.24	18.16	87.57	94.2%

Table 3.1: Loss audit in the proposed design

Based on the total loss of 65.4 W in MOSFETs, MOSFET body diodes, bus bars, and Cu tracks, the heat sink was chosen. Considering a heat sink temperature of 60°C and an ambient temperature of 25°C the required thermal resistance of the heat sink was found 0.535 °C/W. From the T-Clad layout (figure 3.1b) the required mounting dimension was found 120X110 mm^2. At first OHMITE - CP4-114A water cooled heat sink was chosen, which had a thermal resistance of 0.43 °C/W [60]. However, as it was not available at the market at that time, an alternative heat sink from the laboratory was used. It was a forced air-cooled heat sink from HS Marston with a thermal resistance of 0.08 °C/W (model 890SP-01500-A-100 [61]). It means that the proposed design can work at a higher ambient temperature of around 54.77°C. Finally, the T-Clad board was mounted on top of the heat sink. Silicone heat transfer compound was used as thermal interfacing material (TIM) between the heat sink and the T-Clad board. Two copper plates were used on top of the DirectFets for additional cooling. A silicone polymer thermal pad was used between each DirectFet and copper plate. The copper plates were also connected to the base metal of T-Clad board to provide a conductive path for the heat. The final setup is shown in figure 3.2a.

3.3 Construction of Magnetic Components

According to the design specifications established in section 2.4.3 magnetic components were constructed. After the construction they were tested using a high precision LCR meter to find out

their inductance and series AC resistance at different frequencies. Inductance values for both input inductor and IPT closely matched with design specifications.

3.3.1 Input Inductor

Two Metglas AMCC-6.3 C cores were connected together with a cable tie. Two pieces of plastic shim were used between them to create the required air gap. Due to the availability of plastic shim at specific thicknesses, 0.305 mm gap could be achieved in each leg. So the total air gap, lg, was found 0.61 mm which was slightly higher than the design specification (0.55mm). However, fringing flux factor (F) was not considered in the initial design. Because of air gap fringing flux, the effective cross sectional area (Ae) will be increased by a factor of F [55]. So the inductance will also increase by a factor of F. The fringing flux factor was found from the dimension of the core and air gap length using the equation, F= (A+lg)(D+lg)/(A*D) [55]. The dimension of the core is shown in figure A6.1a of Appendix A6. The calculated value of F was 1.1. Now using the inductance equation from [29], $L= \mu_o N^2 Ae/lg$, the value of inductance without considering the fringing factor was found 5.41 µH. Then considering the effect of fringing flux, the inductance value was found 6µH. A copper foil of 23mm width and 0.97mm thickness was used to make the four turns for the inductor. After the final assembly the inductor looked like as figure A6.1b in Appendix A6. After testing it with the LCR meter, the inductance and AC resistance were found 6.71 µH and 0.127 Ω for 80 kHz operation, respectively. Because of the low AC resistance and low ripple specification for the input current, AC resistive loss was neglected for the input inductor.

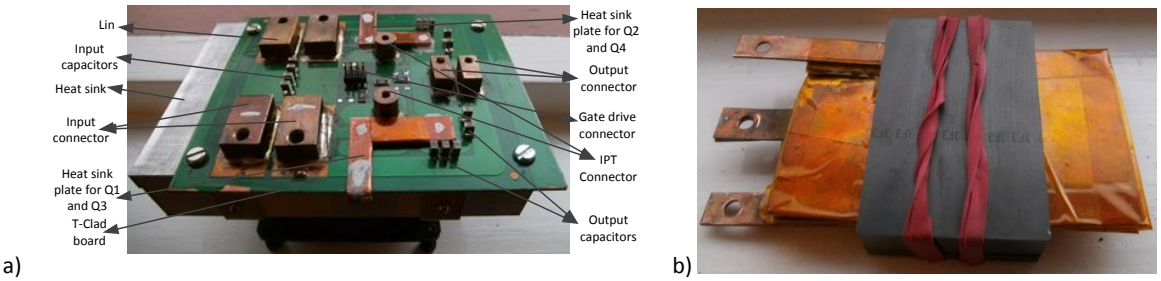

Figure 3.2: a) T-Clad board with mounted components and b) Photo of the IPT

3.3.2 Planar Interphase Transformer

According to the design specification, one E58-3F3 core was attached to a PLT58-3F3 core with 0.1mm plastic shim between them. The four flat turns were made from a copper sheet of 0.45mm thickness. At first, four rectangular copper plates were stamped out from a copper sheet (figure 3.3). Then all of them were cut at a specific distance from the edge to form the individual turns. Then all the turns were soldered in a sequence that a complete winding was shaped. Finally, three tags were connected at appropriate positions to form the three terminals of IPT. After the fabrication of winding, Kapton film was used to insulate the turns. The schematics and dimensions of four individual turns are shown in figure 3.3.

After assembling the winding with the core, the IPT was tested using LCR meter. The differential inductance was found 24.5 µH for 40 kHz operation, which was very close to the predicted value. The short circuit test was done and the leakage inductances for the two windings, L11 and L22, were found 0.376 µH and 0.345 µH, respectively. The low leakage inductance compared to the total differential inductance justified high coupling between the IPT windings, which was an essential criterion for the design to remove the DC flux from the core. Open circuit test was also done and the inductance values for L11 and L22 were found 6.3 µH and 6.25 µH respectively. Change of AC resistance of the winding with respect to frequency is shown in figure A6.2 of Appendix A6. Though the AC resistance was very high at high frequencies, near 40 kHz it was very low (0.03 Ω). The predicted magnitude of AC ripple current was also very small ($\Delta I_{diif}/2$= 5.85A), so the AC resistive loss was neglected for the IPT as well.

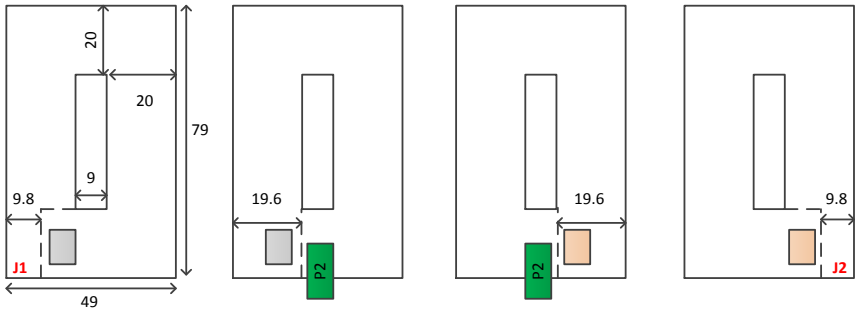

Figure 3.3: Four individual IPT turns, there dimensions and inter-connecting points (all dimensions in mm)

3.4 Experimental Setup

After connecting the inductor and the IPT to the T-Clad board, the top view of the converter looked like figure A6.3 of Appendix A6. Although cables were used for the connection between the T-Clad board and the IPT, they were actually used for the purpose of measuring currents in them. In the final product, IPT will be positioned on top of input connector and will be connected to J1 and J2 using planar copper bus bars. A variable resistor bank was arranged, which could give a load value of 1.5 Ω to 18.5 Ω. So the converter could be tested for a power range of 124.5W to 1500W, considering the 12 V to 48 V operation. To run the converter in open loop mode a gate drive circuit from the laboratory was used. Two current probes were connected in two IPT windings. Necessary voltage probes and multi-meters were also connected during experiments. An infrared imaging camera was used to monitor components' temperature. The photograph of complete setup is shown in figure A6.4 of the Appendix A6.

3.5 Conclusions

The converter circuit layout was done carefully to ensure a symmetrical arrangement and to minimize parasitic impedance in critical paths. The constructed magnetic components showed their predicted values after testing. Magnetic components and the final circuit looked very compact after construction. Next chapter will discuss about the experimental results from the constructed converter.

Chapter 4: Results and Analysis

4.1 Introduction

This chapter will discuss the results of experiments on the designed converter. The interphase transformer (IPT) based dual interleaved boost converter was constructed using only surface mount devices on a thermal clad board. For the IPT, a planar structure was used to make the converter compact and power dense. For input inductor, a Metglas Amorphous Alloy core was used to carry the high DC flux from the input current. Experiments were conducted using a variable resistor bank to see the performance of the converter at different power levels. After the experiments, it was found that the converter showed very good resemblance with the theory and design. Also it showed efficiency close to the predicted value of 94.2% at rated power, meeting the set target. Temperature of the converter was monitored constantly to see the temperature variations in different parts of the converter. The temperature values of different components were also found closely matched with the prediction.

4.2 Experimental Results

Steady state waveforms were captured using digital oscilloscope at different power conditions. Gate pulses with different duty ratios were provided to lower rail MOSFETs, Q2 and Q4 (figure 2.2). The upper rail MOSFETs, Q1 and Q3 were kept off to use their body diodes. At first the circuit was operated in boost mode at lower power. Then the power was increased gradually to the rated power. Finally, the converter was run in buck mode by interchanging the gate pulse connections between lower rail MOSFETs and upper rail MOSFETs. From the input and output power, the efficiency was calculated at different load conditions. During the test, the temperature of the converter was monitored using an infrared camera. Finally, based on the dimension of the whole converter, its power density was calculated.

4.2.1 Steady State Waveforms

Figure 4.1 shows steady state waveforms of the converter at rated condition (1.5 kW). Figure 4.2 and 4.3 show waveforms for less than 50% and equal to 50% duty ratio, respectively. In all three cases the load was a 1.5Ω resistor bank. Each of the plots are comprised of gate of source voltage of MOSFET-Q2, V_{gs}, differential voltage across IPT terminals, V_{diff} , input inductor current, I_{Lin} , IPT winding currents, I_{L11} and I_{L22}, and IPT differential current, I_{diff} . Differential currents were found by subtracting one IPT winding current from another and then dividing it by two, $I_{diff} = (I_{L22}-I_{L11})/2$. The input currents were found by adding the IPT winding currents. In all the cases the output voltage was found to be slightly less than the expected output which was due to the voltage drop in different components and T-Clad copper tracks. Again in all the cases the current sharing between IPT windings was almost perfect. For D=50% both input and output currents were found almost perfectly ripple free.

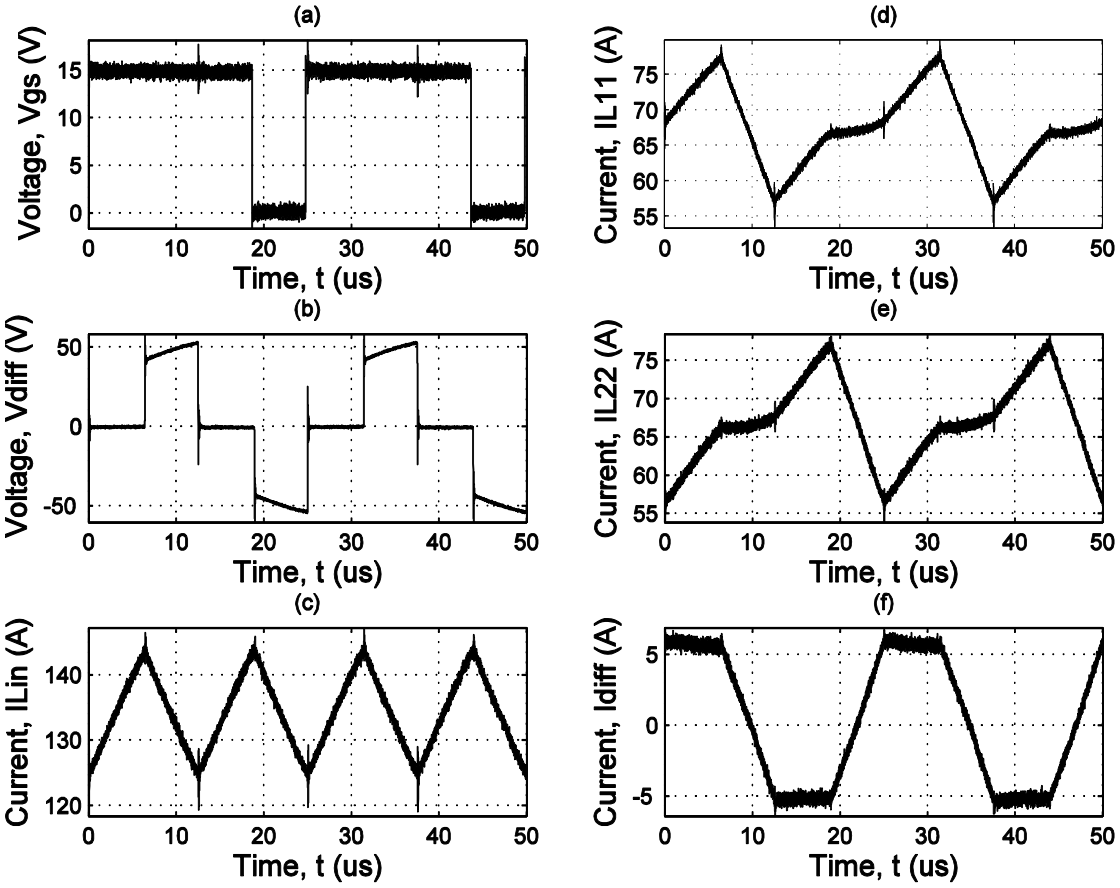

Figure 4.1: Steady state waveforms at rated condition: D= 75.64%, Vin=11.8 V, Vo=45.55 V, Iin= 134 A, and Io=32.5 A. a) Gate to source voltage, V_{gs}, b) Differential voltage across IPT, V_{diff} , c) Input inductor current, I_{Lin} , d) IPT winding-L11 current, I_{L11}, e) IPT winding-L22 current, I_{L22}, and f) IPT differential current, I_{diff}

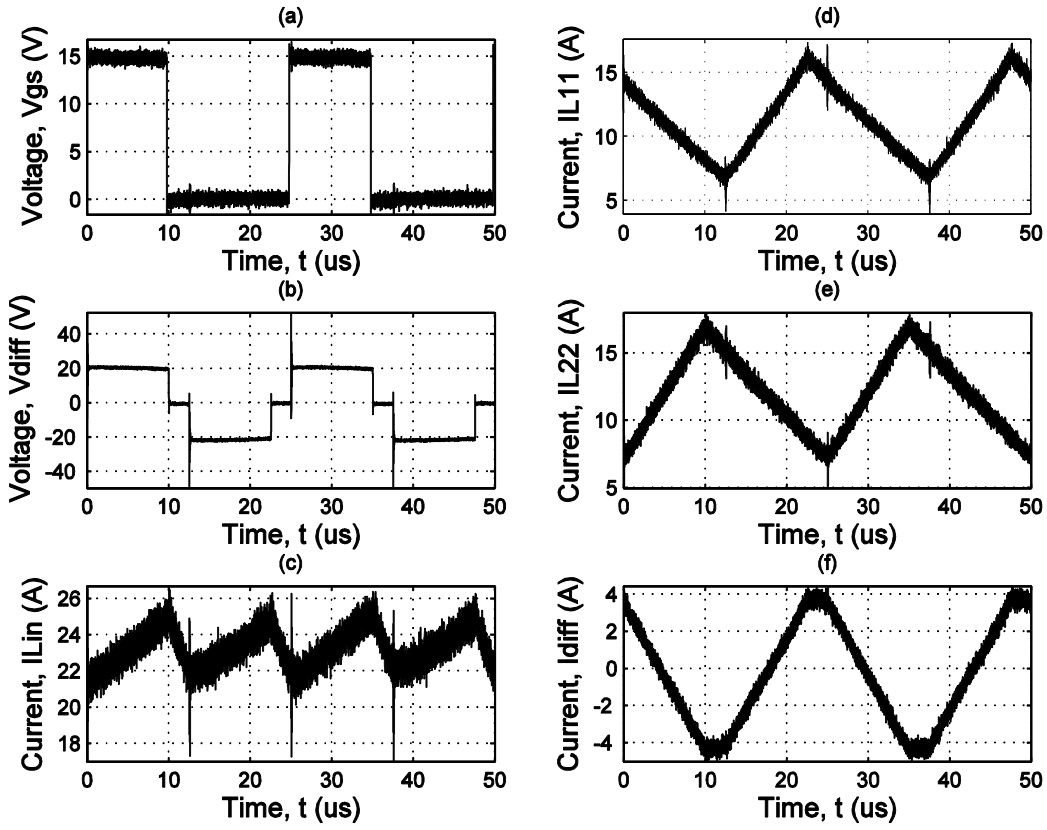

Figure 4.2: Steady state waveforms at condition: D= 40%, Vin=12.04 V, Vo=19.35 V, Iin= 23.12 A, and Io=13.9 A. a) Gate to source voltage, V_{gs}, b) Differential voltage across IPT, V_{diff} , c) Input inductor current, I_{Lin} , d) IPT winding-L11 current, I_{L11}, e) IPT winding-L22 current, I_{L22}, and f) IPT differential current, I_{diff}

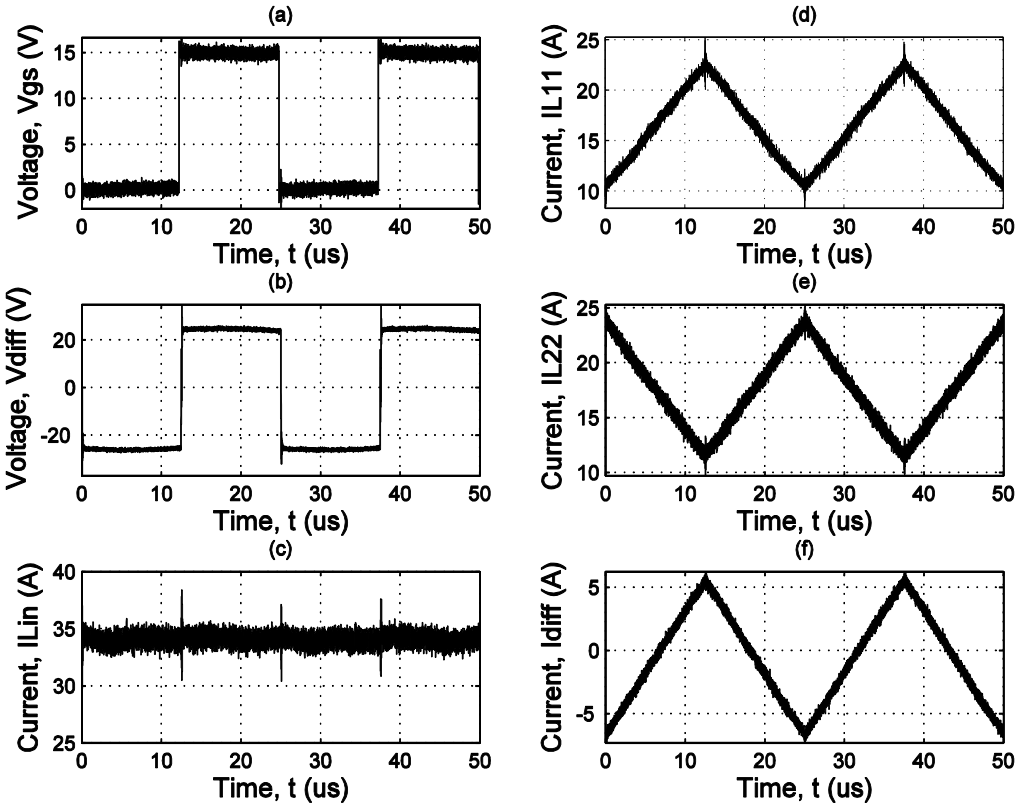

Figure 4.3: Steady state waveforms at condition: D= 50.13%, Vin=11.98 V, Vo=23.4 V, Iin= 33.7A, and Io=17.02A. a) Gate to source voltage, V_{gs}, b) Differential voltage across IPT, V_{diff} , c) Input inductor current, I_{Lin} , d) IPT winding-L11 current, I_{L11}, e) IPT winding-L22 current, I_{L22}, and f) IPT differential current, I_{diff}

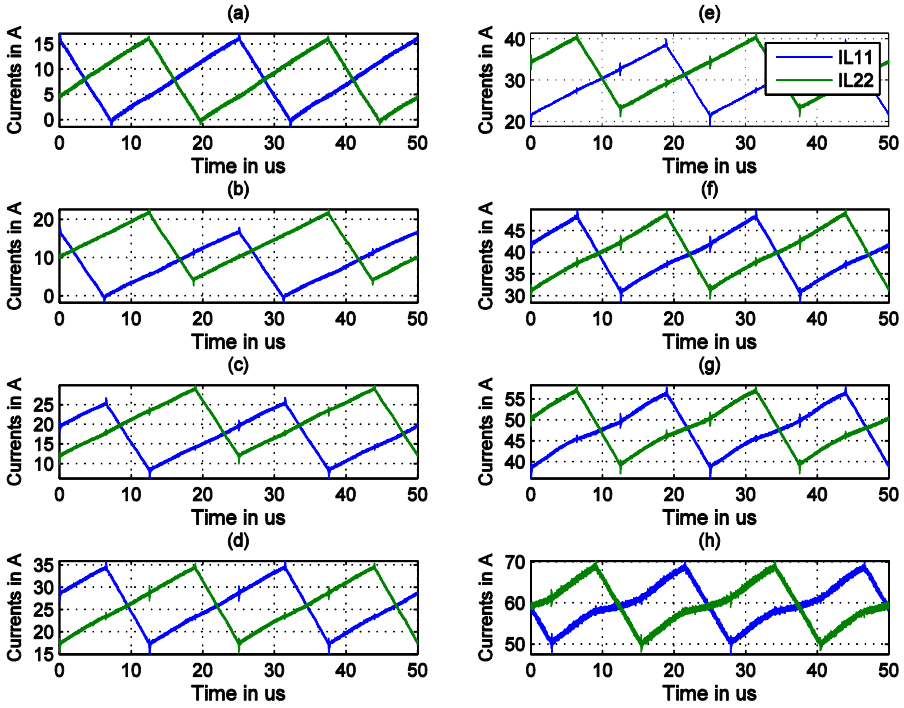

Figure 4.4: IPT current sharing at different power level: a) Pin=192W and In=16.11 A, b) Pin=258 W and Iin= 21.66A, c) Pin= 437.5W and Iin=36.8A, d) Pin= 614.5 W and Iin= 52 A, e) Pin = 732.3W and Iin=62A, f) Pin= 938.5 W and Iin= 79.6A, g) Pin= 1131 W and Iin= 96.5A, and h)Pin= 1407W and Iin= 120.4A

The operation of the converter was also observed at different power levels by changing the resistance of the resistor bank. The duty ratio was around 75% in all the cases. Figure 4.4 shows the current sharing between the IPT windings at different power levels. Figure 4.5 and 4.6 illustrate the corresponding IPT differential currents and input currents, respectively. It is clear from the figure 4.4 and 4.5 that most of the cases current sharing between the IPT windings was

almost perfect. However, in 250W-600W range there was a mismatch between current sharing. Figure 4.5 shows that in almost all cases the input inductor current ripple was between 12.5 A to 15 A. At higher power the ripple was higher. Figure 4.5 actually shows the differential current plus half of the DC current mismatch between IPT windings. Considering the DC offsets in those wave-shapes, the worst mismatch was found around 6A.

Switching transients in V_{ds} were observed during operations when the mismatch between IPT winding currents was very high. Figure 4.7 shows the turn off and turn on switching transients of V_{ds} during the 437.5W operation. The current mismatch was around 5A between the IPT winding currents and the output voltage was 47.2V. V_{ds} transients were observed for the high current carrying MOSFET. It is clear from the figure 4.7a that the peak of the transient wave during MOSFET turn on was 60V, way less than the MOSFET rated voltage. The MOSFET was switching in a very fast manner as less than 50 ns were required for both rise time and fall time (similar to datasheet specification).

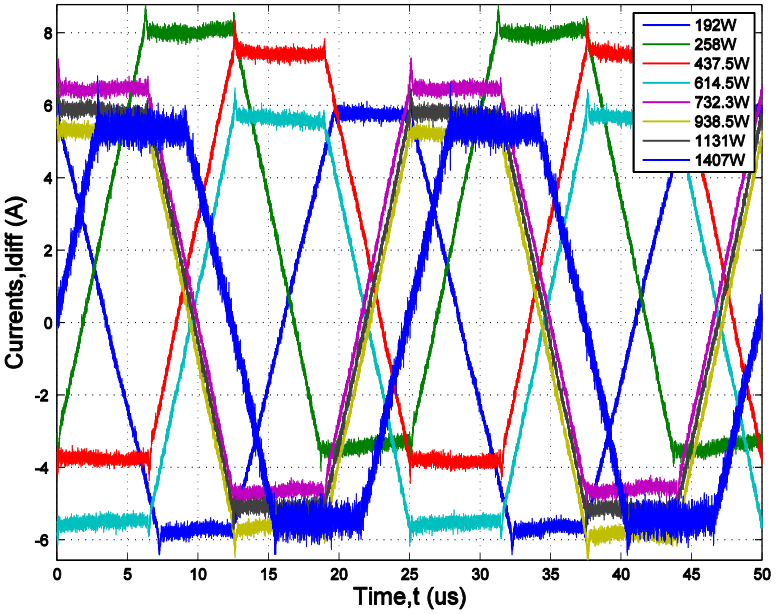

Figure 4.5: I_{diff} plus half of DC current mismatch at different power levels

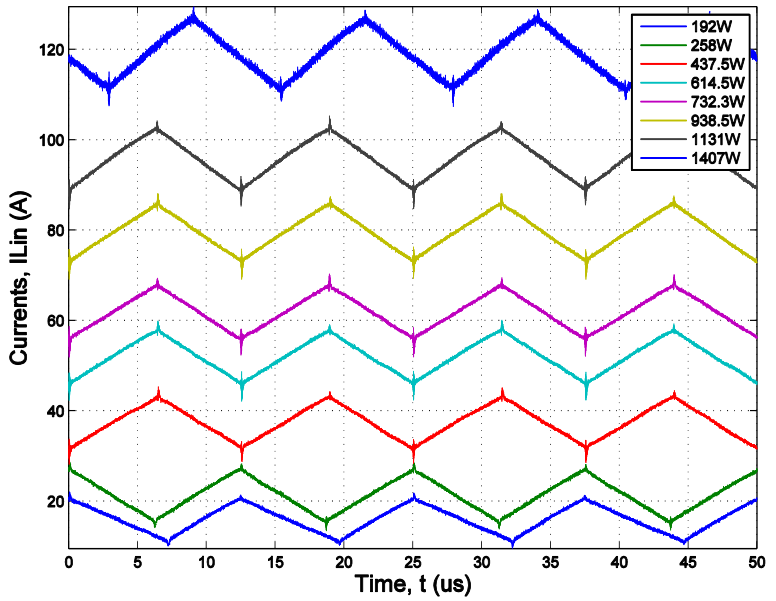

Figure 4.6: Input inductor currents at different power level operations

Figure 4.8 shows the ripple in the output voltage for 1408W operation. The operating conditions for the test were as follows: Vin= 11.69 V, Iin = 120.37A, Vo= 43.25V and Io= 30.34A. The waveform was found multiplying the output current with the load resistor of 1.425 Ω. The peak to peak ripple was found around 4.5V, which was 10.4% of average output voltage. Therefore, the output voltage specification was also closely matched with the experimental result.

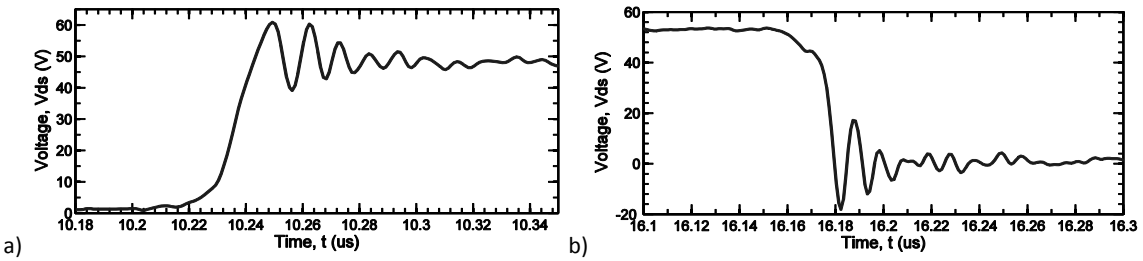

Figure 4.7: V_{ds} transients a) during turn-off and b) during turn-on

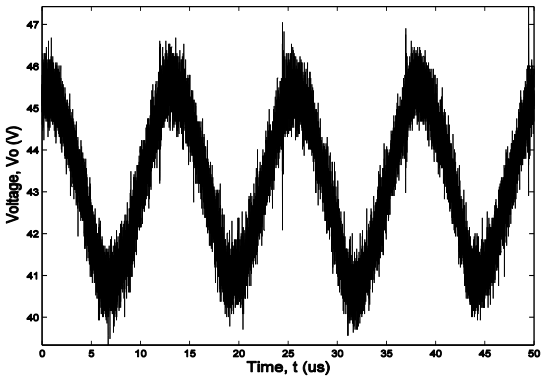

Figure 4.8: Ripple in output voltage, Vo for the operation of Vin= 11.7 V, Iin = 120.37A, Vo= 43.25V and Io= 30.34A

To ensure the circuit's bidirectional capability it was tested in buck mode as well, so the circuit was tested for 48V to 12V operation. In this case, the rated input current would be 31.25A and the output current would be 125A. The required output resistance was 0.096 Ω. Due to the unavailability of an appropriate resistor bank, a single resistor was used which gave a value of 0.09Ω including connecting wires. Tests were conducted for three operational points near the rated power. The results are given in table 4.1. The respective IPT winding currents' wave-shapes and inductor current's wave-shapes are given in figure 4.9. It is clear from the figure that the current sharing between the IPT windings was reasonable and the inductor ripple current was around 12.5A to 14.5A, depending on the incremental power.

4.2.2 Efficiency Measurements

During the experiments at different power levels, input and output voltages, and input and output currents were measured. Voltages were measured by using two digital multi-meters and currents were measured by using two current-probes. For the currents only average values were taken from the oscilloscope. The data were taken at different times of operation, i.e. after 10 minutes, 20 minutes and 30 minutes of operation. Then they were averaged to get a final value. The measured results are shown in the following table 4.1. From the table, it is clear that the converter showed very good performance in terms of efficiency at different power levels. However, the output voltages were slightly less than the expected value which was mainly due to the voltage drop in circuit components. At higher current level voltage drop became higher and the efficiency was slightly reduced. Similarly for the buck mode, the efficiency was calculated from the input and output measurements as shown in table 4.1. It is clear that for buck mode operation almost similar efficiency is found at the rated power condition.

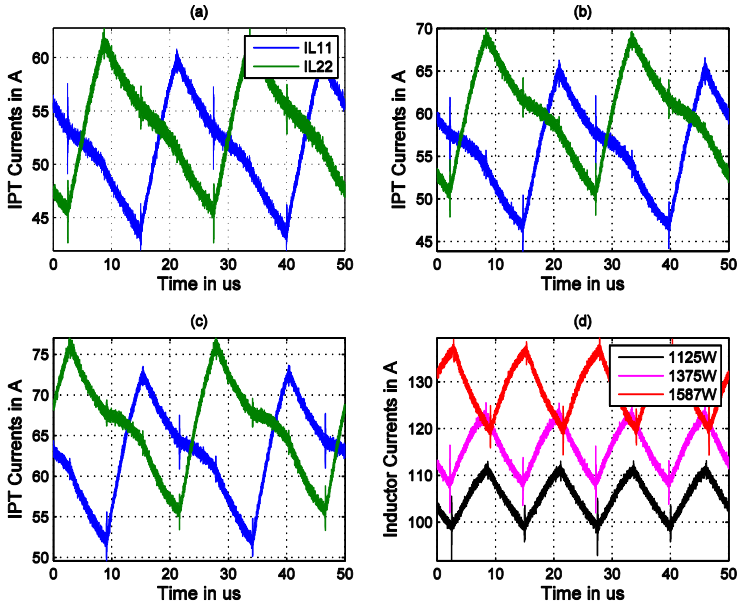

Figure 4.9: Buck mode: IPT currents for a) 1125 W, b) 1375W, c) 1587W operation and d) respective inductor currents

Operation	D	RL (Ω)	Vin (V)	Iin (A)	Vo (V)	Io (A)	Pin (W)	Po (W)	Efficiency
Boost	71.22%	9.3	11.93	16.11	40.58	4.5	192.19	182.61	95.01%
	75.27%	9.3	11.92	21.66	47.07	5.2	258.19	244.76	94.80%
	75.54%	7.5	11.9	26.62	47.5	6.56	316.78	311.60	98.37%
	75.54%	6	11.89	31.7	47.4	7.85	376.91	372.09	98.72%
	75.54%	5.1	11.89	36.8	47.2	9.02	437.55	425.74	97.30%
	75.53%	4.5	11.87	41.9	47.1	10.33	497.35	486.54	97.83%
	75.53%	3.8	11.84	51.9	46.92	12.8	614.50	600.58	97.73%
	75.53%	3	11.83	61.9	46.6	15.2	732.28	708.32	96.73%
	75.53%	2.32	11.79	79.6	46.1	19.43	938.48	895.72	95.44%
	75.53%	1.94	11.73	96.5	45.65	23.6	1131.95	1077.34	95.18%
	75.53%	1.72	11.69	108.8	45.35	26.5	1271.87	1201.78	94.49%
	75.53%	1.64	11.68	113.4	45.2	27.6	1324.51	1247.52	94.19%
	74.60%	1.5	11.69	120.37	43.25	30.34	1407.13	1312.21	93.25%
	75.53%	**1.5**	**11.64**	**129**	**44.6**	**31.6**	**1501.56**	**1409.36**	**93.86%**
	75.64%	**1.5**	**11.8**	**134**	**45.55**	**32.5**	**1581.20**	**1480.38**	**93.62%**
Buck	24.75%	0.09	40.9	27.5	9.47	105.1	1124.75	995.68	88.52%
	24.75%	0.09	44.8	30.68	10.45	115.8	1374.46	1210.21	88.05%
	24.75%	0.09	49.9	31.8	11.6	128.6	1586.82	1491.41	93.99%

Table 4.1: Experimental results and efficiency calculations at different power level operations

4.2.3 Temperature Monitoring

Temperature rise in the components were monitored during different power level operations of the converter by using a Fluke Infrared Imaging camera. In all the cases, temperatures were within expected levels. Highest temperatures in different components were found after 45 minutes of operation at rated power (1513 W). Appendix A7 shows thermal images of input inductor, IPT and MOSFETs. Because the camera works based on the emissivity of components, so portion of magnetic components and semiconductor components were white-coloured and temperatures of those points showed actual device temperatures. The highest temperature

(around 85°-89°C) was found in the core of input inductor because of high core loss, gap loss, and the absence of physical connection to the heat sink. The highest core temperature was near the gap under winding, which resembles a high loss due to fringing flux at the air gap. Again for the IPT, as the copper loss was almost 2.4 times of core loss (section 2.4.3.2), the temperature of the winding (67.3°C) was found to be higher than the core (56.2°C), in spite of very high thermal conductivity of copper. Temperatures of both of the upper heat sink plates were almost similar, (around 55°C) because of the high thermal conductivity of the copper. However, at half power operation, without the upper heat sink plates, it was found that the MOSFET used as diode was hotter (about 5°C) than the MOSFET used as switch, though loss in the MOSFET body diode was calculated lesser (section 2.4.2). Yet, in the theoretical calculation, the junction temperature was higher than the practical junction temperature and the body diode forward voltage drop (V_{FM}) increases with the decrease of junction temperature [45]. Therefore, in the experiment the V_{FM} was higher; as a result the conduction loss was also higher than the prediction. This temperature difference decreased as the power level increased, again because of the increased junction temperature of body diode. The substrate temperature was in a range of 40°-48°C depending on the location of the switching devices, where the temperature was higher than other parts of the circuits. The highest capacitor temperature was found 54.5°C. The heat sink temperature was in the range of 32°-37°C depending on the location of the fan and the T-Clad board.

4.2.4 Power Density Measurement

The power density of the converter was measured based on the dimensions of the whole converter. Sometimes these small converters are cooled together with other components of the electric vehicle, so both with-fan and without-fan power densities were measured. The volume of the total converter was found 0.895 litre and 0.725 litre with the fan and without the fan, respectively. So the rated power density of the converter was 1.8 kW/litre and 2.2 kW/litre with the fan and without the fan, respectively (considering the highest operating power of 1.58 kW). Without the heat sink volume (0.416 litres) the power density was found 5.1 kW/litre.

4.3 Analysis of the Experimental Results

In this section, all the experimental results will be analysed with respect to the theory and paper design of the converter. At first comparing figure 4.1 with figure 2.3b of chapter 2, it can be said that the experimental wave shapes closely matched the theory. Both IPT winding currents had the same shape with a 180° phase shift between them. Again, the input current ripple frequency was double of the switching frequency and the differential current was an AC waveform. Although the differential voltage (V_{diff}) waveform looked almost similar to the theoretical one, it was not constant when only one MOSFET is on. The change was around 5V, which came due to the capacitor voltage ripple and voltage drop in MOSFETs and Cu tracks. Again, the ripple magnitude of the input inductor current (15 A) was found higher than the specification (12.5 A);

contradictory to the fact that the voltage across inductor was smaller because of reduced output voltage (45.55V). The reason is the relationship between the amp-turns and inductance factor (A_L). At high current, because of increased amp-turns, A_L value slightly decreases [54][55], so the inductance also decreases and as a result current ripple increases. Although for Metglas core at higher temperature permeability increases [55], the effect was negligible in this case. Peak to peak IPT winding current (19.5A) also matched the theory, as $\Delta I_{Lin}/2 + \Delta I_{diff} = 7.5+11.5 = 19A$. For D<0.5 in figure 4.2, all the wave-shapes looked very close to their ideal forms. Because of 40% duty ratio, the peak to peak ripple in I_{Lin} was smaller. Ripple in output voltage was also smaller, so V_{diff} waveform was flat topped. In figure 4.3, for D=0.5, all the waveforms had ideal shapes. V_{diff} had a square wave shape and IPT winding currents and I_{diff} had triangular wave shapes. Peak to peak of IPT winding currents were equal to the peak to peak of I_{diff}. In all three figures 4.1, 4.2, and 4.3, V_{diff} and I_{Lin} had transient spikes synchronised to commutations between lower rail MOSFETs and upper rail MOSFET body diodes. Because of the poor reverse recovery characteristics of body diodes, the spikes for D=40% operation in figure 4.2 were very high, almost 150% of Vo in V_{diff} waveform. However, in all the figures, $V_{diff} = L_{diff} * dI_{diff}/dt$ relationship was maintained considering $L_{diff} = 24.5\mu H$.

Figure 4.4 and 4.5 illustrated the current sharing mismatch between IPT windings for 250W-600W operation. The reason for the mismatch is the unequal resistance of IPT windings. At higher power (above half of the rated condition) this mismatch diminishes because of the higher resistance of T-Clad copper tracks. Also as the circuit layout was almost symmetrical, the resistances of IPT winding paths were almost equal. As a result, voltage drops in them was also equal and at high current level this high voltage drop ensured equal current sharing. The maximum current sharing mismatch was found 6A. As the IPT was designed using a flux level which was less than 30% of the saturation flux limit of 3F3 ferrite core (0.44 T at 25°C), it had the ability to take high DC flux. Allowable DC current was calculated using the IPT specifications from table 2.7 such as Ae, A_L, and ΔI_{diff}. The equation of peak flux density is, $B_{max} = NI_{peak}A_L / Ae$ [36]. Now because of higher operating temperature, considering B_{max}=0.35 T, peak current in IPT winding, I_{peak} was found 17A. Ideal I_{peak} was 9A, as $(\Delta I_{Lin}/2 + \Delta I_{diff})/2 = 9$ A, so the allowable DC current mismatch without core saturation was 8A. Thus the core remained unsaturated even for the highest current mismatch between the IPT windings.

In all the I_{diff} wave-shapes in figure 4.5, the current slightly decreased from the ideal constant value, when both MOSFETs were on. The reasons were the resistances of winding and MOSFET. The analytical calculation to draw those waveforms also contributed some error. Figure 4.6 shows that only at two conditions, 1131W and 1407W operations, the ripple was higher than specified 12.5A, because of decreased input inductance. The average level of I_{Lin} showed the net input

current which is evident from table 4.1. Figure 4.6 showed that in all the power level operations, ΔI_{diff} remain almost equal to 11.5A, close to the predicted value (11.7A).

From table 4.1, in boost operation, the efficiency of the converter at rated condition was found 93.62%-93.86%, which closely matched with the predicted efficiency. As the power loss in circuit contacts was not considered and also the body diode power loss calculation was slightly biased by the assumed junction temperature, the loss audit could be considered accurate. In buck mode the voltage levels were slightly different, but similar efficiency was found for the rated condition. Although for the same voltage and power level, the efficiency would be different for buck mode, because of different current carrying paths in the circuit. For the same reason, current sharing between IPT windings was not perfect for buck mode operation.

In all the case the output voltage did not match the theoretical voltage conversion ratio. The reason is the voltage drop in the T-Clad copper tracks and other components. For the rated condition, the T-Clad track voltage drop was calculated 0.37V (Appendix A5). Also both Lin and IPT windings would have an average voltage drop of 0.05V, so in total approximate average voltage drop in the whole circuit is 0.47V. So for rated operation in table 4.1 (1501W), if this voltage is deducted from the input voltage of 11.64V, then the expected output voltage will be 45.65V, which is very close to the experimental value. For lower power as the voltage drop was less, results closer to the ideal voltage conversion ratio was found. Again in all the cases, output current closely matched the ideal conversion ratio.

The temperatures of different components were found to be close to the expected values. As the heat sink temperature was 5°C less than the prediction, the junction temperature of the devices would be around 70°-72° C. Based on the can temperature of the devices similar result was found. Considering 25°C ambient, the calculated inductor and IPT temperature were 82.2°C and 63.12°C, respectively (section 2.4.3), which were close to experimental results. However, the core temperature of the inductor was increasing with respect to its DC bias level because of the increased core loss. For the same reason, its temperature was found higher than the prediction.

4.4 Conclusions

This chapter shows the experimental results and their comparisons with the theory and design specifications. The similarities of experimental results with design specifications confirm the correctness of design calculations. Careful circuit layout and construction ensured low parasitic element in the circuit. The symmetrical arrangement of the circuit ensured symmetrical operation between the two phases of the converter. Careful thermal design ensured proper limits for temperature of different components even for long time operation at rated condition (about an hour). The next chapter with conclude this dissertation report by pointing out contributions and limitations of the research and by showing some paths for future works.

Chapter 5: Discussion

5.1 Introduction

Now-a-days, driving factors for power electronics development are new topologies, new components and new materials. New emerging technologies combined with new design techniques are making power electronic converters more efficient, more compact and more power-dense. This development is very essential for the current electric vehicle industry. To make electric vehicles competitive with conventional fuel based vehicles, vast amount of research is being conducted in power electronic converter design. In recent years, about one third of the total cost of an advanced electric car may be derived from power electronics development and this share is growing continuously [7].

This research showed that a highly efficient and power-dense 12V to 48V bidirectional DC-DC converter design can be possible with the currently available technologies. This 1.5 kW converter may be very useful in the auxiliary power unit of an electric vehicle. Although there are varieties in power train architecture of a modern electric vehicle, in all of them this converter can be used for interfacing the auxiliary power loads to the drive train or to the 12V battery. Similar applications of this converter can also be found in aeroplanes and electric ships. This chapter will summarise the research conducted during the dissertation period. It will also discuss specific contributions and limitations of the research. Finally some guidelines for future work are given.

5.2 Summary of the Research

A detailed literature review was done for designing this converter. At first to realize its usefulness, the power train architecture of electric vehicle was reviewed. Then to discover a suitable design for the converter, different topologies were assessed. A large portion of the total mass of the converter belongs to magnetic components, so different magnetic core materials and magnetic design techniques were reviewed. New technologies for semiconductor device and substrate were also reviewed. These reviews played a significant role in selecting different components for the converter.

The first step of the methodology for this converter design was to ascertain a design with minimum number of components. So the feasibility of design using the basic boost converter was analysed. Semiconductor devices with low loss and small foot-print were considered in the analysis and it was found that this simple design would not be feasible for the specified power. So it was decided to use a two phase configuration. From literature review it was found that an interphase transformer based dual interleaved boost configuration could give an improved efficiency and power density over other topologies, so it was selected for the proposed converter. Detailed operation of this converter was analysed and design equations were derived. Then, an International Rectifier MOSFET model, DirectFet was chosen based on its low profile design,

better cooling capability and higher performance capability over other models. Subsequently, on similar criteria a thermal clad substrate was chosen for the circuit. Careful thermal modelling was done for the MOSFET to see its thermal capability and to optimize the converter's thermal design.

Two magnetic components with different usages were present in the converter circuit. The input inductor required to be rated at the full converter power; thus it had to store a large amount of magnetic energy. On the other hand the interphase transformer (IPT) had to carry a small ripple flux. Amorphous-metal core was chosen for input inductor, because it has the highest saturation flux density limit among all core types. For IPT, low-loss ferrite core was chosen which has the lowest saturation flux density limit. This unique combination actually reduces the size and weight of magnetic components in the converter. For further reduction and more compact design, planar configuration was used for the IPT. Simple design equations were used to select an optimized core and an optimized winding arrangement for each of them. The main basis of the optimization was to utilize the maximum of the core area and window area, for a sensible current density and a small current ripple in the winding. Finally, multilayer ceramic capacitor was chosen for input and output current filtering because of its compact surface-mount design and good thermal capability.

After selecting all the components, a symmetrical power circuit layout was designed for the thermal clad board. Cautious design had to be done to minimise parasitic elements on this single-sided T-Clad board. Based on the detailed loss audit a heat sink was also chosen for the converter. The magnetic components were constructed carefully to get the exact amount of inductance from each of them. Especially for the planar IPT, a unique fabrication method was used to ensure good coupling between the winding turns. Finally, after constructing the whole converter, an experiment setup was prepared to test it.

The experimental results showed an excellent performance in different power levels for both boost mode and buck mode operation. High efficiency and perfect current sharing between the IPT windings depicted the outcome of careful design and construction of the circuit. Current ripples in the input inductor and in the IPT windings were almost similar to the specified design values. Temperature rise in different components showed that the converter could operate continuously for a long period of time at the rated condition. An efficiency of around 94% and a power density of 1.8 kW/litre were found from the designed converter.

5.3 Contributions of the Research

To the best of author's knowledge this is the first 12V to 48V bidirectional interphase transformer (IPT) based dual interleaved DC-DC converter with a power rating of 1.5 kW. Previous literatures showed this type of design for higher voltage and higher power operations, but for lower conversion ratios. Achieving a high efficiency with this high conversion ratio was a big challenge for this project.

No literature was found about the design and fabrication of planar IPT. Also this is the first time planar magnetic is used in IPT based dual interleaved converter. Although thermal clad substrates are becoming common in designing power modules for semiconductor devices, no literature was found about their usage in power rails of DC-DC converters. However, similar products like insulated metal substrates and direct bond copper substrates were used before in various designs. Also for the first time, double-sided cooling MOSFETs are used in IPT based interleaved boost converter. Another unique characteristic of this converter circuit is that all components except the input inductor and the IPT are surface-mount components. This arrangement gave a very compact shape to the whole converter. Although input inductor and IPT were connected to the power circuit using screws, they could work as surface mount components as well, if the shape of winding terminators is slightly changed.

5.4 Limitations of the Research

There is a significant amount of voltage drop and power loss in the copper tracks of the circuit. The reason was the 2oz. copper based T-Clad board. The depth of copper was only 70 µm. As the resistance as well as copper loss is inversely proportional to the cross-sectional area of the copper track, T-Clad board with thick copper layer could improve the efficiency and voltage conversion capability of the converter circuit. Bergquist T-Clad board is available up to 35 oz. which is equivalent to 350 µm [49]. For 40 kHz operation, the skin depth of copper is 352.6 µm, so higher thickness will not increase the AC resistive loss in the tracks. Also thicker copper will ensure lower width of copper track, so the footprint of the power circuit can be minimised. From the circuit layout it is clear that most of the area belongs to copper tracks, so if the copper thickness is made double, the effective area of the circuit will become around half, if similar loss is considered.

Due to the cost issue, a T-Clad substrate model with the least thermal conductivity had to be selected. A substrate with higher thermal conductivity could increase the thermal performance of the circuit and would reduce the required thermal conductivity of the heat sink. As a result, a smaller heat sink could be used. Bergquist T-Clad dielectric is available up to the thermal conductivity of 3 W/m-K [49]. So a better choice of T-Clad substrate would have increased the efficiency and power density of the circuit.

Apart from the input inductor, all other components had operating temperatures way below their specific limits. Specially, MOSFET junction temperature was around 70-72°C, whereas its junction temperature limit is 175°C. For reliable operation, if maximum junction temperature of the MOSFET is limited to 125°C, then the heat sink temperature specification can be increased from 60°C. As a result, the thermal conductivity and the size of heat sink will be decreased. Similarly for IPT, if operating temperature is pushed to its limit by increasing the current density in the winding, a smaller core can be selected, which will again increase the power density of the circuit.

For the input inductor, if Metglas AMCC-4 core was chosen instead of Metglas AMCC-6.3, the size and weight of the input inductor would have been smaller. This choice would eventually increase the power density of the converter at the expense of higher loss (AMCC-4 would have higher gap loss). As the lead time for getting an AMCC-4 core was too long compared to the project period, the available AMCC-6.3 had to be used.

For the purpose of measuring currents in IPT windings it was connected to the T-Clad board using two cables. In the final product it will be connected using flat copper bus bars and will stay on top of the T-Clad board. That configuration will be more compact. Again, a proper gate drive circuit for the MOSFET could not be designed because of the time issue. Although the circuit operated quite well in open loop configuration, closed loop control would have solved the problem of current sharing at lower power.

Now the power density of the converter can be approximated for a hypothetical design with a T-Clad board with double thickness of copper and double thermal conductivity, MOSFETs with operating junction temperature of 125°C, input inductor with AMCC-4 core, IPT with E38 core (double current density in the winding), and a proper heat sink. Assuming 100°C heat sink temperature, the required thermal impedance of the heat sink can be approximated to 1.15 °C/W, considering same power loss as the current design. If Fischer Elektronik-SK57210SA (1 °C/W) is used as a heat sink with a volume of 0.057 litre [62], then the calculated power density of the converter becomes 7.2 kW/litre. Detailed comparison of volumes between the proposed design and this hypothetical design is shown in Appendix A8.

5.5 Future Work

This research opens up the possibility for some further works which can improve the performance of the converter. At first higher frequency operation can be investigated to reduce the size of the magnetic components in the circuit. In that case, the design can be modified to see the zero voltage switching operation to minimize semiconductor device's switching loss. The circuit has to run in discontinuous mode to ensure zero voltage switching. Again at higher frequency core loss will be higher, so an appropriate heat sink for the input inductor has to be designed. The possibility for planar magnetics for the input inductor can be investigated. A number of planar cores can be combined together to increase the effective cross-sectional area of the cores so that the flux density remain low at high current. The application of planar magnetics in high power interleaved boost converter can be examined. Open loop or closed loop control circuit design for the current converter can be another possible investigation. The loss in Metglas core with respect to the DC bias level can be investigated further to explain the phenomena. Finally three-dimensional mechanical design optimization can be investigated to increase the power density of the converter.

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[61] HS Marston, *Product brochure: Ultra-Fin High Density Cooling* [online] available from http://www.farnell.com/datasheets/1692180.pdf
[62] Fischer Elektronik, *Product brochure: SK 572 10 S* [online] available from http://uk.farnell.com/fischer-elektronik/sk-572-10-sa/led-heatsink-standard-extruded/dp/1850080

Appendix A1: Diagrams of Power Net Architectures in Electric Vehicles

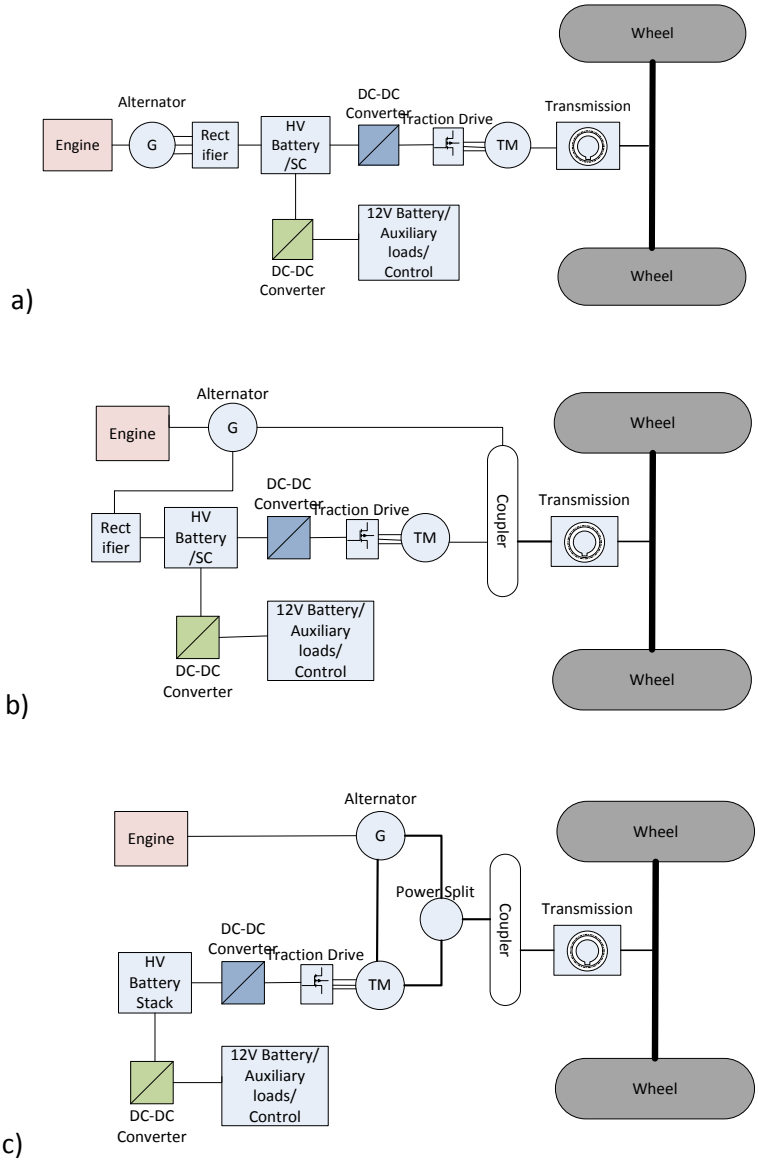


Figure A1.1: Typical powertrain configuration of hybrid electric vehicles: a) series, b) parallel, and c) series-parallel [6],[7]

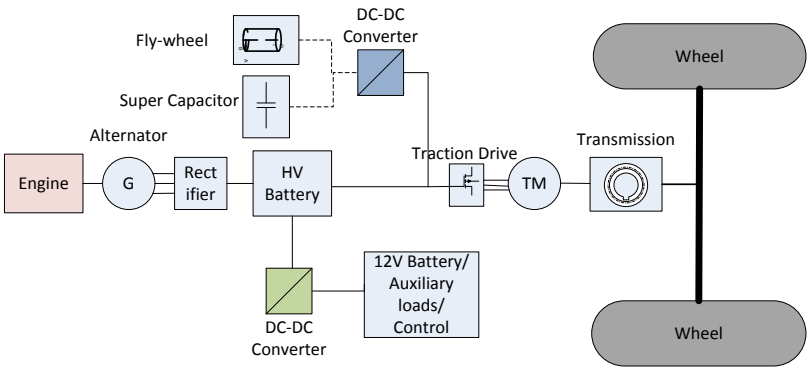


Figure A1.2: Super-capacitor or flywheel based peak power buffer in a series HEV [9]

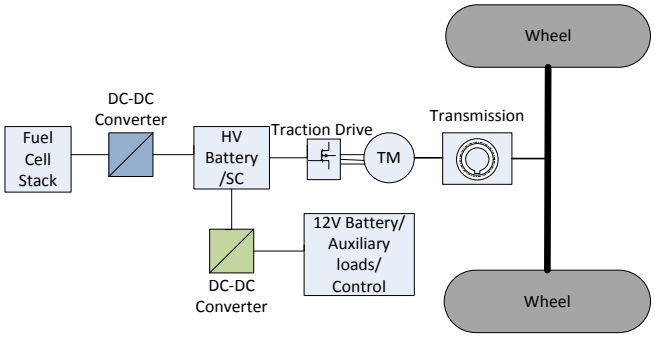


Figure A1.3: Typical powertrain configuration of a fuel cell based electric vehicle [6][7]

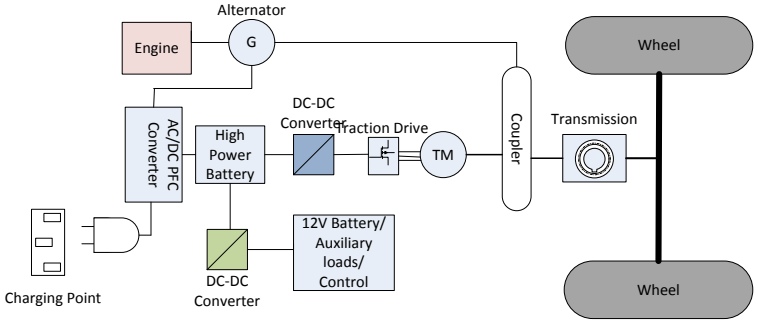


Figure A1.4: Typical powertrain configuration of a plugin hybrid electric vehicle [6]

Appendix A2: Derivation of Boost Converter Equations

A2.1 Boost converter in continuous inductor current mode

In steady state, for the input inductor current, it can be written that:

VinDT= LΔI and (Vo-Vin)(T-DT)= LΔI; where ΔI is the input current ripple.

So, $\frac{\mathrm{Vin}}{\mathrm{Vo-Vin}} = \frac{\mathrm{T-DT}}{\mathrm{DT}}$

Therefore, $\mathbf{\frac{Vo}{Vin} = \frac{1}{1-D}}$

Again, $\mathbf{\Delta I = \frac{VinDT}{L} = \frac{(Vo-Vin)(T-DT)}{L}}$

Now, output capacitor voltage ripple can be found by integrating the capacitor current for DT period.

$\Delta Vo = \int_0^{DT} \frac{Icdt}{C} = \frac{IoDT}{C}$

Therefore, $\mathbf{\Delta Vo = \frac{VoDT}{RC}}$

The MOSFET current waveform is shown in figure A2.1.

$\mathbf{It_{RMS} = \sqrt{\int_0^{DT} \frac{It^2 dt}{T}} = \sqrt{\frac{D(ILmax^2 + ILmax * ILmin + ILmin^2)}{3}}}$

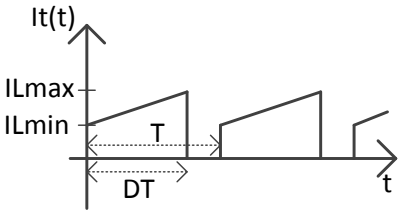


Figure A2.1: MOSFET current in CCM operation

A2.2 Boost converter in discontinuous inductor current mode

From the inductor current waveform it can be written that:

VinDT= LΔI

So, $\mathbf{\Delta I = \frac{VinDT}{L}}$

Now average input current, $I_{Lav} = \frac{\Delta I(D+\partial)}{2} = \frac{VinD(D+\partial)T}{2L}$

Now equating input and output power, $\frac{Vin^2 D(D+\partial)T}{2L} = \frac{Vo^2}{R}$

So, $\frac{Vo^2}{Vin^2} = \frac{D(D+\delta)TR}{2L}$. Again using volt second balance in the inductor current,

DTVin= δT(Vo-Vin), so $\delta = \frac{DVin}{Vo-Vin}$. Considering k= 2L/RT

$\frac{Vo^2}{Vin^2} - \frac{Vo}{Vin} - \frac{D^2}{k} = 0$. Now solving the equation, $\mathbf{\frac{Vo}{Vin} = \frac{1+\sqrt{1+\frac{4D^2}{k}}}{2}}$

Now, output capacitor voltage ripple can be found by integrating the capacitor current in figure A2.2 for Tx period.

$$\Delta Vo = \int_0^{Tx} \frac{Icdt}{C} = \frac{Tx(\Delta I - Io)}{2C}$$

$$Tx = \frac{\delta T(\Delta I - Io)}{\Delta I}$$

So, $\mathbf{\Delta Vo = \frac{\delta T(\Delta I - Io)^2}{2C\Delta I}}$

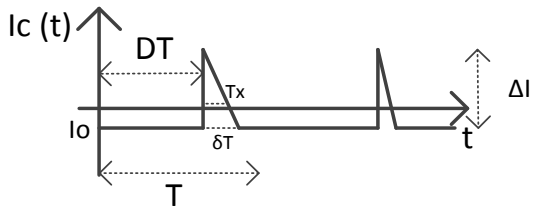


Figure A2.2: Capacitor current in DCM operation

Appendix A3: Input Inductor and Capacitor Design Calculations

A3.1 Input inductor

Energy stored in an inductor, W= $\frac{LI^2}{2} = \frac{\Psi I}{2}$; Ψ =flux linkage = N*B*Ae

So, LI^2 = N*B*Ae*I ; B= flux density

So, LI = N*B*Ae

Therefore **N=** $\mathbf{\frac{LI}{BAe}}$

Again N*I = *R**ϕ ; where *R*= reluctance of the magnetic circuit and ϕ = flux flowing in the circuit.

LI^2 = B*Ae*R*ϕ = B^2*Ae^2*R

Now, *R* = $\frac{lg}{Ae\mu o}$ considering all the reluctance were dropped in the air gap and thus assuming infinite permeability of the magnetic core.

So LI^2 = $\frac{B^2*Ae*lg}{\mu o}$ and thus

lg = $\mathbf{\frac{L*I^2*\mu o}{B^2*Ae}}$

A3.2 Capacitor

From capacitor current waveforms in figure A3.1 (D=0.75), RMS of the output capacitor current can be written:

$Ic_{RMS} = \sqrt{\frac{3Io^2+Icp^2}{6}}$;

Where, Icp = $\Delta I_L/2 + \Delta I_{diff}$

RMS of input current, $I_{cinRMS} = \frac{Icinp}{\sqrt{3}} = \frac{\Delta IL}{2\sqrt{3}}$

Input voltage ripple, ΔVin= $\frac{\Delta ILT(2D-1)}{8\Delta V}$

(only for D=0.75 and D=0.25)

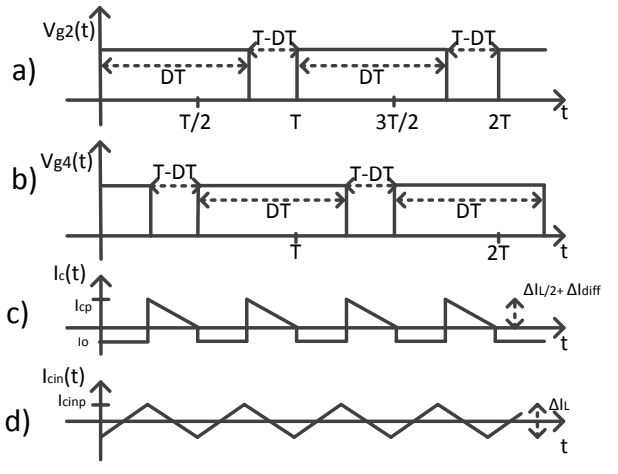


Figure A3.1: a)MOSFET Q2 gate voltage, b) MOSFET Q4 gate voltage, c) Output capacitor current and d) Input capacitor current (D=0.75)

Appendix A4: Bus bar Size Optimization and Loss Calculation

Temperature	70	°C					
ρ	20.8604	μΩ-mm					
Height for all	8	mm	Based on screw size				
P1,P2 width	15	mm	Based on 125A cable crimp size				
J1,J2 diameter	10	mm	Based on 62.5A cable crimp size				
P3 width	5	mm	Based on 31.25A cable crimp size				
P1,P2 area	120	mm^2					
J1,J2 area	78.5	mm^2					
P3 area	40	mm^2					
I1	125	A					
I2	62.5	A					
I3	31.25	A					
Length (mm)	**R1 (μΩ)**	**Power loss 1 (W)**	**R2 (μΩ)**	**Power loss 2 (W)**	**R3 (μΩ)**	**Power loss 3 (W)**	**Total loss (W)**
8	1.39	0.022	2.13	**0.008**	4.17	0.004	0.090
9	1.56	0.024	2.39	0.009	4.69	0.005	0.101
10	1.74	0.027	2.66	0.010	5.22	0.005	0.112
11	1.91	0.030	2.92	0.011	5.74	0.006	0.124
12	2.09	0.033	3.19	0.012	6.26	0.006	0.135
13	2.26	0.035	3.45	0.013	6.78	0.007	0.146
14	2.43	0.038	3.72	0.015	7.30	0.007	0.157
15	2.61	0.041	3.99	0.016	7.82	0.008	0.169
16	2.78	0.043	4.25	0.017	8.34	**0.008**	0.180
17	2.96	0.046	4.52	0.018	8.87	0.009	0.191
18	3.13	0.049	4.78	0.019	9.39	0.009	0.202
19	3.30	0.052	5.05	0.020	9.91	0.010	0.214
20	3.48	0.054	5.31	0.021	10.43	0.010	0.225
21	3.65	0.057	5.58	0.022	10.95	0.011	0.236
22	3.82	0.060	5.85	0.023	11.47	0.011	0.247
23	4.00	0.062	6.11	0.024	11.99	0.012	0.259
24	4.17	0.065	6.38	0.025	12.52	0.012	0.270
25	4.35	**0.068**	6.64	0.026	13.04	0.013	0.281
26	4.52	0.071	6.91	0.027	13.56	0.013	0.292
27	4.69	0.073	7.17	0.028	14.08	0.014	0.304
28	4.87	0.076	7.44	0.029	14.60	0.014	0.315
Total loss for the selected sizes			**0.24**	**W**			

*Total loss= Power loss 1*3+ Power loss 2*2+Power loss 3*2

Table A4.1: Bus bar size optimization and loss calculation

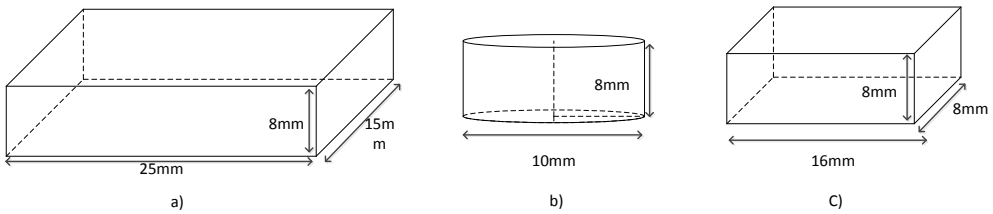


Figure A4.1: Bus bars for a) input connector and inductor connector, b) IPT connectors, and c) output connector

Appendix A5: Power Loss Calculation in T-Clad Tracks

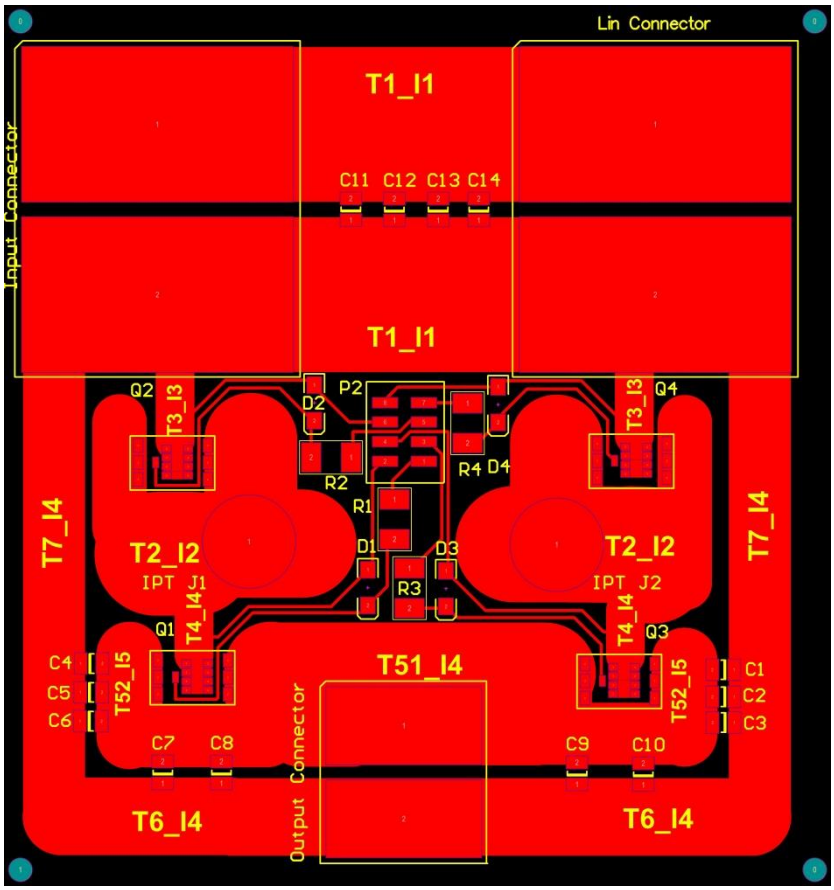
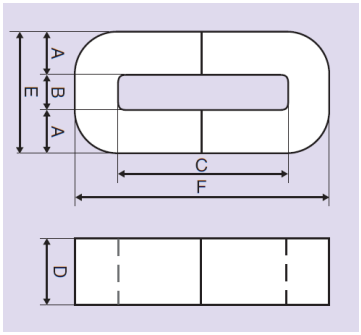


Figure A5.1: T-Clad Copper tracks numbered according to the widths and currents

Temperature	70	°C						
ρ	20.8604	μΩ-mm						
Cu height	0.07	mm					Current density (A/mm^2)	
T1 length	28.5	mm	Width	20	mm		89.29	
T2 length	77.2	mm	Width	14	mm		63.78	
T3 length	20.2	mm	Width	4.75	mm		140.98	
T4 length	20.2	mm	Width	4.75	mm		46.99	
T51 length	35.45	mm	Width	19.5	mm		11.45	
T52 length	48.7	mm	Width	8.25	mm		13.53	
T6 length	89.35	mm	Width	10	mm		22.32	
T7 length	123.15	mm	Width	8	mm		27.90	
Currents (A)			**Resistances (μΩ)**			**Ploss (W)**		**Vdrop (V)**
I1	125		R1	424.6581		P1	6.64	0.05
I2	62.5		R2	1643.289		P2	6.42	0.10
I3	46.875		R3	1267.309		P3	2.78	0.06
I4	15.625		R4	1267.309		P4	0.31	0.02
I4	15.625		R51	541.7591		P5	0.13	0.01
I5	7.8125		R52	1759.137		P6	0.11	0.01
I4	15.625		R6	2662.681		P7	0.65	0.04
I4	15.625		R7	4587.425		P8	1.12	0.07
						Total	**18.16**	**0.37**

Table A5.1: Power loss calculation in T-Clad tracks

Appendix A6: Input Inductor Dimensions, AC Resistance of IPT Winding and Experimental Setup



A=10, B= 11, C= 33, D=20, E=31, F=53, Ae=164

a)

b)

Figure A6.1: a) Dimension of AMCC-6.3 core (all dimensions in mm/mm^2) [54] and b) Photo of input inductor

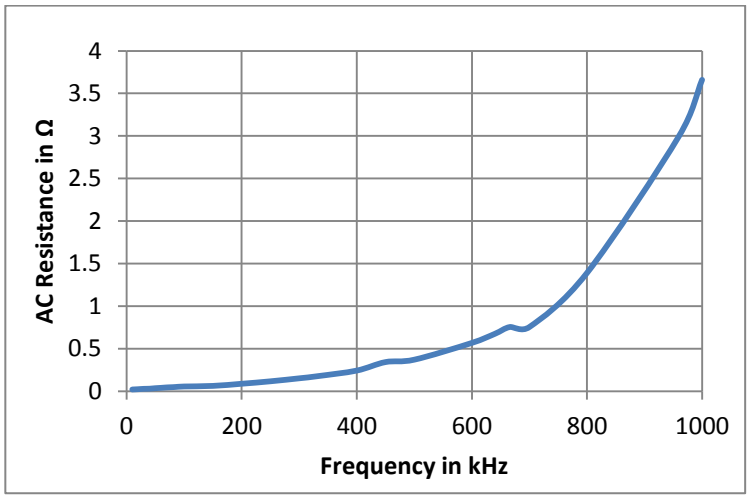


Figure A6.2: AC resistance vs. frequency for IPT winding

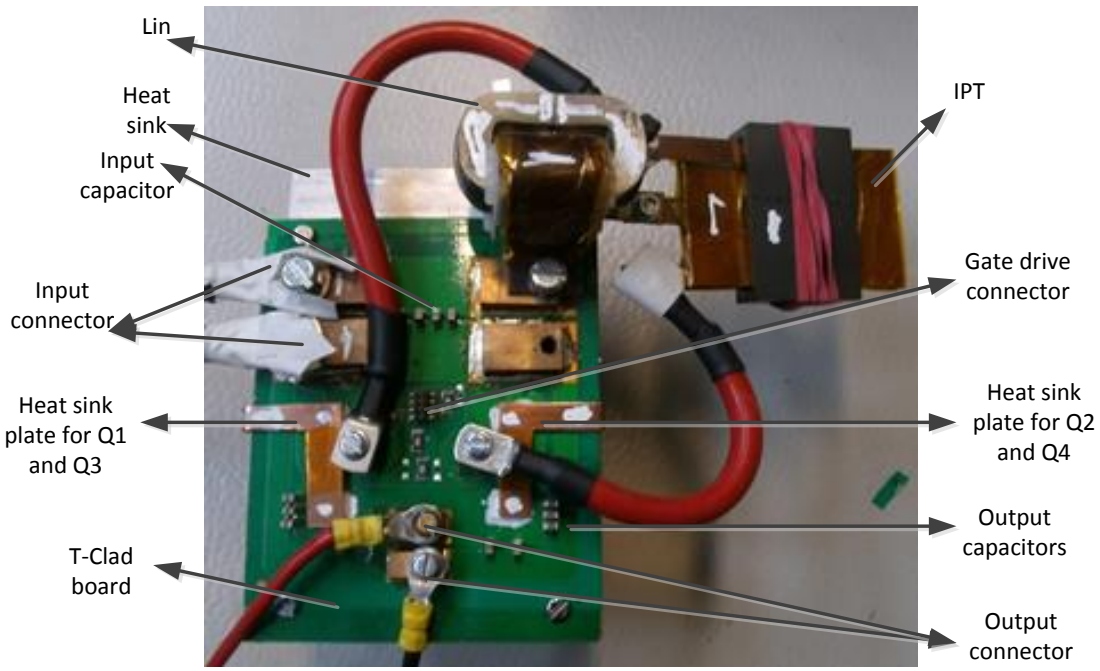


Figure A6.3: Top view of the converter circuit

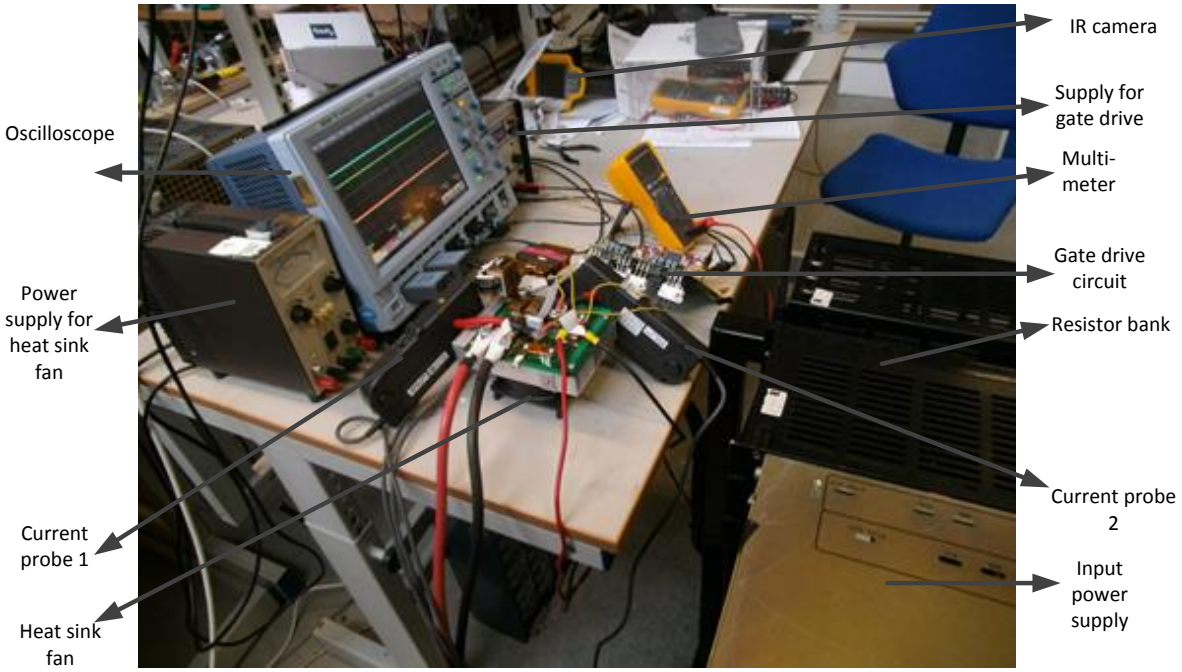


Figure A6.4: Experimental set-up

Appendix A7: Temperature Monitoring at Rated Condition

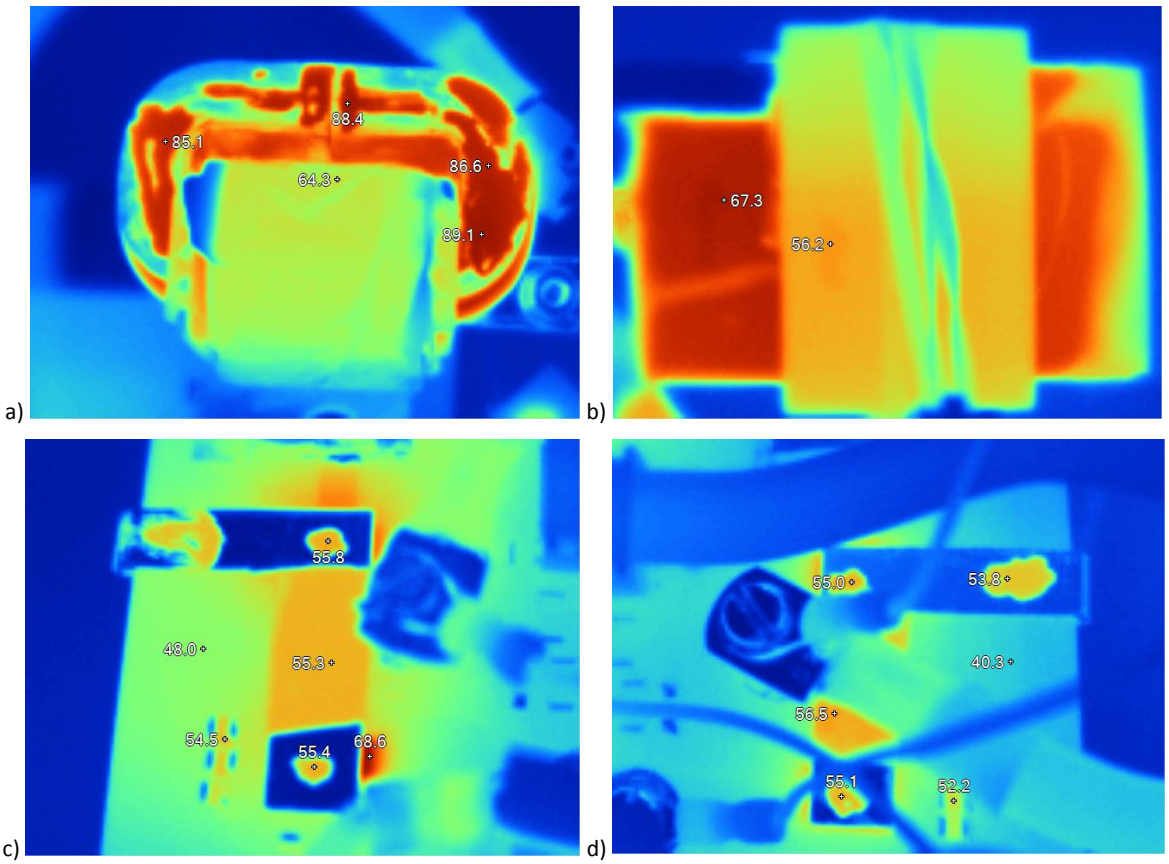


Figure A7.1: Temperature of different components of the circuit a) input inductor, Lin, b) interphase transformer, IPT, c) MOSFETs in the first phase leg and d) MOSFETs in the second phase leg

Appendix A8: Power Density Comparison between the Proposed Design and a Hypothetical Design

	Volume of component (litre)					
	Heat sink*	T-Clad board with mounted components	Input inductor	IPT	Total	Power density** (kW/litre)
Proposed design	0.416	0.143	0.096	0.07	0.725	2.2
Hypothetical design	0.064	0.0715	0.0625	0.022	0.2201	7.2

*Heat sink fan is not considered for the proposed design

**Considering the highest achieved power of 1.58 kW

Table A8.1: Power density comparison between the proposed converter and a hypothetical one

Appendix A9: Feasibility Study Report

Abstract

The power density of DC-DC converter is one of the most important issues in the electric vehicle industry. Several power dense converter topologies and component design techniques are reviewed in this report to find out an optimum design for a power dense 12V to 48V DC-DC converter. This boost converter has various automotive applications like interfacing power rails and connecting auxiliary loads to the 12V battery in a more electric vehicle. A bidirectional converter is selected to accumulate the zero voltage switching which ensures higher efficiency because of the increased available switching frequency and lower diode reverse recovery losses. A four phase interphase transformer based interleaved boost converter is primarily selected. This design has lower ripple magnitude and higher ripple-frequency in the input current than a dual interleaved boost converter. So the power density of the converter will be increased due to reduced size and weight of magnetic components. The objectives and methodology of this project is clearly described. The time plan for the project shows that it is possible to complete the project successfully within twelve weeks. Different risk associated with the project and their mitigations are also discussed to find out the feasibility of this project.

Introduction

In many engineering applications where the mechanical system is being replaced by electrical system the power electronic converter has become quite common. Examples of these types of application are electric vehicle, more electric aircraft, more electric ship, production industry etc. Here the mechanical, hydraulic or pneumatic loads and systems are being replaced by the electrical loads and distribution system. The reason for these changes is to improve the system efficiency and reliability by reducing the overall system mass and complexity.

In case of any vehicles the torque and hence the power is mostly dependent on the combined mass of the vehicle and payload [1]. So the more mass means more power requirement which means more fuel consumption and more emission. The ever increasing fuel price and the movement for green technology have established the need for lighter and efficient vehicles in all the transportation sectors. Though the more electric concept was adopted earlier in the aerospace applications, for the last two decades there has been an enthusiastic expansion of commercial electric vehicles as well. Considering the broad definition of electric vehicle (EV) i.e. any vehicle with the electric propulsion there are three types of electric vehicle in the automotive industry: i) Battery electric vehicle, ii) Hybrid electric vehicle and iii) Fuel cell electric vehicle [2]. In all the models of EV power electronic converters are used to interface the energy storage components to the actuators and other auxiliary electrical appliances. Essentially it is the enabling technology for the next generation vehicles, which have to be smarter, cleaner, more efficient, more precise, and more flexible [3]. However, because of the size, efficiency and cost issues the power electronic systems were not so popular initially [3]. But due to the need of new architecture for increased electrical loads, on demand power and voltage conversion, precise electronic control and high power-fast motion automotive power electronic system had gained increased interest [3]. And now-a-days about one third of the total cost of an advance car may belong to the power electronics development and this share continues to grow steadily [3].

The power density of a power electronic converter means the power processed in per unit volume or mass of the converter. The needs for improvements in comfort, convenience, safety, reliability, performance, cost, communication, entertainment, and environmental issues necessitate the needs for improved technologies like power dense bi-directional converters in the future EV [3],[4]. A high power DC-DC converter is required to interface fuel cell/ super-capacitor/battery stack with the traction motor drive through the DC link. The DC link voltage is normally in the range of 200 V to 600 V [5]. Again due to the increased auxiliary loads in the EV another low power (around 1.5 kW) DC-DC converter is required to interface the load with the 12 V auxiliary battery. For example the Toyota Hybrid Synergy Drive II power electronic system unit is composed of an inverter for the air conditioner, an inverter for the starter and the generator, an inverter for the traction motor, a dc–dc converter for the auxiliary 12 V battery, and a dc–dc bidirectional converter for the high voltage battery [6].

The basic components of a DC-DC converter are inductor/ transformer, capacitor, transistor, diode and heat sink. Though the inductor/transformer and heat sink are liable for most of the weight of the converter, the quantity, size and weight of all the basic components should be optimized to make the converter power dense.

The feasibility for design and construction a novel bidirectional 12V to 48V DC-DC converter is discussed in this report. The converter is proposed for the use in automotive application especially in the electric vehicles where power density is very crucial as discussed above. So several techniques like unique converter topology, planner magnetics, surface mounted devices and soft switching are considered to be implemented to make this converter smaller, lighter, energy efficient and reliable.

Section 1: Aims and Objectives

The aim of this project is to design, construct and evaluate a power dense bidirectional 12V to 48V DC-DC converter for automotive application. The major objectives of the project are:

1. Identifying the power dense DC-DC boost converter topologies which are applicable to the automotive application especially in the EV and also applicable for miniaturization.

2. Identifying the most suitable converter components like inductor, transistor and capacitor.

3. Identifying the fabrication method for the inductor

4. Paper design of the converter circuit focusing into its electrical, mechanical and thermal optimization for target efficiency of 95% and power density of 6.5 kW/kg.

5. Constructing and testing the 1.5 kW bidirectional 12V to 48V DC-DC boost converter in the laboratory using the soft switching technique and a simple peak current mode controller.

Section 2: Literature Survey

Several publications in the last five decades showed the development of the power dense boost converter for different application. However few publications are found regarding design of power dense boost converter with similar power and voltage level configuration as targeted in this project. In this section at first the basic boost topology will be reviewed, then several other topologies regarding the compact or power dense boost converter will be discussed, then some topologies specially designed for electric vehicle will be discussed and finally some techniques of choosing and designing basic converter components (inductor, capacitor and transistor) will be reviewed from previous literature.

2.1 Boost Converter Basic Architecture and Operation

Figure 1 show the basic circuit of a DC-DC boost converter which comprises of an inductor, a transistor, a diode and a capacitor and the input/inductor current. The circuit can operate in two modes: continuous inductor current mode (CCM) and discontinuous inductor current mode (DCM). In both cases the inductor stores the energy when the transistor switch is on and then transfers it to the load and capacitor when the switch is off. If the duty ratio of the of the gate signal of the switch is D then the relationship between the input and output voltage can be written as [7]:

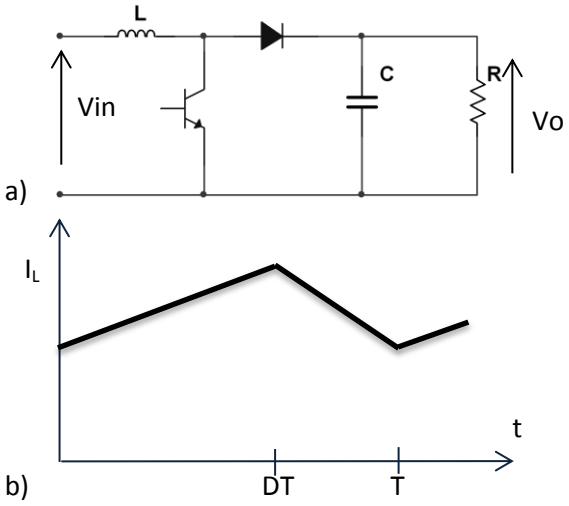


Figure 1: a) Basic circuit diagram of boost converter and b) Inductor current in CCM[7]

For CCM, $\frac{Vo}{Vin} = \frac{1}{1-D}$ (1)

For DCM, $\frac{Vo}{Vin} = \frac{1+\sqrt{1+\frac{4D^2}{k}}}{2}$ (2)

where, k=2L/RT

The peak to peak ripple in the inductor current of figure 1 can be written as [7]:

$$\Delta I = \frac{VinDT}{L} = \frac{(Vo-Vin)(T-DT)}{L} \quad (3)$$

Again the expression of capacitor peak to peak voltage ripple is [7]:

$$\Delta Vo = \frac{DTVo}{RC} \quad (4)$$

From equation 3 and 4 it can be said that if the switching frequency for the transistor is higher then for the same input current ripple and output voltage ripple specification the size/ value of

the inductor and capacitor will be lower. However in practice there is a switching frequency limit for each and every electronic switch depending on the thermal capability and switching loss [7]; also magnetic loss increases with the square of the frequency [8]. Equation 4 also shows that the output voltage ripple specification fixes the capacitor size and equation 3 shows that the inductor value is determined by requirement to limit the peak current level depending on the core material. The choice of operating mode i.e. CCM or DCM also affects the choice of inductor in the boost circuit. So the design of the converter requires a compromise among the switching frequency, inductor size, capacitor size and switching losses [8]. Nevertheless the DCM mode operation cause pulsating current in both input and output and thus cause electromagnetic interference (EMI) problem in the circuit.

2.2 Bidirectional Boost Converter with Zero-voltage Switching

The bi-directional boost converter with the lossless snubbers shown in figure 2 is explained in [7]. In this circuit one additional transistor Q1 and one additional diode D2 are used to facilitate the zero voltage switching (ZVS) and as well as bidirectional power flow. Before the turn on of each of the transistor the antiparallel diode conducts which ensures the loss less turn on process for the transistors. Again the current in the diodes falls to zero gradually which diminishes the reverse recover loss in the diodes. The lossless snubber operation using C1 and C2 capacitors ensures minimum turn off loss for the transistor. The advantage of this circuit is if the power Mosfet is used as a switch then the diode and capacitor will be a part of the device i.e. not separate components. Also no additional switch is used to facilitate ZVS. However the boost circuit has to be operated in the DCM mode and a large ripple current in the input inductor is required for this converter operation. So the EMI noise problem is still present in this circuit. Again ZVS ensures higher achievable switching frequency because of lower power dissipation in the device as a result of lower switching loss. This can help to achieve higher power density by making inductor and capacitor size smaller. [7]

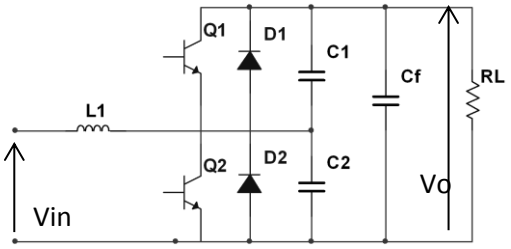


Figure 2: Bidirectional boost converter with lossless snubbers [7]

2.3 Cuk Converter with Coupled Inductor

The Cuk converter shown in figure 3 is based on the capacitive energy transfer, which causes the input current to be always continuous in both CCM and DCM mode [8]. It is shown in [9] that by coupling the inductors L1 and L2 into a single core two winding configuration it is possible to remove the ripple from either input or output inductor current as the voltage waveforms across both inductors are identical [9] (considering fixed voltage across C1).

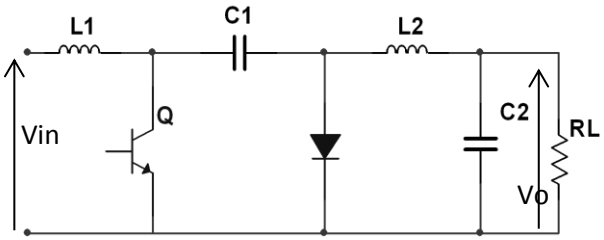


Figure 3: Circuit diagram of Cuk converter [8]

Using appropriate coupling coefficient (k=√(L2/L1)) between the winding it is possible to shift the ripple current from input to output and vice versa for k=√(L1/L2) [9]. Again using multiple-output, multiple-gap coupled inductor structure it is possible to make the both input and output current ripples simultaneously zero [9]. This technique ensures more efficient use of magnetic materials and thus increases the power density of the converter. The Cuk converter also has the advantage of overload protection because of the intermediate capacitor C1 [10]. However the capacitor is stressed as it has to carry large input and output current with a DC voltage across it [10]. The voltage stress across the transistor and diode is also higher than the boost converter. The peak current in the transistor is also very high as it has to carry the both inductor's current. For these reasons for boost only operation it is not an effective model in spite of having lower current ripples and better EMI.

2.4 Modified Boost Converter with Ripple free Input Current

A modified boost converter circuit is presented in figure 4 which has a ripple free input current in both CCM [10] and DCM [11] operation. The voltage conversion relationship and the voltage stress across the switch and diode are similar to the conventional boost converter for both CCM [10] and DCM [11]. Using similar coupling of the two inductors (k= √(L2/L1)) as shown in previous sub-section, it is possible to get a ripple free input current in both inductor current modes [10] [11]. Though the number of components is equal to the Cuk converter, Cs voltage stress is lower in this circuit as it is working as an output filter rather than an energy transfer device. The current and voltage stress in the switches are also lower than the Cuk converter. So this circuit has the advantages of the both conventional boost and coupled inductor Cuk converter. Even in the DCM mode if the inductors are not coupled the current ripple in L1 is actually lower than the conventional boost converter. In fact in the DCM mode none of the inductor currents are discontinuous. Instead of L1 current falling to zero, in this circuit a constant current flows in both of the inductors (diode remains off and L1 and L2 acts as constant current source in L1CsL2 loop by charging Cs). The ripple free current in L1 is found independent of load in the coupled configuration. [11] Though this modified boost converter shows a better power density than the previous coupled Cuk converter, still the ripple in the L2 current is very high and additional components are required with respect to conventional boost converter. Again the switch voltage and current stress are exactly similar to the conventional boost converter.

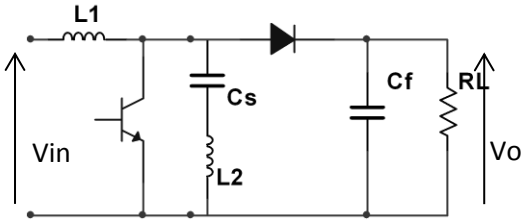


Figure 4: Circuit diagram of modified Boost converter [10][11]

2.5 Interleaved boost converter

Figure 5 shows the two-phase unidirectional and bidirectional interleaved boost converter. The purpose of interleaving the boost converter is simple; it reduces the input current ripple of the converter as shown on figure 6. For two-phase the gate pulses for the transistors in each leg in figure 5 are 180° shifted. If three phases are used it would be 120° shifted. For two-phase if the duty ratio of both transistors is 0.5 then the input current will be ripple free. Again the frequency of the input current and the output filter capacitor current increases without increasing the switching loss [12],[13]. Also the input current always remained continuous because of interleaving even in the DCM operation [13]. The important drawbacks of this type of converter are limited voltage conversion ratio, un-equal current sharing between the phases, enhanced complexity in control and the presence of input current ripple [12],[11].

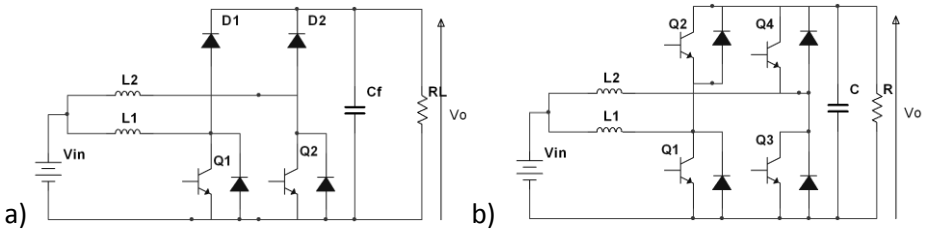


Figure 5: Two-phase interleaved boost converter a) unidirectional and b) bidirectional [12]

Several research papers showed the application and advantage of interleaved boost converter in power factor correction operation. In [13] it was shown that the interleaving can reduce the size of the magnetic components and size of the EMI filter without reducing the efficiency. It also

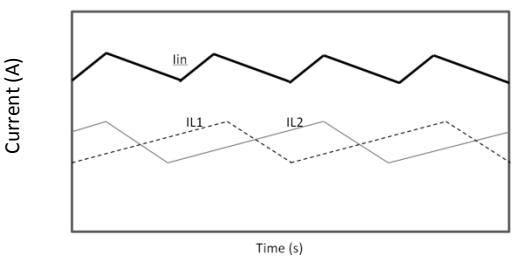


Figure 6: Ideal input current waveforms in two phase interleaved boost converter [12]

described the design of a 3kW telecom power supply with dual interleaved boost converter which had an efficiency of 97.5% and power density of 8.5 W/in^3, including the heat sink, EMI filter and auxiliary hardware. A solution to the unequal current sharing problem was also given using average current mode control and by monitoring the switch current using operational amplifier. [13]

For an N interleaved configuration if the energy storage is considered fixed then the ripple amplitude reduction will be at least N times than the single cell ripple. Moreover, in case of interleaving the maximum reduction occurs over the duty ratio range when the ripple is largest, so the worst-case interleaved ripple amplitude is reduced from the worst-case non-interleaved ripple amplitude by a further factor of N. So in total there will be a factor of N^2 reduction in worst-case ripple amplitude of the single cell configuration. Again for the interleaved configuration it is possible to reduce the switching frequency by a factor of N and to reduce the inductance per cell by a factor of N. If net interleaved ripple is unchanged then the per-cell ripple will become N^2 times larger than a single-cell converter. So the interleaving can increase the power density and power conversion efficiency as well as reduce the input ripple amplitude. Thus the converter design can be optimized by predicting appropriate ripple magnitude reduction. [14]

A multi-device interleaved DC-DC boost converter for EV application is shown in [15] where each transistor in figure 5a was replaced by a pair of two parallel transistors. Although it shows better performance than the usual interleaved boost converter with respect to the efficiency and power density because of the double switching frequency in the inductor currents without the increment of switching loss, the technique utilizes semiconductor switches poorly as the maximum achievable duty ratio was less than 50%.

Now coupling the two inductors in figure 5 in a single core can provide further advantage to the interleaved boost converter like size reduction and better current sharing. Reference [16] shows that the closely coupled inductors provide good current sharing even in the presence of large duty cycle mismatch between the two phases. It also shows that the DCM operation significantly improves converter efficiency by eliminating the reverse recovery loss in the diode [16]. Lower average diode and transistor current, lower peak transistor current are also found in this converter circuit than the conventional boost converter [16].

Figure 7 shows a modified configuration of interleaved boost converter where the individual cell inductors are coupled in a way that the resulting circuit becomes more efficient and power dense. Such integration of two inductors in a single core with an inverse coupling can be called as an interphase transformer (IPT) [12]. It is shown in [17] that using a small value of Lin and closely coupled inductor L11 and L22 it is possible to achieve reduced size and lower losses in the magnetic components than the loosely coupled inductors in the interleaved boost converter circuit. The reason is with the lower coupling coefficient the DC flux in the core cannot be completely cancelled [17]. Because of the high power density, high efficiency and low temperature increase in high current, this boost converter can be considered ideal for the electric vehicles applications [17]. However this sort of integrated magnetics may require unconventional and complex core design [18].

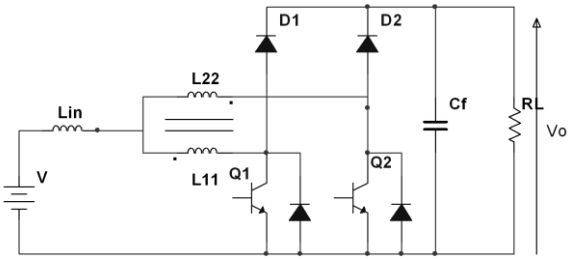


Figure 7: Dual Interleaved converter with closed coupled inductor/ IPT [12]

Detailed steady state operation, design and construction of an IPT and input inductor based dual interleaved boost converter are shown in [12]. It is found that due to the inverse close coupling and considered perfect current sharing between the branches the DC flux in the IPT core will be zero. The use of IPT interleaved boost converter has the advantage of reduced size and weight of the overall magnetic components without using any special cores [19]. For the same amount of DC inductive stored energy and same input ripple in the circuit of figure 5 and figure 7 the input

inductor for IPT based converter is half of the individual branch inductance in figure 5 [12]. Again the LΔI value (ΔI is the input ripple current) is much lower for Lin in figure 7 than the inductors in figure 5, which affects it's size and core loss [19]. Again a large DC current will flow in the Lin, so a core with high saturation flux will be required for it. Again the ripple in the L11 and L22 is high, but that does not hamper the power density as high frequency ferrite (low saturation flux and low core loss) core can be used to design IPT as the is no DC flux in the IPT core. A 10 kW prototype design (for EV application) in [19] shows that the resultant circuit has lower loss and lower weight than the conventional dual interleaved boost converter. A similar situation is found in [20] where bidirectional IPT based dual interleaved boost converter was evaluated for power dense EV application. The power density and the maximum efficiency of the converter were found 6.5 kW/kg and 94% respectively.

For the zero voltage switching operation the technique shown in subsection 2.2 can be used. So there will be two additional switches in the two phase of IPT based interleaved boost converter replacing the diodes D1 and D2. The switches will also ensure the bidirectional power flow and ZVS in the circuit. It is shown in [21] that if the ratio between the IPT inductance and input inductance is low (<0.7) for a large range of duty ratio and load conditions the circuit remains in DCM and ZVS operation is achieved even with the constant switching frequency. The design procedure of IPT transformer using distributed gap ferrite core and the peak current mode control to ensure equal current sharing the IPT branches are also explained in the paper. This simple open loop control shows a very good performance [12],[21].

In [22] a detailed comparison between the IPT based interleaved boost converter and only inductor based interleaved boost converter is shown for wide ranges of load. Again it was found that the power density in the IPT based converter is much higher than the usual only inductor based one. Also the impact of magnetizing inductance of IPT in the ZVS operation was investigated in this paper.

2.6 Magnetic component design

An appropriate magnetic component design is very crucial for increasing the power density of DC-DC converters. Several publications investigated different core materials and core structures like shape and gap design to reduce the size and weight of the magnetic components. Reference [18] shows a compact integrated magnetics core structure for integrating 3 inductors of a 3 phase interleaved boost converter. The core had one central leg which was shared by the three outer legs corresponding to the 3 phases [18]. The deign reduced the ripple current magnitude in each of the inductor which was dependent on the reluctance ratio between the outer leg and central leg. Lower reluctance ratio ensures lower ripple; so two different materials i.e. ferrite and powdered iron were proposed for the outer legs and central leg respectively [18]. Though the design ensured power dense magnetics and higher efficiency of the converter the custom core design poses a problem to its practical implementation.

Planar magnetic components can be considered as an ideal solution for the power dense converters. Reference [23] gave a detailed analysis on the applications of planar magnetic components in the medium power (less than 500 W) DC-DC converters. As the winding is built up in the Z direction instead of conventional XY direction, these components have a greater surface area to volume ratio. So the thermal management is easier for them as more area can be connected to the heat sink. The winding is normally made by the PCB which also contains the converter power circuit. The most important advantages are low high frequency winding loss and controlled leakage inductance. However there are also disadvantages associated with the PCB based planar magnetic design like low window utilization factor, requirement for custom cores, stray capacitance formation in the interleaved configuration etc. If the number of parallel winding is high then the conventional magnetic structure can be considered economically equivalent to the planar components. [23]

Section 3: Summary of the Literature Review and Preliminary Decision

From the literature survey it is found that the interleaved boost converter shows a power dense configuration for the DC-DC boost conversion. Because of the paralleling of the boost cells the current in the each transistor switch is low and the voltage stress across the switch is also inherently low in the boost converter circuit. Because of the lower current ripples the electromagnetic interference is also low in this circuit. The IPT based bidirectional interleaved converter shows further lower weight and higher efficiency type improvements. In the DCM operation the zero voltage switching can be achieved and the diode reverse recovery losses are minimized which increases the efficiency of the circuit. For all these reasons the IPT based interleaved boost converter can be considered as an attractive solution for the future EV applications. In magnetic component design the IPT based converter has several advantages and challenges. Planner magnetics can be considered for compact design of the magnetic components. Based on the literature review, a preliminary decision is made to use the circuit in figure 8, where two IPT based bidirectional boost converters are paralleled to get further advantages like more power density, reduced input current ripple, higher ripple frequency and lower current stress in the switches.

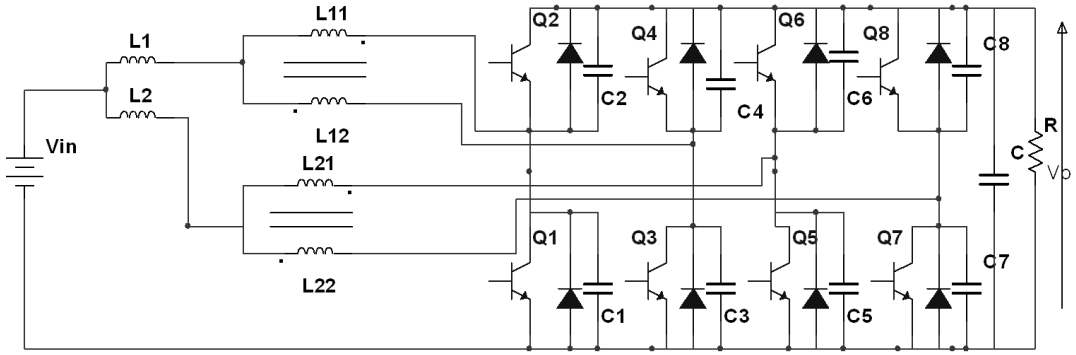


Figure 8: Paralleled IPT based interleaved bidirectional boost converter

Section 4: Methodology and Project Plan

The methodology for this research is based on subdivided tasks to achieve the objectives of this project. According to the methodology a project plan chart is also presented in the table 1 of the subsection 4.2.

4.1 Methodology for the project

The following figure 9 gives an overview of the methodology for this project. The detailed tasks are described below the figure.

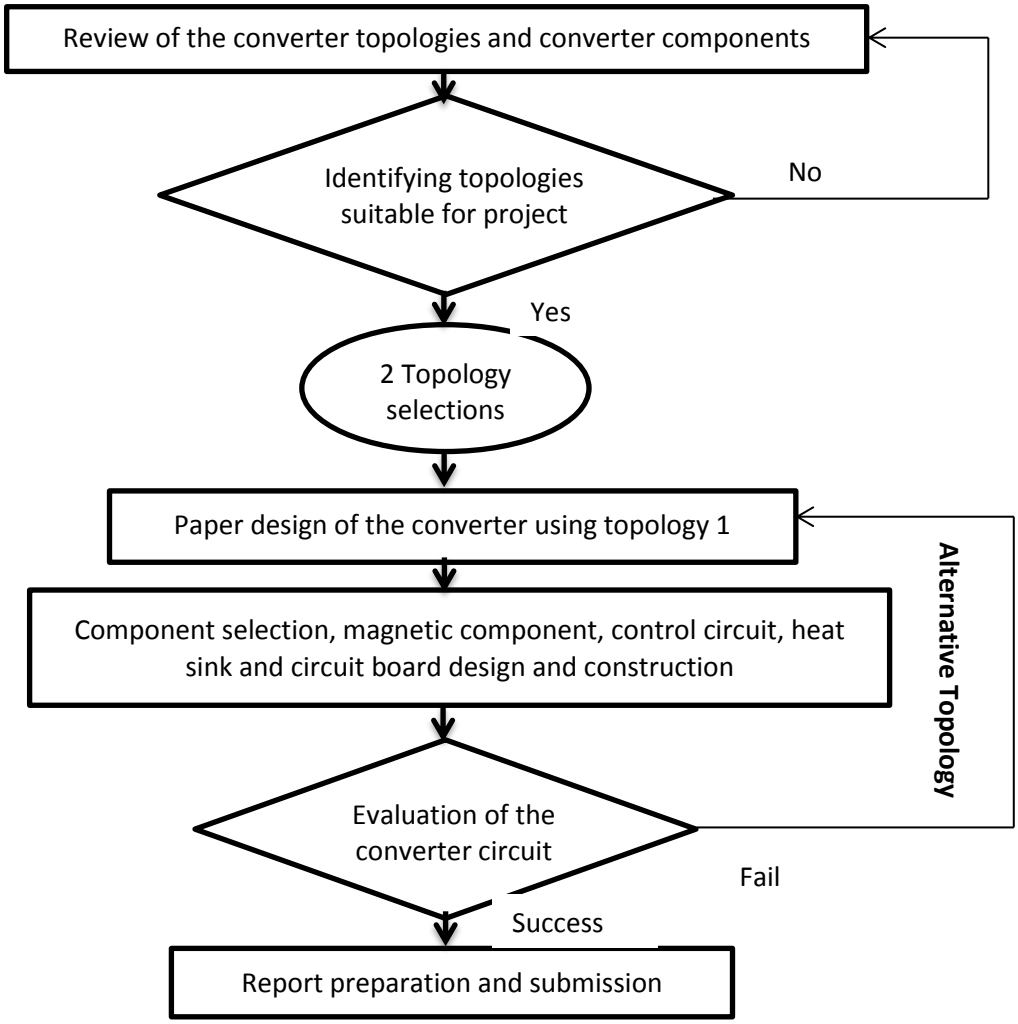


Figure 9: Project methodology flow chart

Task 1: Review of the power dense DC-DC boost converters for automotive application

This will be a continuous review of research publications regarding the power dense DC-DC converters for the automotive application for the first seven weeks. The review will be done parallel to the design works. The different converter topologies and their modelling scope will be investigated and ranked according to their advantages and applicability in this project. The size, weight, efficiency, power density, thermal management and control technique will be carefully analysed. In essence any new power dense configuration will be analysed and an effort will be given to find out their applicability in the automotive application. Considering the project time constraint very complex design will be discarded from this analysis. Though this will be a continuous review the final choice of topology for the project will be done in the first week as shown in the project plan chart in table 1.

Task 2: Review of the converter components

The major electrical components of the converter will be reviewed and components will be categorized according to their advantages in a power dense design. At first the inductor design will be reviewed as it weighs typically 20-30% of the whole converter [18]. The existing state of the art inductor design will be surveyed. The applicability of different core materials, core types and winding arrangements will be investigated. The custom design of cores will not be considered because of the time constraint in the project. The range of semiconductor technologies and the power dense capacitor design will also be investigated. The rating of the devices like current and voltage rating, allowable switching frequency and switching losses, thermal rating etc. will be pointed out from the datasheet and the application notes of the devices. The focus will be given to the planner magnetic components, surface mounted semiconductors and ceramic capacitors to reduce the size and weight of the circuit. The possible opportunities for the substrate of the circuit will also be investigated. Because the power dense configuration of the circuit special focus will be given in the thermally conducting substrates. Though the review will run in parallel to the design works the decision will be made in the first week of project.

Task 3: Selection of converter topology

Based on the literature review two converter topologies will be identified for the final design based on their advantages for this specific application. Initially the paralleled IPT based interleaved bidirectional boost converter circuit of figure 8 is selected as the first choice for the project and the dual interleaved IPT based boost converter circuit of figure 7 is selected as the second choice. The reason for selection of first choice is given in the section 3. The second choice is selected as an alternative because the circuit has already been constructed and evaluated by the power conversion research group for a different voltage and power rating than the targeted one in this project. So considering the risk associated with the project described in section 5 this alternative design can be constructed and evaluated in a short period of time. However this is just an initial decision and the final decision will be made at the beginning of the project period (in the first week). In this period effort will also be given to modify the designs for better performance.

Task 4: Paper design of the converter power circuit

Based on the selected topology and the given voltage and power specification and assumed switching frequency and output voltage ripple specification the capacitance value can be found from equation 4 of the subsection 2.1. The input current ripple and the differential current ripple (flowing in the winding loop of the IPT transformer) in each of the IPT in figure 8 will also be specified. Then the average input and output current and the peak transistor current will be calculated using the basic boost converter equations as shown in subsection 2.1. The inductance values for in input inductor and the IPT will also be optimized to find a small ratio between them, so that zero voltage switching can be found for large range of duty ratio [21]. In each phase several transistors series and parallel combination have to be done to achieve the current and voltage rating. Similar arrangement will have to be done for the output capacitor as well. The mechanical and thermal optimization for the circuit will also be considered to make the converter power dense.

Task 5: Component selection

Again based on the literature review and the selected topology different components will be selected and ordered at the end of first week. The application notes and datasheets of the commercially available transistors and capacitors will be examined thoroughly. The size, weight and the thermal characteristics will be studied carefully before making any selection. High frequency and high current rated surface mounted Mosfets will be investigated primarily. Also low voltage rating ceramic capacitor will be the initial choice. Two or three different models for each component will be ordered to avoid the risk of device failure. Again because of the project time constraint only the Si based devices will be considered.

Task 6: Magnetic component design

The design of magnetic component is very crucial in increasing the power density in the converter. At first based on the chosen topology and the calculations described in the previous task 4 the inductance of the input inductor and IPT will be calculated. The effort will be given to find a suitable input inductor off the shelf to save time and reduce complexity in the project. However if a suitable inductor is not found in the market the inductor will be designed by hand. For the preliminary selection the IPT has to be designed by hand because it is not commercially available. Again because of the high flux density in the input inductors amorphous core material will be considered for them instead of conventional crystalline cores. The reason is the amorphous core material can take higher flux before becoming saturated. Again for this type of inductor design some software like Metglas's inductor design software will have to be used. As the IPT takes large AC flux, ferrite core will be used for them to reduce the core losses and cost. The design has to be tolerant for the transient overvoltage, transient over current, mismatch in current sharing etc. The calculation of inductance for the alternative circuit design will also be done. The core materials, wires, ribbon etc. will be ordered for both of the designed inductors and both of the IPT models. Two weeks are allocated for the magnetic components design and construction.

Task 7: Control circuit design

The peak current mode control described in [12]/[21] will be implemented for the designed converter. This simple open loop control strategy for the converter is selected because of the time constraint. This type of controller can be implemented using the off the shelf integrated circuit from the market. A printed circuit board will be used for this PWM controller to control the gate signals of the Mosfets of the power circuit. Current transducers will be used to sense the IPT winding currents. The control circuit will be designed in the third week of the project.

Task 8: Loss audit and heat sink design

A theoretical power loss audit will be done based on the circuit calculations and the components' specifications. The Mosfet conduction and switching loss will be calculated based on the datasheet and circuit calculations. The conduction losses in the inductors and IPTs will also be calculated based on the calculated winding resistance. The core losses will be calculated by using the catalogue specification based on the calculated flux density, assumed core temperature and switching frequency. The losses in the ceramic capacitor will be calculated based on its equivalent series resistance. However the losses in the power cables, connecting cables and joints, planar bus bar and PCB will not be considered for simplicity. The calculation will be done for different duty ratios to find out the worst case scenario. After calculation the efficiency will be checked with respect to the target efficiency and appropriate changes will be done if the calculated efficiency falls below the target. Based on the power loss calculation an appropriate heat sink or fan or specific thermally conducting substrate will be proposed for the circuit. One week is allocated for this task.

Task 9: Planar bus bar and PCB layout design

Basic familiarization with the software (Protel DXP or NI Multisim or Quartus) for the planner bus bar and PCB design will be done in parallel to the previous tasks in the 4^{th} week as shown in the table 1. Then the next week is allocated for designing the circuit layouts. The planar bus bar is selected for this project to keep the stray inductance low and to avoid large over-voltage transients across the transistors during the commutation instants [12].

Task 10: Constructing and testing of the circuit

After receiving all the components the circuit will be constructed in the power electronic laboratory. The constructed inductors and IPTs along with the Mosfets and capacitors will be assembled to the planar bus bars. Using PWM signal generator from the control circuit to produce the gate pulses for the Mosfet, the circuit will be tested to see if it is working according to the

design. If any anomaly happens then the circuit connection will be checked and the transistors or capacitors will be changed to different models or the arrangements will be changed. An important challenge will be the ensuring the proper current sharing in the parallel branches of the inductor, IPT winding and transistor switch. A detailed risk mitigation associated with the circuit evaluation is given in the section 5.

Task 11: Alternative circuit design in case of first design failure

If it becomes impossible to fix the constructed circuit, then the alternative circuit will be constructed. More Mosfets have to be paralleled in each phase, because in the alternative circuit the current become double. The control circuit will be the same. The inductors and IPTs will be paralleled and the connection in the planer bus bar will be changed. After constructing the alternative circuit it will be tested again.

Task 12: Report writing

The report writing will be done in parallel with the other tasks from the 2nd week to 6th week. After successful testing of converter circuit data will be collected for incorporation in the final report. The last two weeks will be solely allocated for finalizing, printing and binding of the report.

4.2 Time plan for the project

The following Gantt chart (table 1) lists all the major activities in the project period (3 weeks) and also gives time plan for each of the activities. Different milestones are also pointed out in this chart. Literature review on the converter topology will be done in the week 1, 4, 5, 6 and 7. Reviews on inductor design, transistor, capacitor and control circuit will be completed within the first three weeks. The design works will start in parallel to the literature review from the first week. In the first week the working topology and the alternative one will be finalized. The Mosfet, capacitor and inductor calculations will also be done in this week. The Mosfets and capacitors will be ordered at the beginning of the second week. Also in this week the paper design for inductor and IPTs will be done and at the end of the week the required components will be ordered. The control circuit will be designed in the next (3rd) week and the required components will be ordered. At the end of 3rd week the milestone 1 'converter circuit and components paper design completion' will be achieved. It is assumed that within the 5th week all the ordered circuit components will be available. So ample amount of time is allocated for the arrival of transistors & capacitors, inductor & IPT components and control circuit components. The least amount of time is allocated for control circuit components as the circuit is a very common circuit and the components (UCC28220 or UCC28221) will easily be found in the local market.

In the 4th week of the project a theoretical loss calculation and some thermal design for the circuit will be done and in parallel the planer bus bar and PCB design will also be started. At the end of this week heat sink, planar bus bar and PCB will be ordered. Again the software layout will be done within 5th week. The inductors will be constructed in the 6th week as the components will be available by this time. By this week the circuit boards (PCB and Planar bus bar), circuit protecting box and heat sink will be available. The whole circuit will be assembled in the 7th week. So after this week the second milestone 'circuit construction' will be accomplished. During the next two weeks (8th and 9th) the circuit will be tested and data will be collected. Any problems regarding the designed circuit will be solved within this period. If it becomes impossible to solve the problem an alternative design will be tried during the contingency period (10th week).

The draft report writing will be started from 2nd week in parallel to the design works and literature review. Two weeks are allocated for each of the first three sections of the draft report draft: literature review, circuit design and operation, and inductor design. The last two weeks of the project period are allocated for finalizing the report. Milestone 3 will be achieved after submitting the final report at the end of the 12th week.

Activity ID	Activity Title	Week 1	Week 2	Week 3	Week 4	Week 5	Week 6	Week 7	Week 8	Week 9	Week 10	Week 11	Week 12
1	**Literature review**												
	Review of converter topology												
	Review on inductor design												
	Review on transistor and capacitor												
	Review on control circuit												
2	**Detailed design and component selection**												
	Finalizing the topology												
	Selection of Mosfet, capacitor and inductor												
3	**Ordering and receiving of the components**												
4	**Magnetic components design and construction**												
	Design of the inductors and IPTs												
	Construction of Magnetic Components												
5	**Control circuit design**												
	Milestone 1: Converter Circuit and components paper design completion												
6	**Circuit construction and connection**												
	Loss calculation and heat sink design												
	Learning the tutorials for Planar bus bar and PCB design												
	Design of the circuit layouts in the software												
	Ordering and receiving the designed heat sink, circuit boards and protection box from the workshop												
7	**Assembly of the circuit**												
	Milestone 2: Circuit construction completion												
8	**Testing of the constructed circuit**												
9	**Contingency for alternative design**												
10	**Generating dissertation**												
	Draft report on literature review												
	Draft report on the circuit design and operation												
	Draft report on the inductor design												
	Finalizing the draft report												
	Printing and binding												
	Milestone 3: Dissertation submission												

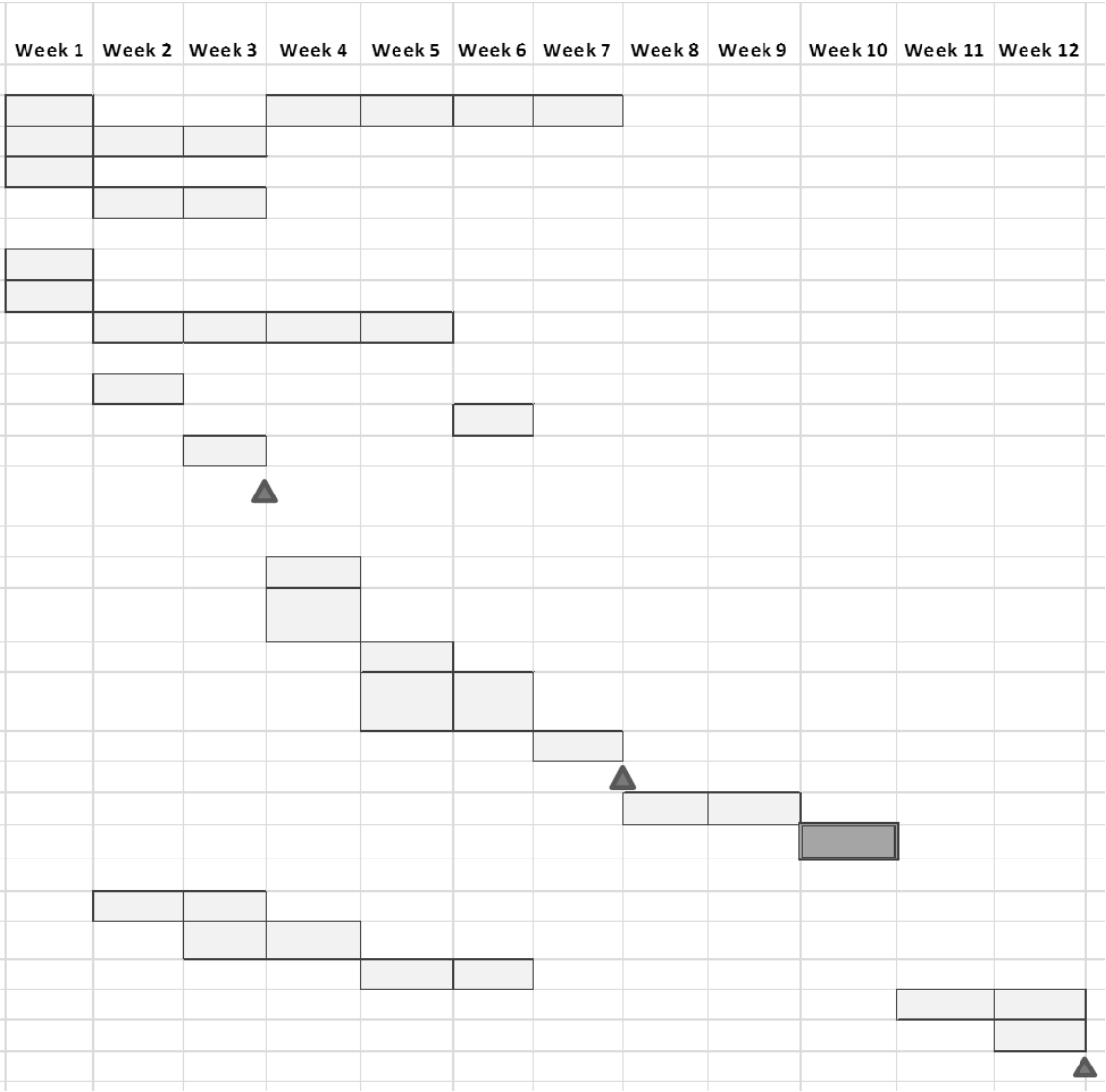


Table 1: Project plan chart/ Gantt chart

Section 5: Project Risk Analysis and Mitigation

This section gives an overview of the possible risks and their mitigation strategies in this project. From the project plan in the previous section, it is clear that almost half of the project period is allocated for the practical construction and evaluation of the circuit. So several risks associated with the converter will have to be mitigated to complete the project within this specified period. The major risks and their mitigations are given below:

Risk 1: Component availability

Getting the different components for the converter circuit in time is a challenge. Because of power dense design specific inductor/ transformer cores, Mosfets, capacitors and ICs will be required in this project. If any of the items come late then the construction of the converter may be delayed.

Risk 1 mitigation strategy

As the complicated converter circuits will not be considered, so the possibility for unconventional circuit components like custom made inductor cores will be low. The Mosfets, capacitors and ICs will be selected based on the up to date commercial materials like recent application notes, datasheets etc. There availability will be checked over the internet and also discussion will be made with the experienced members of the research group in this field. Finally the components will be ordered at the beginning weeks of the project and a reasonable amount of lead time is allocated in the project plan between the ordering and receiving of the components to fulfil the mitigation strategy for this plan.

Risk 2: Equipment availability for construction and testing of the converter

During the circuit construction and testing period all the necessary equipment like soldering machine, soldering stand, Regin, measurement equipment and a proper workstation in the laboratory should be available. If not the circuit construction will be delayed and the project will be at risk. There is risk of getting the heat sink, safety cover box and circuit boards in time from the workshop. Also during the circuit construction and testing week the availability of laboratory will be ensured.

Risk 2 mitigation strategy

At the beginning of the project probably in the second week the laboratory will be inspected to see if all the necessary equipment for construction and testing of the circuit are available in the laboratory. If not necessary arrangement will be done after discussing the issue with the project manager. Two weeks are allocated in the project plan for the equipment coming from the workshop. A simple heat sink/ thermal management solution and a simple open lid safety box for the circuit will be ordered in the workshop for the tight time constraint of this project.

Risk 3: Methodology/ design failure

As there will be no simulation for the designed converter circuit there is a risk of methodology failure. Also there is a possibility that the constructed circuit will not work properly and also will give poor efficiency and power density.

Risk 3 mitigation strategy

A careful analysis of the selected topology for the project will be done in the first week of the project. As the draft report on the circuit operation will also be done in the initial weeks so any mistakes in the design can be found at an initial stage of the project. The target efficiency and power density is selected based on the previous published works related to this project. Still the circuit may not work properly because of the overheating of the Mosfets, in that case more Mosfets will be paralleled to reduce the conduction loss in them. Also additional forced air cooling arrangement for the circuit will be done. Alternative models of Mosfets and capacitors will be

used as well to see if the performance enhancement can be done. To mitigate the risk of accidental damage, circuit connection will be checked thoroughly before powering up the circuit. Also the circuit will be tested initially for the below rated condition, so the worst operating condition (duty ratio corresponding to high power loss) will be checked at last. The unbalanced current sharing in the parallel components can be a reason for the design failure, which will be solved by using matched components and careful construction. Again a reasonable amount of time (2 weeks) is allocated for testing the circuit in the project plan. In case of total failure after a week of testing, the alternative circuit will be tried to complete the project.

Risk 4: Time slippage

Risk 4 mitigation strategy

One week contingency period is included in the project plan so that if there is a time slippage in any activity there will be a chance to cover it up. Different milestones are fixed in the project lifetime so that work can be assessed time to time and any time slippage can be pointed very easily.

Conclusion

DC-DC boost converter has a great importance in the future more electric vehicle system. Continuous research and development is going on in this field both in the industry and academia. Power density of the converter is being considered as the most important criterion in designing these converters; as power dense equipment will ensure more efficient and cost effective vehicle for the current highly competitive automotive market. The 12V to 48V DC-DC boost converter has several applications like interfacing the 12V bus and 48V bus in the EV or connecting 48V auxiliary loads like air conditioning, entertainment equipment, power steering etc. to the 12V bus or 12V auxiliary battery. So a power dense 12V to 48V DC-DC converter is highly needed in the industry at this moment.

A bidirectional interphase transformer based interleaved boost converter is initially selected for this project after doing the initial review on the power dense boost converters. This design has a proved good power density and high efficiency. Reduced ripple with higher frequency in the input and output currents and compact magnetic circuit design are the main reasons for the vast popularity of this topology. Some improvements to the previous design of dual interleaved IPT based converter is being considered for further miniaturization of the circuit. The detailed analysis of the circuit will be done during the initial weeks of the project. Some research papers are also reviews for the compact magnetic component design and it is found that interphase transformer and the input inductor design will be the most crucial step to make the converter power dense. At present the planar magnetic design for the IPT is being considered. As the input inductor core material will have to carry a large amount of flux amorphous core is being considered for it. However, these cores are only available in ‘C’ shapes in the market; so making a planar design with that core is considered to be a challenge.

The methodology and the project plan for the 12 weeks project period are clearly defined to achieve the objectives of the project. The major tasks are pointed out and presented in a sequential manner for the successfully completion of the project. Two review points are included in the project plan to identify the advancement of the project. This will help to neutralize any mishaps in the different tasks of the project. Also a contingency period is allocated in the plan for mitigating various risks associated with the plan. A detailed risk analysis is done and corresponding mitigation strategies are provided. The methodology is developed in such a way that any risk cannot hinder the aim of this project. A design plan with which the Power Conversion group is familiar is considered as an alternative to the primarily selected topology. The literature review and report writing are distributed in several numbers of weeks so that lead time for getting the components can be effectively utilized. A detailed initial health and safety risk assessment is also done, which is attached as the Appendix 1 of this feasibility report. To ensure

the safety of the experimenter and the associated people several strategies are provided and relevant measures are included in the methodology and plan of the project.

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