A low power linear phase programmable long delay circuit

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Abstract—A novel linear phase programmable delay is being proposed and implemented in a 0.35 μm CMOS process. The delay line consists of N cascaded cells, each of which delays the input signal by T_d/N, where T_d is the total line delay. The delay generated by each cell is programmable by changing a clock frequency and is also fully independent of the frequency of the input signal. The total delay hence depends only on the chosen clock frequency and the total number of cascaded cells. The minimum clock frequency is limited by the maximum time a voltage signal can effectively be held by an individual cell. The maximum number of cascaded cells will be limited by the effects of accumulated offset due to transistor mismatch, which eventually will affect the operating mode of the individual transistors in a cell. This latter limitation has however been dealt with in the topology by having an offset compensation mechanism that makes possible having a large number of cascaded cells and hence a long resulting delay. The delay line has been designed for scalp-based neural activity analysis that is predominantly in the sub-100 Hz frequency range. For these signals, the delay generated by a 31-cell cascade has been demonstrated to be programmable from 30 ms to 3 s. The measured power consumption from a 1.1 V supply was 270 nW for a 0.3 s delay.

Index Terms—Delay lines, switched capacitor circuits, FG-MOS, offset compensation, weak inversion

I. INTRODUCTION

RECENTLY there has been significant interest in sensor-based real-time signal processing within low-power miniaturized medical devices [1]–[6]. Such devices sense biological signals (such as heart beat or electrical activity of the brain) and analyse the signal in real-time on the sensor itself in order to provide a measurement or pertinent diagnosis. In those devices, parallelized signal processing is crucial in reducing processing time. In parallel processing algorithms, the intrinsic delay of each circuit block could lead to information becoming unsynchronized across parallel processing chains. The duration of such delays can sometimes range from a few milliseconds to a few seconds. For example, low frequency Continuous Wavelet Transform (CWT) filters could introduce over 100 ms delay [1]. Thus delay cells that match the intrinsic delay of these circuits are necessary to synchronize parallel processing chains in these low power applications.

One such application is electroencephalography (EEG) systems [2] where real-time algorithms have been proposed [1], [6], [7] to analyse the sensed neural activity in the interest of aiding clinical diagnosis. An example of a parallelized EEG signal processing algorithm employing CWT filters is shown in Fig. 1 [1]. This algorithm utilizes two CWT filters that extract frequencies up to 10 Hz and introduce delays of up to 300 ms [1]. These delays have to be introduced in order to compensate for the low power analog approximation of the wavelet transform [3], [8]. The approximation is necessary because physically stable implementations are not possible otherwise due to the mother wavelet function being non-causal [3], [8]. Wavelet transforms are becoming very popular for online signal processing of physiological signals that are non-stationary since the wavelet transform provides uneven sampling of the time-frequency domain with higher time resolution at high frequencies and higher frequency resolution at low frequencies [3], [4], [9], [10]. It is expected that power optimized hardware implementations of algorithms based on them will have to use similar kinds of delay based strategies to deal with causality problems.

This paper presents a novel circuit designed to compensate for this 0.3 s delay consuming under 300 nW of power [11]. Note that very low power is desirable due to the fact that in physiological systems that are processing signals simultaneously from more than one channel, the power available for each channel proportionally decreases with the number. In scalp EEG systems for long term monitoring the power per channel can be very limited [12], and will mostly be needed by the instrumentation amplifier, A/D converter (prior to transmitter/recorder) and the transmitter/recording circuit blocks. Hence the power remaining for processing will be almost negligible in comparison [12]. Consequently, when split into the different blocks in the processing chain this will result in nanoWatts power budgets for each one of them.

Several delay circuits have been reported in the literature for delaying digital inputs or clock signals using digital shift registers/timers and inverters, but these cannot be used to delay analog input signals. Mixed signal implementations that that use an analog input and give a digital output have also been considered. For example, [13] presents a low power programmable analog-in–digital-out FIR filter that consumes approximately 226 nW (when clocked at 100 Hz and using 31 taps to be comparable to our delay line). However, without an additional D/A converter such circuits would not be suitable for use in analog information processing systems, such as ours presenting in Fig. 1 or others from the literature such
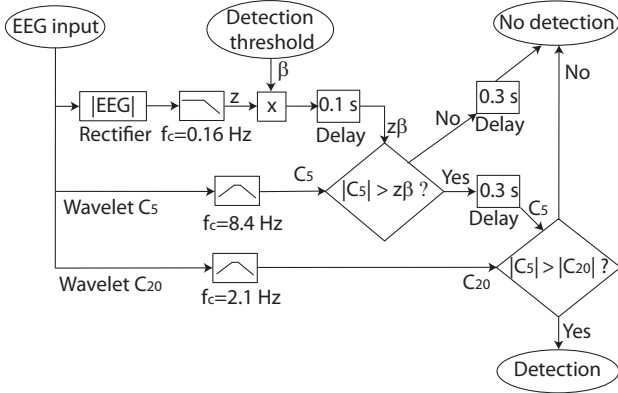
Fig. 1. An example of parallelized signal processing requiring long analog delays. Reported in [1].

(a)

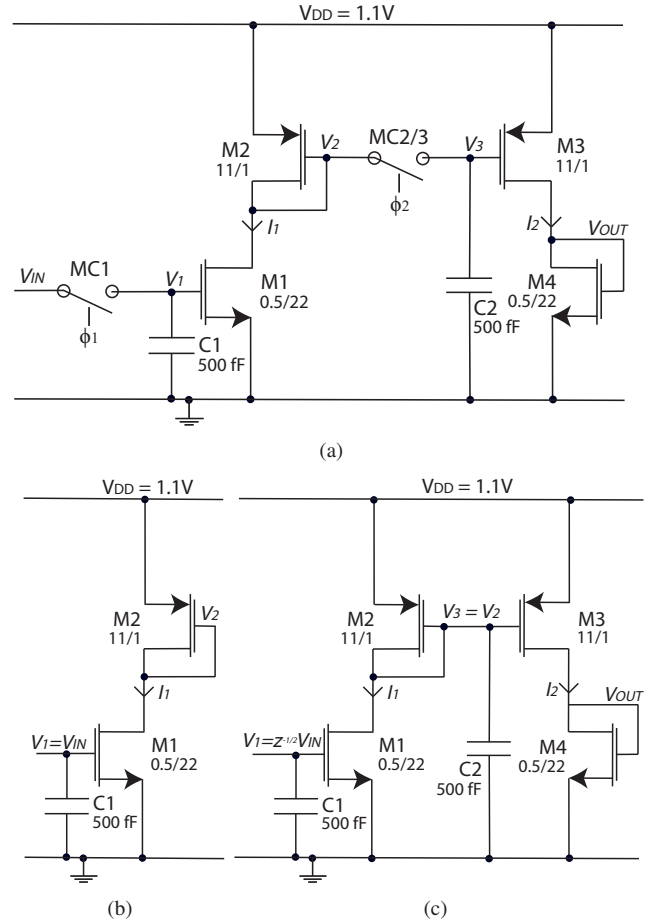(b)   (c)

Fig. 2. Complete delay cell and the two phases of the circuit in operation. (a) Complete delay cell. (b) Phase one of delay cell. (c) Phase two of delay cell.

as [14], [15].

An alternative for analog systems is to use an analog filter, such as a Bessel low pass filter or linear-phase all pass filter. Pseudo-resistor elements can be used to create very large on-chip time constants in filters and there has been much recent work on improving programmability [16], [17], current mode operation [18] and distortion reduction [13]. However for an analogue filter to provide 300 ms group delay at 10 Hz, the filter must delay the input signal by three full periods. Hence the filter must have $-1080°$ phase shift at 10 Hz which corresponds to a minimum of 12 poles within the 10 Hz bandwidth, each generating a $-90°$ phase shift. This requires a minimum of a 12th order low pass or all-pass filter with a maximally flat group delay. Lower order filters generating shorter delays have been previously reported, such as a 0.75 μs group delay for frequencies up to 500 kHz from 4th order Bessel low pass filter consuming 13.3 mW [19], and 587 μs group delay for frequencies up to 5.4 kHz from a 9th order all pass filter consuming 360 nW [14]. A maximally flat group delay of 300 ms may be achieved by increasing the filter order but this would significantly increase the power consumption of the circuit.

The new programmable delay circuit presented in this paper is able to achieve very long delay values independent of the frequency of the input signal, with a very small area. This paper is structured as follows: Section II describes the single delay cell and the delay line, together with an offset compensation strategy that is necessary to prevent the accumulative effects of mismatch when cascading a number of cells. Section III presents the simulated and measured results of the fabricated delay line. The performance of the delay line is then compared to previous delay circuits in Section IV.

II. STRUCTURE OF THE DELAY LINE

A. Delay cell

The delay cell has been designed in a 0.35 μm CMOS process and is shown in Fig. 2. Multiple delay cells are cascaded to achieve the required delay duration. The single delay cell is based on two switched capacitors (MC1–C1

and MC2/3–C2) to introduce the necessary delay. Switched capacitors were chosen as they have negligible static power consumption and are thus suitable for low power applications. However it is also well-known that switched capacitors cannot be intrinsically cascaded to form a long delay line as charge injection/redistribution errors and clock feed through errors cause significant signal distortion. The simple circuit based on switched capacitors is designed to mitigate these issues.

The delay cell is designed for low-power miniaturized portable devices and thus the supply voltage and current drawn must be kept to a minimum. Assuming a single button cell or coin cell battery is used in this device, the nominal supply voltage will be about 1.4 V [2], [20] and the supply voltage will reduce over the lifetime of the battery. Considering this, in Fig. 2, the supply voltage V_{DD} is selected to be 1.1 V, V_{SS} is 0 V and all transistors are biased in weak inversion saturation with $V_{GS} < V_{TO}$ and $V_{DS} > 4U_T$ (where V_{TO} is the threshold voltage and U_T is the thermal voltage). In Fig. 2 the bulk-source voltage of all transistors except the switches is zero. For NMOS switches, the bulk is connected to 0 V while the bulk of PMOS switches is connected to V_{DD}.

The switched capacitors (MC1–C1 and MC2/3–C2) in Fig. 2 are controlled by two complementary clocks ϕ_1 and ϕ_2 that switch between 0 V and V_{DD}. The time delay d introduced

by each switched capacitor is calculated as

$$d = (1 - D)T \qquad (1)$$

where T is the period of the clock and D is the duty cycle of the same clock.

The clock frequency has been selected to ensure that the input signal is sampled at ten times the maximum frequency of the signal to reduce the mean squared error introduced by sampling the continuous-time signal. Thus the clocks ϕ_1 and ϕ_2 operate at 100 Hz with 50% duty cycle. The corresponding delay of a single switched capacitor, from (1), is 5 ms and the cell in Fig. 2 has a total delay of 10 ms.

In Fig. 2 the widths and lengths of the switches have been kept to a minimum to reduce charge injection errors due to redistribution of the charge stored in the channel. Distortion due to charge redistribution has been minimised by ensuring that transistors connected to the drain and source of these switches have identical aspect ratios. In contrast, the size of the capacitor should be maximised to reduce signal distortion through charge injection but this comes at the cost of larger die area. As a trade-off, capacitors C1 and C2 are selected to be 500 fF.

In Fig. 2 the switch MC2/3 is a transmission gate to ensure that an increase or decrease in V_2/V_3 will not affect the ON-OFF functionality of the switches. This is not a problem for MC1 as V_{IN} will be approximately constant as opposed to the voltages V_2/V_3 at the drain and source of the transistors in MC2/3. As such MC1 is a single 2 μm / 0.5 μm NMOS transistor. In MC2/3, transistor MC2 is a 2 μm / 0.5 μm NMOS device and MC3 a 2 μm / 0.35 μm PMOS device. To control the transistor MC3, clock ϕ_2 is fed into an on-chip inverter (simple PMOS–NMOS configuration) and the inverted clock is fed to the gate of MC3. This ensures that the NMOS switch (MC2) and the PMOS switch (MC3) will turn ON and OFF at the same time.

The delay cell in Fig. 2 is symmetric since transistors M1 and M4 are matched and the current mirror transistors M2 and M3 are matched. The aspect ratios of the transistors have been selected to limit the power consumption of the entire 300 ms delay line to 200 nW. As a single delay cell achieves 10 ms delay, 30 cells should be cascaded to achieve the required 300 ms delay. Hence the power budget of a single cell is less than 6.7 nW and the current drawn by each branch (I_1 and I_2) should be less than 3 nA from a 1.1 V supply. For an input signal with a d.c. bias of 500 mV (selected to minimize power whilst maximizing signal swing, not just of this block but of the previous one at the system level), the aspect ratio of M1 and M4 has been selected to be 0.5 μm / 22 μm. The drain current of M1 and the aspect ratios of the transistors M2 and M3 set their gate voltage (assuming the switches are ideal). Hence the transistors M2/M3 have an aspect ratio of 11 μm / 1 μm to ensure that the current mirror transistors are also biased in weak inversion saturation.

The circuit operates in two phases as shown in Fig. 2: in phase one clock ϕ_1 will be high while clock ϕ_2 will be low; in phase two clock ϕ_2 will be high while ϕ_1 will be low. At the start of phase one (time t = 0 s), clock ϕ_1 will rise from 0 to 1.1 V. MC1 turns ON when ($\phi_1 - V_{IN}$) exceeds V_{TO} and

C1 starts charging until it reaches V_{IN}. Thus the gate voltage of transistor M1 will be equal to V_{IN} and this will generate a drain current given to the first approximation as:

$$I_1 = I_{S1}e^{V_1/nU_T} \qquad (2)$$

where n is the slope factor, V_1 is the gate voltage of transistor M1 and I_{S1} is the specific current of transistor M1.

The drain current sets the voltage (V_2) at the gate of transistor M2:

$$V_2 = V_{DD} - V_1 - nU_T \ln\left(\frac{I_{S1}}{I_{S2}}\right). \qquad (3)$$

Meanwhile ϕ_2 is low and thus MC2/3 forms an open circuit cutting off the remainder of the circuit as shown in Fig. 2(b).

In phase two, ϕ_2 rises from 0 V to 1.1 V while ϕ_1 falls to 0 V. Capacitor C1 holds the voltage V_{IN} (t = 0 s) from phase one as shown in Fig. 2(c). When ($\phi_2 - V_2$) exceeds V_{TO}, the transmission gate turns ON and the capacitor C2 is charged until V_3 reaches $z^{-1/2}V_2$, where $z^{-1/2}$ denotes half a unit delay and a unit delay is equal to the period of the clock. This sets the drain current of transistor M3. As the aspect ratios of the current mirror transistors are identical the drain currents I_1 and I_2 will be identical to a first approximation. Furthermore the aspect ratios of M1 and M4 are also matched and hence the output voltage V_{OUT} will be the delayed voltage V_1.

When multiple cells are cascaded there will be an additional delay at the input switched capacitor of $z^{-1/2}$ (in other words $V_1 = z^{-1/2}V_{IN}$) as ϕ_1 of the subsequent delay element will be complementary to ϕ_2 of the preceding delay cell. Hence the overall transfer function of a single delay cell is given as

$$\frac{V_{OUT}}{V_{IN}} = z^{-1}. \qquad (4)$$

It should be noted here that the first delay cell in the cascaded delay line will only sample the input signal and will not introduce a delay. Hence 30 delay cells will introduce $29.5T$ delay where T is equal to 10 ms. An additional cell with a single switch will be introduced at the start of the delay line to generate the complete $30T$ delay.

B. Problems caused by mismatch

So far the mismatch between transistors (M1–M4 and M2–M3) has not been considered in the circuit model. If there is mismatch in either the threshold voltage or mobility of carriers between the otherwise identical transistors M1 and M4, or M2 and M3, the specific current $I_{S1} \neq I_{S4}$ and $I_{S2} \neq I_{S3}$. Thus the current gain of the current mirror would be:

$$\frac{I_2}{I_1} = z^{-1/2}\left(\frac{I_{S3}}{I_{S2}}\right). \qquad (5)$$

Incorporating this, in addition to non-identical specific currents of transistors M1 and M4, the output voltage in (4) is modified to be:

$$V_{OUT} = z^{-1}V_{IN} + nU_T \ln\left(\frac{I_{S1}}{I_{S4}}\frac{I_{S3}}{I_{S2}}\right). \qquad (6)$$

From (6) it can be seen that mismatch between transistors M1–M4 and M2–M3 would introduce an offset at the output,
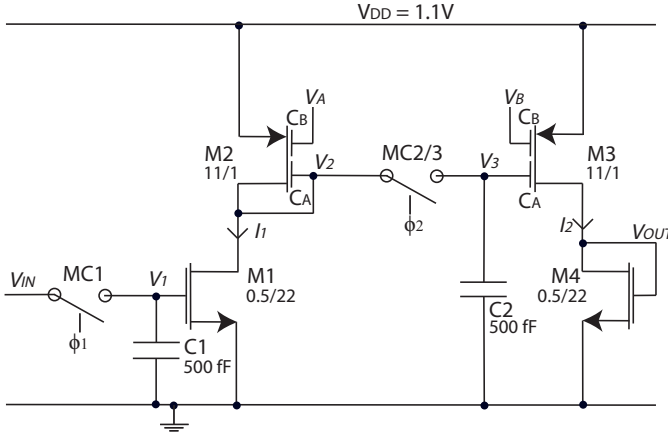
Fig. 3. Floating gate PMOS transistors used to correct for offset variation in the delay line.

where the latter is a function the specific currents of these transistors. This poses a significant problem in cascaded delay lines as any offset in the output voltage of a delay cell could potentially increase linearly with the number of cascaded cells. In this case, the input signal to one of the latter delay cells within the delay line could eventually be outside the input signal range of the circuit in Fig. 2.

A potential solution is to correct for any systematic offset at strategic positions within the delay line itself. To this end, the delay circuit in Fig. 2 will be next modified to incorporate offset programmability (or correction).

C. Offset correction cell

The proposed offset correction cell is shown in Fig. 3. In this circuit offset correction is achieved by introducing floating gate PMOS transistors M2 and M3 to replace the simple current mirror in Fig. 2. The gate of each floating gate transistor (FGMOS) is connected to the bottom plate of two capacitors C_A (50 fF) and C_B (57.4 fF). The top plate of capacitor C_A is connected to V_2 or V_3 for transistor M2 and M3 respectively, while the top plate of capacitors C_B are connected to bias voltages V_A or V_B for M2 and M3 respectively. The voltage at the gate of these transistors, ignoring parasitic capacitances, is now given by [21],

$$V_{FG2} = \frac{C_A}{C_T} V_2 + \frac{C_B}{C_T} V_A \qquad (7)$$

$$V_{FG3} = \frac{C_A}{C_T} V_3 + \frac{C_B}{C_T} V_B \qquad (8)$$

where $C_T = C_A + C_B$.

The current gain of the floating gate current mirror is hence modified from (5) to:

$$\frac{I_2}{I_1} = z^{-1/2} \left(\frac{I_{S3}}{I_{S2}} \right) e^{\frac{C_B}{C_T} \frac{(V_A - V_B)}{n U_T}}. \qquad (9)$$

Using this, it is possible to derive the new output voltage,

(without parasitic capacitances) as:

$$V_{OUT} = z^{-1} V_{IN} + \frac{C_B}{C_T} (V_A - V_B)$$
$$+ n U_T \ln \left(\frac{I_{S1}}{I_{S4}} \frac{I_{S3}}{I_{S2}} \right). \qquad (10)$$

Thus the systematic offset at the output of this cell can be corrected for by adjusting the bias voltages, V_A and V_B, this is:

$$\frac{C_B}{C_T} (V_B - V_A) = n U_T \ln \left(\frac{I_{S1}}{I_{S4}} \frac{I_{S3}}{I_{S2}} \right). \qquad (11)$$

Note that this correction is a one-off process, which only tackles systematic offset. The offset can also dynamically change due to changes in temperature. However, unlike systematic offset caused by mismatch, this does not pose a problem because changes in the output signal due to temperature variations are considerably smaller than those caused by mismatch (6 mV in a 70°C temperature range, 3.2 mV in a a 0–40°C range), falling into the input ranges of subsequent stages and consequently not affecting the delay functionality. Hence dynamic offset compensation is not required.

The offset also has a weak dependency with supply voltage variations, since the output resistance of the cell will change and this will have a small second order effect not modelled by the previous equations. This was confirmed by simulation. Assuming ±10% variation in the power supply the variation in offset was less than ±0.5 mV. Again, this falls into the input ranges of subsequent stages and hence does not affect the functionality.

D. Overall delay line

The offset correction cell in Fig. 3 must be strategically placed within the delay line to systematically correct for any offset generated by mismatch or process variations in the normal delay cells.

A histogram of the offset variation in the output voltage of a single delay cell, generated through Monte Carlo simulations, is shown in Fig. 4. The maximum–minimum bounds of the output offset voltage are of specific interest as the maximum and minimum offset should not be outside the input signal range of the subsequent delay cell.

Based on Fig. 4, the range of possible offset voltages is within [-20 mV, +20 mV] for a single cell. Since the normal delay cell has an input signal range of 400 mV to 600 mV, a maximum of 5 delay cells can be cascaded before the output of the delay cell risks exceeding the input range of the subsequent cell. In the interest of reducing the offset to be corrected at any single point within the delay line, the offset correction cell is interleaved with 3 normal cells to form a 4-cell repeating block that is then cascaded to form the delay line, as shown in Fig. 5.

The overall delay line contains 8 repeating blocks. The reference voltage V_A or V_B from all offset correction cells have been connected together in order to reduce the number of external bias voltages to be adjusted. In the present configuration, if there is an offset of +80 mV at the output of the delay line, it would require a change of -10 mV at the
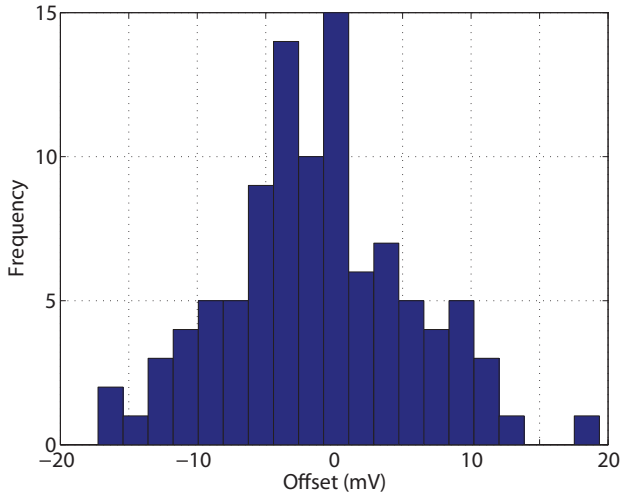
Fig. 4. Histogram of offset variation at the output of a single delay cell under mismatch and process variations.
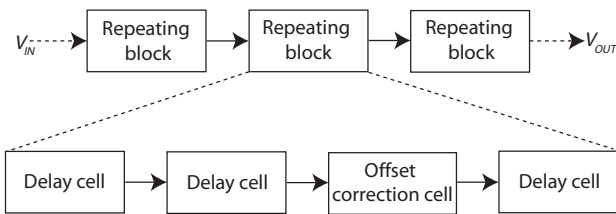

Fig. 5. The order of the delay and offset correction cells in the cascaded delay line.

Fig. 6. Microphotograph of the delay line.

TABLE I
EXTRACTED AND MEASURED RESULTS OF THE DELAY LINE.

Parameters	Simulation	Measured
Power supply	1.1 V	
CMOS process technology	0.35 μm	
Area	0.264 mm^2 (612×432 μm)	
Current	175 nA	245 nA
Delay	302.2 ms $\pm$1%	302.2 ms $\pm$1%
Bandwidth (sampling frequency $f_s/2$)	50 Hz (f_s = 100 Hz)	50 Hz (f_s = 100 Hz)
Gain	-7.8 dB	-10.33 dB
Offset	-16 mV	-76 mV
Input referred noise	-88 dB (0.04 mVrms)	<-74 dB (0.21 mVrms)
Input range	40 mVpp	40 mVpp
Dynamic range	70 dB	> 46 dB
THD (2 Hz)	0.46%	0.84%
IMD3 (6 Hz and 7 Hz)	-32 dBc	-37 dBc

output of each of the 8 offset correction cells within the delay line. Hence $(V_A - V_B)$ should be adjusted to -18.7 mV by either increasing V_B or reducing V_A. Any further increase or decrease in the reference voltages will lead to a further proportional change in the output offset voltage as demonstrated in Section III-B.

Finally, inside our algorithm (Fig. 1) the delay is always preceded by a low pass filtering stage: either a 0.16 Hz filter as part of the envelope detector, or the wavelet bandpass filter high frequency roll-off beginning at 8.4 Hz. As a result an anti-aliasing filter is not necessary, and is not present, as a built-in part of the current delay. However an explicit filter may be added in other applications where this intrinsic band-limiting is not present.

III. EXPERIMENTAL RESULTS

The cascaded delay line was fabricated in a 0.35 μm, double well, 2 poly, 4 metal CMOS process. A microphotograph of the fabricated delay line is shown in Fig. 6. Each repeating block in Fig. 6 has been laid out as a 2×2 cell structure to reduce mismatch between the transistors. The delay line is then connected as a folded structure to further reduce mismatch, with the input at the bottom left and the output at the top left.

The performance of the delay line has been characterized in Table I through simulation and PCB-based measurements of the fabricated delay line. The measurements were taken on a single chip and the output of the delay line was buffered.
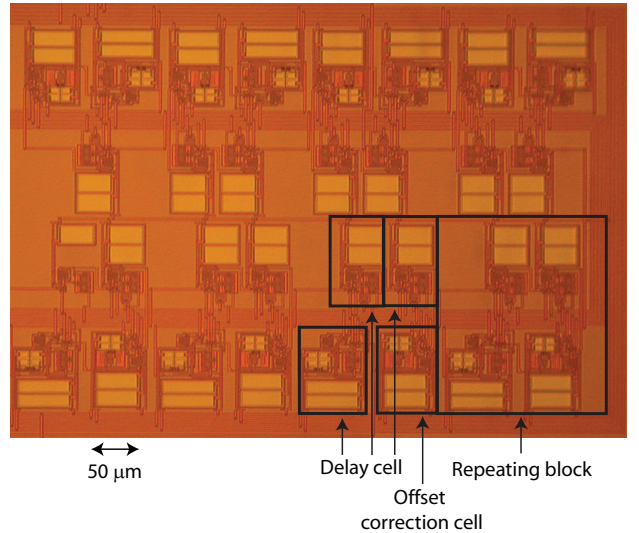
A. Cascaded delay line

The measured output of the fabricated delay line for an input EEG signal with a d.c. bias of 500 mV is shown in Fig. 7. The signal was the replica of a real EEG signal. It was generated with an external signal generator which additionally amplified it by a factor of the order of magnitude that would be expected from the front end instrumentation amplifier, present in any EEG system, and added the same d.c. bias that would be expected from it. The reference voltages V_A and V_B are set to 500 mV. The clocks ϕ_1 and ϕ_2 are set to 100 Hz with a duty cycle of 50%. Fig. 7 shows the measured delay of 298 ms at the output of the cascaded delay line. As the clock is ten times the maximum frequency of the input signal its impact can easily be removed by low pass filtering and this has been done in Fig. 7.

The delay duration can be programmed by changing the clock frequency as shown in Fig. 8 which for demonstration includes the raw interference from the clock signal. Using the same input voltage, the delayed output for three different
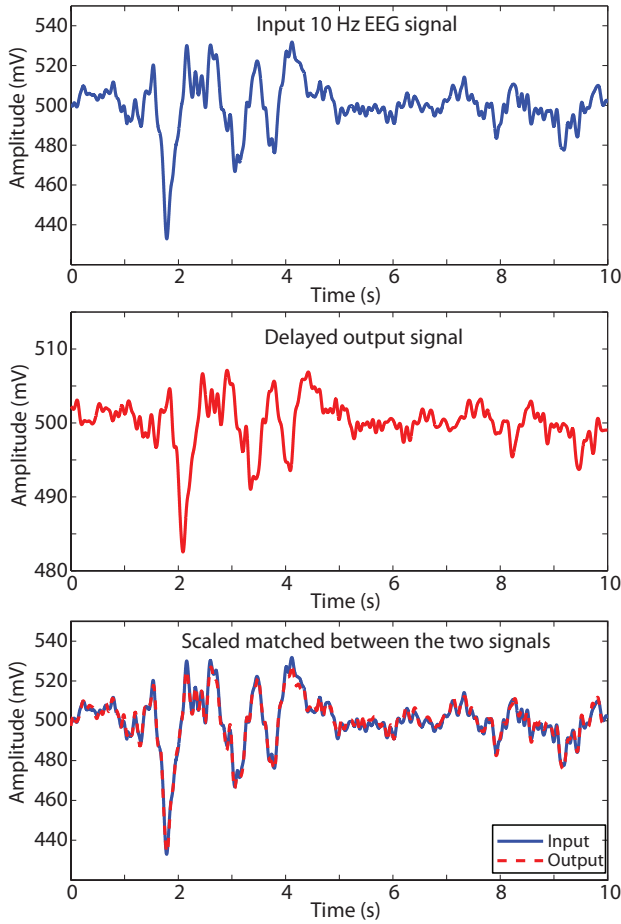
Fig. 7. The measured 298 ms delayed output of the cascaded delay line for an input EEG signal with a maximum frequency of 10 Hz.
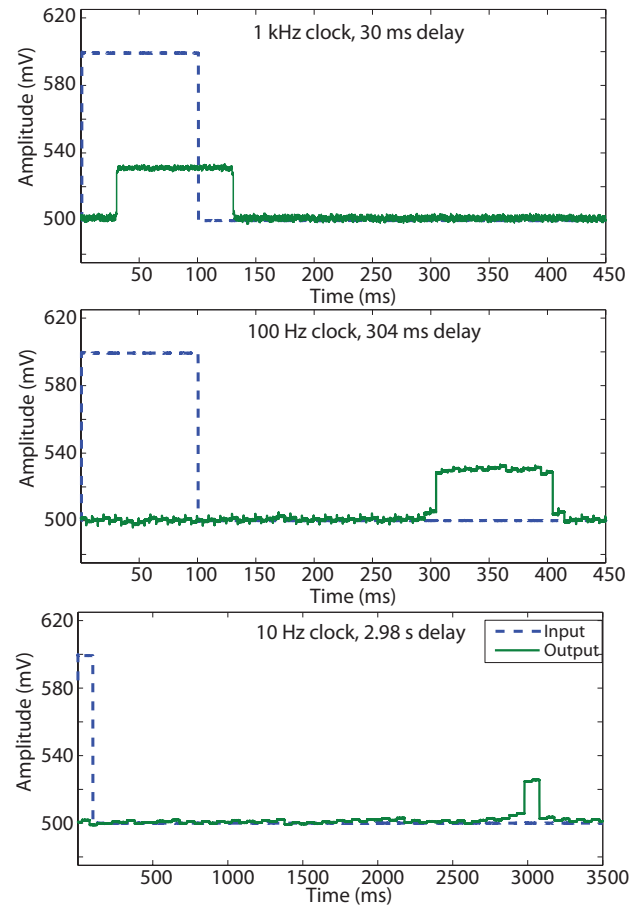

Fig. 8. Programmability of the delay line through change in clock frequency: 1 kHz clock gives 30 ms delay; 100 Hz clock gives 304 ms delay; and 10 Hz clock gives 2.98 s delay.

clock frequencies—1 kHz, 100 Hz and 10 Hz—is shown in Fig. 8. The corresponding delay durations shown in Fig. 8 are 30 ms $\pm 4.3\%$, 304 ms $\pm 1\%$ and 2.98 s $\pm 1.6\%$ respectively. The offset present in the measured output has been removed here. It should be noted that the clock frequency should be selected to be significantly higher than the maximum frequency of the input signal. Thus a clock frequency of 1 kHz could be used to generate 30 ms delay from input signals up to 100 Hz, assuming the input continuous-time signal is sampled at ten times the maximum frequency of the input signal. If the same over-sampling ratio was maintained, then the 10 Hz clock can be used for input signals up to 1 Hz. Although for the sake of clarity an input pulse is used in Fig. 8 to demonstrate the delay programmability over a 30 to 3 s range, this programmable range has also been tested with input EEG signals.

The time delay over a range of frequencies can be evaluated through the circuit phase response as shown in Fig. 9. The linear phase characteristic expected for a constant 300 ms delay has also been plotted in Fig. 9 together with the measured phase response of the fabricated delay line. The measurements closely match the theoretical perfectly linear phase response over the 10 Hz bandwidth denoting that all frequency components will be delayed by a constant 300 ms.
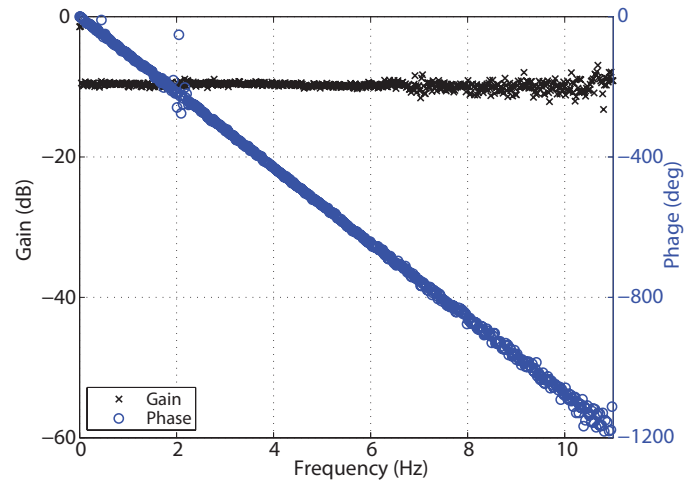

Fig. 9. Gain and phase response of the fabricated delay line showing the linear phase and constant gain characteristics.

The cascaded delay line was simulated under the worst corner (fast NMOS/PMOS at 70°C) and the resulting delay duration was 301.1 ms which is well within 1% accuracy.

In Fig. 7 and Fig. 8, a significant loss in gain is visible in the output voltage. This is due to the floating gate transistors M2 and M3 in the offset correction cell. As the voltage at the

floating gate node is determined by all capacitances associated with that node, the associated gate-drain parasitic capacitance C_{GD} leads to the gain loss seen at the output. Table I shows the measured and simulated loss in gain for the cascaded delay line. The measured result is higher than that seen in simulation; however the measured gain is within the range of the Monte Carlo simulations shown in Fig. 10, hence it can be explained by mismatch and process variations. The gain loss can be compensated either at the output or within the delay line itself using a simple amplifier.

The measured output voltage has a substantial offset of -76 mV in comparison to -16 mV seen in simulation. However the measured offset is well within the Monte Carlo variation expected for the cascaded delay line and hence it can be explained by mismatch and process variations. The maximum–minimum bounds of the offset in Fig. 11 are [-83 mV, +80 mV] and can be easily corrected as shown in (11) and demonstrated in Section III-B.

The measured dynamic range was 46 dB which is higher than the required dynamic range for the system in Fig. 1 (40 dB [22]) and more than that of traditional pen-writer based EEG systems (42 dB) [23]. This value is lower than the simulated one, although this was very likely to be caused by the existing distortion of the input signal which imposed a limitation on what we could measure. The Total Harmonic Distortion (THD) of the circuit listed in Table I was measured using a 40 mVpp 2 Hz sinusoidal input signal with a d.c. bias of 500 mV. The measured THD was 0.84%, slightly higher than the simulated THD of 0.46%. In contrast, the IMD3 was smaller, although within the range predicted by Monte Carlo simulations, so it can again be explained by process and mismatch variations. Due to the fact that the principle of operation of this circuit is based on switching, noise can potentially become more of an issue than it would be in a continuous time delay implementation. However, the noise floor of the proposed topology was always low enough as to not affect the 40 dB SNR typically required by this kind of application. As illustrative figures though, noise in the 0.1 Hz to 1 Hz frequency range for the circuit sampled at 10 Hz was 31 μVrms. Similarly, the equivalent noise integrated over 0.1 Hz to 10 Hz, for the circuit with a 100 Hz clock was 44 μVrms, and with 1 kHz clock the noise integrated from 0.1 Hz to 100 Hz was 55 μVrms. The noise of the circuit without sampling would have been 15 μVrms, 23 μVrms and 42 μVrms respectively.

The experimental input referred noise shown in Table I appears as an overestimation of the circuit actual noise. The reason for this is that in the used testing set up the noise of the input d.c. biasing signal dominated at the output, so we could not precisely measure the circuit noise. However since even with this input noise the circuit would meet the typical SNR target for this kind of specification we did not put extra effort on trying to measure a more exact value.

The simulated PSRR of the delay cell was 47 dB. It is however expected that when the circuit is to be used as part of a whole system, a low power voltage regulator together with a battery will be used for all analog blocks. The experimental characterization was carried out this way. The PSRR measured
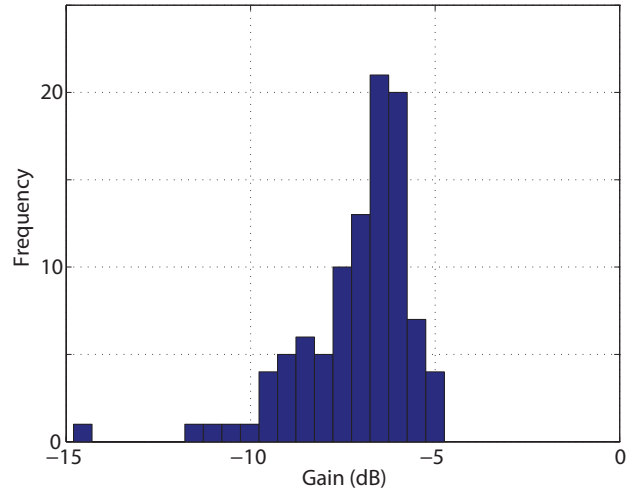

Fig. 10. Histogram showing the expected gain loss at the output of the delay line under mismatch and process variations.

was >74 dB, hence not affecting the dynamic range of the circuit. The sensitivity of the delay duration to supply voltage variation, evaluated for a range of 1.0 V to 1.2 V, was 0.21% which is well within the accuracy of the delay duration (1%) as specified on Table I. The gain variation as the voltage supply varied from 1.0 V to 1.2 V was also simulated and found to be -0.1 dB and 0.8 dB from the room temperature value. It can be seen how these are much smaller than variations caused by mismatch and process variations (Fig. 10).

The current drawn by the cascaded delay line was experimentally measured to be 245 nA as listed in Table I. To quantify the change in current caused by mismatch, the current drawn by the circuit across multiple dies were measured. Four out of the six dies drew currents between 172 nA and 245 nA, while the other two circuits drew higher currents of 323 nA and 464 nA. In Monte Carlo simulation, the maximum and minimum currents considering mismatch and process variation were 1.76 μA and 9.43 nA. The current drawn by the circuit is also sensitive to changes in temperature. When the circuit was simulated for temperatures between 0 and 70°C, the current drawn increased from 80 nA to 538 nA. However, none of these changes affected the functionality of the circuit. The delay value always remained within 1% of the nominal value. The gain variation due to temperature changes was also much smaller than that predicted by Monte Carlo and caused by mismatch and process variations (2 dB difference with respect to the room temperature value at 0°C, and -0.5 dB at 70°C).

B. Offset programmability

To correct for a maximum predicted offset of ± 83 mV (from Monte Carlo simulations in Fig. 11) across the 8 offset correction cells present in the delay line, a single offset correction cell only needs to compensate for about ± 10 mV. To investigate this programmability, a single offset correction cell was also fabricated (separate from the delay line) and the measured results are presented here from a single chip that will be representative of the performance of the offset correction cells within the delay line.
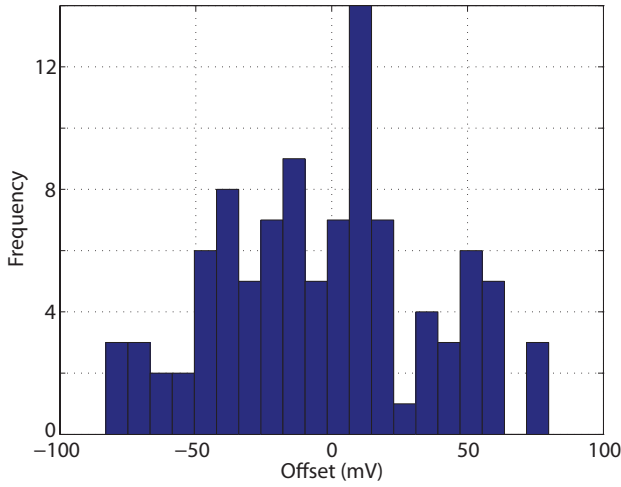
Fig. 11. Histogram showing the expected variation in offset at the output of the delay line caused by mismatch and process variations.
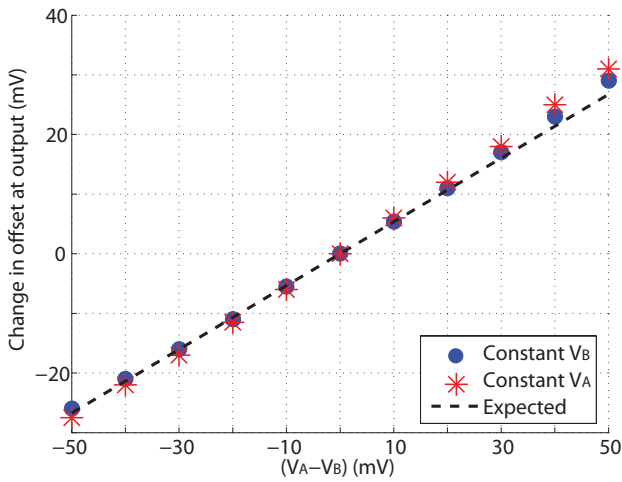

Fig. 12. Measured offset of output common mode voltage for a change in the reference voltages within a single offset correction cell.

Fig. 12 shows the offset tuning range of the single cell for a change in reference voltage $(V_A - V_B)$ from -50 mV to +50 mV. For this, reference voltage V_B is initially increased from 450 mV to 550 mV in steps of 10 mV whilst keeping V_A constant at 500 mV. The corresponding change in the offset at the output voltage has been plotted in Fig. 12. Next, V_B is kept constant while V_A is stepped up from 450 mV to 550 mV. In addition to the measured change in offset, the theoretical prediction for the offset tuning range obtained from (10) has also been plotted in Fig. 12. Based on (10), a change of 1 mV in $(V_A - V_B)$ would translate to a 0.53 mV change in the offset at the output of a single offset correction cell. The measured results in Fig. 12 are coherent with the theoretical prediction, especially for a small (± 20 mV) imbalance in the reference voltages.

It should be noted that since only *coarse* programmability of the offset is required—to ensure offset generated by mismatch between transistors does not lead to the output signal of any delay cell being outside the input signal range of the subsequent cell, leading to signal loss—several delay lines

could be implemented with common external bias voltages V_A and V_B.

IV. DISCUSSION

The delay duration can be changed in two ways: firstly, the number of cells in the cascaded delay line can be increased (for longer delays) or decreased (for shorter delays) at the same clock frequency, provided offset and gain loss are compensated at strategic positions within the delay line. However the number of delay cells in the cascade must be determined prior to fabrication. An alternative method to program the delay duration is to change the clock frequency as shown in Fig. 8 for the same input signal and the same number of cascaded cells. Using this approach, longer delays can be achieved from the same number of delay cells using lower frequency clocks provided higher mean squared error between the sampled output voltage and the delayed continuous-time input signal can be tolerated. Shorter delays do not pose a problem as the continuous-time input signal will be now be over-sampled by a larger factor.

The performance of the proposed delay circuit is compared to that of previously published delay circuits that achieve delay times longer than 1 μs in Table II. From Table II it can be seen that none of the previous circuits achieve the required 300 ms delay duration. The maximum delay duration is provided by [24]. The thyrister based circuit in [24] achieves a delay of 76.3 ms with only 10 nW power consumption and very small area. In [24], the delay duration is a function of the threshold voltage and $(1/I_{ctrl})$, where I_{ctrl} is an external bias current. This poses two problems: the delay duration is sensitive to process variations; and longer delay duration would require precise control of pico-Amps of current. Furthermore, the power consumption reported in [24] seems to be for a single sample delay and thus to sample the signal at the same frequency as the clock in the proposed circuit, multiple delay cells should be considered, and the sensitivity to process variation must be compensated.

Other millisecond delays have been generated by the circuits in [25] and [26]. The delay cells in [25] and [26] achieve shorter delay times than [24] and have higher power consumption. Even shorter delay durations have been reported in [14], with higher power consumption but smaller area. The all pass filter presented in [14] has 18 poles and zeros and achieves only 0.5 ms delay. It is possible to cascade these delay circuits to achieve the required delay duration but this would be at the cost of increased power consumption, and potentially impractical areas. Alternatively it would be possible to re-design that topology to realize a longer delay but not within the reported bandwidth. As the authors clearly explain in the paper for filter realizations delay and bandwidth are not independent parameters, and hence a longer delay would come at the cost of a proportionally lower bandwidth.

Table II also compares the intermodulation distortion, noise and input range of the circuits. However only the two circuits presented in [14] have reported these performance specifications.

Finally a Figure Of Merit (FOM) has been added in order to quantitatively try to compare different topologies. This is

TABLE II
COMPARISON WITH OTHER DELAY CIRCUITS.

Parameters	Gosselin [14]	Gosselin [14]	Kim [24]	Wang [25]	Rieger [26]	This work
Delay	546 μs	587 μs	2.6 ns – 76.3 ms	5 ms – 46 ms	30 μs – 2.4ms	30 ms – 3 s
Delay method	9th order all pass filter	9th order all pass filter	CMOS thyristor	1st order low pass filter	Sample & hold (multiple)	Sample & hold ($\times$30)
Post-fabrication tunable delay?	Yes (range NR[a])	Yes (range NR)	Yes (2.6 ns – 76.3 ms)	Yes (5 ms – 46 ms)	Yes (dependent on max input frequency)	Yes (dependent on max input frequency)
Bandwidth (sampling frequency)	5.97 kHz $\pm$8% (—)	5.4 kHz $\pm$8% (—)	NR	NR	7 kHz (14 kHz)	5 Hz–500 Hz (10 Hz – 1 kHz)
Power consumption	360 nW	360 nW	10 nW – 0.3 W	<6.5 μW – 7.2 μW	<700 nW	269.5 nW
Area (mm^2)	NR	0.03 mm^2	0.001 mm^2	<0.02 mm^2	0.41 mm^2	0.26 mm^2
IMD3	-23 dBc	-32.9 dBc	NR	NR	NR	-37 dBc
Input referred noise	-55 dB	-62dB	NR	NR	NR	-74 dB (0.1 Hz – 10 Hz)
Input range	40 mVpp	40 mVpp	NR	NR	NR	40 mVpp
FOM (nW $\times$ mm^2 / Hz) (300 ms, 3 s)	No area reported, no layout	>1, >9.8	No bandwidth reported	No bandwidth reported	640.6, 64062.5	0.14, 0.14

[a]NR stands for not reported.

defined as:

$$\text{FOM} = \frac{\text{Effective Power} \times \text{Effective Area}}{\text{Effective Bandwidth}} \quad (12)$$

where effective power, area and bandwidth represent the values of those parameters for a circuit like the one reported in the different references but designed to have a value of delay identical to the one achieved by our circuit. This figure of merit could only be calculated for some of the circuits because the others did not report one of the parameters needed for the calculation (either the area or the bandwidth).

In the case of the circuits reported in [14], these are filter based realizations. As explained above, in filter based topologies the delay value and the bandwidth are not independent parameters. Hence those topologies would only be able to implement a 300 ms delay within a 11.8 Hz and 10.8 Hz bandwidths respectively (3 s within 1.1 Hz bandwidth). These were the Effective Bandwidths used for the calculations. The Effective Area would also be larger since the longer delay would require bigger capacitances. However, it is not possible to calculate exactly the value because the area reported accounts also for the transconductors. A theoretically possible alternative to increasing the capacitances would be to reduce the currents of the transconductors to achieve smaller g_ms. However, in the reported design they are already as low as 1.5 nA, and the authors mention saturation problems caused by matching. Hence, reducing the currents to the 0.3 pA required for a 3 s delay, would not be a practical option leaving capacitor size increase as the only feasible one. For the circuit in [26] as explained in the paper, a longer delay is achieved by cascading individual cells. Hence, the way to increase the delay value would be to multiply the number of cells by a factor of 125 for a 300 ms delay and 1250 for a 3 s delay.

This would result in completely impractical realizations with Effective Areas proportionally larger and Effective Powers of 87.5 μW and 875 μW.

For the circuit in [25], although the figure of merit has not been reported, it is worth mentioning that it is a 1st order low pass filter realization, which implies a non-linear phase and hence a frequency dependent delay.

Overall, this circuit has the best FOM for large values of delay with the bandwidth constraints (i.e. signals that are at least 10 times faster), typical of the application presented in the paper. Furthermore most circuits (except for [24]) have higher power consumption.

V. CONCLUSION

Tunable long–duration low–power delay circuits are vital in parallelized signal processing algorithms which will have an increased presence in low-power biomedical devices, such as portable EEG systems and pacemakers. However there is no precedent in literature on circuits that can implement delays in the order of a second, to be used on signals which are at least 10 times faster. A novel low power, linear phase programmable delay line is presented in this paper. The duration of the delay can be easily changed by varying the frequency of an external clock. Experimental results illustrate this programmability with delay durations varying from 30 ms to 3 s. An even longer delay could however also have been achieved by cascading more delay cells. Offsets generated by the mismatch between transistors which could in principle limit the number of cells in the cascade are not a problem in this implementation because a novel offset compensation strategy has also been proposed. This strategy is based on tuning two bias voltages in FGMOS transistors strategically placed within the delay line.

When compared to experimentally measured delays previously reported in literature, the proposed circuit achieves delay durations that are 40 times greater than any other linear phase delay circuit.

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