OPEN ACCESS

University of BRISTOL

Zhou, Z., & Warr, P. A. (2016). An Analog Integrated Front-End Amplifier for Neural Applications. In 2016 International Conference on Integrated Circuits and Microsystems (ICICM 2016): Proceedings of a meeting held 23-25 November 2016, Chengdu, China. Institute of Electrical and Electronics Engineers (IEEE).

Peer reviewed version

Link to publication record in Explore Bristol Research
PDF-document

University of Bristol - Explore Bristol Research
General rights

An Analog Integrated Front-End Amplifier for Neural Applications

Zhijun Zhou[1], and Paul Warr[2]

[1]University of Bristol, Bristol, BS8 I UB, United Kingdom, zhijun.zhou@bristol.ac.uk

[2]University of Bristol, Bristol, BS8 I UB, United Kingdom, paul.a.warr@bristol.ac.uk

Abstract — **Within neural monitoring systems, the front-end amplifier forms the critical element for signal detection and pre-processing, which determines not only the fidelity of the biosignal, but also impacts power consumption and detector size. In this paper, a novel combined feedback loop-controlled approach is proposed to compensate for input leakage currents generated by low noise amplifiers when in integrated circuit form, alongside signal leakage into the input bias network. This loop topology ensures the front-end amplifier maintains a high input impedance across all manufacturing and operational variations. This front-end amplifier consumes 30 μW in 0.053 mm², achieves input impedance of 42 GΩ, and 58.7 $nv/\sqrt{Hz}$ input-referred noise.**

Index Terms — **Neural recording, analog integrated circuits, CMOS technology, biomedical signal processing, low-noise amplifiers.**

I. INTRODUCTION

The Front-End Amplifier (FEA) is a key element for signal detection within neural activity monitoring systems. Growing interest in the field of neuroscience has accelerated research into such systems [1]. Electrically-observable signals generated by neural activity are low in both amplitude and frequency [2]. The bandwidth of the biosignal applications varies from a few hundred to several thousand Hertz [3]. Hence, a relatively wide-bandwidth FEA capable of sensing a signal near to DC is required. The sensor-seen interface impedance varies from a few kΩ to a few MΩ [3]. With regards to the FEA in biosignal detection, this impedance invariably forms a voltage divider. A high input impedance FEA reduces the attenuation caused by the interface. Furthermore, as multiple-channel sensing becomes increasingly standard practice across neuroscience research, pivotal advances in low noise amplifier (LNA) front-end signal detection are necessary to counteract the aggregating external noise sources. A low input-referred noise FEA design lowers the overall noise figure, to increase the Signal-to-Noise Ratio (SNR) of the entire neuro-sensing system.

Capacitive feedback (CF) has become a popular topology in neural sensing applications within integrated form. It configures the gain by the ratio of capacitors, whilst simultaneously rejecting the DC offset [4]. A large input impedance may be achieved by selecting a small input capacitance. The input impedance of this topology is, however, limited by the Operational Amplifier (OPAMP) design, due to the input gate leakage current. Also, a low noise Op-amp requires a relatively large geometry input gate, as the flicker (1/f) noise is inversely proportional to the transistor's area. Large devices yield a large parasitic capacitance, resulting in an increase in the leakage current.

Several techniques are used to improve the trade-off between high input impedance and low noise for the FEA. For instance, auto zeroing (AZ) is commonly used, which employs a two-state sample-and-hold technique [5]. During the sampling phase, the amplifier is disconnected to avoid the input leakage current. The offset is sampled and then subtracted from the input signal. The noise (mainly the 1/f noise) of this sampling technique is reduced by the addition of chopper stabilization (CS) [6]. This modulates and amplifies the input signal to a higher frequency range to avoid the amplification of the 1/f noise. The demodulation stage translates the signal back to base-band after the amplification. The drawback of the CS technique is that it suffers from a narrow bandwidth compared with the broader range of bandwidths required by implantable devices. This may be overcome using a timing control block; however, this increases circuit complexity, size and power consumption, rendering it unsuitable for the IC multi-channel system.

Real-time biosignal processing on an IC platform may employ the conventional neutralization technique to avoid the need for external digital controllers. This topology delivers current, via a capacitor, back to the input stage, to neutralize any leakage current [3]. The FEA can maintain a high input impedance with this compensation technique only if the feedback capacitor is closely matched to the input gate capacitance. In the small-scale IC circuit domain, perturbations to the voltage on any of the MOSFET terminals (source (S), gate (G), drain (D) and body (B)), will bring about variations in the gate capacitance. This yields a mismatch between leakage current and neutralization current, which reduces the input impedance and triggers instability in the feedback loop. Hence, in an IC implementation, a fixed-value capacitor neutralization (FCN) loop is not sufficient in practice, due to the statistical

variance intrinsic to IC manufacturing and the conditions of operation, characterized by Process, Voltage and Temperature (PVT) variations.

In this paper, we propose a purely analog neutralization-based loop control (NLC) scheme. This topology is a loop-controlled feedback without the need for any external digital blocks, thus reducing chip area, circuit complexity and power consumption. The effective compensation of leakage current allows for a LNA to be implemented, to suppress noise while maintaining high input impedance, in a compact IC form across frequency and PVT variations. This topology provides an easy-to-implement, real-time FEA design solution for multi-channel biosignal detection and monitoring applications.

II. CIRCUIT TOPOLOGY

In Fig. 1, the proposed FEA includes two feedback loops, one each for neutralization (to address the leakage current of amplifier) and bootstrapping (to address current into bias network). A1 and A2 are two low-noise two-stage Complementary Metal-Oxide Semiconductor (CMOS) amplifiers [6]. Pseudo Resistors (PR) are used in the design. The PR comprises two Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) back-to-back, to create a large resistance with acceptable layout area [7]. The device geometries are given in TABLE I.
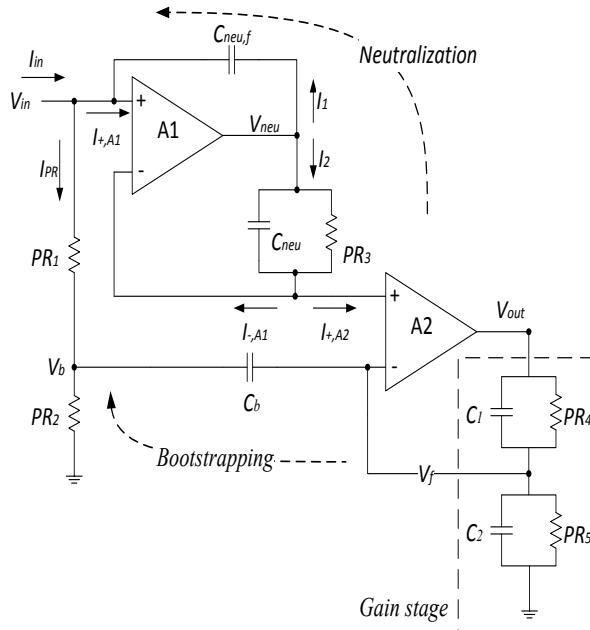

Fig. 1. Circuit topology of proposed NLC FEA design.

Bootstrapping is a voltage feedback loop technique to minimise the signal current entering PR_1 [3]. The current through PR_1 can be written as,

$$I_{PR} = \frac{V_{in} - V_b}{R_{PR_1}} \qquad (1)$$

Where, V_b is the bootstrapping voltage, via a capacitor C_b, written as equation (2). The lower cut-off frequency of this feedback, as given in Fig. 1, is defined by the product of R_{PR2} and C_b. V_b can track the input signal while the frequency is above approximately 300 mHz for a modest IC capacitor area, due to the PR structure's high resistance.

$$V_b = V_f \times \frac{R_{PR_2}}{R_{PR_2} + \frac{1}{j\omega C_b}}$$

$$\approx V_{in} \cdot \left(\frac{A_{op}}{A_{op} + 1}\right)^2 \times \frac{R_{PR_2}}{R_{PR_2} + \frac{1}{j\omega C_b}} \qquad (2)$$

A_{op} is the open loop gain of amplifiers A1 and A2. As given in equation (1), the closer the V_b tracks V_{in}, the lesser the signal current drawn into the bias circuit.

Neutralisation is a current feedback technique to deliver the substantial part of the leakage current into the amplifier A1 ($I_{+,A1}$). This leakage current is predominantly determined by the gate parasitic capacitance of the input transistor. In fact, it becomes the major current at the input stage in IC form after bootstrapping, given the use of PR. In Fig. 1, the voltages V_f and V_{in} are approximately the same ensuring that the gate leakage currents at all terminals are equal ($I_{+,A1} \approx I_{-,A1} \approx I_{+,A2}$). The output voltage of A1, called V_{neu}, will be that which is required to deliver the leakage currents for the two amplifiers' terminals: '+' of A2 and '-' of A1. The current through the capacitor C_{neu} (ignoring the much greater impedance of PR_3, added to provide a DC feedback path) is equal to the sum of $I_{-,A1}$ and $I_{+,A2}$. Because A1 and A2 are of the same topology, geometry and laid out using conventional matching techniques [8], the current I_2 is twice $I_{+,A1}$. This current-controlled voltage loop is connected to the input via a capacitor $C_{neu,f}$, whose capacitance is half that C_{neu}. Thus, as written in equation (4), I_1 is half of I_2, and is substantially the same amount of current as the amplifier's leakage current. With these two loops, the input current can be expressed as,

$$ \qquad (3)$$

$$I_{in} = I_{PR} + I_{+,A1} - I_1$$

Where,

$$I_1 = \frac{I_2}{2} = \frac{1}{2} \cdot \frac{V_{neu}}{Z_{C_{neu}||PR_3}} = \frac{1}{2}(I_{-A1} + I_{+A2}) \approx I_{+,A1} \qquad (4)$$

Hence, a higher input impedance of the FEA can be achieved by increasing the gain of A1 and A2.

The voltage gain of the FEA is configured by the non-inverting amplifier A2,

$$A_{NLC} = \frac{V_{out}}{V_{in}} \approx \frac{Z_{C_1||PR_4} + Z_{C_2||PR_5}}{Z_{C_2||PR_5}}$$

$$\approx \frac{\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2}} = \frac{C_1 + C_2}{C_1} = \frac{C_2}{C_1} + 1 \qquad (5)$$

TABLE I
DIMENSION CONFIGURATIONS OF FRONT-END AMPLIFIER DESIGN

Device	Size
C_m	1.5pF, $\frac{41.2um}{41.2um}$
C_b	1.33pF, $\frac{90um}{17um}$
$C_{neu,f}$	180fF, $3 \times \frac{8um}{8um}$
C_{neu}	360fF, $6 \times \frac{8um}{8um}$
C_1	100fF, $\frac{10.2um}{11um}$
C_2	1pF, $\frac{33.5um}{34.3um}$

III. RESULTS AND DISCUSSION

The AC currents at the input stage of the NLC technique is shown in Fig. 2. The leakage current of the OPAMP *A1*, $I_{+,A1}$, increases with increasing frequency. The current into bias network, I_{PR}, is suppressed by the bootstrapping feedback. Another feedback current I_1 neutralizes the leakage current to minimize the input current (I_{in}). The impedance of this FEA is circa 42 GΩ at 1 kHz.
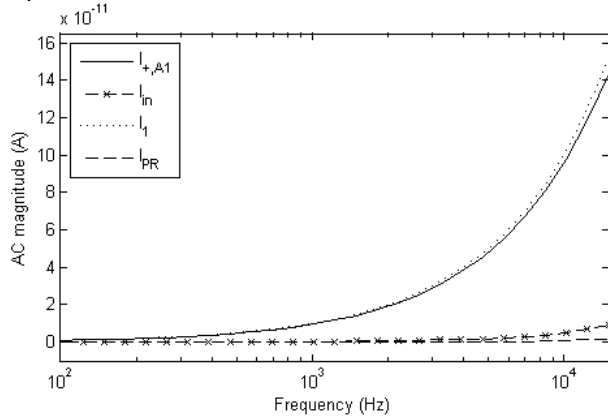

Fig. 2. AC currents of NLC technique.

The gain of the NLC technique is depicted in Fig. 3. As given in equation (5), the gain of this FEA can be easily adjusted by the capacitors, C_1 and C_2. It achieves approximately 20.81 dB at 1 kHz, and the bandwidth of this FEA is about 213.9 kHz.
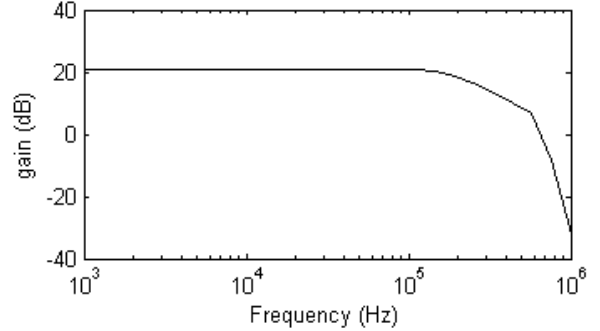

Fig. 3. Voltage gain of NLC technique.

PVT variation is a standard evaluation tool for CMOS circuit performance in IC manufacturing. The process-corner simulations are given in Fig. 4. F and S are the nomenclature for Fast and Slow corners for the electron and hole carriers' mobility respectively, the normal convention of writing F/S for NMOS and PMOS devices respectively is adopted here. For the FCN, the feedback capacitor is chosen to minimize the input current under the typical process corner (center of manufacturing range). By changing the process corners for the transistors, as shown in Fig. 4(a), (c), (e) and (g), the leakage current is changed whilst neutralization current remains fixed. Results indicate that the overall input current is not effectively suppressed by this FCN scheme, especially in FS and SF corners. On the other hand, simulation curves in Fig. 4(b), (d), (f) and (h) demonstrate that, the NLC will always substantially negate the input leakage current across process variation. Hence, a NLC scheme improves neutralization to consistently provide a high input impedance over process variations.

Voltage corner simulations are illustrated in Fig. 5. It is clear that, the gate parasitic capacitance is voltage-dependent. The leakage current is, hence, sensitive to supply voltage variation. Here, a 10% voltage sweep is set, between 2.97 to 3.63 V for nominal 3.3 V power rails (consistent with industry practice). Fig. 5(a) and (b) show that, the NLC is able to maintain a high input impedance for standard supply voltage variations.

In Fig. 6(a), it is shown that the neutralization current of a FCN scheme decreases with temperature. The resulting increase of input current leads to a reduction of the input impedance. Unlike using a fixed capacitor, in Fig. 6(b), the proposed NLC substantially mitigates the current difference between leakage and neutralization current. This results in a constantly suppressed input current over temperature variations.
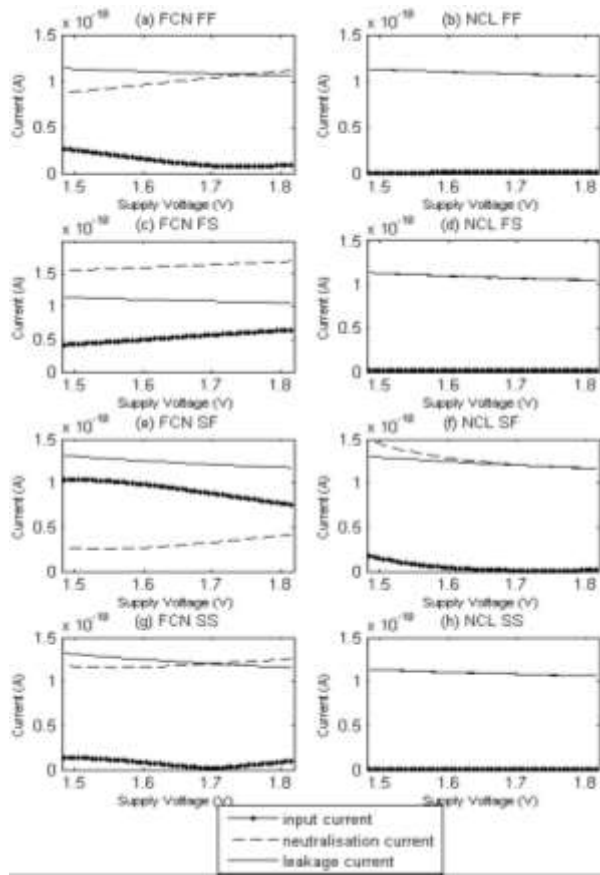
Fig. 4. Process corners (a) FF of FCN. (b) FF of NLC. (c) FS of FCN. (d) FS of NLC. (e) SF of FCN. (f) SF of NLC. (g) SS of FCN. (h) SS of NLC
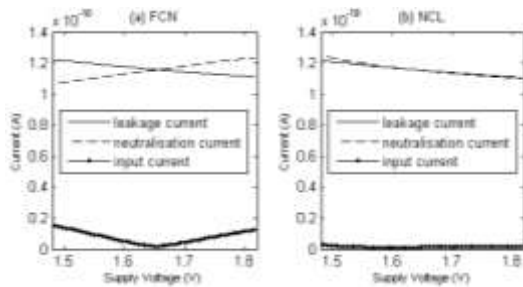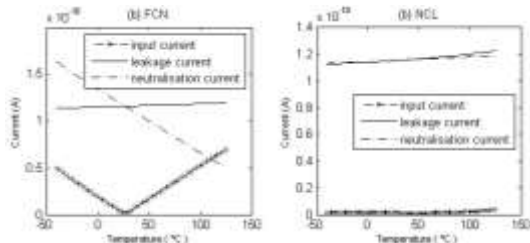

Fig. 5. Voltage corner of (a) FCN. (b) NLC.

Fig. 6. Temperature corner of (a) FCN. (b) NLC.

Consequently, the proposed NLC topology performs a compensation current that tracks input leakage current across all PVT corners.

IV. SUMMARY AND CONCLUSIONS

In this paper, a FEA with a new NLC technique for neural monitoring is presented. The proposed FEA is targeted at IC implementation and was simulated on the AMS 0.35µm CMOS process [9]. This FEA can achieve an input impedance of 42 GΩ (at 1 kHz) and 58.7 $nv/\sqrt{Hz}$ input-referred noise while consuming 30 µW in 0.053 mm^2. Furthermore, the NLC design is not sensitive to manufacturing variations and operational variations. The FEA achieves high input impedance in a wide bandwidth by compensating gate leakage via the NLC feedback loop.

REFERENCES

[1] M. Azin, D. Guggenmos, S. Barbay, R. Nudo and P. Mohseni , "A Battery-Powered Activity-Dependent Intracortical Microstimulation IC for Brain-Machine-Brain Interface," *IEEE J. Solid-State Circuits*, vol.46, no.4, pp.731,745, April 2011.

[2] D. Barsakcioglu, Y. Liu, P. Bhunjun, J. Navajas, A. Eftekhar, A. Jackson, Q. Quiroga, T. Constandinou , "An Analogue Front-End Model for Developing Neural Spike Sorting Systems," IEEE Trans. Biomed. Circuits Syst, vol.8, no.2, pp.216,227, April 2014.

[3] Y. Chi, C. Maier and G. Cauwenberghs, "Ultra-High Input Impedance, Low Noise Integrated Amplifier for Noncontact Biopotential Sensing," IEEE Trans. Emerg. Sel. Topics Circuits Syst, vol.1, no.4, pp.526,535, Dec. 2011

[4] R. Harrison and C.Charles, "A low-power low-noise CMOS amplifier for neural recording applications," IEEE J. Solid-State Circuits, vol.38, no.6, pp.958,965, June 2003.

[5] E. Spinelli, M. Haberman, P. García & F. Guerrero, "A capacitive electrode with fast recovery feature", *Physiological Measurement*, Volume 33, Number 8, July 2012.

[6] S. Song, M. Rooijakkers, P. Harpe, C. Rabotti, M. Mischi, A. van Roermund and E. Cantatore, "A Low-Voltage Chopper-Stabilized Amplifier for Fetal ECG Monitoring With a 1.41 Power Efficiency Factor," *IEEE Trans. Biomed. Circuits Syst*, vol.9, no.2, pp.237,247, April 2015.

[7] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad and A. Sodagar, "Analysis and Design of Tunable Amplifiers for Implantable Neural Recording Applications," *IEEE Trans. Emerg. Sel. Topics Circuits Syst*, vol.1, no.4, pp.546,556, Dec. 2011.

[8] A. Hastings, (2005) "Art of analog layout", the 2nd edition. United States: Pearson/Prentice Hall.

[9] Austria Micro System, 'CMOS C35 process parameters', 2015. [Online]. Available: http://asic.ams.com/cgi-docs/ENG-182_rev8.pdf. [Accessed: 01- Jul- 2015].