Zhou, Z., & Warr, P. A. (2016). A High Input Impedance Low Noise Integrated Front-End Amplifier for Neural Monitoring. IEEE Transactions on Biomedical Circuits and Systems. DOI: 10.1109/TBCAS.2016.2525810

# A High Input Impedance Low Noise Integrated Front-End Amplifier for Neural Monitoring

Zhijun Zhou, and Paul Warr

***Abstract*—Within neural monitoring systems, the front-end amplifier forms the critical element for signal detection and pre-processing, which determines not only the fidelity of the biosignal, but also impacts power consumption and detector size. In this paper, a novel combined feedback loop-controlled approach is proposed to compensate for input leakage currents generated by low noise amplifiers when in integrated circuit form alongside signal leakage into the input bias network. This loop topology ensures the FEA maintains a high input impedance across all manufacturing and operational variations. Measured results from a prototype manufactured on the AMS 0.35µm CMOS technology is provided. This FEA consumes 3.1 µW in 0.042 mm², achieves input impedance of 42 GΩ, and 18.2 $nv/\sqrt{Hz}$ input-referred noise.**

***Index Terms*— Neural recording, analogue integrated circuits, CMOS technology, biomedical signal processing, low-noise amplifiers.**

## I. Introduction and Current Techniques

THE Front-End Amplifier (FEA) is a key element for signal detection within neural activity monitoring systems [1], [2]. Growing interest in the field of neuroscience has accelerated research into such systems. However, these are restricted by a lack of suitable Integrated Circuit (IC) techniques [3], [4]. An integrated FEA within a small chip area enables neuroscientists and clinicians to simultaneously record and observe larger arrays of neural data, using multiple electrodes and multi-channel monitoring systems [5], [6], [7]. Further, acquiring neural activity data via high-density array sensing enables future research in disease and neuro-prosthetic devices [8].

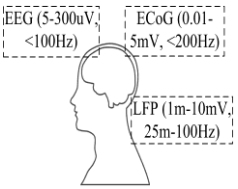
Electrically-observable signals generated by neural activity are low in both amplitude and frequency. Typically, the signal is comprised of two components, the Action Potential (AP) – also known as neural spikes – and the Local Field Potentials (LFP). APs have amplitudes ranging from $5\mu V_{pp}$ to $50\mu V_{pp}$, across frequencies of 300*Hz* to 7.5*kHz*, whilst LFP amplitudes are around $1mV_{pp}$ to $10mV_{pp}$, across a range of 25*mHz* to 100*Hz*, as described in [3]. Typical biosignal monitoring applications, such as Electroencephalography (EEG), Electrocardiography (ECG) and Electromyography (EMG) are given in TABLE I. The bandwidth of these applications varies from a few hundred to several thousand Hertz. Hence, a relatively wide-bandwidth FEA capable of sensing a signal near to DC is required.

Z. Zhou is with the Department of Electrical and Electronic Engineering, University of Bristol, England; P. Warr is with the Department of Electrical and Electronic Engineering, University of Bristol, England; e-mails: zhijun.zhou@bristol.ac.uk and paul.a.warr@bristol.ac.uk.

The sensor-seen interface impedance, as shown in TABLE I, varies from a few kΩ to a few MΩ and may be modelled as discussed in [9], [10], [11], [12]. With regards to the FEA in biosignal detection, this impedance invariably forms a voltage divider, where the higher the input impedance of the FEA, the lower the attenuation caused by the interface. Furthermore, a low input-referred noise FEA design lowers the overall noise figure, to increase the Signal-to-Noise Ratio (SNR) of the entire neuro-sensing system. As multiple-channel sensing becomes increasingly standard practice across neuroscience research, pivotal advances in LNA front-end signal detection are necessary to counteract the aggregating external noise sources that result from utilising more channels [6], [7]. Typical noise targets for various applications are also listed in TABLE I.

TABLE I
TYPICAL RECORDING APPLICATIONS

| | ENG | ECG | EMG |
|---|---|---|---|
| *Bandwidth (Hz)* | 4k | 250 | 2k |
| *Interface impedance (Ω)* | 2-5 k | 5-30 k | 2k-1M |
| *Noise* $v/\sqrt{Hz}$ | 20n | 800n | 80n |




Conventionally in neural monitoring systems, the instrumentation amplifier was widely used for Printed Circuit Board (PCB) scale systems due to its high input impedance and ease of gain adjustment using external resistors, as shown in Fig. 1(b). However, it is not suitable for implantable devices due to its large form factor [13]. The concept of a single IC die supporting a compact but high-number array of sensors overcomes this, enabling true in-vivo neural monitoring [14], [15]. To negate the large chip area of resistors, as shown in Fig. 1(a), capacitive feedback (CF) is typically used, as it configures the gain by the ratio of capacitors, whilst simultaneously rejecting the DC offset [16]. This method has become a most popular topology in neural sensing applications [17], [18]. A large input impedance may be achieved by selecting a small input capacitance, $C_1$ in Fig. 1(a), to reduce signal attenuation for low frequency neural applications. The input impedance of this topology is, however, limited by the Operational Amplifier (Op-amp) design, due to the input gate leakage current. Also, a low noise Op-amp requires a relatively large geometry input gate, as the flicker (1/f) noise is inversely proportional to the transistor's area. Large devices yield a large parasitic capacitance, resulting in an increase in the leakage current.

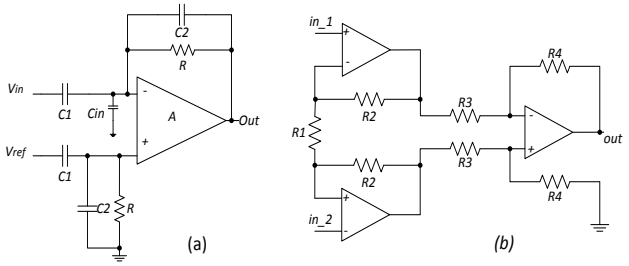



Fig.1. (a) Circuit topology of capacitive feedback biasing. (b) Structure of conventional instrumentation amplifier.

Several techniques are used to improve the trade-off between high input impedance and low noise for the FEA. For instance, auto zeroing (AZ) is commonly used, which employs a two-state sample-and-hold technique [19]. During the sampling phase, the amplifier is disconnected to avoid the input leakage current. The offset is sampled and then subtracted from the input signal. The noise (mainly the 1/f noise) of this sampling technique is reduced by the addition of chopper stabilisation (CS) [20], [21]. This modulates and amplifies the input signal to a higher frequency range to avoid the amplification of the 1/f noise. The demodulation stage translates the signal back to base-band after the amplification. The drawback of the CS technique is that it suffers from a narrow bandwidth compared with the broader range of bandwidths required by implantable devices, as shown in TABLE I. This may be overcome using a timing control block; however, this increases circuit complexity, size and power consumption, rendering it unsuitable for the IC multi-channel system.

Real-time biosignal processing on an IC platform may employ the conventional neutralisation technique to avoid the need for external digital controllers [22]. This topology delivers current, via a capacitor, back to the input stage, to neutralise any leakage current [23]. The FEA can maintain a high input impedance with this compensation technique only if the feedback capacitor is closely matched to the input gate capacitance. In the small-scale IC circuit domain, perturbations to the voltage on any of the MOSFET terminals (source (S), gate (G), drain (D) and body (B)), will bring about variations in the gate capacitance. This yields a mismatch between leakage current and neutralisation current, which reduces the input impedance and triggers instability in the feedback loop. Hence, in an IC implementation, a fixed-value capacitor neutralisation loop is not sufficient in practice, due to the statistical variance intrinsic to IC manufacturing and the conditions of operation, chartered by Process, Voltage and Temperature (PVT) variations.

In this case, the real-time measurement of an Op-amp's gate parasitic capacitance becomes the key to implementing neutralisation. The Current injection technique is discussed previously [24]. This approach implants DC current with chopped-phase to an AC bridge-based comparison circuit. As a result, the differential outputs of in-phase and quadrature-phase emulate the mismatch of detected capacitances. This output can then be used to control a reconfigurable capacitor, implemented by a switchable capacitor array (CA), to produce a real-time neutralisation current [9]. However, this array requires too great a chip area for future multi-channel implantable devices.

It is known that the chopping instrumentation amplifier achieves low input-referred noise and high input impedance, but its power consumption and circuit complexity is relatively high [19]. Therefore, a neutralisation-based loop control scheme is chosen in this design. We propose a novel purely analogue loop-controlled capacitance-matching neutralisation (LCN). This circuit is feedback loop-controlled without the need for any external digital blocks, thus reducing chip area, circuit complexity and power consumption. The biasing topology provides a real-time matching of the FEA's gate parasitic capacitance and neutralisation capacitor both across frequency and PVT variations. The effective compensation of leakage current allows for a LNA to be implemented to suppress noise while maintaining high input impedance in a compact IC form. This topology provides an easy-to-implement, real-time FEA design solution for multi-channel bio-signal detection and monitoring applications.

## II. CIRCUIT DESIGN

### A. Overview of circuit design

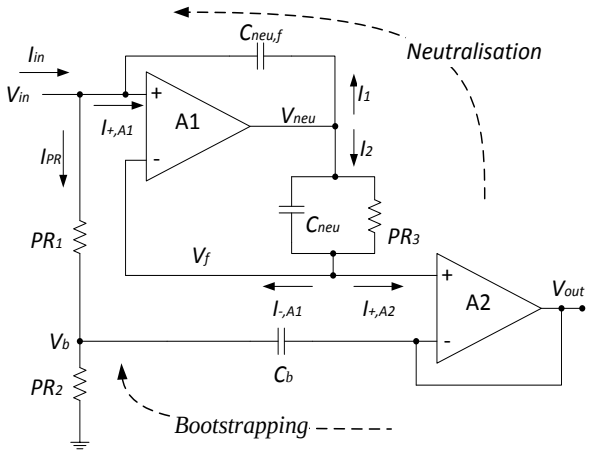



Fig. 2. Circuit topology of proposed FEA design with bootstrapping and neutralisation loop.

In Fig. 2, the proposed FEA includes two low-noise two-stage Complementary Metal-Oxide Semiconductor (CMOS) amplifiers (A1 and A2, details discussed in Section B) and two feedback loops, one each for neutralisation (to address the leakage current of amplifier) and bootstrapping (to address current into bias network). Pseudo Resistors (PR) are used in the design. The PR, as shown in Fig. 4(b), comprises two Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) back-to-back, to create a large resistance with acceptable layout area [25].

Bootstrapping [23] is a voltage feedback loop technique to minimise the signal current entering $PR_1$. The current through $PR_1$ can be written as,

$$I_{PR} = \frac{V_{in} - V_b}{R_{PR_1}} \quad (1)$$

Where, $V_b$ is the bootstrapping voltage, driven by the buffered output $V_{out}$ via a capacitor $C_b$, written as equation (2). As given in Fig. 2, the lower cut-off frequency of this feedback is defined by the product of $R_{PR2}$ and $C_b$. $V_b$ can track the input

signal while the frequency is above approximately 300 *mHz* for a modest IC capacitor area, due to the PR structure's high resistance. The device geometries are given in TABLE II.

$$V_b = V_{out} \times \frac{R_{PR_2}}{R_{PR_2} + \frac{1}{j\omega C_b}} = V_{in} \cdot \left(\frac{A_{op}}{A_{op}+1}\right)^2 \times \frac{R_{PR_2}}{R_{PR_2} + \frac{1}{j\omega C_b}} \quad (2)$$

$A_{op}$ is the open loop gain of amplifiers A1 and A2. $V_{out}$ is buffered twice with respect to $V_{in}$. In realisation, this equation is approximate due to the current through $PR_1$. As given in equation (1), the closer the $V_b$ tracks $V_{in}$, the lesser the signal current drawn into the bias circuit.

Neutralisation is a current feedback technique to deliver the substantial part of the leakage current into the amplifier A1 ($I_{+,A1}$). This leakage current is predominantly determined by the gate parasitic capacitance of the input transistor. In fact, it becomes the major current at the input stage in IC form after bootstrapping, given the use of PR. In Fig. 2, the voltages $V_f$, $V_{in}$ and $V_{out}$ are approximately the same ensuring that the gate leakage currents at all terminals are equal ($I_{+,A1} \approx I_{-,A1} \approx I_{+,A2}$). The output voltage of A1, called $V_{neu}$, will be that which is required to deliver the leakage currents for the two amplifiers' terminals: '+' of A2 and '-' of A1. The current through the capacitor $C_{neu}$ (ignoring the much greater impedance of $PR_3$, added to provide a DC feedback path) is equal to the sum of $I_{-,A1}$ and $I_{+,A2}$. Because A1 and A2 are of the same topology, geometry and laid out using known matching techniques [26], the current $I_2$ is twice $I_{+,A1}$. This current-controlled voltage loop is connected to the input via a capacitor $C_{neu,f}$, whose capacitance is half that $C_{neu.}$ Thus, as written in equation (4), $I_1$ is half of $I_2$, and is substantially the same amount of current as the amplifier's leakage current. With these two loops, the input current can be expressed as,

$$I_{in} = I_{PR} + I_{+,A1} - I_1 \quad (3)$$

Where,

$$I_1 = \frac{I_2}{2} = \frac{1}{2} \cdot \frac{V_{neu}}{Z_{C_{neu}||PR_3}} = \frac{1}{2}(I_{-_{A1}} + I_{+_{A2}}) \approx I_{+,A1} \quad (4)$$

Hence, a higher input impedance of the FEA can be achieved by increasing the gain of A1 and A2.

When implemented in IC form, other parasitic capacitances at the input stage, for example generated by metal proximity across different layers, can be eliminated by shielding. Shielding is a layout guarding technique which surrounds the input stage with a low resistance buffered voltage. Thus, while the shielding voltage, $V_{out}$ in Fig. 2, tracks the input, no AC current crosses the parasitic capacitance, details are discussed in Section E.

### B. Low noise two-stage Op-amp design

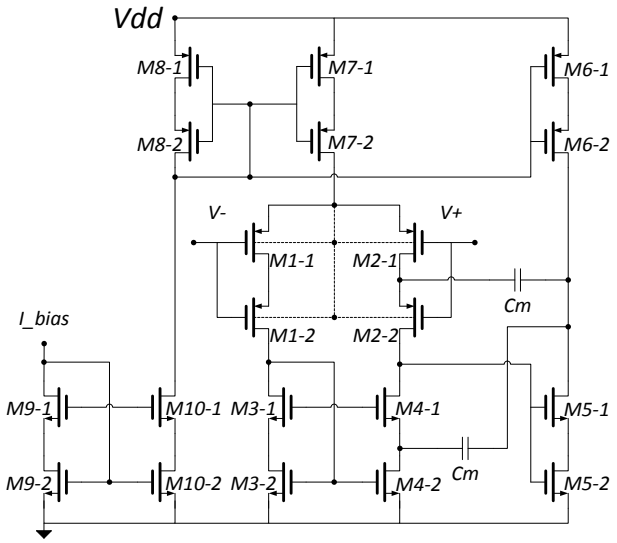



Fig. 3. Circuit schematic of CMOS low noise two-stage Op-amp.

Lower input-referred noise in IC Op-amp design, as shown in Fig. 3, is achieved by increasing the size of the amplifier's cascoded input devices (*M1-1*, *M1-2*, *M2-1*, *M2-2*). The Op-amp comprises two stages with Miller compensation. In the first stage, PMOS differential pairs in an isolated N-well are chosen due to the inherent lower 1/f noise over N-channel MOS (NMOS). Other transistor bulks (back gates) are connected to the appropriate rails (not explicitly shown for clarity). The cascode structure increases the open loop gain ($A_{OP}$) without increasing current consumption or noise [27], [28]. *M6_1,2*, *M7_1,2*, *M8_1,2*, *M9_1,2* and *M10_1,2* are current mirrors driven by a reference bias current. These cascoded mirrors increase the active load resistance to increase the gain of amplifier. The capacitors $C_m$ are used to employ Miller compensation, concordant with conventional IC design [27].

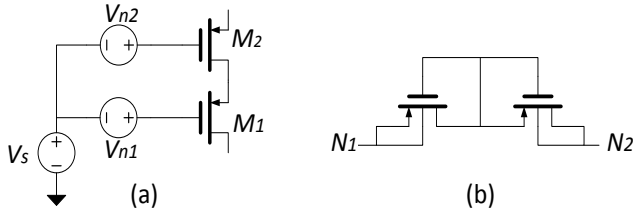



Fig. 4. (a) Noise mode of cascode amplifier. (b) Structure of fixed Pseudo Resistor.

For a single MOS input, the voltage and current noise are given in equations (5) and (6)

$$\overline{dV_G^2} = 4kTR_G df \quad (5)$$

$$\overline{di_{DS}^2} = \frac{4kT}{R_{CH}} df = 4kT\frac{2}{3} g_m df \quad (6)$$

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $R_G$ is the resistance of gate, $R_{CH}$ is the channel resistance and $g_m$ the is small-signal transconductance of the transistor.

A noise model of the cascoded amplifier is illustrated in Fig. 4(a), where $V_{n1}$ and $V_{n2}$ represent the input-referred noise of $M_1$ and $M_2$ respectively. The input-referred noise for the cascoded structure is given by.

$$\overline{dV_{ieq}^2} = \overline{dV_{n1}^2} + \overline{dV_{n2}^2} \cdot \frac{1}{g_{m1} r_{o1}} \approx \overline{dV_{n1}^2} \tag{7}$$

It can be seen in equation (7) that the use of the cascoded structure will increase the transconductance and output resistance of the transistors without inducing any noticeable increase in the input-referred noise.

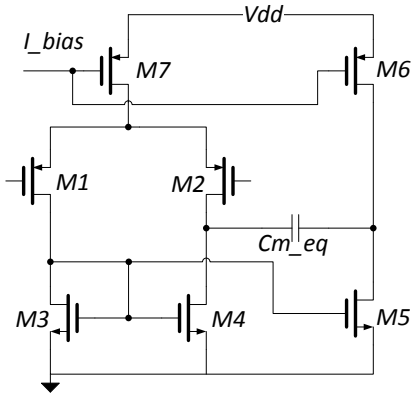



Fig. 5. Equivalent Circuit schematic of Op-amp design in Fig. 3.

To simplify the input-referred noise analysis, each cascoded pair is replaced by a single transistor, where the equivalent length of the transistor is the sum of its corresponding cascoded gates, for example,

$$L_i = L_{i\_1} + L_{i\_2} \tag{8}$$

Similarly, the equivalent Miller capacitance is the sum of these two capacitors in Fig. 3,

$$C_{m\_eq} = C_m + C_m \tag{9}$$

The gain bandwidth of the Op-amp is given by,

$$\omega_{GB} = \frac{g_{m1}}{C_{m\_eq}} = \frac{\sqrt{2k_p(\frac{W}{L})_1 I_{SD1}}}{C_{m\_eq}} \tag{10}$$

where $W$ and $L$ are the width and length of a corresponding transistor, $I_{SD}$ is the source-to-drain current. Likewise, the overall open loop gain of the Op-amp is the product of these two stages, written as,

$$A_{op} = \frac{g_{m2}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6}} \tag{11}$$

where,

$$g_{ds} = I_D \lambda \tag{12}$$

Here, $I_D$ is the drain current for a transistor and $\lambda$ is the channel-length modulation parameter depending on the manufacturing process. The input referred current noise of this structure is given by

$$\overline{I_n^2} = [(2\pi f)^2 C_{in}^2 \overline{V_n^2}]\Delta f \tag{13}$$

where $C_{in}$ is the capacitance of the input devices and $V_n^2$ is the input-referred voltage noise. As shown in equation (14), the voltage noise consists of thermal and 1/f noise.

$$\overline{V_{n,op}^2} = \overline{V_{n\_thermal}^2 + V_{n\_flicker}^2} \tag{14}$$

The thermal noise is calculated as

$$\begin{aligned}\overline{V_{n,thermal}^2} &= \frac{16kT}{3}\frac{1}{g_{m1}^2} \times [g_{m1} + g_{m3} + \frac{g_{m5} + g_{m6}}{2g_{m5}^2(r_{o2}||r_{o4})} \\ &\approx \frac{16kT}{3}\frac{1}{g_{m1}^2}(g_{m1} + g_{m3})\end{aligned} \tag{15}$$

While the 1/f is given by

$$\begin{aligned}\overline{V_{n,flicker}^2} &= \frac{2k_p}{W_1 L_1 c_{ox} f} + \frac{2k_n}{W_3 L_3 c_{ox} f}\left(\frac{g_{m3}}{g_{m1}}\right)^2 \\ &\quad + \frac{1}{g_{m2}^2 g_{m5}^2 (r_{o2}||r_{o4})}\left[\frac{g_{m5}^2 k_n}{W_5 L_5 c_{ox} f}\right. \\ &\quad \left. + \frac{g_{m6}^2 k_p}{W_6 L_6 c_{ox} f}\right] \\ &\approx \frac{2k_p}{W_1 L_1 c_{ox} f} + \frac{2k_n}{W_3 L_3 c_{ox} f}\left(\frac{g_{m3}}{g_{m1}}\right)^2 \\ &= \frac{2}{c_{ox} f}[\frac{k_p}{W_1 L_1} + \frac{\mu_n k_n L_1}{\mu_p W_1 L_3^2}]\end{aligned} \tag{16}$$

where $\mu$ represents the mobility and $k$ is the process-dependant constant. As shown in (15), the thermal noise can be suppressed by increasing the transconductance $g_m$ of $M_1$. This can be achieved by increasing the drain current as given in (17).

$$g_m = k(V_{GS} - V_t) = \sqrt{2ki_D} \tag{17}$$

For a neural signal application, 1/f noise is the major contribution to the input-referred noise. As shown in equation (16), this noise is inversely proportional to $L_3^2$. Hence, *M3* and *M4* are chosen to have relatively long length to reduce 1/f noise. Also, a wider width of $M_{1,2}$ not only reduces 1/f noise, but also increases the amplifier's transconductance to further suppress the thermal noise. The parameter configurations of the FEA design can be found in TABLE II.

TABLE II
DIMENSION CONFIGURATIONS OF FRONT-END AMPLIFIER DESIGN

| Device | Size |
|---|---|
| *M1-1, M1-2, M2-1, M2-2* | $4 \times \frac{100um}{0.5um}$ |
| *M3-1, M3-2, M4-1, M4-2* | $1 \times \frac{20um}{25um}$ |
| *M6-1, M6-2, M8-1, M8-2* | $1 \times \frac{10um}{0.5um}$ |
| *M7-1, M7-2* | $1 \times \frac{20um}{0.5um}$ |
| *M5-1, M5-2* | $1 \times \frac{2um}{1um}$ |
| *M9-1, M9-2, M10-1, M10-2* | $1 \times \frac{10um}{1um}$ |
| $C_m$ | 1.5pF, $\frac{41.2um}{41.2um}$ |
| $C_b$ | 1.33pF, $\frac{90um}{17um}$ |
| $C_{neu,f}$ | 180fF, $3 \times \frac{8um}{8um}$ |

### C. Feedback loop-controlled neutralisation

Neutralisation is a current feedback technique, which compensates for the gate leakage current dominated by the gate oxide capacitance of the device at the input stage of the amplifier, to minimise the input current. The gate leakage current of a MOS can be written as,

$$I_{gate} = WLA(\frac{V_{ox}}{t_{ox}})^2 \exp\{\frac{B[1-(1-\frac{V_{ox}}{\emptyset_{ox}})^{3/2}]}{\frac{V_{ox}}{t_{ox}}}\} \quad (18)$$

where, $W$ and $L$ are the width and length of the transistor respectively, $A = q^3/16\pi^2 h\emptyset_{ox}$, $B = -4\pi\sqrt{2m_{ox}}\emptyset_{ox}^{\frac{3}{2}}/3hq$, $m_{ox}$ is the effective mass of the tunnelling particle, $\emptyset_{ox}$ is the tunnelling barrier height, $h$ is Planck's constant, $q$ is the electron charge $t_{ox}$ is the oxide thickness and $V_{ox}$ is the gate oxide breakdown voltage. Therefore, for a given transistor, the gate leakage current is proportional to the product of width and length.

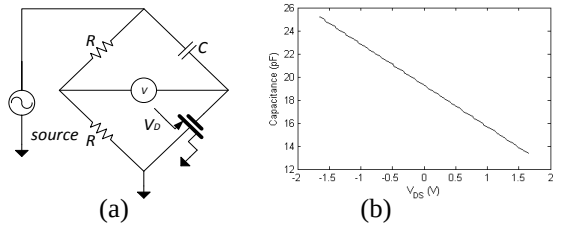



Fig. 6. (a) AC bridge circuit to detect parasitic capacitance of a MOS. (b) Simulation results of bridge detection.

Fig. 6 depicts the voltage-dependent gate capacitance variation of a MOS, detected by using an AC-bridge. The bridge identifies the equivalent capacitance with respect to a rail-to-rail sweep of $V_D$. Setting the source voltage to 1.25V, the simulation in Fig. 7(b) indicates that a 0.35um AMS $10 \times 1\ \mu m$ PMOS exhibits approximately between 13.3 and 25.2 pF gate parasitic capacitance at 1kHz. This leads to an operational variation of gate leakage current.

The conventional neutralisation technique [22] compensates input leakage current using a low impedance source, tracking the input signal, connected to the input via a series fixed-value capacitor. Precise control of either the feedback capacitance or the output voltage is required, implemented via configurable resistance and capacitance. This approach is not suited to compact IC implementation as the IC platform suffers from significant variations of the leakage current with operational and manufacturing variations. The proposed loop provides a circuit topology for neutralising real-time gate leakage current over various manufacturing processes and operational conditions.

### D. PVT comparison of fixed capacitor and loop-controlled neutralisation

PVT variation is a standard evaluation tool for CMOS circuit performance in IC manufacturing. In this section, a PVT comparison between a fixed-capacitor neutralisation (FCN) and LCN is presented. A FCN employs a capacitor with a feedback voltage to compensate input leakage current. Meanwhile, as depicted in Fig. 2, the LCN aims to feedback a voltage that is always adapted to whatever neutralisation capacitance is selected.

The process-corner simulations for the neutralisation schemes are given, in Fig. 7. F and S are short for Fast and Slow corners for the carriers mobility respectively, the normal convention of writing F/S for NMOS and PMOS devices respectively is adopted here. For the FCN, the feedback capacitor is chosen to minimise the input current under the typical process corner. Then, by changing the process corners for the transistors, as shown in Fig. 7(a), (c), (e) and (g), the leakage current will be changed and the neutralisation current is not adjusted accordingly. Results indicate that the overall input current cannot be suppressed by this FCN scheme, especially in FS and SF corners. On the other hand, simulation curves in Fig. 7(b), (d), (f) and (h) demonstrate that, the LCN will always substantially negate the input leakage current. Hence, a LCN scheme improves neutralisation to consistently provide a high input impedance over process variations.

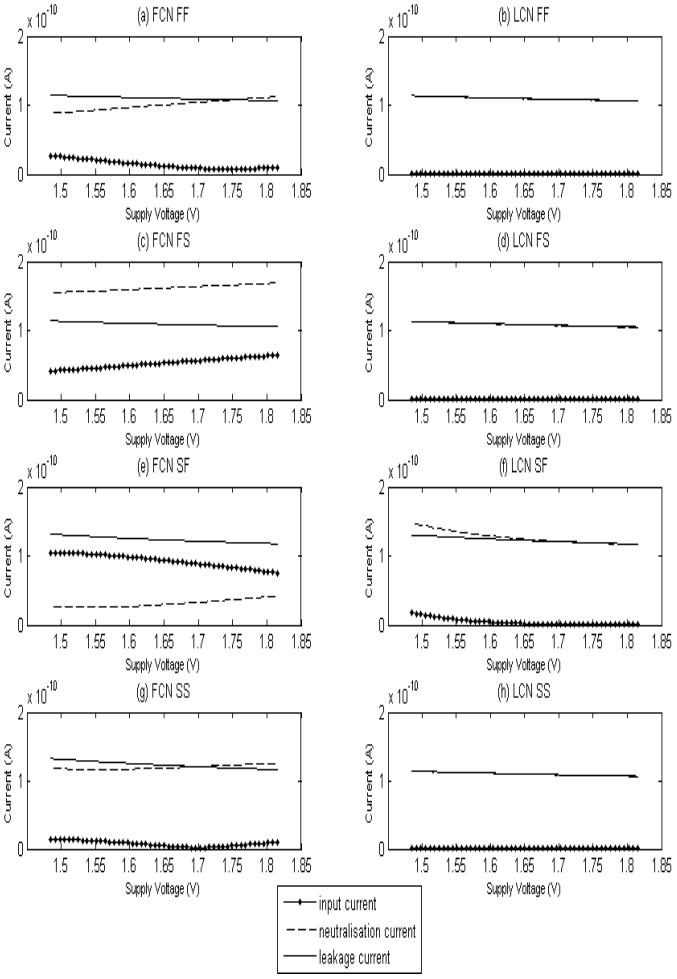



Fig. 7. Process corners (a) FF of FCN. (b) FF of LCN. (c) FS of FCN. (d) FS of LCN. (e) SF of FCN. (f) SF of LCN. (g) SS of FCN. (h) SS of LCN.

Voltage corner simulations are illustrated in Fig. 8. It is clear that, the gate parasitic capacitance is voltage-dependent. The leakage current is, hence, sensitive to supply voltage variation. Here, a 10% of voltage sweep is set, between 2.97 to 3.63 V for a nominal 3.3 V power rails (consistent with industry practice). Fig. 8(a) and (b) show that, the LCN is able to maintain a high input impedance for standard supply voltage variations.

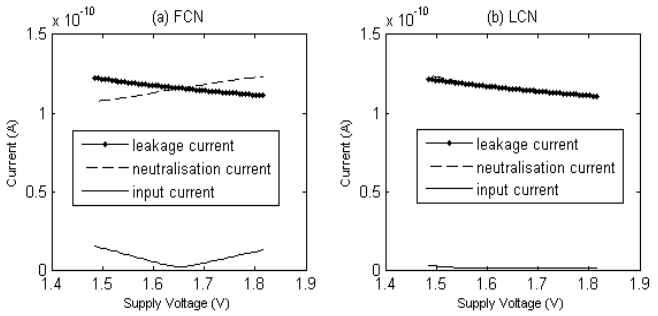



Fig. 8. Voltage corner of (a) fixed capacitor neutralisation. (b) loop-control neutralisation.

In Fig. 9(b), it is shown that the neutralisation current of a FCN scheme decreases with temperature. The resulting increase of input current leads to a reduction of the input impedance. Unlike using a fixed capacitor in Fig. 9(a), the proposed LCN avoids any current difference between leakage and neutralisation current. This results in a constantly suppressed input current over temperature variations.

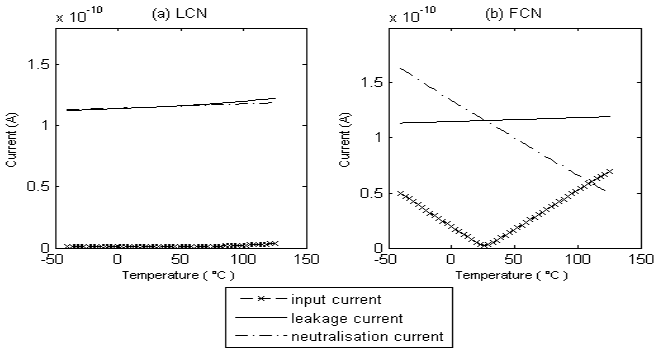



Fig. 9. Temperature corner of (a) fixed capacitor neutralisation. (b) loop-control neutralisation.

Consequently, the proposed LCN topology performs a compensation current that tracks leakage across all PVT corners.

### *E. Shielding*

As discussed in section II.A, the parasitic capacitance due to conductor implementation may be compensated by shielding (also known as guarding). As given in Fig. 10, the highlighted 'Metal 2' is the target layer carrying the signal. Metals around the target, including via connections between metal layers, are maintained at the metal 2 potential as a shield. In this case, any parasitic capacitance between the target and its environment draws no current from the driving signal. In Fig. 2, this shielding technique is implemented to $PR_1$ and the metallisation of the entire input stage.

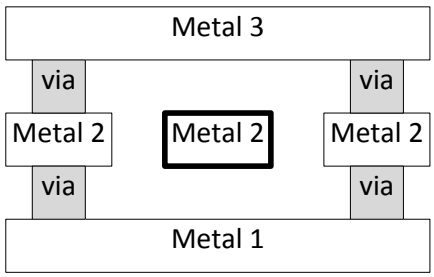



Fig. 10. Cross section of shielding technique.

## III. Experiment Results

The proposed FEA is designed and fabricated on the 0.35µm AMS CMOS technology **Error! Reference source not found.**. A chip photograph of the fabricated FEA is shown in Fig. 11, the chip area of a single channel FEA is 0.042 mm$^2$. This chip provides 20 channels to carry out five individual tests of different biasing techniques, and each test contains 4 channels.

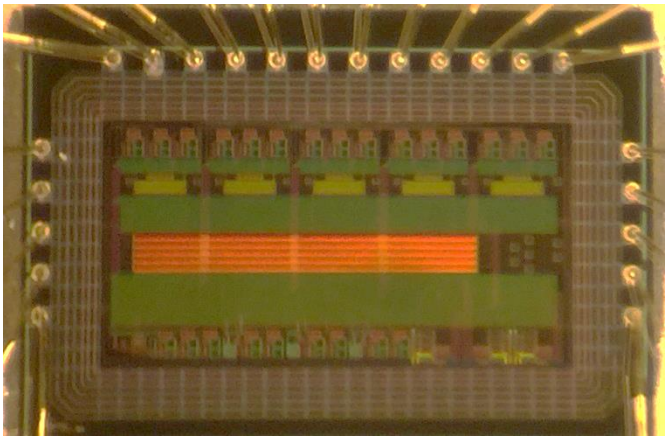


Fig. 11. Chip photograph of the fabricated FEA with on-chip testbench

An on-chip testbench (TB) is implemented in the concept-providing prototype. In Fig. 12, the testbench combines a resistor, $R_S$, in series with the FEA. The $R_S$ forms a voltage divider with respect to the input impedance of the FEA, and the voltage across $R_S$ is detected by an instrumentation amplifier.

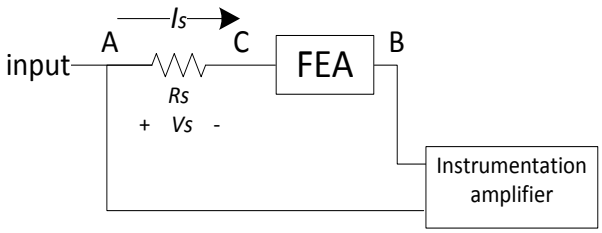



Fig.12. Testbench of measuring input impedance for FEA.

The output of the instrumentation amplifier can be written as,

$$V_o = A_{ins} \cdot (V_B - V_A) = A_{ins} \cdot \left(\frac{A_{op}}{A_{op}+1} \cdot V_C - V_A\right)$$
$$= A_{ins} \cdot \left(\frac{A_{op}+1}{A_{op}} \cdot \left(\frac{V_{output}}{A_{ins}} + V_A\right) - V_A\right) \quad (19)$$

where, $V_A$, $V_B$, $V_C$ are the node voltages in Fig. 12, $A_{op}$ is the open-loop gain of Op-amp design and $A_{ins}$ is the gain of the instrumentation amplifier. In this case, the input impedance of the amplifier can be expressed as,

$$R_{in} = \frac{V_{in}}{I_s} - R_s = \frac{V_{in}}{\frac{\frac{A_{op}+1}{A_{op}} \cdot \left(\frac{V_o}{A_{ins}} + V_A\right) - V_A}{Rs}} - R_s \quad (20)$$

where, $V_{in}$ is the input signal and $V_O$ is the output of the instrumentation amplifier. The measured and simulated results are shown in Fig. 13.

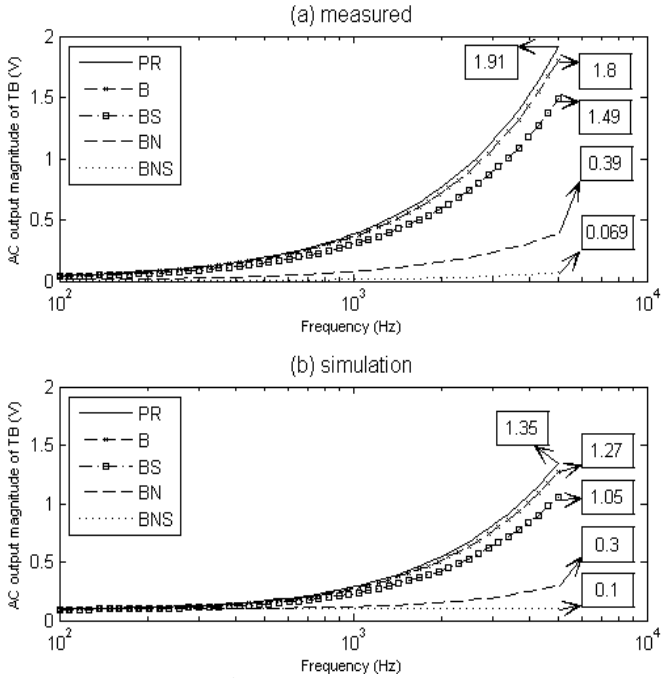



Fig. 13. Input impedance of FEA (a) Measured. (b) Simulation results.

The curves shown in Fig. 13 are the AC output magnitude of the instrumentation amplifier. Five tests were designed and implemented to compare the input impedance of different compensation techniques. This includes Pseudo Resistor (PR), Bootstrapping (B), Bootstrapping with Shielding (BS), Bootstrapping with Neutralisation (BN), and Bootstrapping, Neutralisation with Shielding (BNS). As given in Fig, 13(a), the measured AC magnitude is higher than the simulation, which indicates that the measured voltage across the series resistor is larger and, therefore, the practical input impedance is moderately less than that predicted by simulation. By using equation (21), the input impedance of the FEA can be calculated, shown in Fig. 14. At 1 kHz, the amplifier biased by PR provides circa 3.2 GΩ of impedance. The bootstrapping voltage feedback loop increases the impedance to 3.4 GΩ. By implementing the shield, the bootstrapping produces up to 4.1 GΩ. When the neutralisation current loop is implemented, this impedance increases to 16.6 GΩ. Upon introducing the shielding, these two loops work together to achieve about 42 GΩ input impedance. Therefore, the proposed loop-control neutralisation can further increase the input impedance of FEA biasing technique.

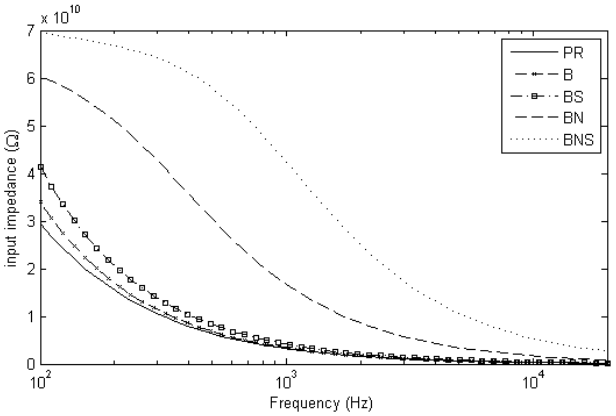



Fig.14. Calculated input impedance for FEA (measured results).

The experimental results are summarised in TABLE IV, with comparison to other reported FEA designs. With the proposed neutralisation technique, the FEA can achieve higher input impedance within lesser chip die and consumes lower power. A wide bandwidth is also achieved to support different neural signal detections.

TABLE IV
PERFORMANCE COMPASSION AND SUMMARY OF FEAS

| | This work | [23] | [19] | [9] | [18] |
|---|---|---|---|---|---|
| *Technology or process* | 0.35µm CMOS | 0.5µm CMOS | 0.18µm CMOS | 0.35µm CMOS | 0.13µm CMOS |
| *Biasing technique* | LCN | FCN | CS | CA | CF |
| *Chip area ($mm^2$)* | 0.042 | - | 0.076 | 0.08 | 0.072 |
| *Supply voltage (V)* | 3.3 | 3.3 | 1 | 3 | 1 |
| *Power (uW)* | 3.1 | 4.95 | 13 | 930 | 12.1 |
| *Gain (dB)* | 75 | - | 44.5 | 6-47 | 40 |
| *Bandwidth (Hz)* | 22.8M (Gain=0) | 800k (Gain=0) | 0.3~1k-10k | 100~12k | 0.05~10.5k |
| *Input impedance* | 42GΩ (at 1kHz) | >50TΩ | - | - | 4M |
| *Input-referred noise ($v/\sqrt{Hz}$)* | 18.2 n at 1kHz | 28 n at 1kHz | 4.4 µ at 10kHz | 0.68 µ | 2 µ |

## IV. CONCLUSION

In this paper, a FEA with a new loop-controlled capacitance-matching neutralisation compensation technique for neural monitoring has been proposed. The proposed FEA is targeted at IC implementation and was manufactured on the AMS 0.35µm CMOS process with a test bed. This chip can achieve an input impedance of 42 GΩ and 18.2 $nv/\sqrt{Hz}$ input-referred noise while consuming 3.1 µW in 0.042 $mm^2$. The measured results show approximately 2.5 times higher input impedance than conventional fixed-value capacitor neutralisation implemented in IC form. Furthermore, the LCN design is not sensitive to manufacturing variations and does not increase the input-referred noise. The FEA achieves high input impedance in a wide bandwidth by compensating gate leakage via a LCN feedback loop.

## REFERENCES

[1] S. Teng, R.Rieger and Y. Lin, "Programmable ExG Biopotential Front-End IC for Wearable Applications," *IEEE Trans. Biomed. Circuits Syst*, vol.8, no.4, pp.543,551, Aug. 2014.

[2] M. Azin, D. Guggenmos, S. Barbay, R. Nudo and P. Mohseni , "A Battery-Powered Activity-Dependent Intracortical Microstimulation IC for Brain-Machine-Brain Interface," *IEEE J. Solid-State Circuits*, vol.46, no.4, pp.731,745, April 2011.

[3] D. Barsakcioglu, Y. Liu, P. Bhunjun, J. Navajas, A. Eftekhar, A. Jackson, Q. Quiroga, T. Constandinou , "An Analogue Front-End Model for

Developing Neural Spike Sorting Systems," *IEEE Trans. Biomed. Circuits Syst*, vol.8, no.2, pp.216,227, April 2014.

[4] T. Wang, M. Lai; C. Twigg and S. Peng, "A Fully Reconfigurable Low-Noise Biopotential Sensing Amplifier With 1.96 Noise Efficiency Factor," *IEEE Trans. Biomed. Circuits Syst*, vol.8, no.3, pp.411,422, June 2014.

[5] M. Fatoorechi, J. Parkinson, R.J. Prance, H. Prance, A.K. Seth, D.J. Schwartzman, "A comparative study of electrical potential sensors and Ag/AgCl electrodes for characterising spontaneous and event related electroencephalagram signals", *Journal of Neuroscience Methods*, Volume 251, 15 August 2015.

[6] M. Guermandi, R. Cardu, E. Scarselli and R. Guerrieri, "Active Electrode IC for EEG and Electrical Impedance Tomography With Continuous Monitoring of Contact Impedance," *IEEE Trans. Biomed. Circuits Syst*, vol.9, no.1, pp.21,33, Feb. 2015.

[7] C. Lopez, A.Andrei, S. Mitra, M. Welkenhuysen, W. Eberle, C. Bartic, R. Puers, R. Yazicioglu and G. Gielen, "An Implantable 455-Active-Electrode 52-Channel CMOS Neural Probe," *IEEE J. Solid-State Circuits*, vol.49, no.1, pp.248,261, Jan. 2014.

[8] W. Chen, H. Chiueh, T. Chen, C. Ho, C. Jeng, M. Ker, C. Lin, Y. Huang, C. Chou, T. Fan, M. Cheng, Y. Hsin, S. Liang, Y. Wang, F. Shaw, Y. Huang, C. Yang and C. Wu, "A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic CMOS SoC for Real-Time Epileptic Seizure Control", *IEEE J. Solid-State Circuits*, 49(1), pp.232-247, 2014.

[9] A. Demosthenous, I. Pachnis, D. Jiang and N. Donaldson, "An Integrated Amplifier With Passive Neutralization of Myoelectric Interference From Neural Recording Tripoles," *IEEE Sensors J*, vol.13, no.9, pp.3236,3248, Sept. 2013.

[10] Y. M. Chi, T. P. Jung, and G. Cauwenberghs, "Dry-contact and noncontact biopotential electrodes: methodological review," *IEEE Rev. Biomed. Eng*, vol. 3, pp. 106-119, 2010.

[11] M. Nelson, "Review of signal distortion through metal microelectrode recording circuits and filters", *J. Neurosci. Meth*, vol.169, pp.141,157, 2008.

[12] P. Mohseni and K. Najafi, "A fully integrated neural recording amplifier with DC input stabilization," *IEEE Trans. Biomed. Eng*, vol.51, no.5, pp.832,837, May 2004

[13] M. Steyaert and W. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol.22, no.6, pp.1163,1168, Dec 1987.

[14] T. Akin, K. Najafi and R. Bradley, "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," *IEEE J. Solid-State Circuits*, vol.33, no.1, pp.109,118, Jan 1998.

[15] P. Mohseni and K. Najafi, "A fully integrated neural recording amplifier with DC input stabilization," *IEEE Trans. Biomed. Eng*, vol.51, no.5, pp.832,837, May 2004.

[16] R. Harrison and C.Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol.38, no.6, pp.958,965, June 2003.

[17] W. Wattanapanitch, M. Fee and R. Sarpeshkar, "An Energy-Efficient Micropower Neural Recording Amplifier," *IEEE Trans. Biomed. Circuits Syst*, vol.1, no.2, pp.136,147, June 2007.

[18] F. Zhang; J. Holleman and B. Otis, "Design of Ultra-Low Power Biopotential Amplifiers for Biosignal Acquisition Applications," *IEEE Trans. Biomed. Circuits Syst*, vol.6, no.4, pp.344,355, Aug. 2012.

[19] E. Spinelli, M. Haberman, P. García & F. Guerrero, "A capacitive electrode with fast recovery feature", *Physiological Measurement*, Volume 33, Number 8, July 2012.

[20] S. Song, M. Rooijakkers, P. Harpe, C. Rabotti, M. Mischi, A. van Roermund and E. Cantatore, "A Low-Voltage Chopper-Stabilized Amplifier for Fetal ECG Monitoring With a 1.41 Power Efficiency Factor," *IEEE Trans. Biomed. Circuits Syst*, vol.9, no.2, pp.237,247, April 2015.

[21] L. Toth and Y. Tsividis, "Generalization of the principle of chopper stabilization," *IEEE Trans. Circuits Syst. I, Fundam. Theory*, vol.50, no.8, pp.975,983, Aug. 2003.

[22] W. Beall and J. Choma, "Charge-neutralized differential amplifiers," *Analog Integr Circ Sig Process*, 1(1), pp.33,44, 1991.

[23] Y. Chi, C. Maier and G. Cauwenberghs, "Ultra-High Input Impedance, Low Noise Integrated Amplifier for Noncontact Biopotential Sensing," *IEEE Trans. Emerg. Sel. Topics Circuits Syst*, vol.1, no.4, pp.526,535, Dec. 2011

[24] D. Buxi, S. Kim; N. van Helleputte, M. Altini, J. Wijsman, R. Yazicioglu, J. Penders and C. Van Hoof, "Correlation Between Electrode-Tissue Impedance and Motion Artifact in Biopotential Recordings," *IEEE Sensors J* , vol.12, no.12, pp.3373,3383, Dec. 2012

[25] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad and A. Sodagar, "Analysis and Design of Tunable Amplifiers for Implantable Neural Recording Applications," IEEE Trans. Emerg. Sel. Topics Circuits Syst, vol.1, no.4, pp.546,556, Dec. 2011.

[26] Austria Micro System, 'CMOS C35 process parameters', 2015. [Online]. Available: http://asic.ams.com/cgi-docs/ENG-182_rev8.pdf. [Accessed: 01- Jul- 2015].

[27] C. Wu, W. Chen and L. Kuo, "A CMOS Power-Efficient Low-Noise Current-Mode Front-End Amplifier for Neural Signal Recording," *IEEE Trans. Biomed. Circuits Syst*, vol.7, no.2, pp.107,114, April 2013.

[28] B. Bhowmik, M. Pattanaik and P. Srivastava, "A Low Power Low Noise Two Stage CMOS Operational Amplifier for Biopotential Signal Acquisition System," *international journal of emerging technology and advanced engineering*, vol.3, pp.224,228, 2013

**Zhijun Zhou** received his B.Eng. (Electronics Engineering) from the Birmingham City University in 2010, and his M.Sc. (Advanced Microelectronic Systems Engineering) from the University of Bristol in 2011. He is currently working toward his Ph.D. degree at the University of Bristol in the Centre for Communications Research group. His research covers analog integrated front-end amplifier circuit design and biosignal communication.

**Paul A. Warr** received his B.Eng. (Electronics and Communications) from The University of Bath in 1994, and his M.Sc. (Communication Systems) and Ph.D. (Radio Frequency Engineering) from The University of Bristol in 1996 and 2001 respectively. He is currently a Senior Lecturer in Electronics at the University of Bristol where his research covers the front-end aspects of Software-Defined Radio, analog integrated circuit design and distributed microwave structures.