Improving the Stability of the Battery Emulator – Pulsed Current Load Interface in a Power Hardware-in-the-Loop Simulation

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***Abstract*—Replacing a battery pack with a battery emulator (BE) in a Power Hardware-in-the-Loop Simulation (HILS) setup facilitates the testing of new prototype hardware but stability and high fidelity are not a priori ensured. Due to the large output capacitance that devices implementing BEs usually have, their dynamic response differs compared to a real battery which operates like a voltage source with a series resistance. This problem becomes particularly intense when the hardware under test (HUT) also has a large input capacitance. The intuitive solution proposed is to connect a series resistor between the BE and the HUT to replicate the battery series resistance. This paper describes the conditions that this resistor needs to follow in order to ensure stability. It is also shown that the limited bandwidth of the power device used to implement the BE is possible to bring the emulation into stability even if those conditions are violated. Finally, examples are given on how a low sampling frequency in the feedback loop cause oscillations. Simulations and experiments are used to demonstrate all the findings.**

Keywords—Power Hardware-in-the-Loop Simulation; battery emulation; stability; current feedback; voltage feedback

I. INTRODUCTION

Hardware-in-the-Loop Simulation (HILS) is a technique that facilitates the testing of new prototype hardware. In this method, an experiment is conducted where the critical parts of the equipment are physically present while the rest of the system is simulated in real time. Depending on the way the real hardware interacts with the simulated equipment, the simulation can be implemented on Signal (or Control), Power or Mechanical level [1]. When it comes to testing hardware designed to be used in association with batteries, battery emulators (BE) can be used instead of a battery pack in a Power HILS setup offering numerous advantages [2]:

- Less time-consuming. After each operation, the battery should be brought back to the initial state in order to repeat the experiment. This task could take several hours. On the other hand, in a Power HILS setup it can be done instantaneously.
- Easy initialisation and repeatability of experiments. The battery voltage and output impedance depend not only on the present operating conditions but also on how they were treated in the past. Thus, it is difficult to re-initialise the battery in order to repeat the test.
- Unlimited number of experiments. As the battery goes through charging and discharging cycles, degradation phenomena are observed and eventually the cell has to be replaced.
- Savings in space and cost. It is not necessary to buy a whole battery pack. In addition, the behaviour of several battery types can be replicated by a single emulator.
- It is easier to ensure safe operation. It is not necessary to address issues of cell imbalance or taking extra care to protect the battery from overcurrent, overcharge or overdischarge.

The emerging question is how accurately a BE can replicate the behaviour of a real battery pack. In Fig. 1a, the original experimental setup is shown in which a battery pack is connected to the hardware under test (HUT). The battery is modelled as a voltage source in series with a resistance and the HUT as a current source with a parallel capacitor. In Power HILS, the battery pack is replaced with a converter with an output capacitance like the one shown in Fig. 1b. The challenging part of the emulation is to make the BE – HUT power interface resemble the behaviour of the battery pack – HUT power interface. In other words, a method should be found to make a device with a low output impedance behave as if its output impedance was higher.

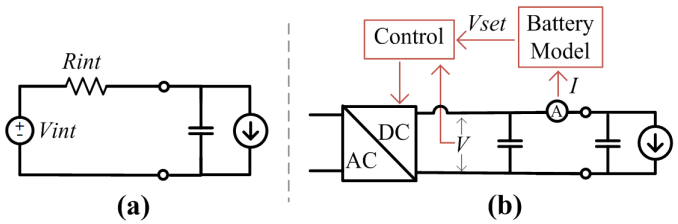

Fig. 1. Equivalent circuit representations of the battery pack – HUT (a) and the BE – HUT (b) power interfaces.

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The most important feature required by a Power HILS is stability. This is studied in Section IV assuming that the only non-ideality of the power device implementing the BE is a time delay equal to the time-step of the sampler used by the feedback loop. The other important characteristic a Power HILS requires is high fidelity. The Power HILS setup should make sure that the measured dynamics are caused by the HUT and do not result from the presence of the BE. The devices implementing BEs are seldom ideal. Effects of limited bandwidth, harmonic injection and time delay are observed which can result in high inaccuracy [3]. An example of highly inaccurate behaviour is shown in Section II. This behaviour is analysed in order to locate the mechanisms causing the observed distortion and methods are demonstrated for preventing it. While Section IV describes the operation of an ideal Power HILS, Section V expands the analysis for non-ideal systems and Section VI relates the simulation results with experimental data. Finally, Section VII describes the related work found in the literature while Section VIII concludes the findings suggesting some guidelines that should be followed when a BE is used in a Power HILS.

II. The Problem – Motivation for the Study

The motivation of the present study is unwanted behaviour observed during a Power HILS [4]. The HUT is the half-bridge DC/DC converter which is developed in [5] and is shown in Fig. 2. The BE is connected to the high side in parallel with the capacitor C_1. The device implementing the BE is the Delta Elektronika SM 52-AR-60 power source [6]. Since this device does not natively support two-quadrant operation, a current sink resistor is used in parallel with the voltage terminals as shown in Fig. 3. When the device has to emulate charging behaviour, the current coming from the HUT will go through R_{sink}. The series diode is used for protection and it remains forward biased. This way, the power supply always sources current and consequently dictates the voltage in the power interface [4].

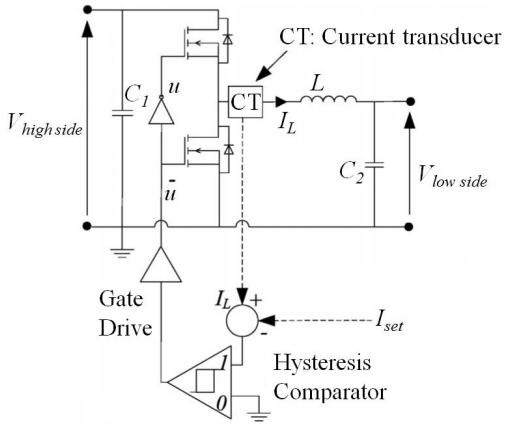

Fig. 2. The half-bridge DC/DC converter with hysteresis control loop [5] that constitutes the HUT. The BE is connected to the high side.

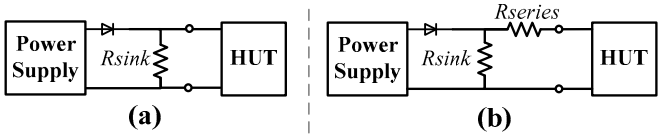

Fig. 3. Power supply connected in two-quadrant configuration (a) and the modification proposed for oscillation suppression (b).

The emulation runs smoothly but after a certain power level, the voltage and current of the BE – HUT interface start to oscillate as shown in Fig. 4a. When a lower value of R_{sink} is used, the system starts oscillating at lower power. The problem is solved by adding a series resistor R_{series} in the interface as shown in Fig. 3b. The improved behaviour is presented in Fig. 4b in which the oscillations have been suppressed. If the value of R_{series} is low, the oscillations will reappear when an operation point with a higher power is required. The emerging questions are why these oscillations occur, how the series resistor supresses them and if it is possible to design the Power HILS in a way to ensure that the system will not oscillate no matter what the operation point is.

III. System Description and Modelling

A. The Hardware under Test

The HUT as described in Section II is a half-bridge DC/DC converter using a current hysteresis controller as shown in Fig. 2. This system is modelled as a pulsed current load in parallel with a capacitor which has an equivalent series resistor (ESR).

B. Power Device

Fig. 5 shows a simple model derived to describe the Delta Elektronika SM 52-AR-60 power device for operation in voltage control mode. Its basic components are a DC voltage source controlled by a PI controller which charges the output capacitor through the series resistance R_1 and a diode. The diode prevents the capacitor from being discharged through the internal voltage source. Consequently, when a voltage decrease is demanded, the capacitor can be discharged only via the built-in resistor R_2 and the externally connected hardware. This behaviour is presented in Fig. 6a. Another important feature is the presence of a current limiter. After a voltage increase is requested, the capacitor has to be charged to reach the set voltage. When the current of the internal voltage source exceeds the value of 30A, a current limiter is activated. The activation of the current limiter is presented in Fig. 6c while a voltage increase that does not activate it is shown in Fig. 6b.

The non-linear behaviour caused by the diode and the current limiter make the system have a response delay similar to a low-pass filter. In other words, the power device can be considered to be linked to a non-linear low-pass filter, the cut-off frequency of which depends on the operating conditions.

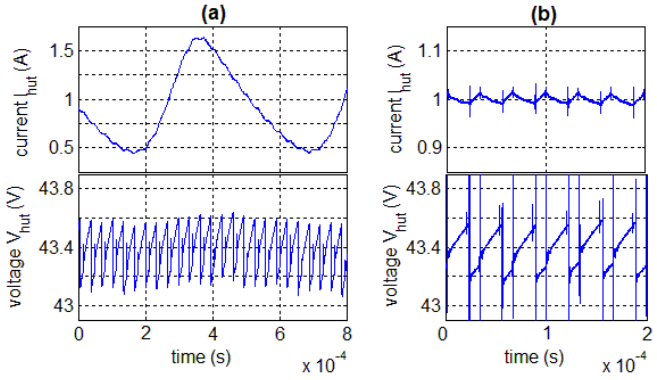

Fig. 4. Battery emulation with R_{sink} = 13.8 Ω and model parameters V_{int} = 45 V and R_{int} = 1.51 Ω. Current and voltage oscillations are observed when the BE and the HUT are connected as in Fig. 3a (a) but they are suppressed when the topology of Fig. 3b is used with R_{series} = 1Ω (b).

C. Battery Model and Real-Time Platform

The battery model used to supply the reference voltage for the BE is the equivalent circuit model (ECM) that is developed in [7] and shown in Fig. 7a. The ECM used consists of a voltage source in series with a resistance and a ladder of two RC networks. The first one has a time constant in the range of tens of seconds and the second one in the range of hundreds of seconds [7]. Consequently, for the study of dynamic effects with a time-scale less than 100 ms the model can be reduced to a voltage source V_{int} in series with a resistance R_{int} as shown in Fig. 7b, both of which are functions of the state of charge (SoC).

The real-time platform used to execute the battery model and supply the reference voltage to the power device is the dSpace DS1104 R&D Controller Board. The algorithm used is built in a Simulink/MATLAB environment using the ode1 solver as in [7]. The execution time-step is 40 μs.

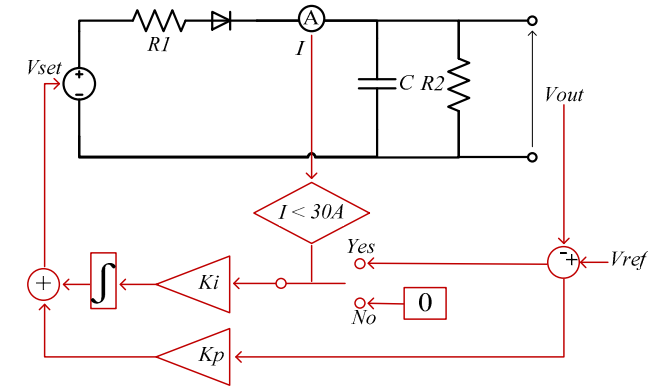

Fig. 5. The Delta Elektronika SM 52-AR-60 model for operation in voltage control mode.

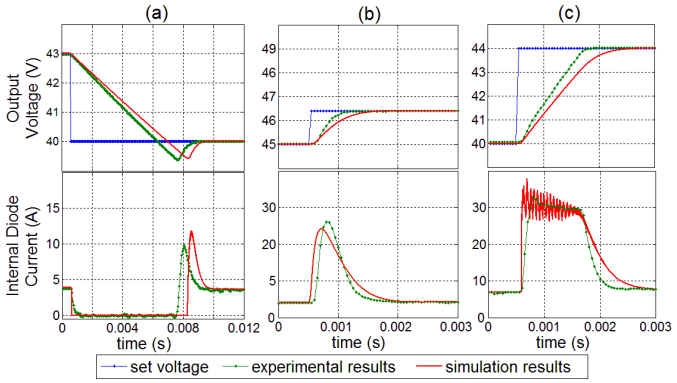

Fig. 6. The measured and modelled response of Delta Elektronika SM 52-AR-60 when operating in voltage control mode and the set voltage changes. Part (a) shows the response to a set voltage decrease, (b) shows a voltage increase in which the current limiter is not activated and (c) shows a voltage increase with activation of the current limiter.

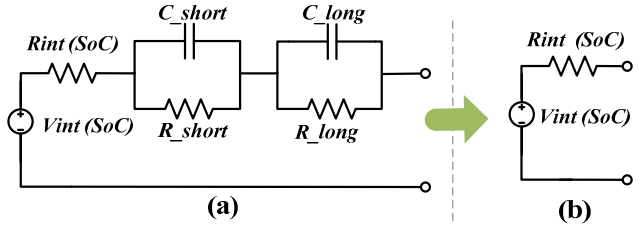

Fig. 7. The equivalent circuit battery model used in [7] and how it can be simplified when dynamic effects with a time-scale less than 100 ms are studied.

D. Model of the System

Based on the above, the resulting model of the Power HILS setup is presented in Fig. 8. The right part of the system shows the model of the actual experiment taking place. It is called "*hardware part*" because all its components correspond to real devices taking part in the experiment. As explained in Section III/A, the HUT model consists of a current load I in parallel with a non-ideal capacitor C and an ESR r_c. The Delta Elektronika power supply is modelled by the ideal voltage source V_{Delta}, the value of which is set by a non-linear low-pass filter. Between V_{Delta} and HUT, the series resistor R_{series} is placed.

The left part of the system shows the battery model. As explained in Section III/A, this is reduced to a voltage source V_{int} in series with a resistance. Since a part of the battery model series resistance R_{int} is emulated by the resistor R_{series}, the virtual resistance R_{virt} used in the left part of the system is given as:

$$R_{virt}(SoC) = R_{int}(SoC) - R_{series} \quad (1)$$

Unlike the hardware part of the experiment, the battery model is executed only in simulation. Thus the left part of the system is called "*software part*". The simulation inputs current measurements from the hardware part in real time and outputs the voltage value to be fed into the non-linear low-pass filter. Inevitably, the signal exchange between the software and the hardware part has a time delay the consequences of which are explained in the paragraphs to follow.

IV. Circuit Analysis for an Ideal Voltage Source

A. Current Feedback

The first step for analysing the Power HILS setup of Fig. 8 is to describe the system operation with an ideal voltage source that does not operate like a low-pass filter. In the following calculations, the delay of the current feedback loop remains but it is assumed that the sampling frequency is considerably higher than the frequency of the pulsed current load. It is also assumed that the value of the HUT input capacitor C is high enough so that the capacitor voltage V_C remains constant. Applying discrete-time analysis, the input current of the HUT I^n_{hut} is:

$$I^n_{hut} = \frac{V^n_{Delta} + I \cdot r_c - V_C}{R_{virt} + r_c} \quad (2)$$

Where:

n the present time step

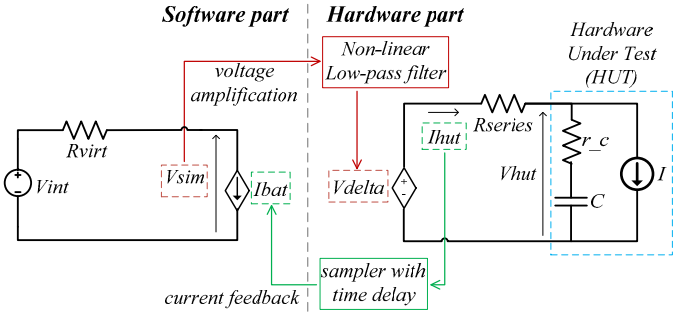

Fig. 8. The model of the Power HILS setup for operation in current feedback loop.

I the current source
r_c the ESR of the HUT input capacitor
V_C the capacitor voltage
V^n_{Delta} the value of the voltage source dictated by the software part of the emulator as:

$$V^n_{Delta} = V^n_{sim} = V_{int} - I^n_{bat}\cdot R_{virt} = V_{int} - I^{n-1}_{hut}\cdot R_{virt} \quad (3)$$

Where:
V_{int} the battery model voltage
V^n_{sim} the voltage estimated by the software part of the emulator which is used as a reference for the voltage source V^n_{Delta} of the hardware part
I^n_{bat} the current source of the software part, the value of which is fed by the hardware part through a sampler with a time delay, $I^n_{bat}=I^{n-1}_{hut}$.

Substituting (3) into (2), the final equation for I^n_{hut} becomes:

$$I^n_{hut} = \frac{V_{int} + I\cdot r_c - V_C}{R_{series} + r_c} - \frac{R_{virt}}{R_{series} + r_c}\cdot I^{n-1}_{hut} \quad (4)$$

Equation (4) describes a stable system only if:

$$\left|\frac{R_{virt}}{R_{series} + r_c}\right| < 1 \leftrightarrow |R_{virt}| < |R_{series} + r_c| \quad (5)$$

Since in practice it is difficult to estimate the exact value of r_c, it is simpler to omit it. Then (5) becomes:

$$|R_{virt}| \le |R_{series}| \leftrightarrow -R_{series} \le R_{virt} \le R_{series} \leftrightarrow$$

$$0 \le R_{series} + R_{virt} \le 2\cdot R_{series} \leftrightarrow 0 \le R_{int} \le 2\cdot R_{series}$$

It is reminded that R_{int} is a function of SoC. Thus, the resistor R_{series} should fulfil the condition:

$$R_{series} \ge \frac{R^{max}_{int}}{2} \quad (6)$$

B. Voltage Feedback

Relation (6) can be used as a guide to select the appropriate value of R_{series} but if the expected value of R^{max}_{int} is high then the power loss in the emulation will be elevated. An alternative implementation is to feed back the voltage V_{hut} instead of the current I_{hut} from the hardware to the software part as presented in Fig. 9.

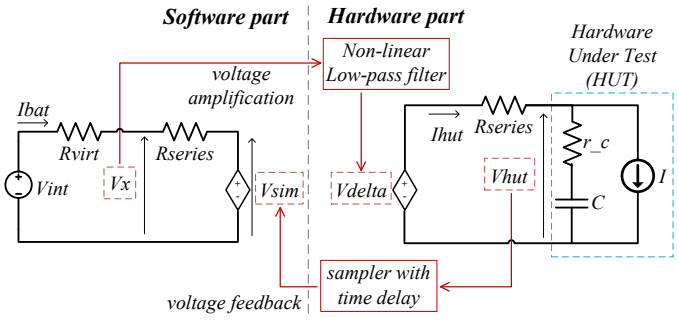

Fig. 9. The model of the Power HILS setup for operation in voltage feedback loop.

For the case of an ideal voltage source in the hardware part, V^n_{hut} is given as:

$$V^n_{hut} = \frac{V^n_{Delta}\cdot r_c + V_C\cdot R_{series} - I\cdot R_{series}\cdot r_c}{R_{series} + r_c} \quad (7)$$

The equation estimating the voltage source value V^n_{Delta} is:

$$V^n_{Delta} = V^n_x = V^n_{sim}\frac{R_{virt}}{R_{virt}+R_{series}} + V_{int}\frac{R_{series}}{R_{virt}+R_{series}} \leftrightarrow$$

$$V^n_{Delta} = V^{n-1}_{hut}\frac{R_{virt}}{R_{virt}+R_{series}} + V_{int}\frac{R_{series}}{R_{virt}+R_{series}} \quad (8)$$

Substituting (8) into (7), the final equation for V^n_{hut} becomes:

$$V^n_{hut} = V^{n-1}_{hut}\frac{R_{virt}\cdot r_c}{(R_{virt}+R_{series})\cdot(R_{series}+r_c)}$$

$$+\frac{V_{int}\cdot R_{series}\cdot r_c + V_C\cdot R_{series}\cdot(R_{virt}+R_{series}) - I\cdot R_{series}\cdot r_c\cdot(R_{virt}+R_{series})}{(R_{virt}+R_{series})\cdot(R_{series}+r_c)} \quad (9)$$

In order to achieve stability, inequality (10) must be fulfilled:

$$\left|\frac{R_{virt}\cdot r_c}{(R_{virt}+R_{series})\cdot(R_{series}+r_c)}\right| < 1 \quad (10)$$

If $R_{series}<R^{min}_{int}$ then $R_{virt}>0$ and the inequality (10) is always valid. For $R_{virt}<0$, we can substitute $R_{virt}=-|R_{virt}|$. Provided that $R_{series} \gg r_c$, (10) becomes:

$$R_{series}\cdot(R_{series} - |R_{virt}|) + r_c\cdot|R_{virt}| > 0 \quad (11)$$

$$\text{and } R_{series}\cdot(R_{series} - |R_{virt}|) + r_c\cdot(R_{series} - 2\cdot|R_{virt}|) > 0 \quad (12)$$

The simplest way to ensure that both (11) and (12) are fulfilled is to select:

$$R_{series} \ge 2\cdot|R_{virt}| \leftrightarrow R_{series} \ge -2\cdot R_{virt} \leftrightarrow$$

$$-2\cdot R_{series} + R_{series} \ge -2\cdot(R_{virt}+R_{series}) \leftrightarrow$$

$$R_{series} \le 2\cdot R^{min}_{int} \quad (13)$$

C. Simulation Results

Examples of how the type of the feedback loop chosen and the selection of R_{virt} and R_{series} affect the Power HILS behaviour are shown in Fig. 10. In the simulations shown, the circuit parameters used are V_{int} = 45 V, R_{int} = 5 Ω, r_c = 0.2 Ω, C = 1mF with a 2-μs sampler. The pulsed current load is the one shown in Fig. 10a with a frequency of 20 kHz and a duty cycle of 50%. Fig 10b shows the ideal HUT input current. In Fig. 10c the distortion caused by the current feedback can be seen but the system remains stable because the inequality (6) is fulfilled. On the contrary, in Fig. 10d in which (6) is violated the system is unstable. Fig. 10e and Fig. 10f present operation with voltage feedback.

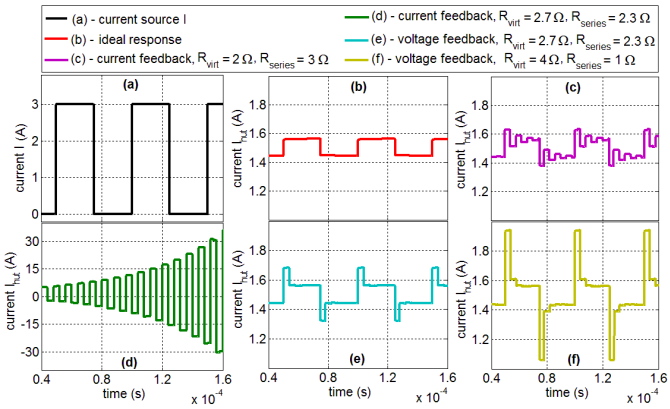

Fig. 10. Simulation results of the Power HILS systems shown in Fig. 8 and 9 ignoring the non-linear low-pass filter. The circuit parameters chosen are V_{int} = 45 V, R_{int} = 5 Ω, r_c = 0.2 Ω, C = 1 mF and with a 2-μs sampler. Part (a) shows the current source waveform while parts (b) to (f) show the HUT current I_{hut}.

V. Behaviour of the Non-Ideal System

A. Voltage Source operating like a Low-Pass Filer

The analysis shown in Section IV assumes that the hardware voltage source is ideal. However, as explained in Section III/B, the device used to implement the voltage source has a behaviour resembling a low-pass filter. In order to investigate the result of this behaviour, a set of simulations is conducted similar to those of Section IV with the only difference that the voltage source of the hardware part operates like a first order low-pass filter. The simulation results for current feedback mode with selected values R_{virt} = 4.5 Ω and R_{series} = 0.5 Ω are shown in Fig. 11. According to (6), this selection would result in an unstable system if an ideal voltage source were used but now, that the voltage source has a low-pass filter behaviour, it can be seen that the whole system is brought into stability.

B. Effect of a Low Sampling Frequency in the Current Feedback Loop

In all the simulations shown so far, the feedback sampler is 2 μs meaning that its frequency is significantly higher than the current source frequency of 20 kHz. However, in practice, it is possible to encounter real-time platforms with a sampling frequency lower than the one of the current source. Some examples are shown in Fig. 12 where the sampler time step is 61 μs, much longer than the 2 μs used until now. As expected, a slow sampler deteriorates the system stability. When the voltage source cut-off frequency is 2 kHz it is found that the system is unstable. For lower frequencies, an oscillating behaviour is observed the amplitude of which falls when the cut-off frequency is further reduced as shown in Fig. 12. These oscillations of Fig. 12b resemble a lot those found experimentally and shown in Fig. 4.

VI. Experimental Verification

The simulation results of Fig. 12 can also be observed during the experiments. Fig. 13a to 13c show the measured current I_{hut} flowing from the BE to the HUT for the current feedback model topology of Fig. 8. The circuit parameters used are V_{int} = 45 V and R_{series} = 0.47 Ω while the sampling frequency is 25 kHz. In Fig. 13a the connected sink resistor is R_{sink} = 20 Ω and the virtual resistance is R_{virt} = 3.5 Ω. According to the findings of Section IV, the system should have been unstable. However, this does not happen due to the low-pass filter behaviour that the Delta Elektronika power supply has. In Fig. 13b the virtual resistance is increased to R_{virt} = 4.8 Ω and the system starts oscillating. This happens because the voltage changes demanded by the software part are so big that even with the presence of an equivalent low-pass filter, they cannot be suppressed. A similar behaviour is observed in Fig. 13c where the virtual resistance takes the previous value of R_{virt} = 3.5 Ω but the value of the current sinking resistor is increased to R_{sink} = 10 Ω. This increase allows the output capacitor of the Delta Elektronika power supply to discharge faster. As a result, the voltage transitions are also faster meaning that the equivalent cut-off frequency has been increased. On the contrary, in Fig. 13d where the Power HILS operates in a voltage feedback mode as shown in Fig. 9, there are no oscillations, even if the chosen resistive values are R_{sink} = 10 Ω and R_{virt} = 4.8 Ω.

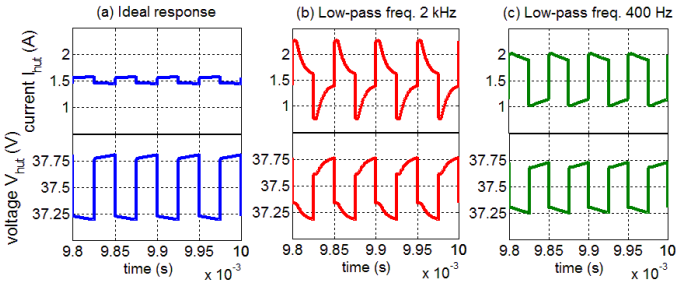

Fig. 11. Simulation results of the Power HILS system with current feedback as shown in Fig. 8 assuming that the hardware voltage source operates like a first order low-pass filter. The circuit parameters are V_{int} = 45 V, R_{int} = 5 Ω, R_{virt} = 4.5 Ω, R_{series} = 0.5 Ω, r_c = 0.2 Ω, C = 1 mF and with a 2-μs sampler.

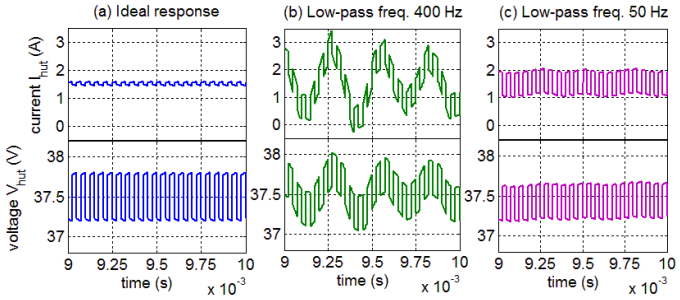

Fig. 12. Simulation results of the Power HILS system with current feedback as shown in Fig. 8 under the same conditions with those of Fig. 11 except for the current feedback sampler which has a step of 61 μs.

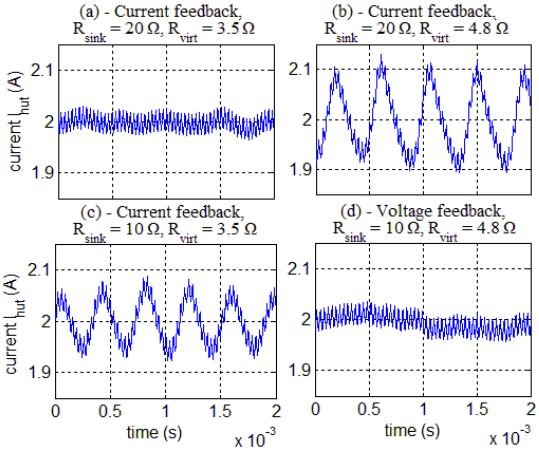

Fig. 13. Experimental results of the current I_{hut} flowing from the BE to the half-bridge converter of Fig. 2. In all the experiments V_{int} = 45 V, R_{series} = 0.47 Ω and the sampling frequency is 25 kHz.

Stable behaviour seems easier to be achieved in a voltage feedback configuration since it is enough to select a low value for R_{series}. However, if the experiment of Fig. 13d is repeated using $R_{series} = 0.2\ \Omega$ it is found that even low noise levels in the measurement of V_{hut} can cause important inaccuracies in the reference voltage estimation. It appears then that (13) is valid for ideal systems but in noisy experimental conditions the value of R_{series} cannot be too low.

VII. Related Work

The problem of stabilizing the power interface in a Power HILS has been studied in the past and several methods have been proposed. In [3], a comparison of five different interface algorithms is presented to provide a guide on how to select the type of signals to be transmitted and the method to process them. The current feedback method used in the present paper can be seen as an expansion of the ideal transformer model (ITM) shown in [3] while the voltage feedback topology is similar to the partial circuit duplication (PCD) method of [3] as it is modified in [8]. Where the present work differs is in applying these configurations for the special case of a HUT operating as a pulsed current load in parallel with a non-ideal capacitor. A third technique described in [3] is the damping impedance method (DIM) which introduces a damping resistor z^* in the software part of the emulator and utilizes both current and voltage feedback. This method is a combination of ITM and PCD and provides superior performance in terms of stability and fidelity, provided that the value of z^* is close to the impedance of the HUT [3, 9]. This requirement increases the implementation complexity of the BE and hence it is not implemented in the present paper. Examples of how DIM can be applied in practice with the value z^* being updated during the emulation are demonstrated in [10] and [11].

The five interface algorithms shown in [3] are tested with simulations in [12] where the HUT is a buck converter. The simulated layout is similar to the one studied here with the difference that there is no capacitor connected in parallel to the input terminals of HUT. Thus, the phenomena analysed here do not occur. An example of the ITM method being applied in battery emulation is presented in [13]. In that study, the HUT used is a current source with a parallel resistor which is connected to the BE through a series resistor similarly to the implementation of the present paper. However, no details are given on how the series resistor value is selected. Finally, a different and holistic approach on using a BE in a PHILS environment is proposed in [2]. In the method presented there, the models of the battery, the BE and the HUT are combined in one configuration and model predictive control (MPC) is used to achieve robust impedance control of the whole system.

VIII. Conclusion

Replacing the battery pack with a BE in a Power HILS facilitates the experimental procedure but due to the highly interactive behaviour of the full system, the observed dynamics will possibly be different to those of a real battery pack. In this paper, two methods of implementing a BE have been investigated. In both of them, the emulator consists of a power supply operating in voltage control mode in series with a resistor R_{series}. In the first case, the current flowing from the BE to the HUT is fed back to the real-time platform to estimate the reference voltage of the power device. This implementation is stable if $R_{series} \geq R_{int}^{max}/2$, where R_{int}^{max} is the maximum expected value of the battery model series resistance. In the second method, it is the voltage of the HUT that is fed back to the real-time platform and the condition that has to be fulfilled is $R_{series} \leq 2 \cdot R_{int}^{min}$, where R_{int}^{min} is the minimum expected value of the battery model series resistance. Both the simulations and the experiments have shown that in a current feedback configuration, the BE is possible to operate smoothly even if the condition stated above is violated. This happens due to the low-pass filter behaviour that the chosen power supply has. However in that case, current and voltage oscillations are possible to occur if the sampling frequency of the current feedback loop is lower than the load switching frequency.

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