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Transient Thermoreflectance for Gate Temperature Assessment in Pulse Operated GaN-based HEMTs

Sara Martin-Horcajo, James W. Pomeroy, Benoit Lambert, Helmut Jung, Herve Blanck, and Martin Kuball

Abstract— An experimental method to measure the gate metal temperature of GaN-based HEMTs is demonstrated. The technique is based on transient thermoreflectance measurements performed from the backside of the device. The thermoreflectance coefficient of the gate metal was calibrated by correlating the relative change of its optical reflectivity with the temperature change measured in the GaN layer using time-resolved Raman thermography during the device cooling transient. Simulated temperature transients were in good agreement with the experimental data. The main advantage of this new method is that it enables the direct assessment of gate metal temperature under device pulsed operation regardless of the device design.

Index Terms—GaN, HEMT, self-heating, time resolved Raman thermography, transient thermoreflectance, gate temperature

I. INTRODUCTION

GaN-BASED high electron mobility transistors (HEMTs) have attracted the attention of the research community because of their excellent properties for microwave-frequency and power applications [1, 2]. These properties include a high sheet carrier concentration, high mobility, and high critical electric field. High power applications require high power densities in the active region of these devices, which leads to highly localized Joule self-heating and potentially high peak temperatures [3, 4]. Commercial applications now exist for GaN HEMTs, often operated in pulsed mode, although performance is typically de-rated for the purpose of thermal management and maintaining channel temperatures within a safe operating area, in particular, avoiding thermally activated degradation of the gate Schottky contact [5]. For this reason, it is essential to use a high spatial and temporal resolution method for device temperature evaluation in pulse operated GaN HEMTs, aiding device design and reliability assessment

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[6]. Several techniques have been proposed for device temperature estimation [7]. Electrical methods [3-4, 8] are non-invasive, fast, straightforward, and only require standard electrical characterization equipment. However, they may underestimate the channel temperature because the results are averaged over the entire device area. Moreover, the results may be influenced by charge trapping effects [9].

Physical contact techniques, such as scanning thermal microscopy [10], enable high resolution temperature mapping with a potentially high spatial resolution. Their main drawbacks are that quantifying the thermal contact resistance between tip and device surface can be challenging, and also that the active device layers are buried under a relatively thick low thermal conductivity surface passivation layer.

Optical methods, in particular micro-Raman thermography [11] as well as thermoreflectance [12], have proven to be powerful techniques for the thermal analysis of devices, providing high spatial resolution temperature analysis; optical access to the device is required for these techniques. Whereas micro-Raman thermography provides the depth-averaged temperature through the GaN layer, thermoreflectance measurements probe the temperature of the metal surfaces including contacts; Raman thermography can also measure the surface temperature by using micro particle thermometers [13]. The limitation of measuring the surface temperature (e.g., on top of field plates or passivation layers) or the depth averaged GaN temperature, is that the temperature at these locations may be lower than the actual peak gate temperature, which is the most relevant for mean time to failure (MTTF) assessment. Therefore, thermal models must be used to extrapolate from the measured temperatures to the actual peak temperatures, introducing some uncertainty. A direct measurement of the gate temperature would offer distinct advantages.

In this letter, we propose a novel procedure to evaluate the gate metal temperature during pulsed device operation, which is based on transient thermoreflectance measurements performed from the transparent backside of the device, combined with time-resolved Raman thermography for calibration of thermoreflectance coefficients.

II. EXPERIMENTAL DETAILS

The thermoreflectance technique is based on the fact that

the optical reflectivity of a material changes with surface temperature. The temperature-induced optical reflectivity variation (ΔR) can be defined as [14]:

$$\frac{\Delta R}{R} = K \cdot \Delta T \quad (1)$$

where R is the mean optical reflectivity, ΔT corresponds to the temperature change, and K is the thermorefectance coefficient which depends on the material and wavelength of the reflected light [15, 16]. Therefore, it is crucial to know accurately the K value of the gate metal but its extraction is not trivial. In the literature, the extraction of K consists of placing the device in a temperature controlled stage and recording the change in reflectivity while the temperature is simultaneously monitored with a thermocouple [12]. However, this procedure has some disadvantages. For instance, the stage can move during the heating process introducing some error in the reflectivity measurement for a small gate metal, requiring larger test structures therefore; considering that the typical values of K are small, e.g., $-2.36 \cdot 10^{-4} \text{ } ^\circ\text{C}^{-1}$ for bare gold at 530 nm [17], and even smaller for other metals used for gate contacts, these measurements have a large error bar in themselves.

Single finger AlGaIn/GaN/SiC HEMTs with source-field plates were used for this study, as shown in Fig. 1. They are 100 μm -wide with a 0.5 μm long T-gate, 1.5 μm gate-source spacing, and 4 μm gate-drain gap. A 532 nm CW laser (2nd harmonic of Nd:YAG) was used as a probe beam to monitor the reflectivity change in the time domain. A Zeiss LD Plan-Neofluar 63x0.75 objective lens with spherical aberration correction was used to focus the laser beam spot onto the gate foot with diameter of about 0.5 μm , similar to the gate foot size. A beam splitter was used to sample the reflected beam intensity, mostly coming from the gate foot, which was recorded using a 200MHz bandwidth silicon photodiode and transimpedance amplifier connected to a digital oscilloscope; each measurement takes ~ 2 minutes. It is worth to mention that the dominant reflection occurs at the gate metal/AlGaIn interface, whereas the Fresnel reflection coefficients at the semiconductor interfaces are lower due to small refractive index contrast ($n_{\text{AlGaIn}} \sim 2.4$, $n_{\text{GaN}} \sim 2.4$, and $n_{\text{SiC}} \sim 2.7$), making this measurement most sensitive to the temperature variation at the gate foot. V_{GS} was pulsed from -3 V (below its threshold voltage) to 0 V with a period of 25 μs , and a 55% duty cycle, while a constant DC voltage (from 25 V to 62.5 V) was applied to the drain.

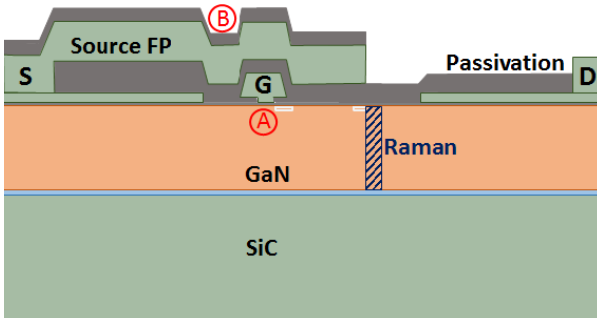


Fig. 1. Schematic cross-section of the studied AlGaIn/GaN-on-SiC HEMT, showing the area in the GaN layer measured by Raman thermography. Position A and B correspond to the locations where backside and topside thermoreflectance measurements were performed.

In order to extract the K value of the gate foot metal, we exploit the fact that after some time in off-state, which we call equilibrium time (t_{eq}), the average GaN temperature close to the gate is equal to the average gate foot metal during the cooling transient. This equilibrium time, which can be deduced from previous experimental studies performed [18], is in the range of 150 ns-250 ns depending on the thickness of the GaN layer. Finite element (FE) thermal simulations were performed to confirm the t_{eq} value. Thermal conductivity parameters of 160 W/m·K ($T^{-1.4}$ temperature dependence) for GaN, 440 W/m·K ($T^{-1.1}$ temperature dependence) for SiC, and 1 W/mK for the passivation layer were used for the simulations [19]. The thermal model was validated using time-resolved micro-Raman thermography (inset of Fig. 2). From Fig. 2 it was verified that t_{eq} was ~ 250 ns. $\Delta R/R$ measured pulsing V_{GS} was correlated with the Raman measured ΔT after 250 ns in off-state (see Fig. 3).

Then, applying Eq. (1), the K value was extracted as the linear fit slope of the $-\Delta R/R$ signal versus Raman measured ΔT in off-state taking into account the error of Raman measurements $K = (-5.0 \pm 0.2) \cdot 10^{-4} \text{ } ^\circ\text{C}^{-1}$ (inset of Fig. 3). This procedure was repeated for different V_{DS} (from 37.5 V to 62.5 V) and for different devices obtaining K values with smaller difference between them than the uncertainty of the extracted K value, as expected.

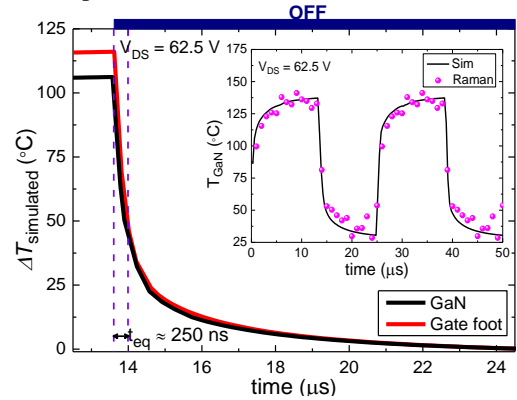


Fig. 2. Comparison of GaN and gate foot simulated temperatures during the device cooling. Good agreement between Raman determined average GaN temperature and simulation is shown as an inset, illustrating the correctness of the thermal model.

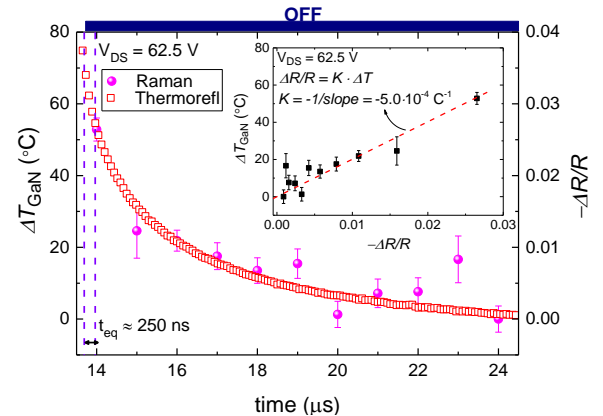


Fig. 3. Raman measured ΔT and $-\Delta R/R$ signal as a function of time when the device is in off-state. The inset shows the extraction of the K value as the linear fit slope of the $\Delta R/R$ signal vs the Raman measured ΔT .

III. EXPERIMENTAL RESULTS AND DISCUSSION

Fig. 4 presents the determined gate foot metal temperature rise (ΔT_{gate}) as a function of time obtained for different drain voltages when the device is V_{GS} -pulsed. Good agreement was observed between the measured and simulated average gate foot temperatures with no need of adjusting any parameter in the thermal model. This confirmed the validity of this new method for the direct and independent measurement of the gate temperature in pulse-operated HEMTs. Therefore, simulations are not required either for the evaluation of gate temperature or for the K calibration. The small difference between the experimental and the simulated ΔT profiles, which were also observed between Raman measured and simulated average GaN ΔT profiles (see inset of Fig. 2), may be due to the presence of a greater thermal resistance than the assumed between the gate and the GaN layer. The temperature error when measuring ΔT_{gate} is $\pm 4\%$, taking into account the estimated error in the extracted K value, which is mainly due to the uncertainty of the Raman measured temperature used during the K calibration.

This technique can be applied to either on-wafer devices or special packaged devices with optical access to the semiconductor chip. However, the simplest approach is usually to perform the measurements for on-wafer devices and carry out complementary measurements to extrapolate to packaged devices since the heat sinking configuration will be somewhat different.

The procedure used here for the calibration of K shows advantages over commonly used methods; it does not rely on measuring DC thermal reflectivity changes and can be performed for the sub-micron wide gate contacts; and the obtained K value is valid from device to device across the wafer.

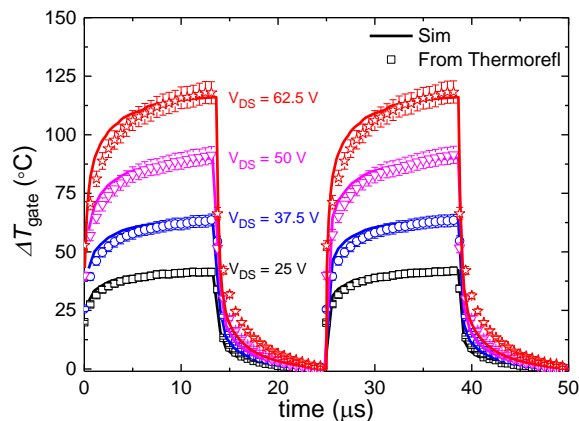


Fig. 4. ΔT gate foot metal as function of time determined from the thermoreflectance measurements for a HEMT operating under different V_{DS} . Simulations were included for validating the experimental technique.

Self-heating leads to reduced device performance and may result in a device failure due to contact degradation [5, 20]. In fact, Schottky contact is the most likely cause for temperature-induced permanent degradation [5, 21]. Thus, knowing gate metal temperature, is essential for reliability purposes. Generally, gate metal temperature can be determined by Raman thermography, but when field plates or air-bridges are present this requires FEM models to extrapolate the gate metal temperature from the Raman thermography measured average

GaN temperature. As Fig. 5 illustrates, the backside thermoreflectance (location A in Fig. 1) measured temperature is very close to the predicted gate foot ΔT , whereas the Raman GaN measured temperature is a good approximation, but underestimates by 9% in this case without extrapolation. Standard topside thermoreflectance measurements, e.g., on the field plate (location B in Fig. 1) provide a ΔT half that of the actual gate metal temperature [22]. This is due to the low thermal conductivity of the dielectric layer between gate and field-plate [13]. Backside thermoreflectance provides thus a fair approximation for the maximum gate temperature for MTF assessment (see Fig. 5). Moreover, the obtained gate temperature can be used as a boundary condition for the refinement of FEM thermal model for the determination of the maximum channel temperature. In addition to this, the combination of Raman thermography and both topside and backside thermoreflectance would enable an exhaustive device thermal mapping, which may provide relevant information for the improvement of the thermal management.

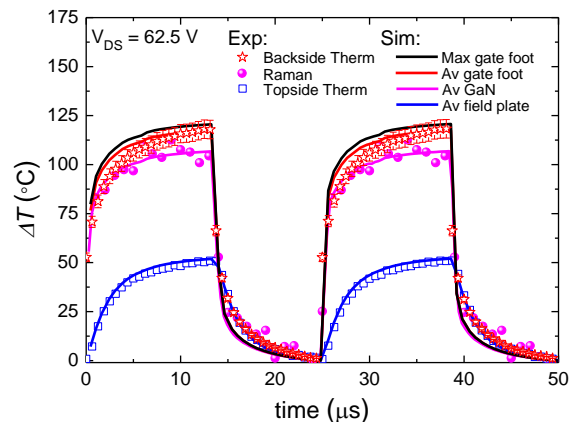


Fig. 5. Comparison of ΔT as a function of time at different device locations: in the GaN, at gate foot metal, and at the source field plate surface on top of the gate contact.

IV. CONCLUSION

We have demonstrated a novel thermoreflectance-based procedure for the direct measurement of the gate metal temperature in pulsed-operated HEMTs. This method requires the extraction of the thermoreflectance coefficient of the gate metal, which can be performed by correlating the $\Delta R/R$ signal with the ΔT measured by Raman thermography during the device cooling down process; this calibration only needs to be done once per device fabrication process. Its main advantage is a generic method enabling rapid assessment of the transient gate metal temperature regardless of the device design, without relying on thermal simulation.

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