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An Ultra-Wideband Digitally Programmable Power Amplifier with Efficiency Enhancement for Cellular and Emerging Wireless Communication Standards

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***Abstract*— The design and measurements of a fabricated novel digitally programmable wideband power amplifier (PA) are presented. The PA is made suitable for use in all communication standards, including GSM, 3G, LTE and Femto-cells, offering a bandwidth of several octaves covering presently 300MHz to 3.5GHz. It meets power, efficiency and linearity specifications. The amplifier showed excellent performances. The uniquely linear and high power SONY GaAs J-PHEMT process along with novel output-stage multiple cascode topology structure are discussed. This enabled a distinctive larger output impedance and power and low voltage operation. The output stage offered 15-20dB of gain without a driver. The circuit requires only little output or input matching for gain or impedance, depending on the application. In order to obtain higher gain and optimal application specific performance, a driver stage was added on the same die. A digitally programmable tuning chip was incorporated to the solution to optimize the performance for large bandwidths exceeding 40%. For smaller bandwidths no digital tuning was required. Digital pre-distortion algorithm was tested for better linearization. To the best knowledge of the authors, this is the first comprehensive plug-and-play solution for multi-band and multi-mode handset transmitters with the single chip one PA.**

***Index Terms*— Mobile Terminal, Power Amplifier, Digital Predistortion, Linearisation, efficiency, PHEMT, 3G, 5G, GSM**

I. Introduction

THE ability to provide good roaming coverage to handset users, almost anywhere in the world, is becoming an essential service, much desired by users and mobile operators. Hardware and Standards challenges are still, however, slowing down the true full-scale implementation of this feature.

The latest Standard release of 3GPP covers spectrum allocations for Long Term Evolution (LTE) and its Advanced version (LTE-A), along with UMTS and GSM allocations [1]. It provides an international map for frequency allocations in various regions and countries round the world. It also recommends certain bands that can be used independently, or combined in a tabulated inter-band or intra-band contiguous mode using Carrier Aggregation (CA) [2].

The challenge is hence at the smart phone and data card levels. It is necessary to support simultaneous operation for all the required standards. These include systems with fixed spectrum, such as GSM, UMTS and HSPA. Add to these, are new systems with wide and spread spectrum allocations of variable bandwidths. To define the boundaries of interest, the 3GPP User Equipment (UE) radio technical specifications (Release 12) provides a detailed table of uplinks (handset transmit) and downlinks (handset receive) operating bands [3]. They span in spectrum from 699MHz to 3.80GHz, the total number of operating bands is at 44 with bandwidths that vary from 1.4MHz to 20MHz.

The handset now needs correctly tuned transmitters and receivers at all the specified operating bands one at a time for the fixed spectrum or combined with variable bandwidths for CA. Traditional narrowband power amplifiers (PA) have presented a good solution for fixed-spectrum systems. Single-band to Quad-band PAs with built-in tuning networks on chip or as part of a module containing the PAs, front-end antenna switching and filters are used today [4-5]. However, with the new LTE systems, the RF transmitter block must be able to adapt its bandwidth and have multiple central carrier frequency. What is in demand in fact, are high power high efficiency power amplifiers for GSM bands that are also very linear for LTE applications [6-7].

The result is a significant and challenging increase in the complexity of the RF front-end design. Solutions can be proposed, however, within the portable and mobile context, not every solution is a viable option. The increase in complexity is

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inevitably manifesting itself in the three worst scenarios for handset and chip designers: an increase in chip and module physical footprints, an increase in manufacturing costs and, user-noticed upsurge in the operational battery power demands.

Ideally what is being sought is that configurable multiband, multimode power amplifier that concurrently possesses high levels of power efficiency and linearity. It also needs to be compatible with various battery management techniques. It needs to meet all the technical and handset standards. Thus far, to the best search and knowledge of the authors, this product is still under development. A short literature review of examples of architectures that were recently published is presented next.

A reconfigurable output network for multiband power amplifier (PA) module was proposed in [8] for 3G UMTS handsets. Two separate InGaP/GaAs HBT MMIC power amplifiers (high band and low band) were used as part of the module. The switching between five various 3G UMTS frequency bands, ranging from 880M to1980M, for the two PAs was achieved using PIN diodes. The module uses a simple logic table that controls biasing points on the output matching networks. The authors reported a Power Added Efficiency between 39-43% across the five selected UMTS bands. The reported linearity at output power of 28dBm was -39dBc (c.f -33dBc specification value). This solution is quite large in footprint and number of used components. The two PAs used operated within 3G frequency bands and power levels. The use of PIN diodes has reduced the efficiency of the module.

In [9], an integrated multiband multimode switching-mode differential power amplifier was proposed in 90nm CMOS technology. The integrated PA module consists of input matching network, driver stage, the output stage, load network and auxiliary circuitry to increase output power and efficiency. Gain control was used to control the PA gain at back-off in order to boost the power-added efficiency (PAE). Measured PA peak PAE was best reported at 43% for an output power of 27 dBm. The high power gain was 22 dB at 1.97 GHz, at 2.8 V. The reported frequency range was, however, limited to 1.6G to 2.2G for output power that ranged from maximum of 27.5dBm down to 25.5dBm. In this rather complex design architecture, the RF devices are used in switching mode to improve efficiency. This, however, has drastic impact on the linearity of the PA. No data was reported by the authors on adjacent channel linearity.

A low- and high-power dual mode PA for LTE, with on-chip switch bias control was reported in [10]. It uses a switching technique to improve the efficiency at low output power. The PA was biased for class-AB operation to improve the linearity. A gain of 27dB was reported along with a PAE of 34.5%. The adjacent channel leakage ratio (linearity) was −31dBc, for the high power mode. The frequency range reported is, however, limited to 824-849MHz.

Another recently-popular design technique to improve the efficiency of multi-mode systems is using Envelope Tracking (ET). In [11], for example, a multimode and multiband power amplifier (PA) was reported. It uses a class-F amplifier to cover the range from 1.7–2 GHz. The linearity is improved by intermodulation-distortion fine tuning best point or sweet-spot tracking at the maximum output power level.

The PA and supply modulator was implemented using InGaP/GaAs heterojunction bipolar transistor and a 65-nm CMOS process. For LTE signal, the Envelope-Tracking (ET) PA delivers a power-added efficiency (PAE) of 33.3%–39% at an average power of 27.8 dBm across 1.7–2 GHz. For UMTS signal across 1.7–2 GHz, the ET PA performs a PAE and an ACLR of 40%–46.3%, and 39-42.5 dBc, respectively, at an average output power of 30.1dBm. Like in the previous cases, the optimization of the PA is focused at one band of frequency. Other ET techniques publications have been reported with similarly competitive performances [12-13].

Another design is based on tuning the output stage of an efficient switching CMOS class-E amplifier, meeting the 3G UMTS linearity demands at specific frequencies using Envelope-Elimination and Restoration (EER) techniques [14]. A triple-band, two-stage differential PA structure comprising wideband driver stage and a simple tunable cascode output power stage for 1.9GHz 3G and 1.8/2.6GHz LTE tuning only. The input of the driver stage and the two output stages are all connected baluns and transformers to match and shift from single ended to differential or vice-versa. This technique requires the use of large, high insertion loss, inductive transformers and needs to be embedded in a linearization loop.

The authors have made an earlier pioneering design for dynamic adaptive bias control, the original form for Envelope Tracking [15-16]. The design was a linear yet highly efficient power amplifier for multimode applications. It was based on a unique junction pseudomorphic high electron-mobility transistor (J-pHEMT) device. The highly efficient PA managed to meet the stringent GSM power and spectrum specifications. The design was then extended for variable envelope modulation scheme for enhanced data rates for global system for mobile communications evolution (EDGE). The authors managed to avoid the need for control loops and linearization schemes. The goal was to meet the required linearity and efficiency, as well as substantially reducing the RF complexity of a cellular handset.

In the above reviews of wideband multi-mode architectures for power amplifiers it was in general evident that compromises were made. Some designs are large and complex to the extent that a sizable Module was the only option to include the PA (or two PAs in some cases), the matching networks at the input and output and a linearity loop. In such cases hybrid CMOS and GaAs process was used. Furthermore, simpler designs were narrower in bandwidth (unless tunable and lossy matching networks were used) with the design optimized for one standard in particular. No clear solution that is truly concurrently wideband and multi-mode in the sense that it includes GSM, 3G and LTE in one single integrated PA was found. What this means is a power amplifier with a bandwidth span from 699MHz-3800MHz that meets high power and high efficiency needs for cases and also meets linearity demands.

The challenge, in the view of the authors, mainly lies in the circuit and device design of the output power stage of the amplifier. If this block can be made to meet the bandwidth,

power efficiency and linearity demands, then this will result in a reduced footprint and cheaper solution.

In this paper, the full potential of an improved release of the J-PHEMT process is explored. A novel power amplifier output stage is presented. It is unique in achieving a bandwidth that has been tested in small-signal gain from 400MHz to 4GHz. It has been fully tested for all major standards including GSM, 3G UMTS, LTE and FEMTO cells, without the need for any major tuning or output matching networks. This unique design presents output impedance close to 50Ω, hence requiring minimum to no matching at the output stage.

The power amplifier has been practically tested for its distortion characteristics. A digital pre-distortion algorithm was subsequently developed for this PA. The full system comprising the multiple-cascode output stage, a driver gain stage and digital predistorter was tested, showing much better improvement in its linearity in-band and out-of-band characteristics.

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II. Design Concept and Architecture

A. Device Design

The Junction Pseudomorphic High Electron-Mobility Transistor (J-pHEMT) exhibits several attractive and unique characteristics when compared to other GaAs devices such as standard HEMT and HBT technologies. These include a small and sharp VDS knee voltage and a much improved breakdown voltage. This extends the large-signal linear range of the device operation to wider voltage AC voltage. Furthermore, the device can be used at lower bias voltages, reportedly down to 1V. The device also enjoys a low channel resistance and comparatively very low standby leakage current, in the order of micro amps. Both characteristics improve the power efficiency performance of the amplifier with reported compressed-mode efficiency levels of up to 65% [17-18]. The success of the JPHEMT device in high power handset antenna switch applications [18] has allowed for the integration of high performance switches onto the same PA die. This has offered much needed area reduction in the handset RF front end.

B. The Cascode Amplifier

The common-source-common-gate (CS-CG) or Cascode topology has been used in classical microelectronics design for a while [19]. Figure one shows a simple configuration for this topology.

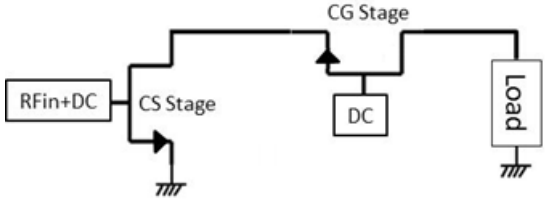

Fig. 1. The cascode amplifier

This topology is of significance for this work. It has been revisited and improved to suit our power amplifier application for multi-band and multi-mode operation. The advantages of the cascode topology have all however been retained if not improved. One of the best known benefits of a cascode stage (common-gate) is driven from its ability to extend the small signal gain over a much wider bandwidth, when compared to a common-source amplifier. This is mainly due to its ability to counter-balance and reduce the preceding common-source device Miller increase in the gate-drain parasitic device capacitance C_{gd}. The latter capacitance generates a frequency pole that causes the small signal gain to roll-down. The Miller increase in the C_{gd} capacitance for a stand-alone common-source amplifier with voltage gain $A_v = g_m R_{load}$ is given by:

$$C_M = C_{gd}(1 + A_v) \quad (1)$$

The increase in Miller capacitance will cause a decrease in the bandwidth of the amplifier. A common-gate (cascode) stage by design is a current buffer topology with unity current gain. The input impedance of the cascode can be simplified to, assuming a large output device resistance [19]:

$$Z_{in} = {}^{1}/_{g_m} \quad (2)$$

Hence, the cascode transistor, connected as a load to the drain of the common-source amplifier has the effect of eliminating the Miller effect regardless of the load impedance. This improves the operating frequency bandwidth of the device up to its physical limits (in this simple case the pole of Cgd). It turns out also that the output impedance of the cascode is quite large. In this paper, the amplifier cascodes were designed to have output impedance close to 50Ω. The topology also means that the unity current gain and the small Zin to large Zout transformation leads to significant voltage and power gain. This consequence was fully exploited in this work. In a typical two device cascode with identical size and gain properties, the small signal open loop voltage gain of the amplifier is given by [19]:

$$A_{vo} = \frac{v_o}{v_i} = -g_{m1} r_{o1} \times (1 + g_{m2} r_{o2}) \approx -g_{m1} r_{o1} g_{m2} r_{o2} \approx -g_m^2 r_o^2 \quad (3)$$

Where g_m is the small signal transconductance gain and ro is the transistor output impedance. With an output load much less in value to the output resistance of the amplifier, this gain value is actually much less than calculated. This design is also limited with voltage headroom limitation that impacts the gain of the amplifier. The use of cascode and double cascode topologies in power amplifier design, for CMOS and in GaAs technologies has been receiving increased interest in recent works [20-22].

C. Power Amplifier Design

The design of the power amplifier in this work relies on individually controlled three stacked transistor designed and fabricated on GaAs Junction-PHEMT technology. All the three devices were identical in size and layout. One device is connected in common source form, constituting the main amplifier. The other two are connected in cascode common gate. The topology of the design is depicted in Figure two.

Each device in this topology has its own DC feed. Typically the bias value is the same at 3.6V for most applications. However, the flexibility of the individual biasing proved useful for mobile GSM and basestation applications. In this case 5V were needed at the bias input of the third device (second cascode) to get the correct amount of high power and compressed mode efficiency requirements.

The inductors were used for AC blocking and for providing grounds to the sources of cascode devices. They are placed off chip. Typical value used on the board and in simulation was 18nH. The capacitors, however, were used for to ensure stability of design in the case of C3 and C4. Capacitors C1 and C2 were optimized by design to obtain maximum small signal gain.

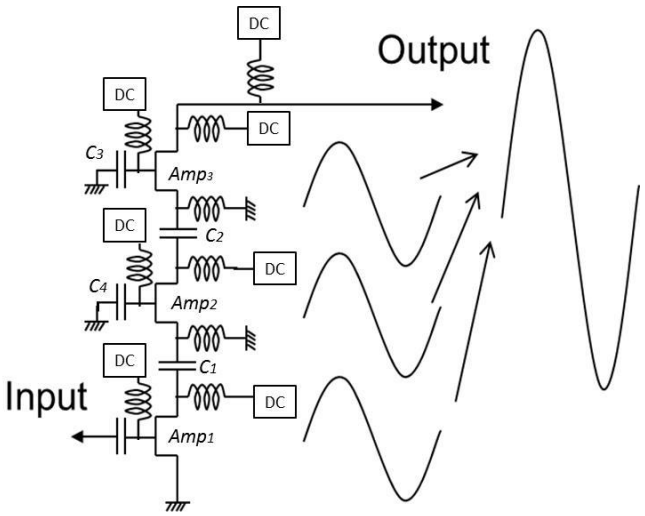

Fig. 2: Proposed 3 stacked cascode power amplifier

Each of the transistors 2 and 3 are current buffers but provide large power and voltage gain. The gain analysis will show this, however, during evaluation stages it was observed that the output swings of all the stages must be aligned in phase so they all add up constructively. In practice, device physical behavior is influenced by parasitic capacitances embedded within, but not fully modeled. Hence, C1 and C2 also provided some matching. The impact of these capacitors is analyzed later in this paper.

D. Double Cascode Gain Analysis

Nodal analysis was applied for the 3 stacked devices (output stage and double cascode). The small signal model of the amplifier was used [19]. The capacitors in Figure 2 were ac coupled for simplicity. The stage output current was also assumed to be zero given that an open circuit load was applied. The small signal model used for the gain derivation is given below in Fig 3.

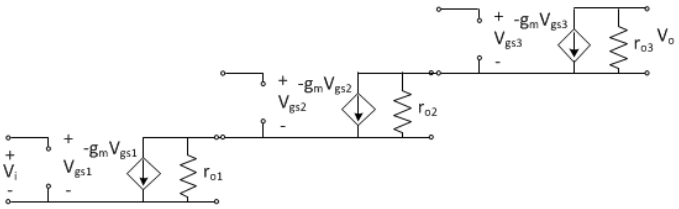

Figure 3 Small signal model of three stage cascode PA

For the third stage, applying nodal analysis yields:

$$\frac{V_O - V_2}{r_{O3}} + g_{m3} V g_{s3} = 0$$

Hence,

$$V_O = (1 + g_{m3}.r_{O3})V_2 \qquad (4)$$

For the second stage:

$$\frac{V_2 - V_1}{r_{O2}} + g_{m2} V_{gs2} \quad + i_{o2} = 0$$

Where i_{o2} is set to zero since the output load is an open and V_{gs2} is set to V_1, hence:

$$V_2 = V_1 (1 + g_{m2} r_{O2}) \qquad (5)$$

For the first stage, applying nodal analysis again:

$$\frac{V_1 - 0}{r_{O1}} + g_{m1} V g_{s1} - g_{m2} V g_{s2} + \frac{V_1 - V_2}{r_{O2}} = 0$$

But V_{gs1} equals V_i and V_{gs2} equals $-V_1$, hence

$$\frac{V_1}{r_{O1}} + g_{m1} Vi + g_{m2} V_1 + \frac{V_1 - V_2}{r_{O2}} = 0 \qquad (6)$$

This becomes:

$$V_1 \left(\frac{1}{r_{O1}} + \frac{1}{r_{O2}} + g_{m2}\right) + g_{m1} V_i - \frac{V_2}{r_{O2}} = 0 \qquad (7)$$

Substituting equations (1) and (2) in (4) yields after some manipulations:

$$\frac{V_O}{Vi} = -\frac{g_{m1}}{\left(\frac{1}{r_{O1}} + \frac{1}{r_{O2}} + g_{m2}}{(1 + g_{m3}.r_{O3})(1 + g_{m2}.r_{O2})} - \frac{1}{(1 + g_{m3}.r_{O3}).r_{O2}}\right)}$$

For the identical cascode devices used, $g_{m1} = g_{m2} = g_{m3}$ & $r_{O1} = r_{O2} = r_{O3}$, hence:

$$\frac{V_O}{Vi} = \frac{-g_m(1 + g_m r_O)^3 . r_O}{\left(\frac{2r_O}{r_O{}^2} + g_m\right)(1 + g_m r_O) r_O - (1 + g_m r_O)^2}$$

(8)

After further mathematical manipulations, the voltage gain comes out to be:

$A_{vo} = \frac{v_o}{v_i} = -g_m r_o \times (1 + g_m r_o)^2$

In equation (6), it is assumed that the three devices are of equal size and identical small signal properties. When compared to a typical two devices cascode, the amount of predicted maximum gain is clearly much higher. This advantage was successfully tested and exploited in this work.

The next analysis looks into the stability of the design in face of the feedback topology of a cascode as well as the added gain.

E. Cascode gate capacitors

While this design provides many advantages, its stability must be carefully observed due to its feedback nature and the high gain it provides. Therefore, the selection of capacitors C_3 and C_4 was based on ensuring gain stability across the entire bandwidth. In addition, given that we now have more stacked devices, the reverse isolation, with signals internally feeding back from the output to the input is much lower and very small values for (S_{12}) were measured. The analysis below is done for two devices, the cascode and the output amplifier for simplicity and was partially reported in [22]. This is shown in Figure 4.

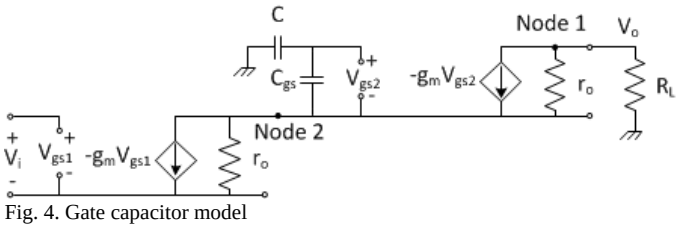

Fig. 4. Gate capacitor model

The sum of Zc and Zc_{gs} would be:

$$Z_{Cgs} + Z_C = \frac{1}{j\omega}\left(\frac{1}{Cgs} + \frac{1}{C}\right) = \frac{1}{j\omega}\left(\frac{C + Cgs}{CgsC}\right)$$

Applying voltage division for the voltage at gate 2, Vg2:

$$V_{g2} = \frac{Vds1}{Z_{Cgs} + Z_C} \times \frac{1}{j\omega C} = \frac{Cgs}{C + Cgs} V_{ds1}$$

To determine the value of the Vgs2 amplitude, we need the value of C

$$V_{gs2} = V_{g2} - V_{ds1} = \left(\frac{Cgs}{C + Cgs} - 1\right) V_{ds1}$$

And hence:

$$V_{gs2} = \frac{-C}{C + C_{gs}} V_{ds1} \qquad (9)$$

Define:-

$$C` = \left(\frac{-C}{C + Cgs}\right)$$

Applying nodal analysis at node 1

$$\frac{V_o}{R_L} = -g_m V_{gs2} + \frac{1}{r_o}(V_{ds1} - V_o) \qquad (10)$$

Therefore, using equation (9)

$$V_o = \frac{1}{\frac{1}{r_o} + \frac{1}{R_L}}\left(\frac{1}{r_o} - g_m C`\right) V_{ds1}$$

Define

$$R` = \left(\frac{1}{r_o} + \frac{1}{R_L}\right)^{-1}\left(\frac{1}{r_o} - g_m C`\right)$$

Applying the nodal analysis at node 2 (at V_{ds1})

$$g_m V_i + \frac{1}{r_o} V_{ds1} = g_m V_{gs2} + \frac{1}{r_o}(V_o - V_{ds1}) + j\omega C_{gs2} V_{gs2}$$

$$= g_m C` V_{ds1} + \frac{1}{r_o}(R` - 1) V_{ds1} + j\omega C_{gs} C` V_{ds1}$$

Hence,

$$V_i = \frac{1}{g_m}\left[\left(g_m + j\omega C_{gs}\right) C` + \frac{1}{r_o}(R` - 2)\right] V_{ds1} \qquad (11)$$

$$V_{ds2} = V_o - V_{ds1} = (R` - 1) V_{ds1}$$

Using equation 10, V_{ds2} then becomes:

$$V_{ds2} = \left(\frac{1}{r_o}+\frac{1}{R_L}\right)^{-1}\left[\left(\frac{1}{r_o}-g_m C`\right)-\left(\frac{1}{r_o}+\frac{1}{R_L}\right)\right]V_{ds1}$$
$$= \left(\frac{1}{r_o}+\frac{1}{R_L}\right)^{-1}\left[\left(\frac{g_m C}{C+C_{gs}}-\frac{1}{R_L}\right)\right]V_{ds1} \quad (12)$$

In the general cascode case, we can set a large value of C, this means $C_{gs}/C \to 0$; this simplifies equations (9) and (12) as follows:

$$V_{gs2} = \lim_{c\to\infty}\left(\frac{-C}{C+C_{gs}}V_{ds1}\right) = -V_{ds1}$$

This proves the unity gain of the cascode device. Also

$$V_{ds2} = \lim_{c\to\infty}\left[\left(\frac{1}{r_o}+\frac{1}{R_L}\right)^{-1}\left[\left(\frac{g_m C}{C+C_{gs}}-\frac{1}{R_L}\right)\right]V_{ds1}\right]$$
$$V_{ds2} = \left(\frac{1}{r_o}+\frac{1}{R_L}\right)^{-1}\left[\left(g_m-\frac{1}{R_L}\right)\right]V_{ds1}$$

In baising the device, we can make *Vi=Vgs1=Vgs2* by adjusting C`, and from (9) and (11)

$$C` = \frac{1}{g_m}\left[\left(g_m + j\omega C_{gs}\right)C` + \frac{1}{r_o}\left(R`-2\right)\right]$$

If g_m is much bigger than jwC_{gs}:

$$C` = \frac{1}{g_m}\left[\left(g_m C`\right) + \frac{1}{r_o}\left(R`-2\right)\right]$$

Therefore

$\frac{1}{r_o}\left(R`-2\right)$ = 0, and R`=2

Further, it can be shown:

$$V_{ds2} = \left(R`-1\right)V_{ds1}$$
$$V_{ds2} = V_{ds1}$$

For given specification defined output power requirements (GSM and LTE), the high gain of the amplifier meant that the input signal to the amplifier can be lower and the input swing can be reduced in amplitude.. This proved useful in this work in providing a more linear behavior for the PA.. The power amplifier managed to meet the linearity demands for 3G and LTE as well as the power and efficiency expected from a GSM PA. No source degeneration was needed in this design. The device has been practically checked for stable operation across load impedances up to 10:1 VSWR at all angles without oscillation issues. In addition, a simulation study was conducted on the stability of the PA at the load and the source. The study involved optimizing the values of the cascode capacitors against source and load stability circles and the gain. Figure 5 shows the source and load stability circles outside the smith chart with the optimized values of the gate capacitors. In Figure 6, the values of the gate capacitors were not optimized and the stability circles enter the smith chart indicating potential instability.

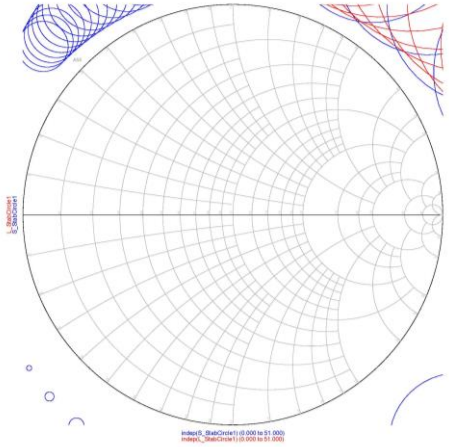

Fig 5 Stable operation of PA with optimized cascode capacitors values, all stability circles are outside the smith chart

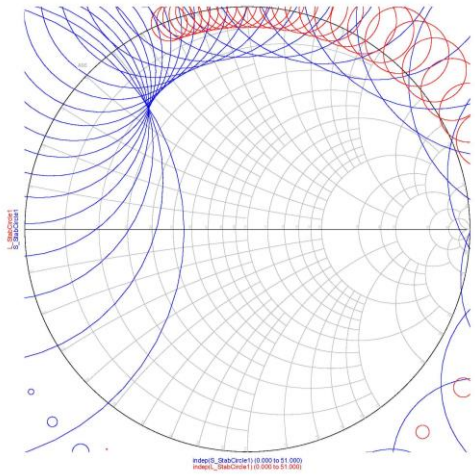

Fig 6 With un-optimized cascode gate capacitors values, showing potentially unstable operation of PA at certain loads

III. Chip Fabrication

The power amplifier was fabricated using Sony Junction-PHEMT GaAs process. Inter stage and stability

capacitors were also fabricated. No matching networks were needed on chip. In addition, a 2mm gate width driver input stage was added to the design. One of the advantages of cascode is higher gain, however, the additional driver stage was particularly important as we go to higher frequencies when the natural gain of the device decreases. Figure 7 shows the final layout of the fabricated power amplifier chip. The layout of the chip is made such that the two stages can be accessed as well as connected externally. All biasing inductors and blocking capacitors were external.

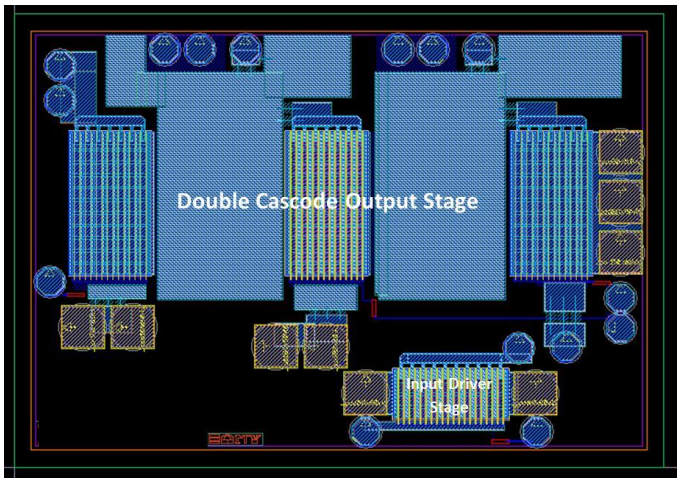

Fig. 7: Fabricated Power Amplifier chip

IV. Simulations and Measured Results of Output Stage

The power amplifier output stage was simulated using Advanced Design Systems (ADS) and tested in the lab under DC, small signal gain scattering parameters, compressed mode GSM and linear 3G and LTE modes. No device major output matching was needed given the high output impedance of the amplifier and its closeness to 50Ω. The levels of agreement between predicted simulation results and measured data were excellent. The properties of the Sony Junction PHEMT device process include high linearity and power handling capabilities. It also provides for excellent low insertion loss property. This relates to the unique properties of the gate junction [17]. A plot of the simulated DC characteristics for the device size used is shown in Figure 8. It shows good low knee voltage and high breakdown voltage (exceeding 18V). This allows for a better signal handling and a more linear behavior.

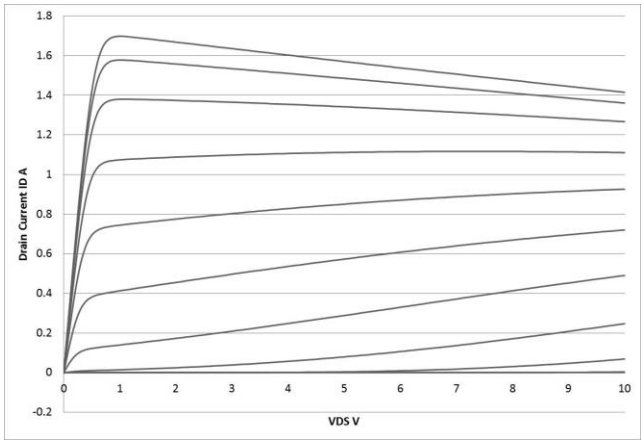

Fig. 8 Sony J-PHEMT simulated DC characteristics for the device used

For simulation purposes, the circuit schematic was built on ADS and the 3GPP test bench provided was modified for sweeping purposes and used for modeling. The device biasing was carefully considered according to the application. For 3G and LTE tests, all the three devices were biased at 3.5V and the gate bias was such that quiescent 30mA drain current was flowing within each device. Given the independent bias arrangement of the three devices, the total quiescent current was hence 90mA. For GSM, however, and in order to get the required high value of gain and power, the top cascode device was biased at 5V and the main amplifier and first cascode devices were biased at 3.5V. A standard booster circuit was used for this voltage up conversion. Figure 9 shows the simulation schematic used.

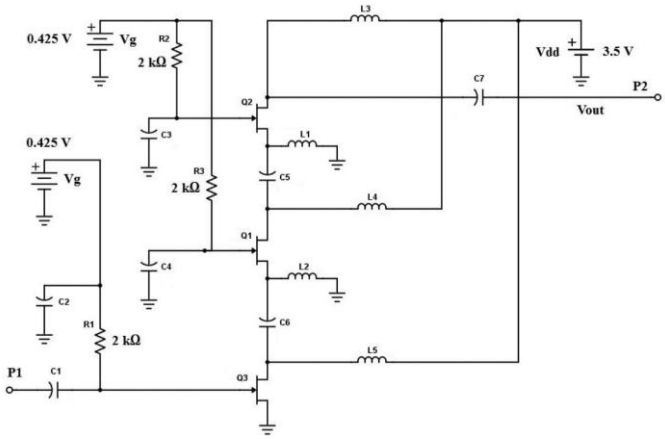

Fig. 9 Simulation schematic of PA

In Figure 10, on the other hand, the output stage evaluation board of the test chip while connected up is shown.

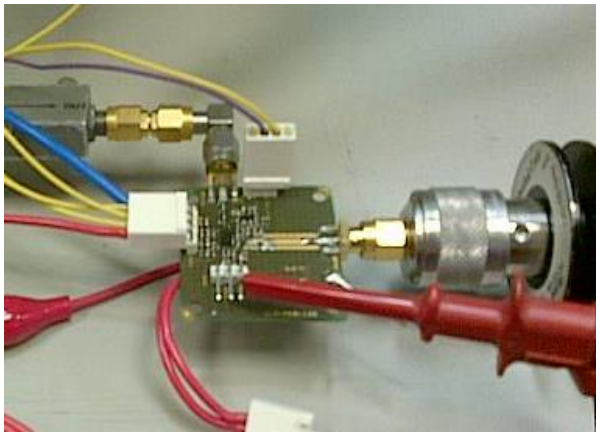

Fig. 10 picture of evaluation board

A. *Small signal results*

The small signal gain characteristic of the cascode output stage is shown in Figure 11. The measurements and simulations were performed from 400MHz to 4GHz. The 6dB/Octave gain roll off is visible as the frequency increases and this is due to normal internal parasitic effects within the device. When higher gain output is required, for example LTE at 3.8GHz, the driver stage was used to boost the gain.

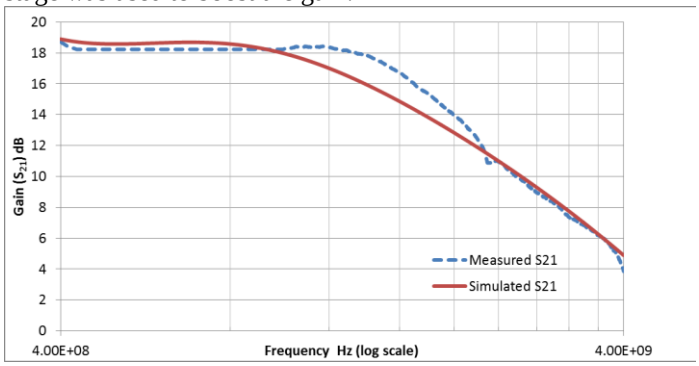

Fig. 11: Simulated versus measured small signal gain

B. *3G WCDMA Simulations and Measurements*

The power amplifier was tested under 3G WCDMA uplink conditions. Simple 50Ω matching was applied at the input and output. It was biased with supply voltage of 3.5V and the Quiescent current drawn from each device was around 30mA. The device was successfully tested for power output, gain, efficiency and linearity (upper and lower band ACPR) at 900MHz and 1800MHz. The plotted results shown below are for the 1800MHz while a summary is given in Table 1. Figure 12 shows the measured and simulated output power, Figure 13 shows the large signal gain while Figures 14 and 15 show the 5MHz lower and upper offset ACPR compared to the input power. The 5MHz upper offset shows similar results both simulated and measured. Measured Power Added Efficiency (PAE) versus input power is shown in Figure 16. All resulted show very good agreement between simulations and measurements. The input referred compression point P1dB was at approximately +13dBm.

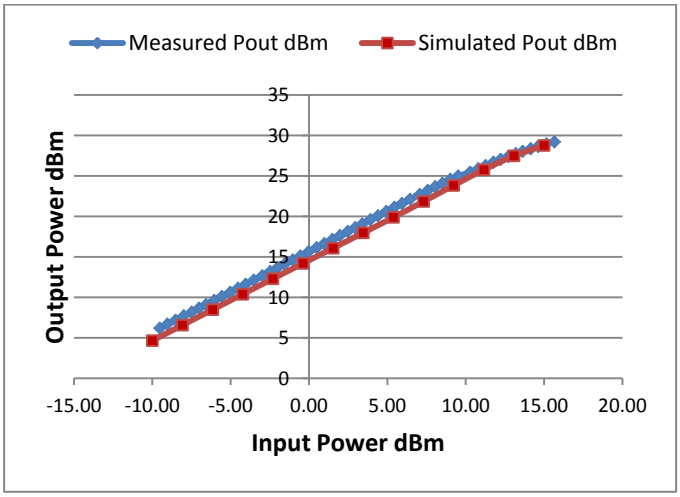

Fig 12: Power Characteristics under WCDMA conditions

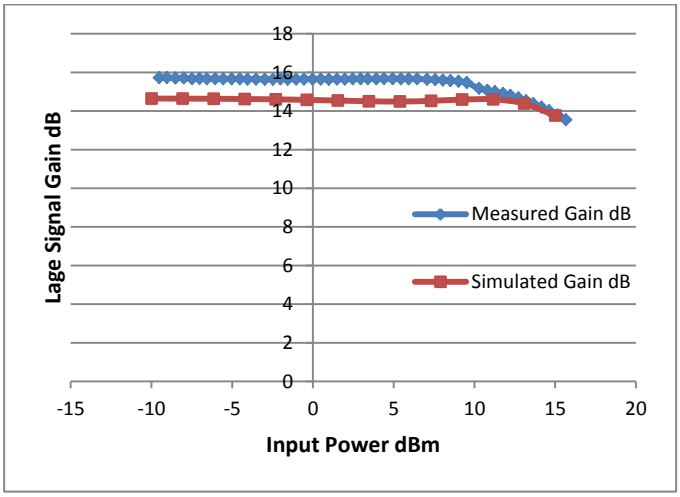

Figure 13 Gain versus Input Power for WCDMA signal

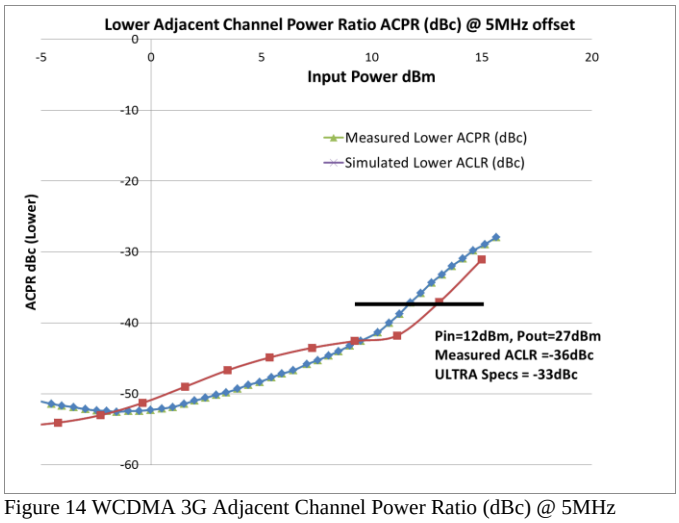

Figure 14 WCDMA 3G Adjacent Channel Power Ratio (dBc) @ 5MHz lower offset.

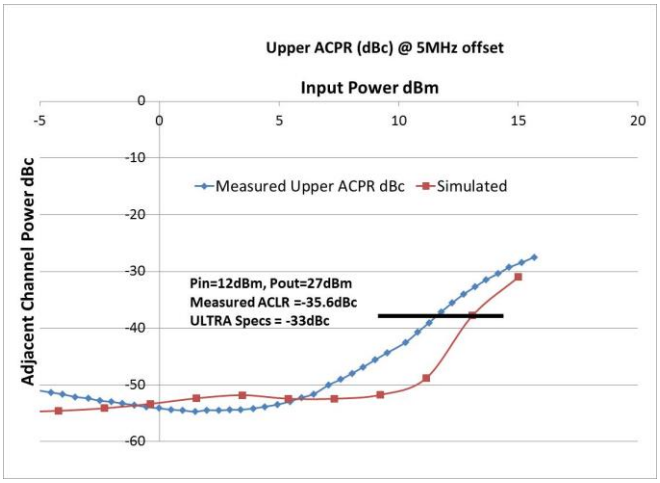

Figure 15 WCDMA 3G Adjacent Channel Power Ratio (dBc) @ 5MHz upper offset

The measured Power Added Efficiency (PAE) for the PA is shown in Figure 13 below.

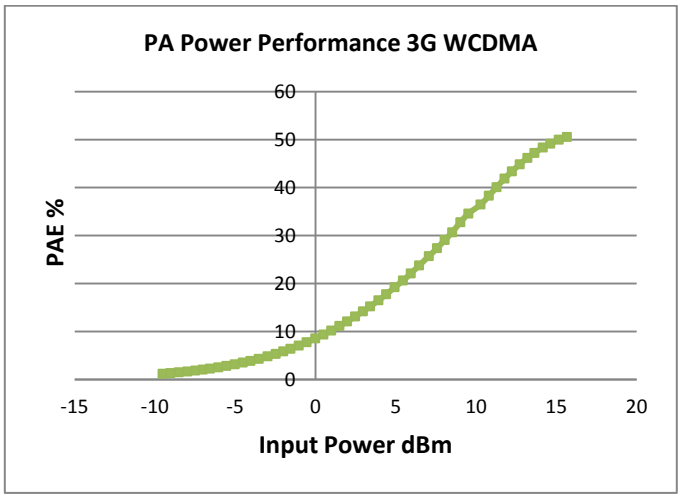

Figure 16 3G Power Added Efficiency PAE versus Input Power at 1800MHz

A summary table of the PA performance at important points at 900MHz and 1800 MHz is shown in Table 1. A good level of agreement is shown between simulation and measurements.

Efficiency calculations are highly dependent on the average currents drawn by the devices on the test board at the time of taking the measurements. Therefore, the levels of difference in the Power Added Efficiency PAE table are acceptable.

C. LTE Measurements

The same device with the same 50Ω input and output matching was tested for different LTE bandwidths and modulations. It met all necessary conditions for linearity and power as defined in the 3GPP standards. Table 2 summarizes the measured data at for different modulations and channel bandwidths at RF frequency of 890MHz. All resource blocks were loaded in this test. The PA was operated at 3.5V and the targeted output power and adjacent channel requirements were +27dBm and -33dBc respectively. The PA meets all the power and linearity needs assuming a 3dB post PA loss.

It is interesting to observe in Table 2 the effect of the bandwidth and modulation schemes on efficiency. The efficiencies of each bandwidth with the three different modulation schemes were averaged and plotted against LTE channel bandwidths. This is shown in Figure 17. It can be seen that the power amplifier efficiency seems to decrease as the single channel bandwidth increases. The reason for this is system related and is due to the increase in DC power dissipation as the bandwidth of the fully loaded channel increases. The class-AB output stage is close to its output referred compression point (P1dB) and to keep the same output power range and linearity with the complex multiple constellation peaks modulation involved, the DC power consumption had to increase. With this, the efficiency of the PA output stage decreases.

Table 1 3G WCDMA Measured versus Simulated Results

	Input Power dBm	Output Power dBm	ACPR +5MHz dBc	ACPR -5MHz dBc	PAE %
1800 MHz					
Simulated	12.5	27.32	-40.7	-39.0	41
Measured	12.3	27.3	-35.0	-34.8	44
900 MHz					
Simulated	9.5	29.33	-34.1	-34.0	43
Measured	9.2	29.69	-37	-36	37
Specifications requirements: -33dBc					

Table 2 Measured RF and Linearity PA perofrmanc FULLY LOADED resource blocks

Channel Bandwidth(MHz)	Modulation	Pout(dBm)	ACPRL(dBc)	ACPRU(dBc)	PAE(%)
20	64QAM	26.71	-33.1	-33.93	27.98
	16QAM	26.72	-33.39	-34.36	28.09
	QPSK	27.25	-33.54	-34.37	30.42
15	64QAM	26.69	-33.22	-33.84	28.14
	16QAM	26.71	-33.45	-34.26	28.46
	QPSK	27.25	-33.42	-34.09	30.76
10	64QAM	27.53	-32.88	-32.88	32.64
	16QAM	27.57	-33.25	-33.4	32.72
	QPSK	28.13	-33	-33.07	35.37
5	64QAM	27.55	-33.5	-34	32.98
	16QAM	27.58	-34.07	-34.68	33.13
	QPSK	28.14	-33.88	-34.18	35.73
3	64QAM	27.55	-33.27	-33.7	33.07
	16QAM	27.59	-33.79	-34.25	33.27
	QPSK	28.14	-33.51	-33.79	35.76
1.4	64QAM	27.92	-33.66	-33.83	34.94
	16QAM	27.95	-34.06	-33.92	35.05
	QPSK	28.48	-33.59	-33.83	37.79

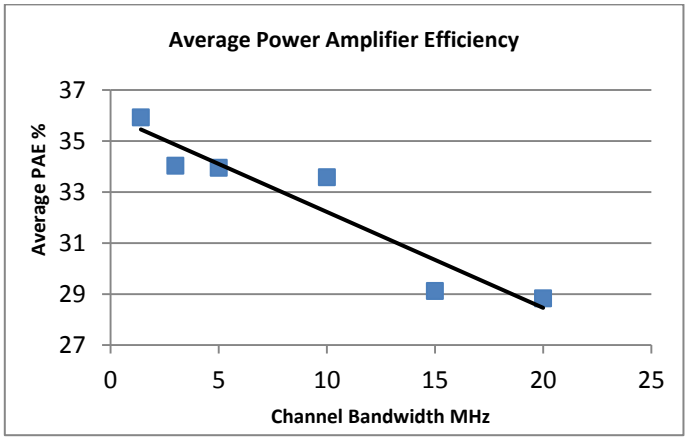

Figure 17 Averaged PAE versus 3G LTE channel bandwidth resource

D. GSM Measurements

GSM power amplifiers allow for compressed mode operation due to constant envelope nature of GMSK. This improves the efficiency of the PA at the expense of the linearity, now less important since no AM data content is present. However, the power demands are higher than other standards. To meet the requirement for higher power demand at GSMand for single stage PA, the top second cascode FET device, was biased at 5V. The other two devices, namely the RF and first cascode devices, remained biased at 3.5V. A DC-DC converter was used for this operation. No further matching or changes were needed.

Figure 18 below shows the measured output power and efficiency and large signal gain performances versus input power. All tests were conducted at 900MHz.

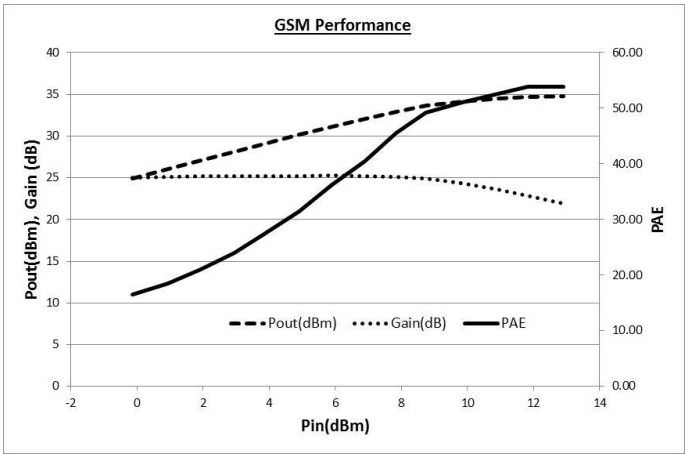

Figure 18 Efficiency and Output power versus input

From the graph it was deduced that the 1dB compression point of the PA was about +34dBm, referred to the output.

E. High Gain Programmable Operation Measurements

The larger bandwidth of the cascode output stage was useful in expanding the operation of the power amplifier to multiple standards. Various modulation schemes were also tested and the PA was shown to meet the linearity and efficiency requirements. However, the output stage, on its own, does not always meet the handset demand for power and voltage gain. The typical power gain of the output stage was around 16dBs.

This has presented a limitation on the applications of the device. To mitigate this challenge, a 2mm input driver stage was designed and built into the same chip. The chip layout for the PA was shown in Figure 7, including the input driver. The input stage provides an additional typical gain of 18-20dB at 800MHz, raising the overall gain of the PA to over 34dBs. The PA input and output impedances are close to 50 Ohms and tuning helps achieve better linearity and efficiency. To cover all applications using dedicated matching networks would not be a practical solution. Therefore, a novel system was developed to overcome the above. A digitally controlled programmable 5-bit series and 4-bit shunt Switchable Step Capacitor (SSC) controller was implemented on the PCB with an externally fixed value inductor, as shown in Figure 19.

The SSC is basically a Tuning circuit which contains internal switched capacitors and an external chip inductor to be used for impedance optimization across frequency at both the interstage and output of the PA

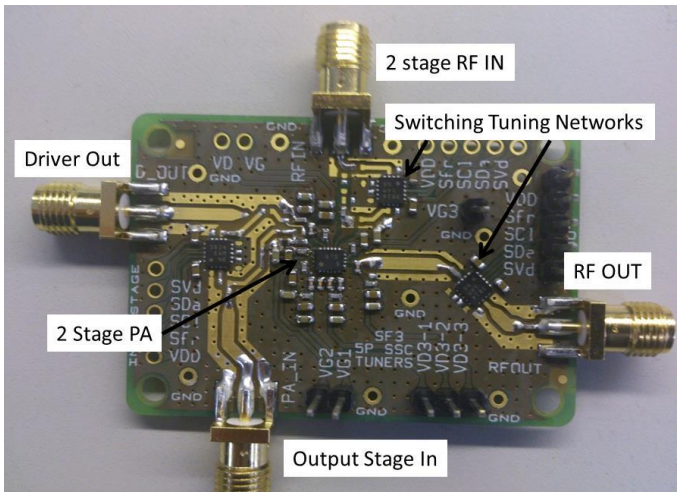

Fig. 19 Two stage Power Amplifier with programmable tuning networks

The programmable step capacitor has tuning bank devices, one is 5-bit series capacitor-array and the other is 4-bit shunt capacitor-array. A through-path is also made available. This device, developed for antenna tuning, allows for programming the PA output matching stage and inter-stage. Sony GaAs JPHEMT process is utilized in this chip for high linearity, high power handling and low insertion loss. The system diagram is shown in Figure 20 and the schematic of the tunable network are shown in Figure 21. This SSC device, including all control logic, is housed in a 3.0x2.8mm package.

Switchable Step Capacitor (SSC) such as Sony MMIC type can be used to perform the matching electronically

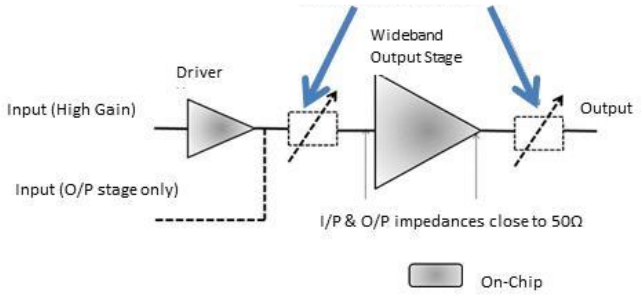

Fig. 20 PA with tuning devices

The process allows for high Q-factor for the built in capacitors and for low voltage operation. It has a frequency range from 700MHz-3GHz, hence covering the operating range of the PA. Any operation beyond this range, the by-pass switch can be used.

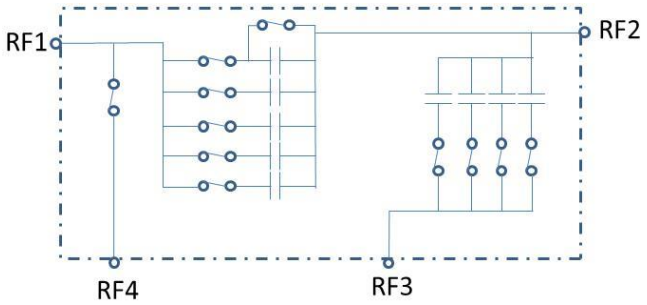

Fig. 21 Tuning SSC schematic

With this new setup the PA becomes software configurable and can be used in several forms, including Output stage plus Input/Output tunable network, 2-stage with Input/Interstage/Output tunable networks, Driver stage with input/Interstage tunable network etc. Typical measured performance of the PA is shown in Figure 21.

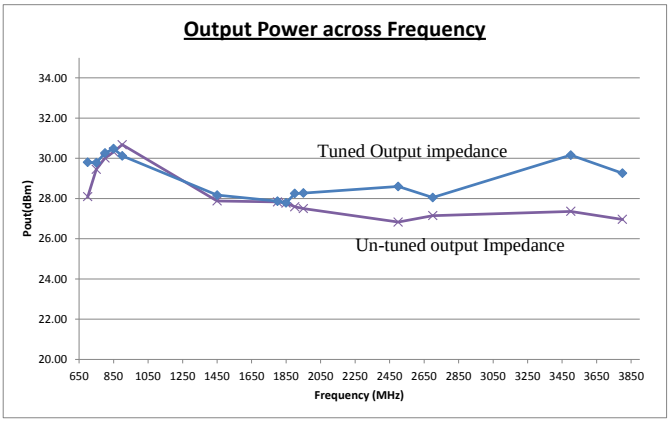

Fig. 21 Typical output power performances at 3.5V with tuned input and output. The device unde test is for an unpackaged die showing its full potential

The PA current consumption, under quiescent and small signal conditions at 800MHz for a 3.5V supply were a total of 63mA for the 3- devices stacked output stage and 17mA for the driver

stage. The PA was tested, in this example for 3G (Release 99 Handset Modulation). The conditions were to meet a 28dBm output power with adjacent channel linearity better than -35dBc at the two sides of the wanted channel. The PA was digitally configured through software and the appropriate combination of series and shunt capacitors in the tuning chip were selected. This along with a 3.9nH fixed inductor formed the required matching network. Figure 22 shows the gain versus frequency performance. While gain is expected to reduce at higher frequencies, due to device parasitic effects, however, the performance obtained for the combined output stage and driver is good and total gain is quite high.

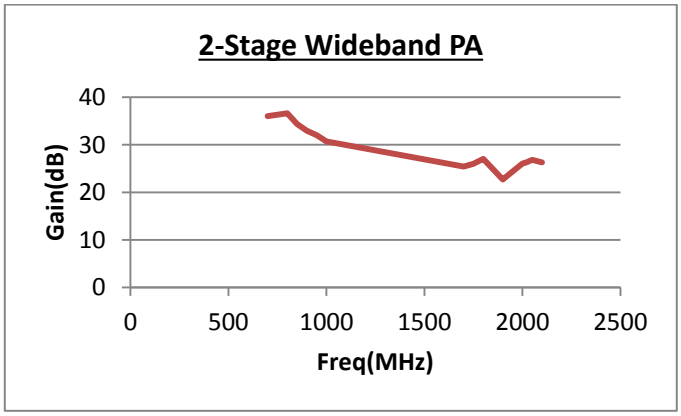

Fig. 22 Gain versus Frequency for the packaged 2 stage PA up to end of band 1 industrial requirements

For 3G operation, 28dBm is required the output power with adjacent channel leakage better than -35dBc. This was well achieved, as shown in Figure 23.

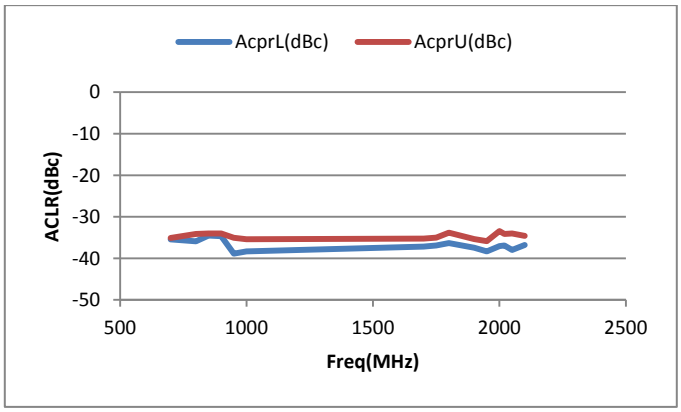

Figure 23 Adjacent Channel Leakage Ratio for the packaged 2 stage PA up to end of band 1 industrial requirements, with Pout=28dBm

The efficiency of the two stage amplifier meeting linearity and output power is shown in Figure 24. Over a wide frequency range it is averaged round 40%. This is a very good result given the increased DC consumption due to the driver stage.

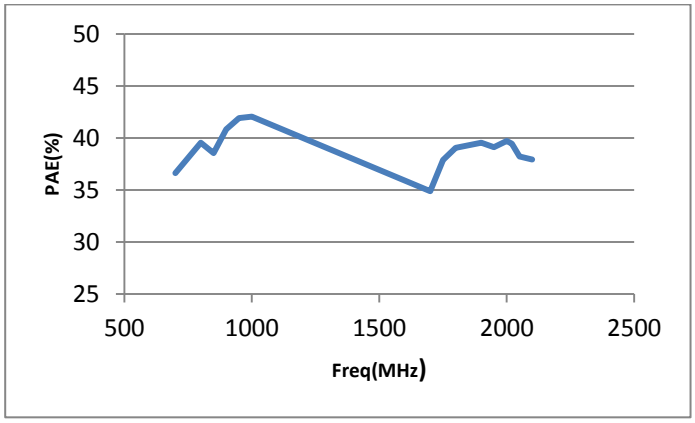

Figure 24 Power Added Efficiency versus frequency for 2 stage PA at Pout=28dBm.

Table 3 below compares the performance of this work and other solutions for key parameters.

Table III Comparison between this work and other work

Reference	Digitally Reconfigurable	Architecture	Technology	Coverage	PAE	Pout dBm	ACPR dB (-33dB 3G)
This Work	Yes	One Chip PA + external match tuning chip	PHEMT MMIC + CMOS	GSM, 3G, LTE	45.5% 3G	27(3G) to 33(GSM)	-35
[8]	No	Two separate PAs module	HBT MMIC+90nm CMOS	GSM, 3G	39-43%	28	-39
[9]	No	Switched mode RF devices	90nm CMOS	1.6-2.2GHz	43%	27	NA
[10]	No	Dual-mode PA	NA	824-849MHz LTE	34.5%	27	-31
[11]	No	Envelope Tracking+ class-F PA	InGaP HBT+65nm CMOS	Optimized to one band 1.7-2GHz LTE	40-46.3% with ET	27.8 to 30.1	-39 to -43

V. LINEARITY AND LINEARIZATION SIMULATIONS

The Linearity of the proposed PA architecture was further investigated. Since the stacked cascode PA architecture is suitable for a mobile terminal application, the behavior of the structure is simulated in the presence of the modern wireless communication standard such as 3GPP LTE and WCDMA. The procedure consist of simulating the PA response under few up-link signal scenarios to find out whether or not the linearity requirements are satisfied [1]. Figure 25 shows the simulated linearity performances of the PA in the presence of a 10 MHz LTE up-link signal versus the average output power level.

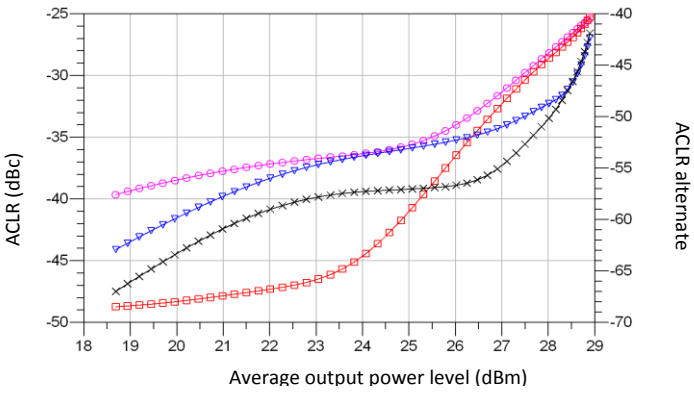

Figure 25: Linearity versus Pout with lower 5MHz ACLR (circles), upper 5MHz ACLR (squares), alt. lower 10MHz ACLR (triangles), and alt. upper 5MHz ACLR (crosses). Signal test 3GPP 10MHz LTE. (Vds=3.5V)

The carrier frequency was set to 1.8GHz. The results show that the proposed PA architecture meets the linearity requirement of the standard of 33dBc in terms of ACLR for an output power level of 26.5dBm. Nevertheless, some back-off needs to be applied to the output power level by decreasing the input power drive level in order to reduce the ACLR to level of, say, 36dBc. One could rather apply some linearization techniques such as digital pre-distortion (DPD) in order to improve the PA linearity in a systematic and reliable manner. The DPD use for PA linearization is widely implemented for down-link applications [23-28]. In this work, we investigated the DPD performances of a PA architecture dedicated to up-link applications. Recent work [29] showed the potential benefit of doing so, but we need to be careful with the type of DPD that should be used since there is more limited computational resources in mobile terminals. Therefore, the DPD applied to the proposed PA architecture here is a very simple memory-less polynomial approach. This method can be implemented efficiently, in the form of a look-up-table baseband architecture in mobile terminal hardware.

TABLE 4
SIMULATION RESULTS OF DIGITAL PRE-DISTORTION APPLIED TO THE PA ARCHITECTURE

Configuration Carrier frequency 1.8GHz Vds=3.5V	ACLR (dBc)		Average output power (dBm)	Average Drain efficiency (%)
	Lower	Upper		
20 MHz LTE memory-less DPD	36.6	37.3	24.5	30.4
20 MHz LTE without DPD	36.1	41.4	21.2	20.2

Table 4 shows DPD results implemented to linearize the proposed PA architecture in the presence of WCDMA and 20MHz LTE up-link signals. In the presence of WCDMA and 20MHz LTE signals, the PA architecture does not meet the linearity requirements of the standards (33/35dBc for WCDMA and 33dBc for LTE). Once memory-less DPD is applied both of WCDMA and LTE standards linearity requirements are satisfied. An additional test is also included which consist of backing off the input signal power until similar linearity performances to the DPD are obtained. This resulted in significant reduction in the efficiency which shows the benefit of DPD.
For 20MHz LTE and ACLR at -36dBc we can say that DPD gain a significant improvement in performance with 3dB increase in output power and 10% increase in efficiency.

Residential and Enterprise BS applications linearity requirements are demanding and have a big impact on efficiency. The -46dBc linearity specification limit for adjacent power ratio in the down-link (DL) is challenging for a high efficiency system. DPD can potentially add a lot of value. In general the applicability of DPD algorithm for the growing small Base-Station applications is expected. In summary, in the presence of signals with a bandwidth higher than few megahertz, the implementation of a memory-less DPD showed enhancement in performance to guarantee acceptable linear behavior. Further work was conducted to test if more improvement could be achieved incorporating memory model DPD [30]. It was shown that the memory model provided more than 2dB of improvement in ACLR when compared to a static (no memory) DPD [30].

V. CONCLUSIONS

The first re-configurable single input single output power amplifier that covers all 3GPP bands was presented. A novel digitally programmable wideband amplifier suitable for use in almost all active communication and data standards has been shown. The simulated and measured results showed excellent correlation in small-signal, large-signal and adjacent channel leakage ratios. The results also meet Standard requirements for operation in GSM, 3G and LTE. The design success of this power amplifier is due to the highly linear SONY J-PHEMT process used and to the novelty of the circuit. The circuit was based on extending cascode topology to three levels instead of the classical two. The output impedance of the amplifier was quite high, hence simplifying matching. A driver stage was also designed-in for higher gain operation. The PA was made programmable in 2-stage and output-stage modes. The digital tuning approach has allowed for a wider band operation that is greater than 40%.
For linearization purposes, a digital pre distortion algorithm (DPD) was implemented. Its benefits were more notable in wider bandwidths, where the PA circuit and device design designs where not sufficient to meet the linearity requirements for LTE systems in some cases. The implementation of a memory less and memory included DPDs were successful to guarantee acceptable linear behavior for complex modulation schemes without the need to back-off the input power. This helped to sustain higher efficiencies while meeting all linearity demands. Simulated results compared well with the measured data of the fabricated chip. To the best knowledge of the authors, this is the first power amplifier design that can be used concurrently for multiple standards and bandwidths with the easiest control configuration and operational simplicity.

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A significant period of his time at Sony has been spent managing the Wireless Semiconductor Development activity in Basingstoke, joining the Sony Semiconductor operation in 1997. During this time the company succeeded in securing significant design wins in the European cellular phone market. After spending a period of time at the main development site in Atsugi, Japan, the design flow for the GaAs MMIC technology was transferred to the UK Design Centre so that European products could be designed locally.
Following the successful set-up of the MMIC design facility by Chris and his team, other areas of Mixed-Signal development were expanded at the Basingstoke facility including cellular RF transceivers, full Bluetooth chipset solutions and analogue devices for DTV applications, under his leadership. In 2001, he became Divisional Director for Wireless products within the European Development Centre.
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Prior to Sony, he held positions as Chief Design Engineer at the GEC III-V semiconductor facility at Caswell and RF Engineering Manager at DSC Communications.
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