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Design of 370 ps Delay Floating Voltage Level Shifters with 30 V/ns Power Supply Slew Tolerance

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***Abstract*—A new design method for producing high performance, power rail slew-tolerant floating voltage level shifters is presented, offering increased speed, reduced power consumption, and smaller layout area compared to previous designs.**

The method uses an energy-saving pulse-triggered input, a high-bandwidth current mirror, and a simple full latch composed of two inverters. A number of optimizations are explored in detail, resulting in a presented design with a dV_{dd}/dt slew immunity of 30 V/ns, and near-zero static power dissipation in a 180 nm technology.

Experimental results show a delay of below 370 ps for a level-shift range of 8 V to 20 V. Post-layout simulation puts the energy consumption at 2.6 pJ/bit at 4 V and 7.2 pJ/bit at 20 V, with near symmetric rise and fall delays.

***Index Terms*—area efficient, dV/dt slewing immunity, energy-efficiency, floating level shifter, high speed, low power**

I. Introduction

As the communication bridge between different power rails, floating voltage level shifters are used to shift the potential of control signals from circuits powered by low voltage power rails to the potential of circuits with floating power and ground rails. A particularly challenging application with high on-chip power-rail slew-rates and strict delay demands is in a gate driver IC for the driving of two power semiconductor devices in a bridge leg, as used in switched mode power supplies.

Fig. 1 (a) illustrates such an application, producing an output voltage "SW". The slew-rate of the switch-node voltage, and hence on-chip power supplies is typically of the order of volts per ns. This is set to increase with the introduction of new power devices such as GaN HEMTs, which promise to reduce switching losses. In practice, the floating low voltage V_{SSH} is usually connected to the SW node [1, 2], or clamped by the SW node [3] with a diode or by V_{DDH} with resistors [4]. V_{SSH} swings from around V_{SSL} to DC_Link, whilst the differential voltage between V_{DDH} and V_{SSH} remains constant. Delay is also critical, since it affects timing resolution of the output channels.

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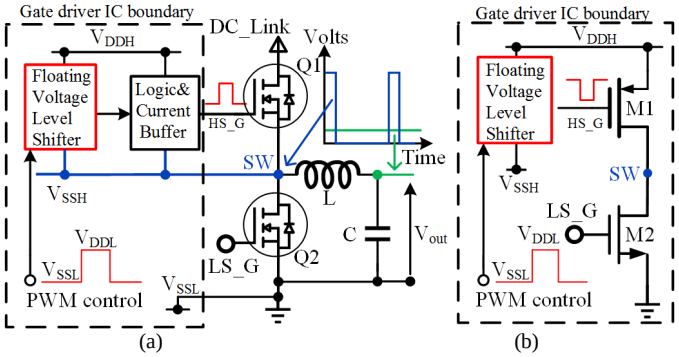

Fig. 1. Level shifters control the high-side devices of half-bridge circuits. (a) Driving off-chip discrete N-channel power devices. (b) Driving on-chip half-bridge with PMOS high-side.

Fig. 1 (b) represents an on-chip system, where the high-side device is a PMOS, and a floating voltage level shifter is working as the pre-driver of the half-bridge circuits [5-8]. In this circuit topology, V_{DDH} and V_{SSH} are typically biased to constant potentials, therefore power-rail slew capability is not required, however low power, low delay, and small layout area are important. In [5, 6] V_{SSH} is biased with an extra voltage source, but [7, 8] employ a diode or diode connected PMOS to clamp V_{SSH} to within a fixed voltage from V_{DDH}.

In this paper, we introduce a new floating-voltage level shifter design, capable of tolerating 30 V/ns of V_{SSH} slew, whilst offering data latency of just 370 ps. This design combines several of the positive features of the reviewed literature, and demonstrates an overall better trade-off between latency, layout area, and power consumption and offers significantly improved immunity to slew of its power rails. The relevant literature is summarized in the next section.

II. Review of Floating Voltage Level Shifters

Three types of floating voltage level shifters are illustrated in Fig. 2. Their operation is based on the low voltage clamping technique of their output V_{OUT}. Red dashed boxes show isolation areas provided by deep N-wells. Fig. 2(a) shows the conventional low voltage (LV) to high voltage (HV) level shifter [6]. This level shifter uses cascaded HV NMOS to protect and clamp the LV input transistors, and HV PMOS to protect and clamp the output floating LV transistors. As graphically analyzed in [9], this class of floating voltage level shifters has a large propagation delay and occupies a large layout area. The level shifter presented in [9] makes significant improvements in these aspects, but at the expense of additional complexity and a control signal to set the initial state, which may not be suitable in some applications. Fig. 2(b) shows a

second type of floating voltage level shifter [8]. This topology uses diode-connected floating LV PMOS transistors to clamp the potential at nodes N1 and N2 to one gate-to-source voltage drop (V_{GS}) below the floating high voltage rail V_{DDH}. This clamping technique allows the level shifters of [8] to operate at high speed, but the drawback is continuous power dissipation due to the alternate turn on of HNM1 and HNM2.

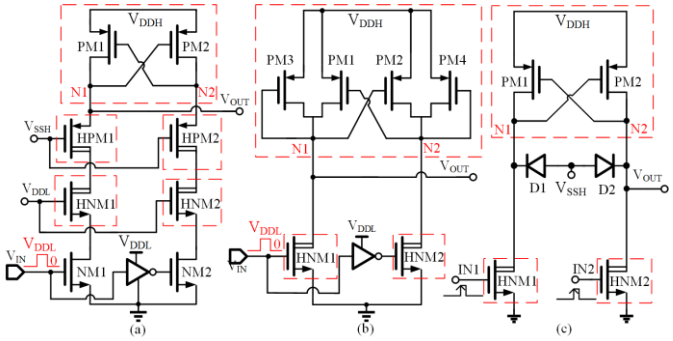

Fig. 2. Three floating voltage level shifters with different floating low voltage clamp techniques. (a) biased HV PMOS clamping. (b) diode connected PMOS clamping. (c) diode clamping. (V_{DDH} is the floating power supply rail, V_{SSH} the floating ground rail, and V_{DDL} is the low voltage supply rail).

A third kind of floating voltage level shifter [3] is illustrated in Fig. 2(c). It uses narrow pulse triggers as input signals to decide the output state. This level shifter has low power dissipation, a simple circuit and a small layout area. However, this circuit uses diodes with their anodes connected to the floating low voltage rail V_{SSH} to clamp the potential at nodes N1 and N2. This clamping technique leads to the V_{OUT} swing of Fig. 2(c) being $V_{OUT} = (V_{DDH} - V_{SSH} + V_F)$, where V_F is the forward diode voltage. This V_{OUT} exceeds safe operating limits of the following circuit, which reduces device life time and induces reliability problems. The level shifter in [10] also has this problem. The pulse trigger method is also used in [4-5] with resistors clamped by V_{DDH}. The output swing can be controlled by the value of the load resistor and the pulse current. However, the choice of resistor value leads to a trade-off between latency and power dissipation.

III. Basic Design of the Floating Voltage Level Shifter

A. Design Approach

In Section II, it is shown that: 1) it is advantageous to employ the diode connected PMOS clamp of the level shifter of Fig. 2(b), and 2) that the pulse-triggered technique is simple and consumes low power. It is therefore desirable to merge these two aspects into one design.

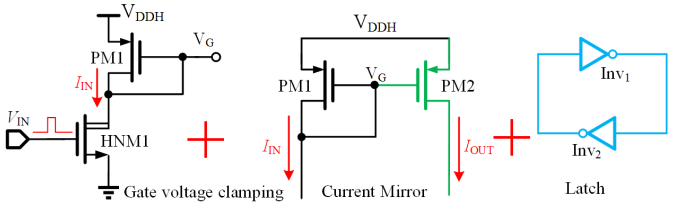

Fig. 3. Gate voltage clamping, current mirror and latch circuit.

The gate voltage clamping circuit (Fig. 3 left), clamps the gate voltage so that $V_G = V_{DDH} - |V_{GS}|$. When V_{IN} goes high, a current I_{IN} will flow through PM1 and HNM1 to ground. Its mirrored and level-shifted current I_{OUT} triggers the output latch, thus providing fast, current-driven level-shifting.

In this method the diode connected PMOS PM1 has two functions: clamping its gate voltage, and detecting the input high voltage pulse. The current mirror circuit copies the input current information, and the latch circuit captures the output state accurately.

B. Realisation

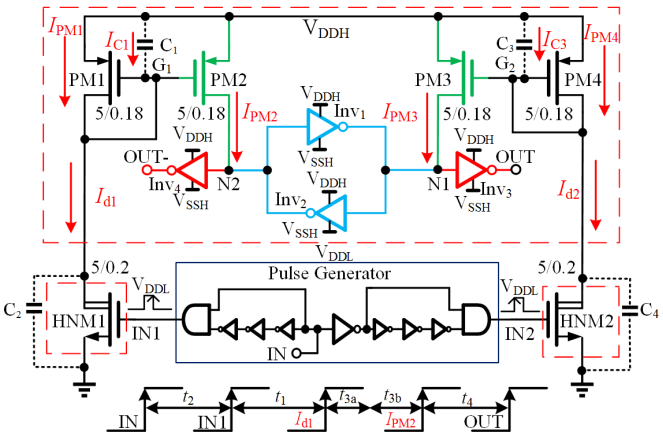

Fig. 4. The basic floating high-voltage level shifter ($V_{DDL} = (V_{DDH} - V_{SSH}) =$ 1.8 V. Red dashed boxes are deep N-wells).

The basic floating voltage level shifter circuit is shown in Fig. 4. The first stage is the pulse generator. On each transition of an input signal, only one path triggers and a pulse is produced at either IN1 or IN2. On the rising edge of IN, IN1 pulses high once, switching HNM1 on, with PM2 mirroring the current flow through PM1, pulling up node N2. As the voltage at node N2 exceeds the trigger voltage of the latch composed of Inv_1 and Inv_2, N1 is thus set to V_{SSH}. The positive feedback of the latch accelerates node N2's rise to V_{DDH}. Simultaneously, the output states at nodes N1 and N2 are maintained. Then output OUT will be held at V_{DDH}, even when HNM1 turns off at the end of the IN1 pulse. Thus, a rising edge on the input signal triggers the latch to lock N2 to V_{DDH} and N1 to V_{SSH}. To change the state of N1 and N2, a falling edge can be applied to the input. This results in a pulse signal at node IN2, triggering a similar sequence via HNM2, PM4, and PM3, pulling N1 to V_{DDH} and forcing OUT to V_{SSH}.

C. Propagation delay analysis and device sizing

We sub-divide the IN-to-OUT signal delay into components t_1 to t_4 defined in Fig. 4. The intrinsic delay t_1 of HNM1 and HNM2 is minimized by using the minimum channel width and length (5/0.2), whilst providing 0.9 mA of drain current when triggered. This presents the minimum load to the pulse generator, thus minimizing its delay t_2. The main advantage of the presented topology over reported level shifters is the reduction of the level-shifting delay $t_3 = t_{3a} + t_{3b}$ due to the use of a current mirror. Using G_1as an example, t_{3a} is the time taken to charge the gate of PM1 from V_{DDH} to $V_{DDH} - V_{TH}$:

$$t_{3a} = \frac{C_1 \times V_{TH}}{I_{d1}} \quad (1)$$

where V_{TH} is the gate voltage threshold.
The second component t_{3b} is the time that I_{PM1} and I_{PM2} take to rise from zero to the value that triggers the latch.
PM1 in the saturation region

$$I_{\mathrm{PM1}}(t) = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS(PM1)}(t) - V_{\mathrm{TH}}\right)^2 . \quad (2)$$

The resistance R_{G1} seen from node $\mathrm{G_1}$ to the power rail is:

$$R_{\mathrm{G1}}(t) = \frac{V_{GS(PM1)}(t)}{I_{d1}} = \frac{2V_{GS(PM1)}(t)}{\mu C_{ox}\frac{W}{L}\left(V_{GS(PM1)}(t) - V_{\mathrm{TH}}\right)^2} . \quad (3)$$

The simplifying assumption that R_{G1} is constant leads to:

$$I_{\mathrm{PM2}}(s) = I_{\mathrm{PM1}}(s) = I_{\mathrm{d1}}\left(\frac{1}{1 + \mathrm{s} \times R_{\mathrm{G1}} \times \mathrm{C_1}}\right) . \quad (4)$$

The gate capacitance $\mathrm{C_1} = 2C_{GS} = \frac{4}{3}WLC_{ox}$.
Under the assumption that R_{G1} is the resistance seen when $V_{GS(PM1)} = V_{GS1}$, the single pole is:

$$\mathrm{p_1} = \frac{1}{R_{\mathrm{G1}} \times \mathrm{C_1}} = \frac{\mu(V_{GS1} - V_{\mathrm{TH}})}{\frac{2}{3}L^2}\frac{1}{4}\left(1 - \frac{V_{\mathrm{TH}}}{V_{GS1}}\right) . \quad (5)$$

Setting $V_{GS1} = 2V_{TH} = 0.8$ V, this simplifies to:

$$\mathrm{p_1} = \frac{1}{8}\frac{\mu(V_{GS1} - V_{\mathrm{TH}})}{\frac{2}{3}L^2} = \frac{1}{8}f_T \quad (6)$$

where f_T is the unity current gain frequency.

From (4) and (6) we see the high bandwidth of the current mirror. The choice of minimum channel length for PM1 and PM2 leads to the maximum possible f_T and the minimum I_{PM2} settling time. As $\mathrm{C_1}$ is proportional to channel area, the channel width of PM1 and PM2 is chosen so that V_{GS} of PM1 is near 1.8 V when HNM1's drain current I_{d1} is 0.9 mA, which in turn, was determined by HNM1's dimensions. This guarantees the minimum $\mathrm{C_1}$ and hence $\mathrm{t_{3a}}$. I_{PM2} is used to trigger the latch composed of $\mathrm{Inv_1}$ and $\mathrm{Inv_2}$. The delay t_4 is the sum of latch and $\mathrm{Inv_3}$ delay. The choice of device size for the latch is a trade-off between speed and reliability. Smaller sizes reduce the required trigger current, however are more susceptible to triggering by slew-rate-induced parasitic current. With this consideration, the PMOS width of 0.4 times of that of PM1 is chosen, and the NMOS size is chosen to have the same current ability of the PMOS. The post-layout simulation delay from IN to OUT is 391 ps, with $t_1/t_2/t_3/t_4$=84/100/44/163 ps when $\mathrm{V_{SSH}}$=12 V

IV. Optimized Level Shifter for Power Converter Applications

A. Limitations of the basic design

The floating level shifter in Section III gives a better trade-off between speed, power dissipation and layout area than the level shifters in Fig. 2. However, specifically for the deployment in power conversion applications, three areas for further improvement are identified:

1) Symmetry of rising and falling propagation delays

A lack of symmetry can lead to data-dependent jitter, and so a symmetric design is desirable. The cause of asymmetry is that the rising edge signal path is via IN1, N2, and the latch composed of $\mathrm{Inv_1}$ and $\mathrm{Inv_2}$, whereas the falling edge path is via IN2 and N1.

2) Immunity to dV_{SSH}/dt slewing

The basic level shifter could be used in the high-side driver of a half-bridge circuit as shown in Fig. 1 (a). The voltage rail $\mathrm{V_{SSH}}$ will have high dV/dt slewing, potentially disrupting the level shifter's operation. Consider Fig. 4, in the case where HNM1 and HNM2 are both off, and the voltages at N1 and N2 are V_{SSH} and V_{DDH} respectively. When V_{SSH} rises, currents I_{d1} and I_{d2} will charge parasitic capacitors $\mathrm{C_2}$ and $\mathrm{C_4}$, with I_{PM2} and I_{PM3} mirroring the charging current. Since $\mathrm{V_{ds}}$ of PM2 is near zero, I_{PM2} is also near zero, and the voltage at N2 is held at V_{DDH}. However, the voltage at N1 is pulled up by I_{PM3}. A high enough value of I_{PM3} will cause OUT to erroneously change to $\mathrm{V_{SSH}}$. Post-layout simulations show rising edges failing to propagate with V_{SSH} slew-rates ≥15 V/ns.

Negative dV/dt of V_{SSH} has no effect on the level shifter. In this event, $\mathrm{C_2}$ and $\mathrm{C_4}$ discharge currents flow via PM1 and PM4, with G1 and G2 clamped to $\mathrm{V_{DDH}} + \mathrm{V_F}$ where $\mathrm{V_F}$ is the forward voltage drop of the bulk to source parasitic diodes of PM1 and PM4. The effect is to ensure that PM2 and PM3 remain turned off so no changes occur at N1 or N2.

3) Balancing the delay against the need to avoid high resistance nodes, current mirror mismatch

Taking node G_1 as an example: When HNM1 is off, G_1 becomes a high resistance node and is more easily disturbed by noise or transient currents. C_1 discharges through the drain to source current of PM1. When C_1 voltage falls below the threshold voltage of PM1, the discharge current reduces to the very small sub-threshold value of PM1. If there is a mismatch between the thresholds of PM1 and PM2, with $\mathrm{V_{TH(PM2)}} < \mathrm{V_{TH(PM1)}}$, this will prolong the time that PM2 conducts, leading to higher power consumption. Such a mismatch also results in higher current in PM2 during mirroring operation.

B. Improved design

Fig. 5 shows an optimized floating high voltage level shifter, which addresses the three issues outlined in Section IV A. The current mirror architecture is improved whilst ensuring ultra-low propagation delay. Asymmetry is addressed and V_{SSH} slew immunity improved by adding N-type current mirrors (in the dark dashed boxes).

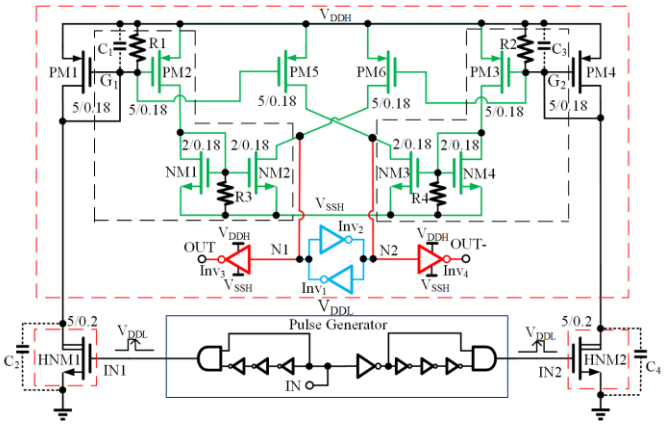

Fig. 5. The optimized high-voltage floating level shifter ($V_{DDL} = (V_{DDH} - V_{SSH}) = 1.8V$). Red dashed boxes are deep N-wells).

The AND gates in the pulse generator block are carefully designed to guarantee the time delays from IN to IN1 and IN2 are matched. To reduce the impedance of the node and the impact of current mirror mismatch, resistors R1 – R4 are added between the gates of the current mirror transistors and the power rails.

1) Rise/fall symmetry optimization

On a rising edge at input IN, nodes N2 and N1 are pulled up and down by PM5 and NM2 respectively. On the falling edge, N1 and N2 will be pulled up and down with the same principle. This optimization removes the need to consider the propagation delay of the latch, equalizing T_R and T_F at the faster speed of the two seen for the original circuit of Fig. 4

2) V_{SSH} slew immunity improvement

Here, slewing of V_{SSH} mirrors a parasitic current to PM5 & PM6, and NM2 & NM3. If the initial state of N1 is V_{SSH}, PM6 will pull up N1, but NM2 will pull down N1 at the same time. The voltage at N1 will greatly reduce, and OUT remains high.

3) Reducing high resistance node and current mirror mismatch problems

When HNM1 and HNM2 are off, nodes G_1 and G_2 (shown in Fig. 5) are high resistance. R1-R4 provide low resistance paths from V_{DDH} and GND to the gates of PM1-PM6 and NM1-NM4. At node G_1 for example, upon HNM1 turning off, R1 supports the sub-threshold drain current in PM1 in discharging C_1 and reducing $V_{GS(PM1)}$. This speeds up the decay of the sub-threshold currents in PM1, PM2 and PM5. The resistor values are 300 kΩ, which leads to a small efficiency cost due to current through the resistor when the current mirror is triggered; this is greatly outweighed by reducing the static current. Larger values increase static current and susceptibility to noise, lower values reduce the trigger current and thus speed.

V. Simulation and Experimental Results

A. Experimental method

The proposed level shifter is fabricated with AMS 180 nm HV Process. A level-up and level-down shifter are configured as a ring oscillator, following the method in [9], to measure propagation delays. A 256-times divider permits off-chip measurement of the oscillation period T_{OSC}. The delay is then given by $T_{AVE} = T_{OSC}/(4 \cdot 256)$.

B. Post layout simulation and measurement results

Fig. 6 provides the post-layout simulation result of the basic level shifter. It shows how changes in the input IN result in corresponding changes at the output OUT. Also shown are the voltages at the internal nodes IN1 & IN2, and the current I_{VDDH} being drawn from the positive power rail.

A square output is reliably generated after a propagation delay of approximately 370 ps, whilst more rounded internal pulses trigger HNM1 & HNM2. These pulses also represent almost all of the circuit's current consumption, which peaks at 1.6 mA for a maximum duration of 0.4 ns. A corner simulation provides ±50 ps around a 370 ps mean.

In Fig. 7, post-layout simulated data are provided for the basic level shifter (dashed lines), and the optimized level shifter (solid lines). Measured data points from the fabricated optimized level shifter are shown without lines. The figure shows the rising (T_R) and falling (T_F) propagation delays, and the energy consumption per transition (E_T), versus the floating low voltage V_{SSH}. Here, the load on a level-up shifter's output is the input of a level-down shifter, which has an input capacitance of 13 fF.

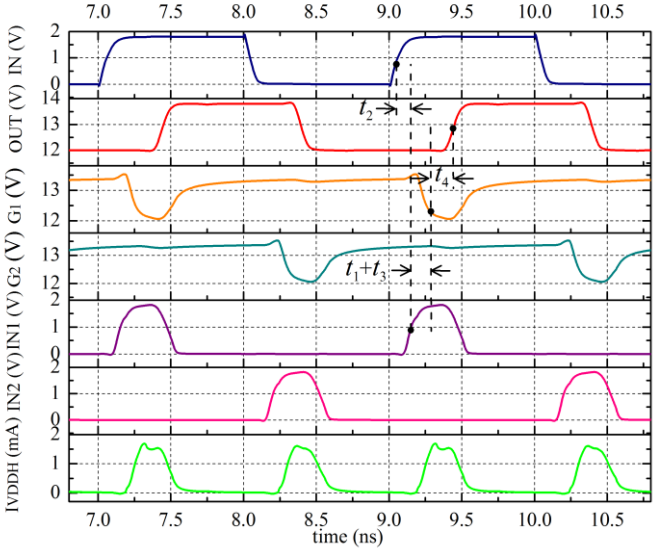

Fig. 6. Transient simulation results of the basic level shifter ($V_{SSH} = 12\,V$, $V_{DDL} = (V_{DDH} - V_{SSH}) = 1.8\,V$), and simulated delay times.

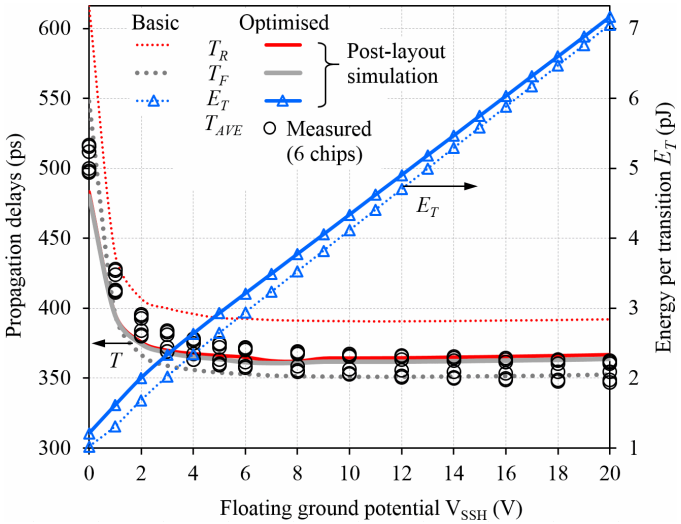

Fig. 7. Post-layout simulated rising (T_R) and falling (T_F) propagation delays and energy per transition (E_T) of basic (dashed lines) and optimized (solid lines) level shifters, and measured average delay T_{AVE} of optimized level shifter.

For the basic level shifter, the propagation delay drops to around 400 ps (rise) and 360 ps (fall) as V_{SSH} increases from 0 V – 4 V. T_R is greater than T_F since it also includes the latch response time. Increases in V_{SSH} cause a linear increase in the per-transition energy. This is because the HV NMOS trigger currents stay almost constant, whilst V_{DDH} increases linearly, and consumption is related to shoot-through current.

The optimized level shifter's simulated rising edge delay is seen to have reduced by around 30 ps, and is almost the same as the falling edge delay at each V_{SSH} biasing condition.

The optimized level shifter's measured propagation delays T_{AVE} are below 380 ps from a V_{SSH} of 4 V, and below 370 ps from 8 V to 20 V. T_{AVE} correlates well with the simulated

values. Compared to the performance of the original level shifter, E_T increases about 20% when V_{SSH} is 0 V, but is nearly the same when V_{SSH} is 20 V. Improvements in three performance aspects are achieved at the cost of at most 20% more power dissipation.

Fig. 8 shows simulated switching at 30 V/ns, with node N1's initial state being V_{SSH}.

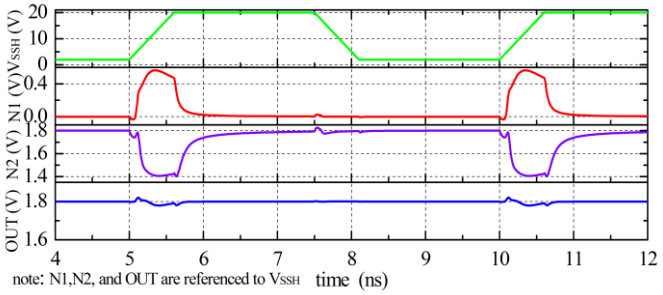

Fig. 8. Post-layout simulation results with V_{SSH} slew rate of 30 V/ns.

When N1 is at V_{SSH}, V_{DS} of NM2 is zero, so it has no pull down ability. With the voltage at N1 pulled to higher than V_{SSH} by PM6, the pull down current through NM2 increases. The final result is that the voltage at N1 is pulled up to V_{SSH} +550 mV, due to the fast slew of V_{SSH}. The same effect happens at N2, whose voltage is pulled down to V_{DDH} – 400 mV. Therefore, the optimized level shifter improves immunity to fast slewing in V_{SSH} to 30 V/ns, compared to less than 15 V/ns for the basic level shifter of Fig. 4.

C. Discussion

All the issues of the basic level shifter of Section III have been addressed. Further parallel pull-down NMOS could be added to reduce the delay at the expense of additional power consumption, slew-rate-capability, and layout area. The circuit layout measures 53.4 um × 90.8 um with an active area of 0.0043 mm^2.

TABLE I
Comparison with previous work

	Process	Voltage (V)	E_T (pJ)	Delay (ns)	FOM	FOM*	
[3]	0.5µm BCD	25	50	1.7	0.14	28	Simulation
[9]	0.35µm HVCMOS	10	10[1]	2.4	0.69	56[1]	Measured[1]
[10]	0.35µm HVCMOS	20	6	3	0.43	21	Simulation
This work	0.18µm HVCMOS	20	7.2	0.37	0.1	23[1]	Measured[1]

FOM from [9]: (Delay)/(Process node·Voltage). Unit: (ns)/ (µm·V)
FOM*: (E_T·Delay)/(Process node^3·Voltage). Unit: (pJ·ns)/ (µm^3·V)
Note 1: E_T is simulated.

Table I shows the level shifter's performance exceeding those summarized in Section II using the Figure of Merit (FOM) of [9]. This FOM includes technology scaling for delays, however does not reflect power dissipation. FOM*, incorporating per transition energy E_T, reflects both speed and power consumption and is suitably scaled for process node [11]. The level shifter's FOM* is similar to the simulated results of [10], and 2.4 × better than the measurements of [9].

VI. Conclusion

This paper presents a novel floating voltage level-shifter design method that offers symmetric propagation delays of 370 ps over a large range of operating voltage alongside 30 V/ns power rail slewing immunity in 180 nm ASIC technology. The level shifter avoids continuous current flow, and does not use HV PMOS transistors, thereby saving significant layout area.

The design combines the benefits of an energy saving pulse-triggered input, a high-bandwidth current mirror and a full latch to stabilize the output state, whilst minimizing the adverse effects of possible current mirror mismatch.

Measured delays are 340 – 370 ps for a level-shift range of 8 V to 20 V, and 520 ps at 0 V level shifting. Post-layout simulation puts the energy consumption at 2.6 pJ/bit at 4 V and 7.2 pJ/bit at 20 V, with near symmetric rise and fall delays.

Delay performance is validated with measured results and post-layout simulations. Detailed discussion of optimizations for the symmetry of output rise and fall delays, power rail dV/dt slew immunity, and tolerance of process variation mismatch are given, presenting a designer with a family of designs, according to requirement.

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