View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by Explore Bristol Research

Kuball, M., Pomeroy, J. W., Calvo, J. A., Sun, H., Simon, R. B., Francis, D., ... Pécz, B. (2015). Novel Thermal Management of GaN Electronics: Diamond Substrates. In ASME 2015 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems collocated with the ASME 2015 13th International Conference on Nanochannels, Microchannels, and Minichannels: Advanced Fabrication and Manufacturing; Emerging Technology Frontiers; Energy, Health and Water- Applications of Nano-, Micro- and Mini-Scale Devices; MEMS and NEMS; Technology Update Talks; Thermal Management Using Micro Channels, Jets, Sprays. (Vol. 3). [IPACK 2015-48145] American Society of Mechanical Engineers. DOI: 10.1115/IPACK2015-48145

Peer reviewed version

Link to published version (if available):
10.1115/IPACK2015-48145

Link to publication record in Explore Bristol Research

PDF-document

This is the author accepted manuscript (AAM). The final published version (version of record) is available online via [insert publisher name] at [insert hyperlink].

University of Bristol - Explore Bristol Research

General rights

This document is made available in accordance with publisher policies. Please cite only the published version using the reference above. Full terms of use are available: http://www.bristol.ac.uk/pure/about/ebr-terms.html

Proceedings of the ASME 2015 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems and ASME 2015 12th International Conference on Nanochannels, Microchannels, and Minichannels
InterPACKICNMM2015
July 6-9, 2015, San Francisco, California, USA

InterPACKICNMM2015-48145

NOVEL THERMAL MANAGEMENT OF GAN ELECTRONICS - DIAMOND SUBSTRATES

Martin Kuball, James W. Pomeroy, Julian Anaya Calvo, Huarui Sun, and Roland B. Simon
Center for Device Thermography and Reliability (CDTR), University of Bristol, Tyndall Avenue, Bristol BS8 1TL, United Kingdom

Daniel Francis, Firooz Faili, and Daniel Twitchen
Element Six Technologies
3901 Burton Drive, Santa Clara, CA 95054, USA

Stefano Rossi, Mohammed Alomari, and Erhard Kohn
Institute of Electron Devices and Circuits (EBS), University of Ulm, Ulm, Germany

Lajos Tóth and Béla Pécz
MFA, Institute for Technical Physics and Materials Science, Hungarian Academy of Sciences, Budapest, Hungary

ABSTRACT

Microwave and power electronics based on GaN enables the performance of systems and their safe operating area to be driven to 'extremes'. One of the major issues that then arises is thermal management. This includes heat transfer limitations across interfaces, however also the need of incorporating novel high thermal conductivity materials such as diamond. Thermal parameters of these novel device systems and their implications on the near junction temperature in the devices are not well known. The role of interfaces between the GaN transistor and the diamond substrate, and of the diamond thermal properties themselves near this interface are discussed, and novel thermal characterization approaches, such as enabling fast determination of the thermal resistance on the wafer level, as well as of lateral diamond thermal conductivity, are presented.

INTRODUCTION

Revolutionizing microwave, radar, communication and power conversion systems has benefited from step changes in the AlGaN/GaN high electron mobility transistor (HEMT) technology development. Presently these new devices enable outstanding performances, however, with device reliability limited by the junction temperature in the devices. Most commonly the GaN based HEMTs are grown on SiC or Si substrates, with in particular SiC providing good thermal management due to its thermal conductivity as high as 420 W/mK, although there are limitations due to the thermal resistance at the GaN-SiC interface, due to the nucleation layer, and the high defect density in the GaN in this area of the heterostructure (1). If one wishes to advance available power density in GaN HEMTs further, the most obvious solution is to replace the commonly used substrates with one of the highest thermal conductivity materials, namely diamond (up to 2000 W/mK). This enabled recently to demonstrate GaN based HEMTs with power densities about three times higher to what is possible with GaN-on-SiC technology (2). Typically GaN-on-Si is the starting material for this new wafer and device technology, with the Si substrate being removed and ultimately replaced by diamond, with the diamond grown on a dielectric seeding layer at the bottom of the GaN based heterostructure. Limitations in the thermal management are obvious, namely the low thermal conductivity of the dielectric layer and the thermal conductivity of the diamond which is impacted by its small grain structure near the GaN-dielectric-diamond interface (3,4). The target to thermally optimize GaN-on-diamond technology requires to separating the different thermal contributions to the total thermal resistance, which is the aim of this work. This ultimately enables to thermally optimize GaN-on-diamond technology for extreme applications. We focus in this paper on the development of new characterization approaches to

 Copyright © 2015 by ASME

characterize these key thermal limiting factors of GaN-on-diamond technology.

EXPERIMENTAL DETAILS

To study the thermal characteristics of the GaN-on-diamond interface on the wafer level prior to any device fabrication, a UV laser pulse from a tripled Nd-YAG (355nm) laser is used to heat the as-grown wafer surface; a doubled Nd-YAG (532nm) laser is used to probe the temperature transient at the GaN surface. No metal deposition on the wafer surface is needed for this measurement, in contrast to ultrafast laser based time domain thermoreflectance (TDTR) (3). The experimental setup used in this work is depicted in Figure 1. More details on the technique can be found in Ref. (5). GaN on hot filament (HF) CVD and microwave (MW) plasma CVD grown diamond wafers (100 μm thick), each having a GaN thickness of 0.7 – 1 μm and a dielectric seeding layer thickness of 28 - 100 nm were used (grown at Element-Six; MW diamond currently the standard commercial approach deployed), to demonstrate this new technique with trends that are observed with dielectric layer thickness variations. More details on the nature of the dielectric seeding layer can be found in Ref. (6), as well as on the microstructure of the HF and MW diamond films.

To gain insight into the diamond thermal properties themselves, in particular in close vicinity of the GaN-on-diamond nucleation interface, free standing diamond membranes were fabricated in this case of hot-filament grown diamond films on Si substrates from a thickness of 300 nm to 1 μm (grown at the University of Ulm, Germany). The HF diamond was grown under conditions to achieve a similar crystal quality and grain structure as MW diamond, resulting in an average grain size, measured at the surface, of 160-210 nm for a 1 μm thick membrane. A metal line heater was deposited on the diamond surface crossing this membrane as illustrated in Figure 2. This part of the diamond layer close to the GaN is a bottleneck with its reduced thermal conductivity due to the extensive microstructure in this part of the diamond layer, and needs to be carefully optimized. Raman thermography was used to measure the temperature rise in the diamond induced by the electrical power dissipated in the line heater. More details on Raman thermography can be found in Ref. (7). The experimental setup used is shown in Figure 2.

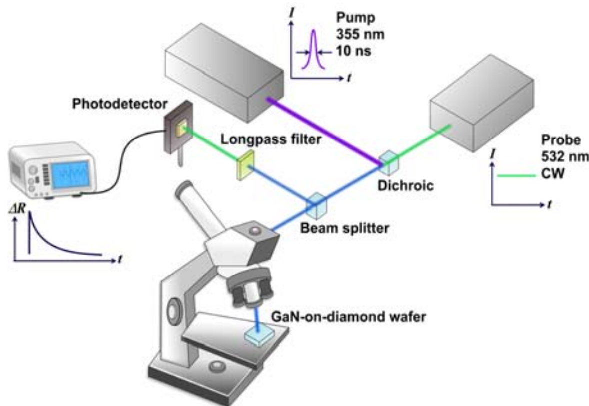

Figure 1: Experimental setup used to characterize the GaN-diamond interface on the wafer level.

RESULTS AND DISCUSSIONS

Figure 3 shows a series of thermoreflectance traces obtained on the wafers studied, with each of the wafers having a different dielectric layer thickness. The thermo-optic coefficient of GaN, *dn/dT*, is ~1×10^{-4} at room temperature at the wavelength used in the experiment, where *n* is the refractive index and *T* the temperature. Both results for a series of GaN-on-HF and GaN-on-MW diamond are shown. The faster the decay is the lower the thermal boundary resistance (TBR) between the GaN and the diamond. This TBR mainly constitutes of contributions from the dielectric layer between the GaN and the diamond, with its low thermal conductivity, and of the very highly defective diamond within its first few nanometers of growth. Figure 4 shows two example traces, illustrating that the initial part of the temperature trace is related to contributions from the TBR, with the long-term behavior reflecting contributions from the diamond thermal properties themselves. Cleary apparent for example in Figure 3 is the difference between HF and MW diamond, with the MW diamond in this measurement having a higher thermal conductivity. Material parameters extracted from a fit of a

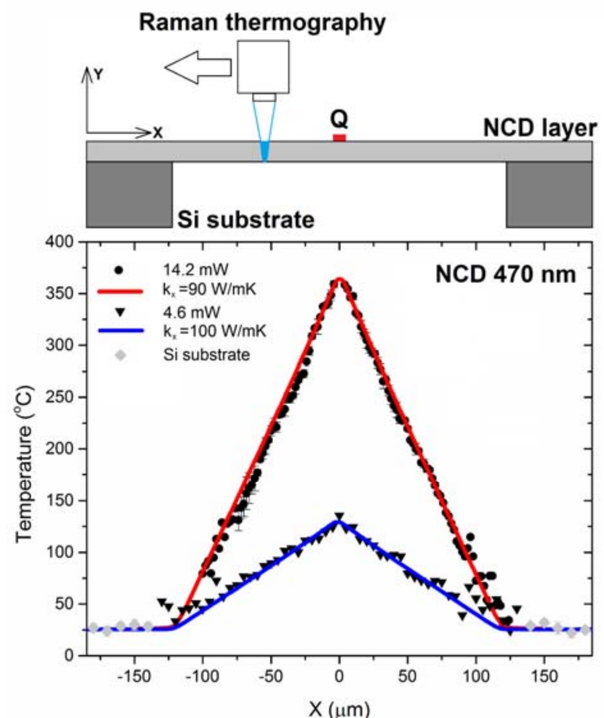

Figure 2: Experimental setup to measure lateral diamond thermal conductivity, and two example results with the metal line heater operated at different electrical powers in a 470 nm thick membrane.

Copyright © 2015 by ASME

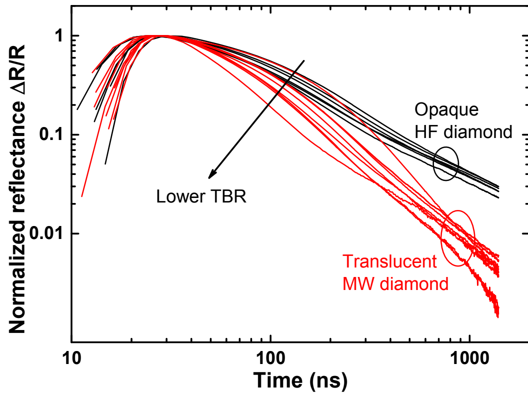

Figure 3: Transient thermoreflectance signals for GaN on HF and MW diamond with different dielectric layer thicknesses. A faster decay on short timescales indicates lower TBR.

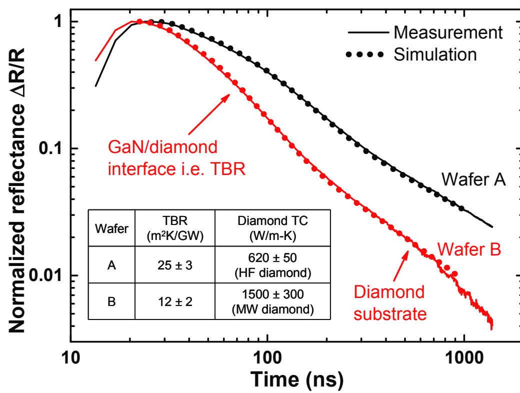

Figure 4: Temperature traces obtained for GaN-on-diamond wafer A with HF CVD diamond and Wafer B of MW plasma CVD diamond. Extracted values from a fit of a simulation to the experimental data of TBR and diamond thermal conductivity are listed in the table (inset).

thermal model (lines in Figure 4) to the experimental data are shown in the inset of Figure 4.

Figure 5 illustrates the TBR as function of dielectric layer thickness ($d_{dielectric}$), including wafer A and B, obtained from the data in Figure 3. Assuming a constant thermal conductivity for the dielectric layer, the total GaN-on-diamond interfacial thermal resistance is given by TBR = $d_{dielectric}/\kappa_{dielectric} + R_0$, where $\kappa_{dielectric}$ is the thermal conductivity of the dielectric. Here the term "TBR" is an effective thermal boundary resistance as technically this resistance contains contributions from finite thickness layers such as the dielectric layer which is in the strictest definition not a pure boundary resistance. Using this formula we can extract, from a linear fit to the experimental data, a thermal conductivity of 1.9 ± 0.4 W/mK which is consistent with what is expected for amorphous materials, i.e. the dielectric layer. Most interestingly is that when extrapolating the TBR to zero dielectric layer thickness, a value of below 7 m^2K/GW is obtained which is in line with what would be expected for the best case scenario case considering the GaN and diamond phonon properties (7). Using the diffuse mismatch model (DMM), the predicted TBR of the GaN/diamond interface is around 3 m^2K/GW (8). The DMM assumes all phonons are scattered diffusely; the transmission coefficient is therefore determined by the ratio of the phonon density of states on each side of the interface. This illustrates that this technology has potential to achieve excellent thermal performance if the dielectric layer is reduced to as small as technologically possible. Other interfacial features, such as the thin diamond nucleation layer near the dielectric surface, can also affect the TBR. Correlations between the TBR and the microstructures at the GaN-dielectric-diamond interface were reported in detail in Ref. (6).

To determine the thermal conductivity of the diamond itself, near the dielectric seeding layer, temperature profiles in a 470 nm thick diamond layer membranes are shown in Figure 2, in this case grown by HF on a Si substrate. The result for temperature line scans obtained for two different electrical power densities dissipated in the metal line heater is displayed. The temperatures were determined using Raman thermography using the diamond Raman modes, and constitute temperature averaged over the full diamond layer thickness. As additional parameter, temperatures measured in the Si substrate (near the diamond membrane edge) were also obtained. A finite element model was fitted to the experimental data determining a thermal conductivity of 95±5 W/mK for the diamond. This measurement approach can be used in the advancement of diamond growth parameters to tune the diamond thermal conductivity near the seeding layer to as high as possible. It provides high certainty on the thermal conductivity which is measured, and can be applied to layers as thin as a few 100nm, mostly limited by when the diamond coalesces during growth.

Figure 6 shows transmission electron images (TEM) of three different ultra-thin diamond layers. All of these layers had

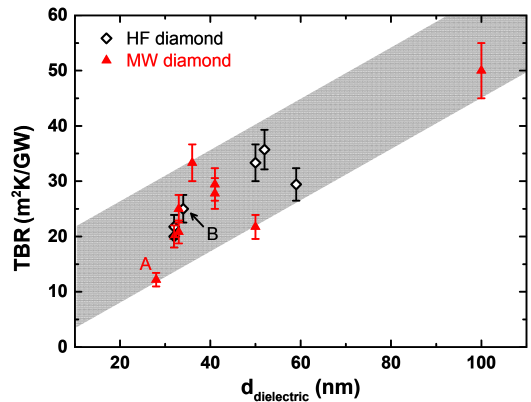

Figure 5: GaN-diamond TBR as function of dielectric layer thickness.

Copyright © 2015 by ASME

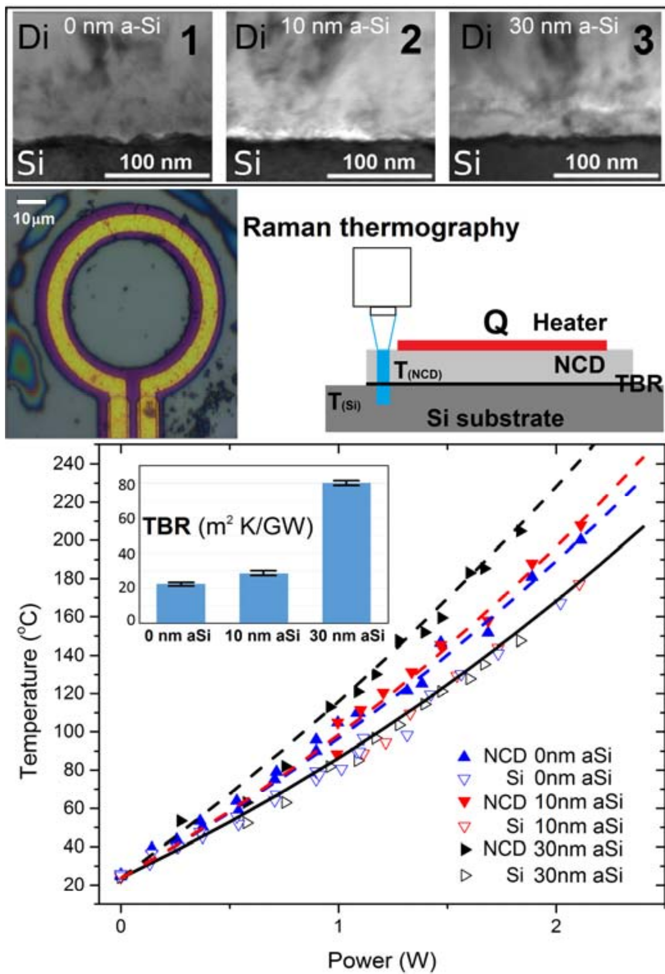

Figure 6: Transmission electron microscopy (TEM) micrographs of diamond grown onto Si substrates with different seeding layers, and test structures fabricated for thermal resistance measurements between the diamond (680 nm thick) and Si substrate with different interlayers are shown. A schematic of the experimental setup is displayed together with temperature versus electrical power in the different samples.

a thickness of 670 nm. They were grown using different seeding layers and thicknesses between substrate and diamond: one was grown on bare silicon, another on 10 nm of amorphous silicon (a-Si) on top of the silicon substrate and the final one was grown using a thicker a-Si layer of 30 nm. To now extract not only the lateral thermal conductivity but also the thermal resistance between the diamond and the original substrate, a variant of the heater structure design was used. On top of the diamond layers, Au ring heaters were deposited with the diamond outside and inside the ring heaters etched away as also shown in Figure 6. This limits the thermal transport to the vertical direction, in contrast to the membranes shown in Figure 2. Using Raman thermography, the temperature near the

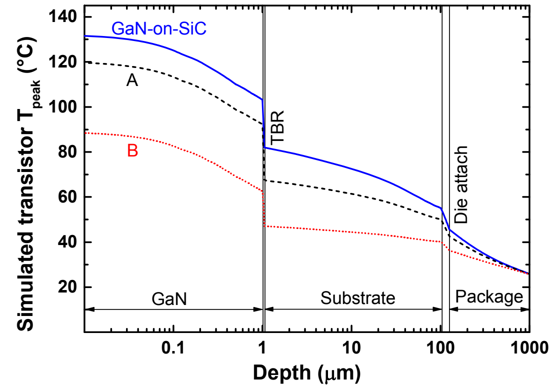

Figure 7: Simulated GaN based transistor device peak channel temperature for a multi-finger GaN RF transistor on SiC and diamond substrates, using material parameters as measured for wafers A and B (from Figure 4).

metal heaters in the diamond and of the silicon just below the diamond layer was extracted. Knowing the lateral thermal conductivity of the diamond (65 W/mK for these particular layers, from an experiment equivalent to the one of Figure 2), the thermal boundary resistance was determined using a finite element thermal model from the difference in these two temperatures. The temperature versus electrical power determined for the three samples is shown Figure 6. Note that the temperature of the silicon is the same for all the three samples, i.e., the only difference between the samples is the TBR between the diamond and the Si substrate rather than other material parameters. Both the diamond samples grown onto bare Si and 10-nm a-Si have similar low TBR, however, the sample grown on 30 nm a-Si shows a four times higher TBR value than the sample grown on bare Si. We note this heater and test structure used for the determination of the TBR, can then subsequently be used to determine the vertical thermal conductivity of the diamond films, using as input parameters the lateral thermal conductivity of diamond and the TBR.

Both the diamond-on-GaN interface properties as well as the diamond thermal properties will ultimately matter for the thermal performance of the GaN based transistors. Using material parameters determined earlier in this work, using thermal simulation, using wafer A and B from Figure 4, transistor channel temperatures were determined. The results are shown in Figure 7. Clearly apparent is the importance to optimizing the thermal parameters of interfaces and the diamond itself. Further reductions in the channel temperature of the devices are possible by additionally incorporating liquid cooling into the diamond substrates; this work here is focused on passive cooling approaches. It is crucial to realize that there is an exponential relationship between mean time to device failure (MTTF) and the inverse of the channel temperature. Any improvement in channel temperature can therefore either be exploited to enhance MTTF keeping the power density unchanged or to increase power capability of the device. We

Copyright © 2015 by ASME

note that the use of GaN-on-diamond technology requires device layout changes compared to GaN-on-SiC devices to fully exploit this new material system (9).

CONCLUSIONS

For the optimization of GaN-on-diamond wafer technology for transistor applications, to reduce device channel temperature, it is crucially important to both minimize thermal boundary resistances in the device structure such as induced by the dielectric seeding layer used between the GaN and diamond, which is possible achieving resistances which are close to the theoretical minimum if done correctly, as well as to maximize the thermal conductivity of the diamond near the seeding site, by optimizing growth parameters. In this work, techniques were presented to characterize accurately these material parameters of the GaN-on-diamond material system to enable GaN-on-diamond transistor development.

ACKNOWLEDGMENTS

We thank the Office of Naval Research Global for financial support (N62909-13-1-N210).

REFERENCES

(1) A. Manoi, J.W. Pomeroy, N. Killat, and M. Kuball, "Benchmarking of Thermal Boundary Resistance in AlGaN/GaN HEMTs on SiC Substrates: Implications of the Nucleation Layer Microstructure," *IEEE Electron Dev. Lett.*, vol. 31, no.12, 1395 – 1397, December 2010.

(2) J.W. Pomeroy, M. Bernardoni, D.C. Dumka, D.M. Fanning and M. Kuball, "Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping," *Appl. Phys. Lett.*, vol. 104, no. 2, 083513, February 2014.

(3) J. Cho, Z. Li, E. Bozorg-Grayeli, T. Kodama, D. Francis, F. Ejeckam, F. Faili, M. Asheghi, and K. E. Goodson, "Improved Thermal Interfaces of GaN-Diamond Composite Substrates for HEMT Applications", *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 1, 79 – 85, January 2013.

(4) J. Cho, Y. Won, D. Francis, M. Asheghi, and K.E. Goodson, Thermal Interface Resistance Measurements for GaN-on-Diamond Composite Substrates, *Compound Semiconductor Integrated Circuit Symposium (CSICs)*, 1 – 4, 2014.

(5) J. W. Pomeroy, R. B. Simon, H. Sun, D. Francis, F. Faili, D. J. Twitchen, and M. Kuball, "Contactless Thermal Boundary Resistance Measurement of GaN-on-Diamond Wafers", *IEEE Electron Device Lett.*, vol. 35, no. 10, 1007 – 1009, September 2014.

(6) H. Sun, R.B. Simon, J.W. Pomeroy, D. Francis, F. Faili, D.J. Twitchen, and M. Kuball, "Reducing GaN-on-diamond interfacial thermal resistance for high power transistor applications", *Appl. Phys. Lett.*, vol. 106, no. 11, 111906, March 2015.

(7) M. Kuball, J.M. Hayes, M.J. Uren, T. Martin, J.C.H. Birbeck, R.S. Balmer, and B.T. Hughes, "Measurement of temperature in high-power AlGaN/GaN HFETs using Raman scattering", *IEEE Electron Dev. Lett.*, vol. 23, no. 1, 7 – 9, January 2002.

(8) Y. Won, J. Cho, D. Agonafer, M. Asheghi, and K. E. Goodson, "Cooling Limits for GaN HEMT Technology", in *Proceedings of the 34th Annual IEEE Compound Semiconductor Integrated Circuit Symposium*, Monterey, USA, 2013, F.1.

(9) J.W. Pomeroy and M. Kuball, "Optimizing GaN-on-diamond transistor geometry for maximum output power", *Proceedings of the 35th Annual IEEE Compound Semiconductor Integrated Circuit Symposium*, Monterey, USA, 2014, C.1.

Copyright © 2015 by ASME