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ELECTRON TRAPPING IN GaN-ON-Si POWER HEMTs: IMPACT OF POSITIVE SUBSTRATE BIAS

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GaN-on-Si power devices are being intensively researched for high frequency, high efficiency switching applications, however they have been found to be susceptible to dynamic R_{ON} instabilities where the on-state resistance is affected by off-state bias. Dynamic R_{ON} is primarily the result of negative charge storage in the buffer during off-state operation, and limits application efficiency. Hence it is critical to understand and control the charge storage and transport mechanisms in the complex multi-layer buffer structure under all possible bias stress conditions. In this work, we demonstrate for the first time that electron injection and trapping can occur under reverse drain-bias conditions resulting in unacceptable increase in R_{ON}. We explain the trapping and de-trapping mechanisms and show that this vulnerability, which could occur in poorly designed switching circuits, applies even to devices showing low dynamic R_{ON} under normal drain bias conditions.

The GaN-on-Si power devices reported here use a buffer stack comprising an undoped GaN channel, a carbon-doped layer, and an AlGaN-based strain-relief layer grown on p-type Si. They have excellent dynamic R_{ON} behavior [1]. We simplify the situation by considering only quasi-1D vertical transport, monitoring the electric field under the channel by measuring the channel conductivity and varying substrate bias. Fig. 1 shows the layer structure and ungated 18µm long TLM device structure which it is important to note is surface insensitive in this experiment.

We consider the impact of positive bias on the Si substrate, corresponding to the situation of negative drain bias in a transistor. Vertical leakage paths and trap location are extracted using the substrate bias ramp technique [2, 3]. Fig. 2 shows that when the substrate is first ramped from 0 to +300V, the channel conductivity is essentially constant, but on the return sweep back to 0V, and all subsequent sweeps, the conductivity changes linearly with V_{SUB} indicating electron trapping during the initial sweep. Complementary current transient measurements [4] (Fig. 3) show an insignificant conductivity increase when V_{SUB} is stepped to +100V (“trapping”), but when V_{SUB} returns to 0V (“de-trapping”), the electron trapping becomes obvious as an unacceptable drop in conductivity. The charge is retained for many hours even at 100°C.

The trapping mechanism and why it results in the long period drop in channel conductivity is explained in Fig. 4. The C-doped GaN layer is very weakly p-type with the Fermi-level pinned ~0.9eV above the valence band at the C_N (0/-) acceptor level [5]. Hence there is a P-N junction between the 2DEG and the C-doped buffer. Applying positive V_{SUB} forward biases the junction and injects electrons into the buffer in an extremely fast process. Those electrons are then trapped in neutral deep acceptors, either in the C-doped GaN or at the top of the strain relief layer (②). The amount of charge injected is self-limiting and proportional to the applied substrate bias since the built-in field associated with this trapped negative charge prevents any further electron injection. This stored charge then reduces the channel conductivity at V_{SUB}=0V (③). The de-trapping transient, involves charge redistribution within the GaN:C (④) followed by eventual leakage of the trapped electrons to the contacts but only after 1000’s of seconds.

Under normal circumstances, GaN power devices would only be exposed to a positive drain bias (corresponding to negative substrate bias), but this study makes it clear that transistors must be protected against any transient conditions that expose the drain to negative drain bias since that would forward bias the channel-to-buffer diode and result in significant and long-period electron trapping.

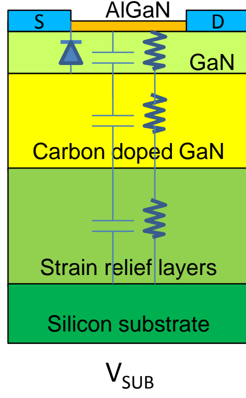

Fig. 1. Schematic cross-section of the device structure. Source-drain gap is 18um, width 100um and V_{SD}=1V. Overlaid is a lumped element circuit representation of the buffer.

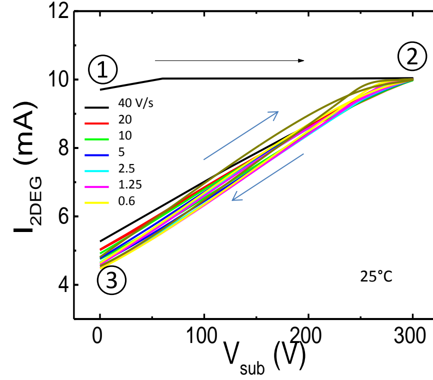

Fig. 2. Substrate ramp experiment. Source-drain current as V_{SUB} is swept from 0 to +300V to 0V at the indicated ramp rates. The initial ramp is clamped at 10mA as trapping occurs, with subsequent ramps showing behavior characteristic of capacitive coupling between the 2DEG and the Si substrate and no further trapping.

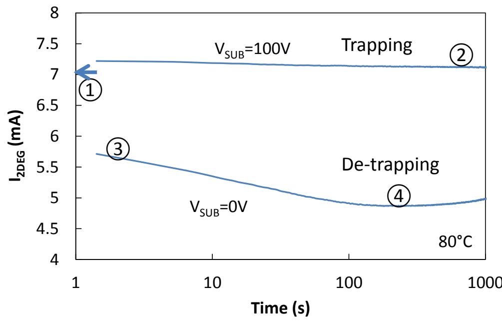

Fig. 3. Transient experiment. Source-drain current, as V_{SUB} is stepped from 0V to 100V and then held for 1000s (trapping phase) before stepping back to 0V for 1000s (de-trapping phase). Initial current at V_{SUB}=0V was 7.02mA and is marked with an arrow. V_{DS}=1V.

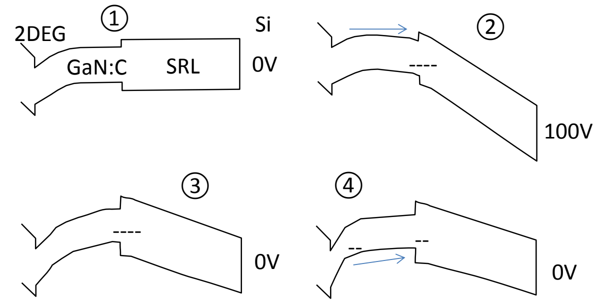

Fig. 4. Schematic band diagrams for the structure during ramp or transient experiment. ① Initial state. ② Barrier is lowered and electrons are injected from 2DEG into the GaN where they are trapped in acceptors in a self-limiting process. ③ Trapped electrons produce a built-in field which lowers the 2DEG density. ④ Hole conduction within the GaN:C results in an equipotential in this layer, increased depletion charge at the top of the layer and a further reduction in 2DEG charge.

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