Jin, B., & Yuan, X. (2016). Power Loss and Efficiency Analysis of a Four-level -type Converter. In 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe 2015): Proceedings of a meeting held 8-10 September 2015, Geneva, Switzerland. Institute of Electrical and Electronics Engineers (IEEE). DOI: 10.1109/EPE.2015.7309379

Power Loss and Efficiency Analysis of a Four-level π-type Converter

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Acknowledgements

The authors would like to thank the UK EPSRC National Centre for Power Electronics under Grant EP/K035096/1 and EP/K035304/1 for supporting the related research.

Keywords

Multilevel Converter, Efficiency, Loss Modelling, Pulse Width Modulation (PWM), Thermal Stress.

Abstract

In this paper, an analytical model has been developed to analyze the device power loss and the efficiency of a new four-level π-type converter. The efficiency of the π-type converter has been evaluated against a conventional two-level converter, three-level T-type converter as well as the three-level NPC converter. It has been found out that the four-level π-type converter has a higher efficiency when switching frequency is above 5 kHz. It can achieve 97% efficiency at 50 kHz switching frequency under the rated current. An experimental four-level π-type inverter topology has been built and the efficiency has been validated.

1. Introduction

Multilevel converters have gained great attention during the last two decades and are generally used due to their significant advantages in medium-voltage (3-33kV) and high-power applications. They are also recently considered for low-voltage (100~480V AC) applications as an alternative to the conventional two-level converter [1]. Converter topologies that generate output voltages of more than three levels, e.g. four levels, have been studied in [2, 3]. Multilevel converters present advantages of lower voltage stress (dv/dt) as well as lower output harmonics. A multilevel converter can generate a higher number of output voltage levels for a given output voltage rating which leads to a lower dv/dt, consequently improved reliability, reduced switching loss as well as lower filter cost. Given the same level of output harmonics, the switching frequency of the multilevel converter can be kept low, thus shrinking the heat sink size due to the reduction of switching loss. On the other hand, for the same switching frequency, the size of filters for multilevel topology can be further reduced compared with the two-level topology. These advantages improve the converter power density, which is desirable for electric vehicle, solar power generation and aerospace systems [4].

A main concern with multilevel converters is the increasing number of power devices as well as the control complexity [5]. A four-level configuration was presented in [6] with only six devices per phase leg as shown in Fig.1, the total component count of which is less than the conventional four-level diode-neutral-point-clamped (NPC) converter, flying-capacitor converter, etc [7] and can be suitable for low-voltage applications. The four-level π-type converter can output four levels per phase and seven levels for the phase-to-phase (line) voltage, which reduces the output harmonics compared with the two-level and three-level converters. Apart from the harmonics, another important aspect is to evaluate the efficiency of the π-type converter, especially how the efficiency varies with the switching frequency and thus whether it is suitable for high switching frequency operation. In theory, the conduction loss of the four-level converter should be higher than a standard two-level converter due to the two middle current

paths, where two devices are connected in series (e.g. T2 and D3, T3 and D2) and have a larger voltage drop. The switching loss on the other hand should be lower given each device only needs to switch a third of the dc-link voltage, rather than a full-dc-link voltage for a two-level converter. Therefore, an effective thermal loss and efficiency model needs to be developed to quantitatively assess the π-type converter against the two-level and three-level converters. In addition, the thermal stress of the devices (e.g. T1~T6, D1~D6) should also be analyzed due to their different locations and the corresponding current paths.

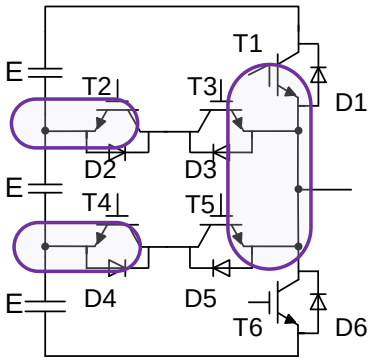


Fig.1. Four-level π-type converter phase leg structure

Generally there are two methods to evaluate the converter loss which are analytical models and numerical simulation [4]. The analytical model is normally derived based on the averaging over one fundamental cycle. The analytical equations can directly reveal the relationship between the power loss and system parameters such as voltage, current, power factor, modulation index, etc. Furthermore, it is computationally efficient. In comparison, the numerical simulation can be time-consuming but is able to show the instantaneous loss generation and reflect the dynamic performance. The relationship between the power loss and system parameters can only be revealed through multiple simulations, e.g. by sweeping the concerned parameters. In this paper, the analytical approach is adopted. The analytical power loss model including both the switching loss and conduction loss for the conventional two-level converter, three-level T-type converter as well as three-level NPC converter have been given in [4, 8, 9]. However, there is very limited literature regarding the four-level converter loss model due to its modulation complexity. This paper has therefore developed an analytical loss model for the four-level π-type converter, which can be used to evaluate the converter efficiency under various modulation index, power factors and switching frequencies. The special challenges to derive the model such as dividing the model according to different modulation indices as well as the numerical solvers for the analytical model have been given in this paper. With the developed model, it has been found out that the four-level π-type converter can have higher efficiency at switching frequencies above 5 kHz compared with the two-level or three-level converters due to the lower switching voltage. The model has also revealed that the thermal stresses are different among the devices. A 5kW four-level π-type inverter prototype has been built to validate the calculated efficiency from the developed loss model as well.

2. Converter Structure and Modulation

For the purpose of a better understanding of this topology, the inverter structure as well as modulation scheme is introduced first.

Fig.1 shows the phase-leg structure of a four-level π-type inverter, which consists of six switching devices. The common collector configuration is used in the neutral paths. With this configuration, T1, T3, T5 can share one gate driver supply. Thus the π-type converter only requires two additional isolated gate driver supply compared to the two-level converter. T1, T6 need to hold the whole dc-link voltage. T3, T4 need to withstand 2/3 of the total dc-link voltage. T2 and T5 need to hold 1/3 of the total dc-link voltage. A total of 3E voltage is shared among the three dc-link capacitors, and each phase leg can output four voltage levels with reference to the negative dc-link, i.e. 3E, 2E, E, 0. A SPWM strategy for this topology is shown in Fig.2. The intersection of the modulation wave and each carrier wave determines the switching states of one pair of the switching devices, which switch ON and OFF in a complementary

fashion (e.g. T1 and T2, T3 and T4, T5 and T6). Table 1 shows the switching states of the devices in a single phase leg.

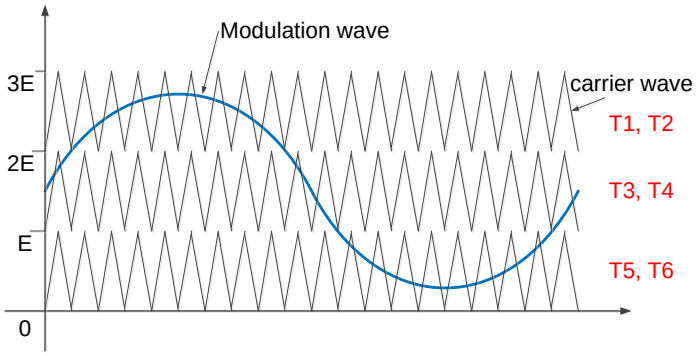


Fig.2. SPWM for the four-level π-type converter

Table 1: Switching states and output voltage levels for the four-level π-type inverter

Device / Voltage-level	T1	T2	T3	T4	T5	T6
3E	ON	OFF	ON	OFF	ON	OFF
2E	OFF	ON	ON	OFF	ON	OFF
E	OFF	ON	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON	OFF	ON

Regarding the device voltage ratings, for a 600V DC-link, T1, T6 generally have to leave a 600V margin and can be 1200V devices. However, during commutation, the voltage across T1 and T6 will be clamped to the neutral points such as N1 or N2. In fact, T1 and T2 only need to hold 1/3 of the totally dc-link voltage (200V in this condition) plus the voltage drop across the parasitic inductance during switching transient, which means a smaller voltage margin is actually required by T1 and T6. The same rule applies for T3, T4 and T2, T5. Since each device only has to switch between the adjacent voltage levels and therefore the switching voltage is a third of the dc-link voltage (200V in this case). This can reduce the switching loss greatly compared with the conventional two level converter which switches the full dc-link voltage.

3. Power Loss Model

The power loss of the switching device can be characterized by the conduction loss caused by forward voltage drop as well as the switching loss during the turn-on and turn-off process.

3.1 Conduction Loss

Conduction loss occurs when a device is at ON-state and current flows through it. Therefore the instantaneous conduction power can be expressed as ON-state voltage drop multiplied by ON-state current.

$$P_{con} = v_{CE} \, | i_c | \tag{1}$$

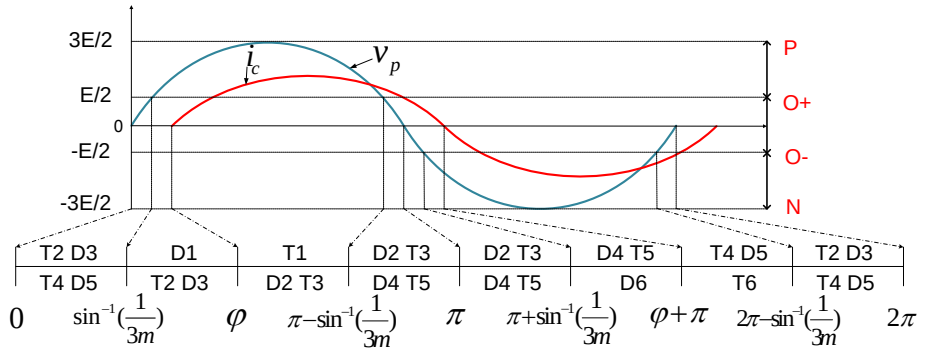
$$v_{CE} = V_{CE0} + \frac{V_{CEN} - V_{CE0}}{I_{CN}} i_c = V_{CE0} + r_0 \cdot i_c \tag{2}$$

Where, v_{CE} is the switching device voltage drop; V_{CE0} is the switching device initial voltage drop; V_{CEN} is the switching device voltage drop at the rated current. i_c is the IGBT collector current or diode forward current and I_{CN} is the rated current for switching devices. The absolute sign used here is to force the value of current to positive in order to calculate the accurate power loss. r_0 represents the device equivalent resistance linearized with device voltage drop. Assuming sinusoidal load current, the average conduction loss over one fundamental cycle should be expressed as an integration formula in (3) by combing (1) and (2)

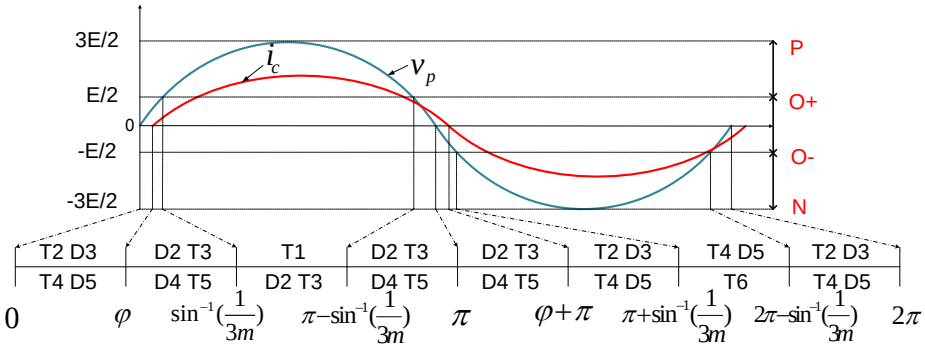
$$P_{con} = \frac{1}{2\pi}\int_{\theta_1}^{\theta_2} k \cdot \left[V_{CE0} \cdot |I_{CM} \sin(\omega t - \varphi)| + r_0 \cdot (I_{CM} \sin(\omega t - \varphi))^2 \right] d\omega t \quad (3)$$

Where I_{CM} is the load peak current. φ is the power factor angle. k is the ON-state ratio which represents the device conducting duty cycle. θ_2, θ_1 are the integration limits depending on the conduction interval of the device. Due to the circuit configuration and SPWM method being used, the ON-state ratio k in (3) has different expressions in various regions which has been derived in [10] as shown in Table 2.

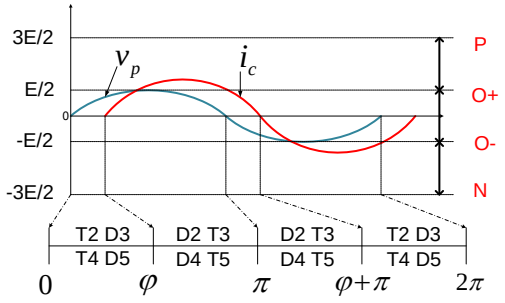
Assuming an inductive load, Fig.5 indicates the conduction intervals in relation to fundamental output phase voltage v_p (with reference to the middle point of dc-link) and load current i_c for the π-type converter. The modulation index m and power factor angle φ will affect the modulation, which means different m and φ will lead to different conduction intervals as shown Fig.3 and Table 2. Here switching state P means T1 is ON, inverter output phase voltage v_p equals to $3E/2$; O+ denotes T2 and T3 are ON, and $v_p = E/2$; O− indicates T4 and T5 are ON, $v_p = -E/2$; while N means N6 is ON, $v_p = -3E/2$, where $3E$ is the total dc-link voltage. As mentioned before, the value of ON-state ratio k of each switching device over one fundamental period of the output voltage is required for the calculation of the average conduction loss.



$$(a) m > \frac{1}{3}, \sin^{-1}(\frac{1}{3m}) \geq \varphi$$



$$(b) m > \frac{1}{3}, \sin^{-1}(\frac{1}{3m}) < \varphi$$



$$(c) m \leq \frac{1}{3}$$

Fig.3. Conduction intervals of a four-level π-type converter

Fig.4 shows the switching states according to the relative position between modulation wave and carrier wave for one switching period T_s. As T_s is much smaller than modulation wave period T_m, thus during one switching period, the modulation wave can be deemed as a straight line. In this way, the relevant ON-state ratio can be obtained by comparing modulation wave with carrier wave by triangle proportional relation. Therefore, the ON-state ratio k of the conducting device for four-level π-type inverter can be evaluated as follow.

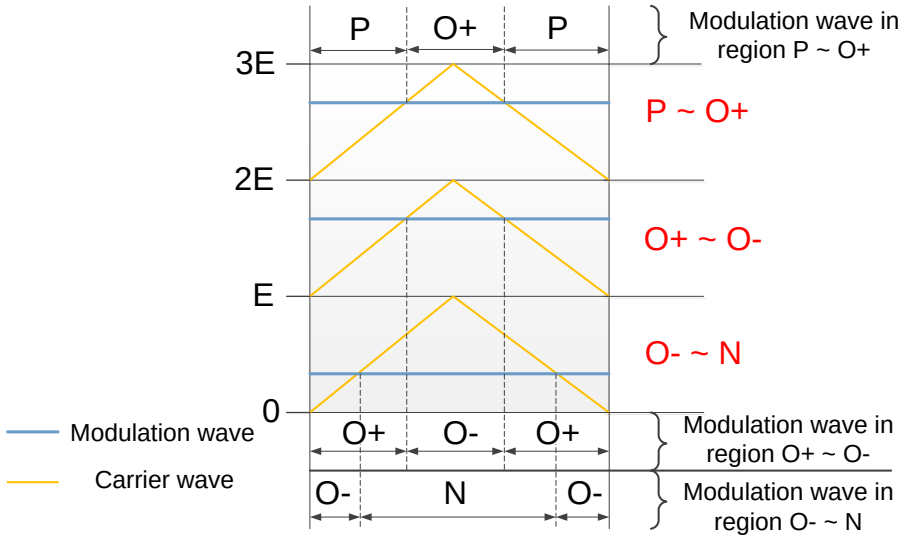


Fig.4. Switching states according to position of modulation signal

(a) P~O+ region

P ~ O+ region

O+ switching state ratio k_{PO+_O+} can be evaluated as

$$(3E-2E):1=(\frac{3E}{2}-\frac{3E}{2}\cdot m\cdot\sin(\omega t)):k_{PO+\_O+}$$

$$k_{PO+\_O+}=\frac{3}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{4}$$

P switching state ratio k_{PO+_P} can be calculated as

$$k_{PO+\_P}=1-k_{PO+\_O+}=-\frac{1}{2}+\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{5}$$

(b) O+ ~ O− region

O− switching state ratio k_{O+O-_O-} can be evaluated as

$$(2E-E):1=(\frac{E}{2}-\frac{3E}{2}\cdot m\cdot\sin(\omega t)):k_{O+O-\_O-}$$

$$k_{O+O-\_O-}=\frac{1}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{6}$$

O+ switching state ratio k_{O+O-_O+} can be calculated as

$$k_{O+O-\_O+}=1-k_{O+O-\_O-}=\frac{1}{2}+\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{7}$$

(c) O− ~ N region

N switching state ratio k_{O-N_N} can be evaluated as

$$E:1=(E-(\frac{3E}{2}+\frac{3E}{2}\cdot m\cdot\sin(\omega t))):k_{O-N\_N}$$

$$k_{O-N\_N}=-\frac{1}{2}-\frac{3}{2}\cdot m\cdot\sin(\omega t) \tag{8}$$

O− switching state ratio k_{O-N_O-} can be obtained as

$$k_{\text{O-N\_O-}} = 1 - k_{\text{O-N\_N}} = \frac{3}{2} + \frac{3}{2} \cdot m \cdot \sin(\omega t) \tag{9}$$

Table 2 has summarized the ON-state ratio *k* for different regions.

Table 2: ON-state ratio with different regions

Region	P ~ O+		O+ ~ O−		O− ~ N	
State	P	O+	O+	O−	O−	N
k	$-\frac{1}{2}+\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{3}{2}-\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{1}{2}+\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{1}{2}-\frac{3}{2}m\cdot\sin(\omega t)$	$\frac{3}{2}+\frac{3}{2}m\cdot\sin(\omega t)$	$-\frac{1}{2}-\frac{3}{2}m\cdot\sin(\omega t)$

3.2 Switching loss

The total switching loss consists of turn-on loss and turn-off loss. For anti-parallel diodes, the reverse recovery loss will be considered as the switching loss. The switching energy of devices can be modelled as in (10), which assumes it is proportional to voltage drop, and has a quadratic relationship with current following through it.

$$E_{switch} = \left(A_0 + B_0 \cdot |i_c| + C_0 \cdot i_c^2\right) \frac{U_{block}}{U_{base}} \tag{10}$$

U_{block} is the actual blocking voltage for the switching device. U_{base} is the voltage for characterizing the switching energy in the device datasheet. A_0, B_0, C_0 are the parameters describing the relationship between switching energy and current. They are different for IGBT turn-on loss, turn-off loss and diode reverse recovery loss, which can be derived using the curve fitting techniques based on the switching energy curves in the devices datasheet. Then, switching power can be generally expressed as

$$P_{switch} = \frac{f_c}{2\pi} \cdot \frac{U_{block}}{U_{base}} \int_{\theta_1}^{\theta_2} \left[A_0 + B_0 \cdot |I_{CM} \sin(\omega t - \varphi)| + C_0 \cdot (I_{CM} \sin(\omega t - \varphi))^2\right] d\omega t \tag{11}$$

Here, f_c is the carrier frequency, and the switching loss is a function of carrier frequency, peak current and the power factor.

Fig.5 shows the current commutation paths in different switching transitions. Switching losses occur in different switching devices depending on the switching transition and the direction of the output current. Table 3 summarizes the results. Given the forward recovery loss of a diode is negligible, thus the turn-on loss of diode has been omitted.

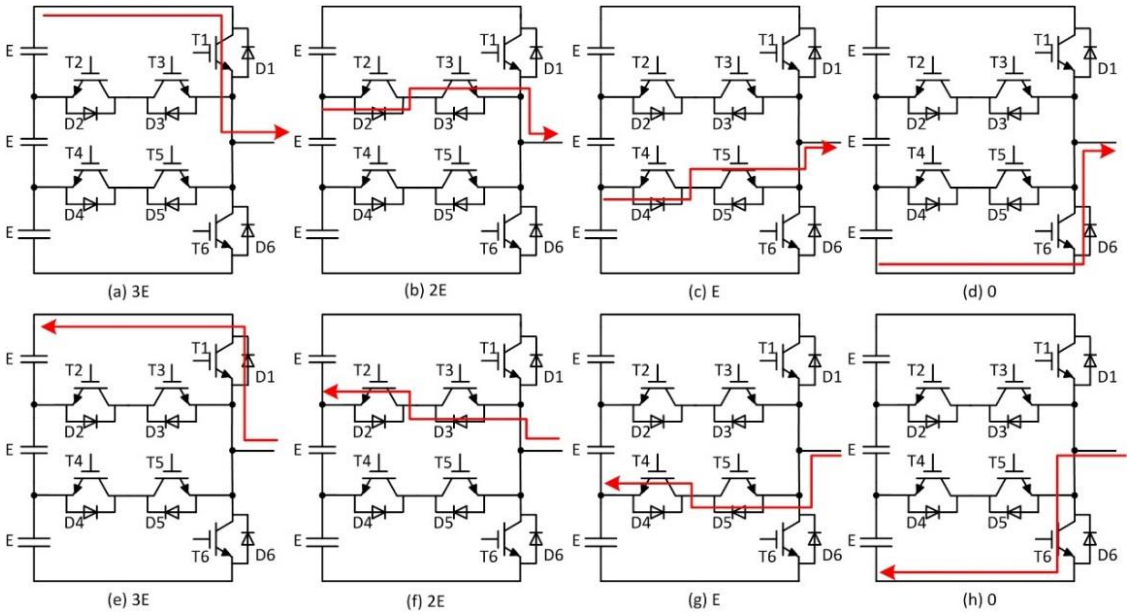


Fig.5. Switching states with current flow path

Table 3: Switching losses during commutation

	Switching Loss	
Switching Transition	$i_c \geq 0$	$i_c \leq 0$
P → O+	$P_{\_T1\_off}$	$P_{\_T2\_on}$, $P_{\_D1\_rr}$
O+ → P	$P_{\_T1\_on}$, $P_{\_D2\_rr}$	$P_{\_T2\_off}$
O+ → O-	$P_{\_T3\_off}$	$P_{\_T4\_on}$, $P_{\_D3\_rr}$
O- → O+	$P_{\_T3\_on}$, $P_{\_D4\_rr}$	$P_{\_T4\_off}$
O- → N	$P_{\_T5\_off}$	$P_{\_T6\_on}$, $P_{\_D5\_rr}$
N → O-	$P_{\_T5\_on}$, $P_{\_D6\_rr}$	$P_{\_T6\_off}$

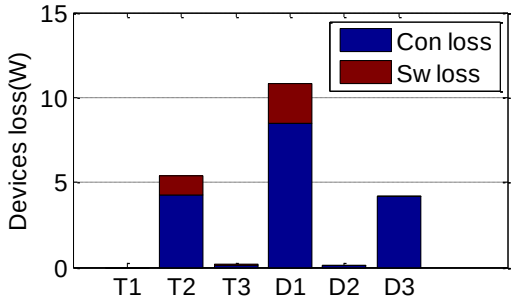
3.3 Simulation Results

Table 4 shows the selected devices used in the calculation based on a 600V total dc-link voltage. In theory the equations in (3) and (11) can be further derived analytically for each devices. However, the expression will be over complicated. In this case, a piecewise numerical method is used to calculate the loss in (3) and (11).

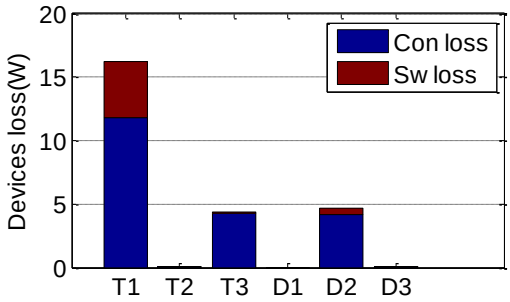
Table 4: Selected IGBT devices for the π-type inverter

Switch	Device
T1, T6	FGW15N120VD (1200V)
T2, T3, T4, T5	IKW30N60H3 (600V)

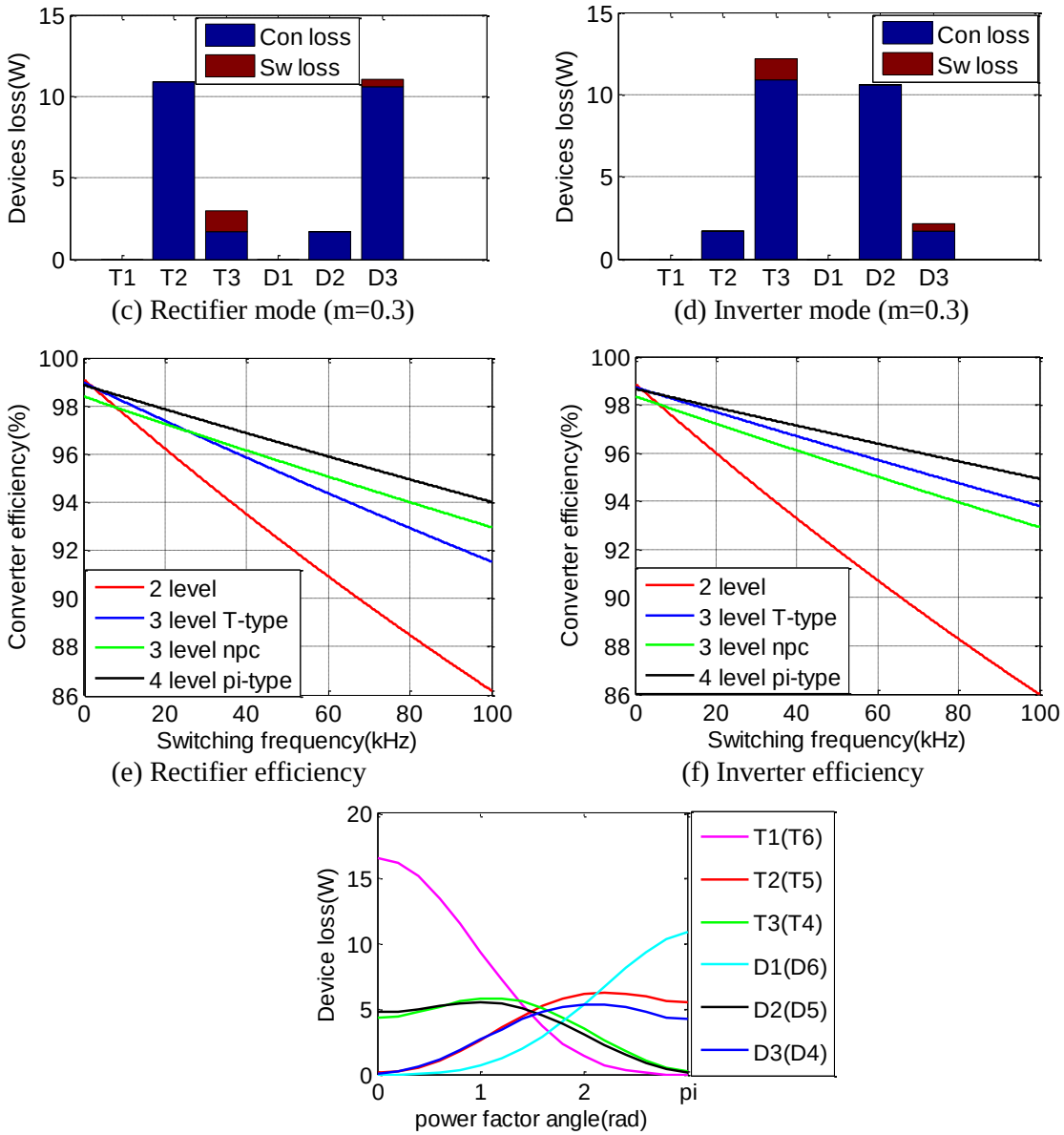
Fig.6 (a) (b) (c) (d) show the loss distribution among various devices for different modulation indices with inverter/rectifier operation based on a 10kHz switching frequency and 15A rated current. At high modulation index (m=0.95) with rectifier operation, D1, T2, D3 generate higher losses than D2, T3, T1. In comparison, in inverter mode, the losses of D2, T3 and T1 are higher. At low modulation index (m<1/3) such as m=0.3, outer devices T1 and T6 do not conduct at all. It is clear that losses are not distributed equally. Fig.6 (e) (f) show the efficiency variation with switching frequency for rectifier and inverter operation under m=0.95 in comparison with two-level and three-level (NPC and T-type) converters. The π-type converter shows higher efficiency when the switching frequency is above 5 kHz. Fig.6 (g) show the switching device loss variation with the power factor angle. T1 is most stressed at inverter operation, whilst T2 and D2 are more stressed in the rectifier mode, and T3, D2, D4 are relatively mild. One thing should be noted that due to the symmetry of the π-type converter circuit in Fig.1, only T1, T2, T3, D1, D2, D3 are analyzed here, as T6, T5, T4, D6, D5, D4 are of the same average loss.



(a) Rectifier mode (m=0.95)



(b) Inverter mode (m=0.95)



(c) Rectifier mode (m=0.3)

(d) Inverter mode (m=0.3)

(e) Rectifier efficiency

(f) Inverter efficiency

(g) Variation of device loss with power factor angle

Fig.6. Loss model calculation results

4. Four-level π-type Inverter Prototype and Experimental Results

Using the switching devices in Table 4, a π-type inverter prototype has been built. The inverter is designed for an output power of 5kW and allows the switching frequency to be set in a range from 5kHz to 50 kHz with a nominal dc-link voltage 600V (900V maximum). For the purpose to reduce the disturbance of the gate signals, gate driver circuits were also integrated in the inverter board.

The inverter is controlled by a DSP-FPGA board which consists of a XILINX SPARTAN XC3S400 FPGA chip and a TI TMS320 F28335 DSP chip, as well as two external AD7656-1 chips from Analog Devices. The prototype is shown in Fig.7.

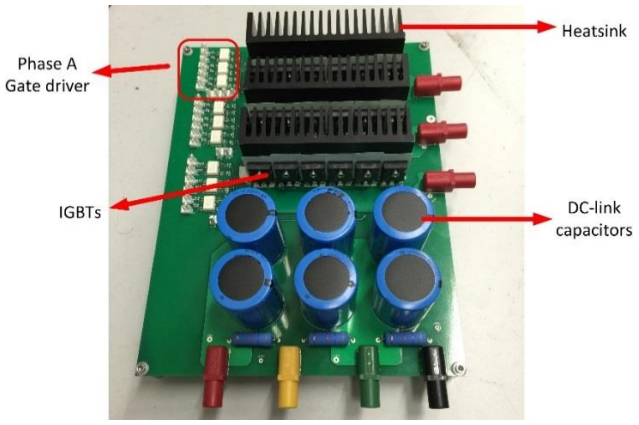
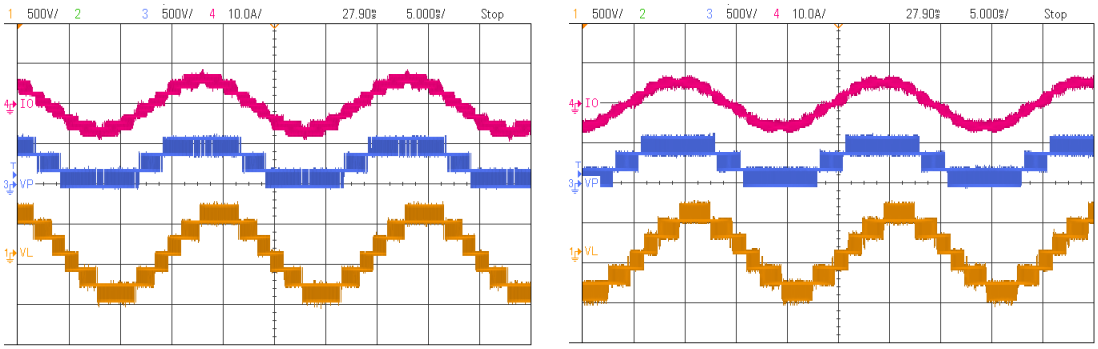


Fig.7. Layout of the four-level π-type inverter prototype

The output power of the four-level π-type inverter has been measured with a NORMA 4000 high bandwidth power analyzer. The error limit is between 0.03% and 0.3%. The measurements were conducted with a fixed RL load (R=44Ω, L=50μH), with a modulation index m=0.95. The input dc-link voltage was fixed in 600V. In order to prevent the short circuit during the commutation, a 2μs dead-time was injected as well. Due to the open-loop operation at this stage, in order to get a balanced voltage sharing on each dc-link capacitor, three individual DC power supplies have been used to supply the three dc-link capacitors individually.

Fig.8 shows the experimental output current and voltage waveforms of the four-level π-type inverter under f_s=10 kHz and f_s=50 kHz respectively. The phase voltage (blue waveform) has four voltage levels and the line voltage (yellow waveform) has seven voltage levels as expected. It is evident in Fig.8. (a) when f_s=10 kHz, the current waveform (red waveform in Fig.8. (a)) has apparent staircase patterns (higher harmonics) due to the small load inductor. This phenomenon can be mitigated by the increase of switching frequency as indicated in Fig.8. (b), where the current waveform is much smoother and the current curve is more like a sinusoidal wave when f_s has increased to 50 kHz. This advantage can reduce the output filters to some extent.



(a) f_s=10 kHz (b) f_s=50 kHz

Fig.8. Output current (red), phase voltage (blue), line voltage (yellow) of the four-level π-type inverter prototype in (a) 10 kHz switching frequency and (b) 50 kHz switching frequency

Fig.9 shows the comparison between the calculated efficiency and the measured efficiency. The measurements were taken under a 600V dc-link voltage with a 0.95 modulation index and a fix RL load (R=44Ω, L=50μH). The input power was obtained by multiplying the current and voltage readings from the three DC power suppliers directly. Then the measured efficiency was calculated by dividing the output power measured from the power analyzer with input power. For the given load condition, the actual rms value of the output current is about 4.6A. The experimental results agree with the analytical predictions reasonably well. The calculated efficiency around 10 kHz switching frequency is slightly lower than the measured efficiency. At higher switching frequencies, the measured efficiency is lower than the analytical prediction. This may due to the additional losses caused by wire resistance and parasitic components in high switching frequencies.

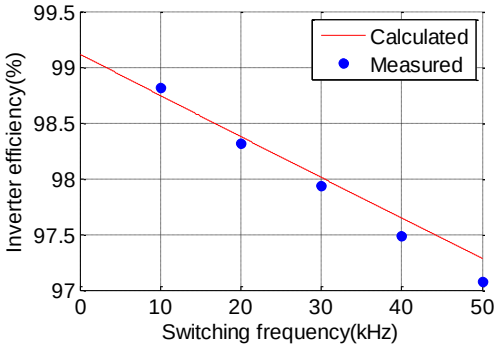


Fig.9. Calculated and measured efficiency of the four-level π-type inverter supplying a RL load

5. Conclusion

In this paper, the loss model for the four-level π-type converter has been presented. The converter has shown better efficiency when the switching frequency is above 5 kHz under rated current. The higher efficiency is due to the lower switching voltage and the resultant lower switching losses compared with the two-level and three-level topologies. It has also been shown that the losses generated among the devices are not equal under different modulation indices and power factors. The calculated efficiency of the π-type inverter has been compared with the measured efficiency of a 5kW π-type inverter prototype but with a 2.8kW actual output, and the measured results match the calculated ones reasonably well.

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