Design of Ultra Low Power Analog-to-Digital Converter for Ambulatory EEG Recording

by

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B.Sc., Ain Shams University (2007)
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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Portable acquisition of biopotential signals requires the design of compact, energy efficient circuits and systems. Such systems typically include analog-to-digital converter for digitizing signals from AFE and feeding it to DBE. An Ultra low power ADC is designed in this work to be integrated within scalable EEG SoC. The full system can capture EEG signals through 1 up to 8 parallel differential channels that are time division multiplexed into a single ADC. The ADC has a fixed resolution of 10 bits which is sufficient for extraction of bio-markers for seizure detection. A SAR ADC architecture is chosen for this design as it is highly energy efficient for medium to high resolution applications with low speed requirements. A differential capacitive DAC is utilized to enhance the CMRR. Concepts of split-capacitor array and sub-DAC are combined to reduce the DAC area and power consumption. Charge pumps are used to boost the control voltage of sampling switches. The ADC performs a conversion every 16 clock cycle while being governed by a self-resetting SAR logic. The sampling rate can be scaled up to 32 kHz by varying the clock frequency to accommodate different number of channels used.

The ADC was designed and fabricated in a 0.18 μm CMOS technology. The entire ADC core consumes 1 μW from 1 V supply at a sampling rate of 32 kHz. The ADC has a maximum DNL and INL of 0.55 LSB and 0.75 LSB respectively. The SNDR and SFDR of the converter are measured at a sampling rate of 32 kHz and 15.5 kHz input tone to be 57.9 dB and 68.5 dBFS respectively. The ADC FOM is 51 fJ/Conv-Step.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Joseph F. and Nancy P. Keithley Professor of Electrical Engineering

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Chapter 1

Introduction

Ambulatory monitoring of biopotential signals is crucial for enhancing health care service. It enables better diagnosis and treatment of a disease, delivering remote health service while reducing its overall cost [1].

Figure 1-1 depicts a generic system for vital signal acquisition. It incorporates an analog front-end to amplify the signals produced by the sensors, analog to digital converter and digital signal processor. The system can involve multiple channels that are combined together using multiplexer. Thus, the design of analog to digital converters with ultra-low power dissipation and relatively compact size is mandatory for such systems. The ADC presented in this thesis is utilized in EEG SoC for seizure detection and recording. The design parameters of the ADC are mainly controlled by system specifications which will be presented in the rest of this chapter. However, the final design can be still utilized in various bio-potential acquisition systems that capture signals with similar bandwidth requirements to EEG.

The rest of this chapter derives the main design parameters of the ADC from system requirements. Then a survey of different ADC topologies is presented for architecture selection. The last section provides an overview of thesis organization.

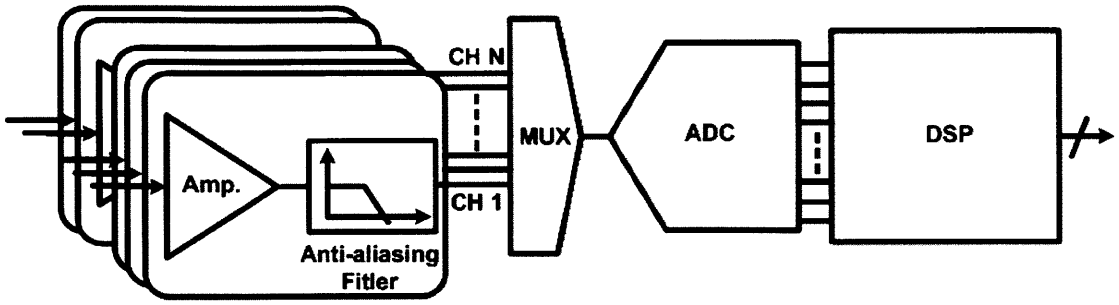


Figure 1-1: Top-level architecture of biopotential acquisition system

1.1 System Requirements

The ADC implemented in this thesis is integrated within a scalable EEG SoC for seizure detection and recording. The full system can capture EEG signals through 1 up to 8 parallel differential channels that are time division multiplexed into a single ADC. The number of the operating channels in the Analog Front-End (AFE) and corresponding ADC sampling frequency are controlled by the Digital Back End (DBE). The ADC supplies the DBE with digital word and an End-of-Conversion (EOC) signal to latch the data. The ADC design parameters are optimized to satisfy the system design requirements and are briefly presented in the next subsections.

1.1.1 Resolution

The ADC resolution is set by the SNR requirements of seizure detection algorithm in the system. A resolution of 10 bits is chosen for this design which is sufficient for extraction of bio-markers for seizure detection by DBE.

1.1.2 Sample Rate

The EEG signal occupies the frequency spectrum from 0.1 to 100 Hz [1]. Thus, the ADC sampling frequency should exceed 200 Hz to satisfy Nyquist requirements. In order to relax the the roll-off of anti-aliasing filters in the AFE, a sampling frequency of 4 kHz is chosen. This allows for optimizing the power consumption and the design

of the whole chip since sharp cut-off analog filters are power consuming. Decimation filter is used in the DBE to minimize the required computation [2].

1.1.3 Scalability

Since the full-chip can be configured to operate one channel only or two or four or eight, the ADC sampling frequency should be scalable. The ADC should have a sampling rate of 4N kHz where N is the number of channels used.

1.1.4 Input Interface

A fully differential ADC architecture is adopted in this design. It enhances the common-mode rejection ratio and eliminates the second order harmonics. This boosts the robustness of the whole system at the expense of higher deign complexity and higher power consumption which will be detailed in chapter 2.

1.1.5 Conversion Plan

The MUX, ADC and DBE should be synchronized for the proper operation of the full system. The ADC is supplied a RST signal at start-up for initialization and a clock signal of scalable frequency. The ADC should provide the DBE with an output and EOC every 16 clock cycles regardless of the number of channels used. Thus, the ADC clock frequency should be equal to 16 times the required sampling rate.

1.2 Architecture Selection

SAR, Pipeline, Sigma-Delta ($\Sigma - \Delta$) and Flash are fundamental architectures of analog to digital converters that cover most of the resolution-bandwidth space in energy efficient way. Figure 1-2 depicts how these architectures typically relate to the ADC resolution and sampling rate [3, 4]. Flash converters can't be utilized for the intended application as they suit low resolution requirements. Pipeline converters are energy efficient at medium-high resolution but at sampling rate in order of Mega samples

per second which don't fit the speed requirements. Oversampling converters such as Sigma-Delta are commonly used at low speed applications but for high resolution requirements for 12 bits or more. SAR ADCs are frequently the architecture of choice for medium to-high-resolution applications with relatively low speed requirements under 5 Mega Samples/Sec. It allows for a FOM in order of femto-joules per conversion step while targeting the required specifications of the EEG SoC [5, 6, 7]. Thus, a SAR ADC architecture is chosen for this design.

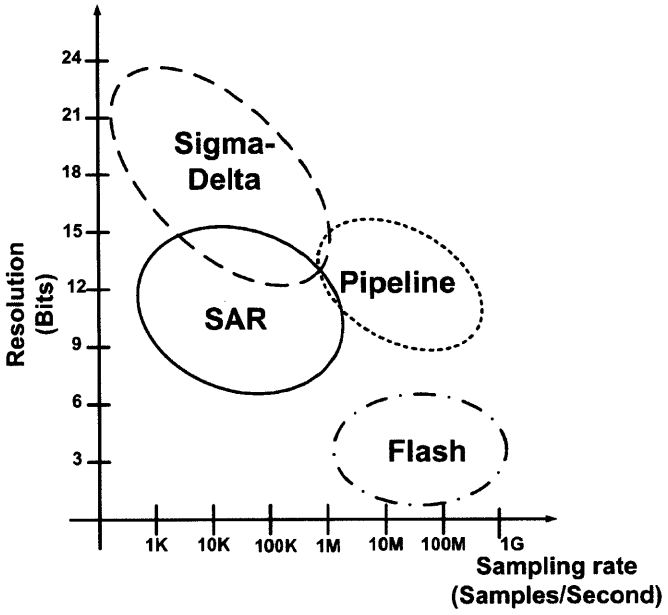


Figure 1-2: ADC architectures comparison

1.3 Thesis Organization

The thesis is organized in four chapters. Chapter 1 serves as the introduction and motivation behind this work. Chapter 2 details the architecture and circuit design of the ADC building blocks. Chapter 3 presents the test-setup and measurements results while chapter 4 provides the conclusion and future work.

Chapter 2

Architecture and Circuit Design

This chapter presents the architecture and the circuit level implementation of the ADC designed in this work. It starts by reviewing the basic operation of conventional SAR ADC in section 2.1. The top level architecture along with the ADC conversion plan are discussed in section 2.2. Section 2.3 to 2.6 details the operation and circuit implementation of ADC building blocks including the binary capacitive DAC, dynamic comparator, charge pumps along with the methodology for sizing the switches. The SAR logic and self-resetting strategy are presented in section 2.7 while section 2.8 provides the summary of the chapter.

2.1 Successive Approximation Conversion Basics

Successive-approximation-register (SAR) ADCs are commonly used for medium to high resolution applications with relatively low speed requirements. It is frequently used for a wide variety of applications, such as portable/battery-powered instruments, industrial controls, and biomedical signal acquisition [8]. In this section, the basic operation principles of single-ended and differential SAR ADC are reviewed.

2.1.1 Single-ended SAR ADC

Figure 2-1 depicts the basic architecture of N-bit SAR ADC. It consists of track/hold circuitry, comparator, N-bit DAC and SAR Logic. Each conversion consists of three main phases: DAC purging (incase of using capacitive DAC) , input sampling and bit-cycling. SAR ADC utilizes a binary search algorithm to generate the digital code during the bit-cycling phase. Figure 2-2 depicts a sample conversion of conventional 4 bit SAR ADC. Each bit of the digital word should be set to 1 on a cyclic basis. If input voltage is greater than the DAC voltage, the bit is permanently set to one otherwise reset back to zero [9].

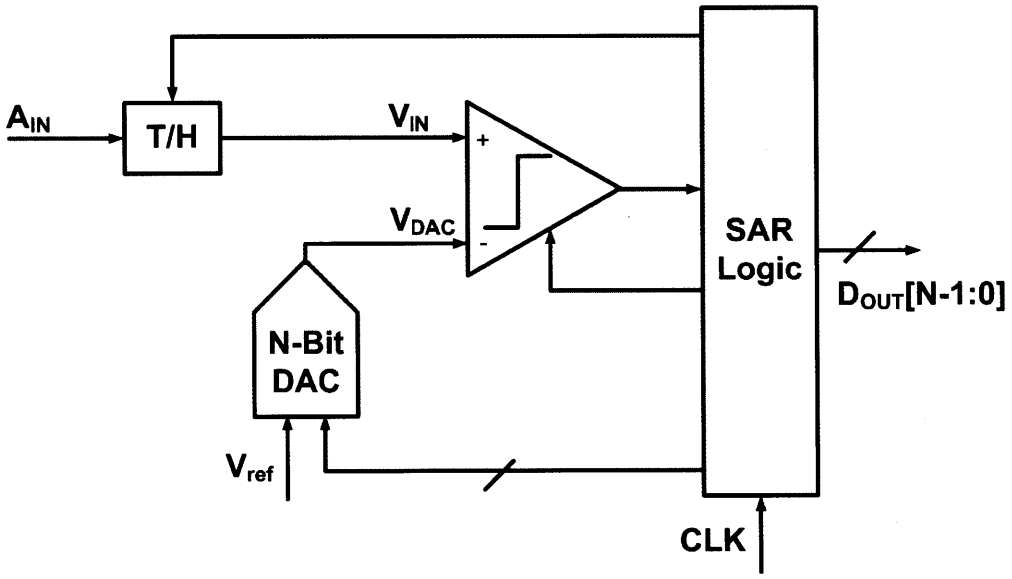


Figure 2-1: Basic architecture of SAR ADC

SAR ADC commonly relies on capacitive DAC that provides inherent track and hold function [8]. Figure 2-3 depicts 4-bit SAR ADC where the DAC consists of an array of 4 binary weighted capacitors plus extra LSB capacitor. The control signals of the switches for purging, sampling and bit-cycling are denoted as PRG, SMPL and BITCYC respectively. The control signal CB for each capacitor identify if it is connected to V_{ref} or ground during each cycle of the bit-cycling phase. The ADC supports input voltage from zero up to the reference voltage V_{ref}. During the purging phase (DAC resetting) the top and bottom plates of the capacitors are shorted to

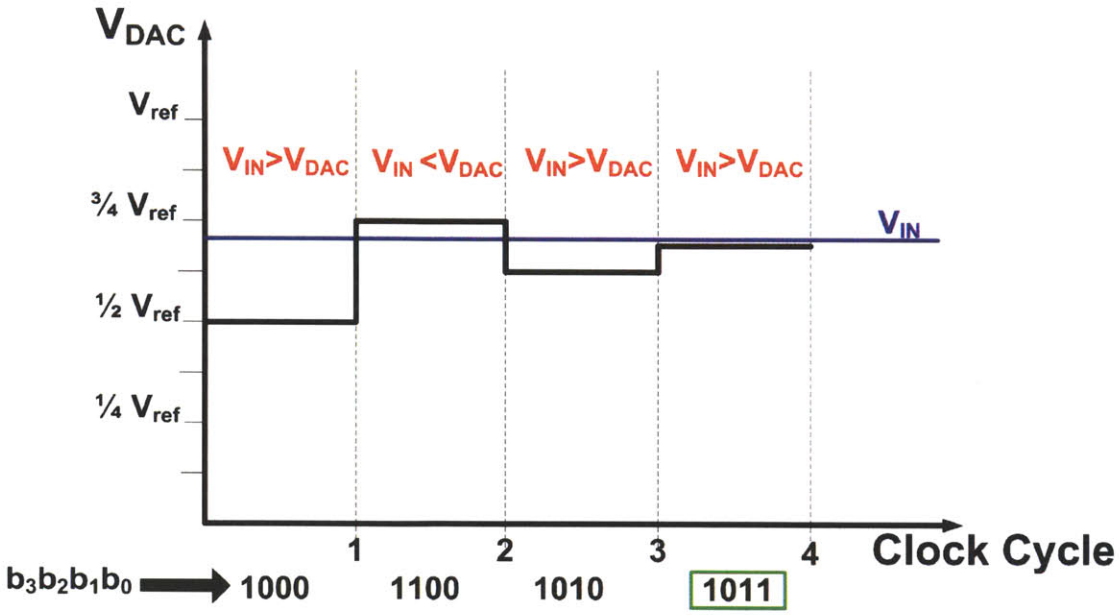


Figure 2-2: Timing diagram of the bit-cycling phase of 4 bit SAR ADC

ground. During the sampling phase, the common top plate is grounded while the capacitors bottom plates are connected to the analog input. By the end of the second phase, the DAC common top plate is disconnected from ground then the bottom plates are grounded to turn the top plate voltage, V_{DAC}, to be equal to $-V_{in}$.

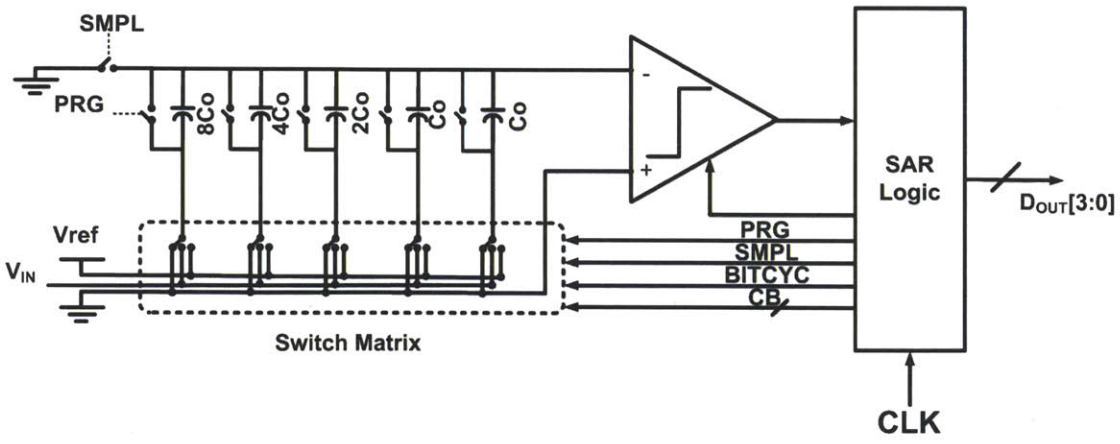


Figure 2-3: 4 bit SAR ADC utilizing binary weighted capacitive DAC

Binary search algorithm is utilized to identify the digital output code which starts by connecting the bottom plate of the MSB capacitor to V_{ref}. DAC performs charge

redistribution and V_{DAC} becomes equal to $-V_{in}+V_{ref}/2$. As in the basic example shown before, if V_{in} is greater than $V_{ref}/2$ i.e. V_{DAC} is less than zero, the MSB bit is set to one otherwise it is reset back to zero. The same procedure is applied to determine the rest of the output code.

2.1.2 Differential SAR ADC

In order to increase the robustness of the whole system, the ADC should support differential analog input as discussed in chapter 1. Figure 2-4 shows an example of 4-bit differential SAR ADC that utilizes a differential capacitive DAC where the ADC differential input voltage range is equal to $\pm V_{ref}$.

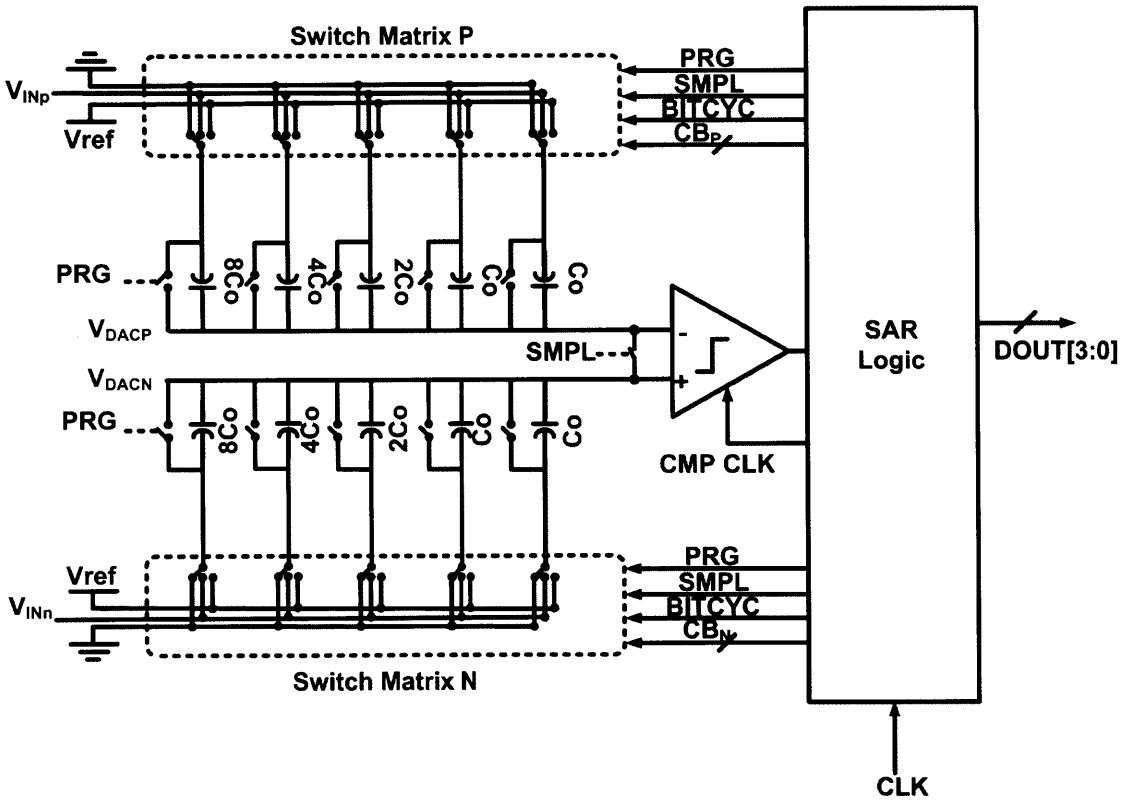


Figure 2-4: Differential 4 bit SAR ADC utilizing binary weighted capacitive DAC

During the purging phase, all the capacitors are shorted to ground to remove stored charges from previous conversion cycles. Then, the ADC samples the differential input signal by connecting bottom plates of the capacitors of the DACp and DACn to V_{INp}

and V_{INn} respectively while shorting their top plates where $V_{DAC,P}$ and $V_{DAC,N}$ settles to the common mode voltage of the input signal.

The bit-cycling phase starts by identifying the MSB bit which acts as the sign of the differential input. Thus, The bottom plate of the MSB capacitor of DACp array is connected to V_{ref} while the rest of the capacitors to ground and the inverse is done to DACn. The comparator generates one if V_{INp}-V_{INn}>0, otherwise it generates zero. It should be noted that the positive input of the comparator is connected to V_{DACN} while the negative one is connected to V_{DACP}. If the comparator generates one, then the MSB is set to 1 and the differential input should be compared to $V_{ref}/2$. This is done in a similar manner to conventional single-ended SAR by connecting the bottom plate of the MSB-1 capacitor in DACp to V_{ref} while doing the inverse to DACn. If the comparator generates zero, then the MSB is set to zero and the differntial input should be compared to -$V_{ref}/2$ and same procedure is applied for the rest of the bits during the bit-cycling phase.

2.2 Global Architecture

Figure 2-5 depicts the global architecture of the 10 bit SAR ADC designed in this work. It includes differential capacitive DAC, digital comparator, SAR Logic and switches. A fully differential architecture is adopted to enhance the common mode rejection ratio as discussed in chapter 1. A binary weighted capacitive DAC is utilized in this design while combining both concepts of sptit-capacitor array and sub-DAC [10].

Figure 2-6 shows the ADC conversion plan where each conversion takes 16 clock cycles. A global active low reset signal (nRST) aligned with the negative clock edge is applied to initialize the registers. The conversion plan includes one clock cycle for purging, two clock cycles for sampling to relax settling time requirements of the capacitor's top plate voltage while the rest of the cycles are used for bit-cycling. The ADC provides the DBE with the End-of-Conversion (EOC) signal as a flag to latch the data at the end of the 16 clock cycles.

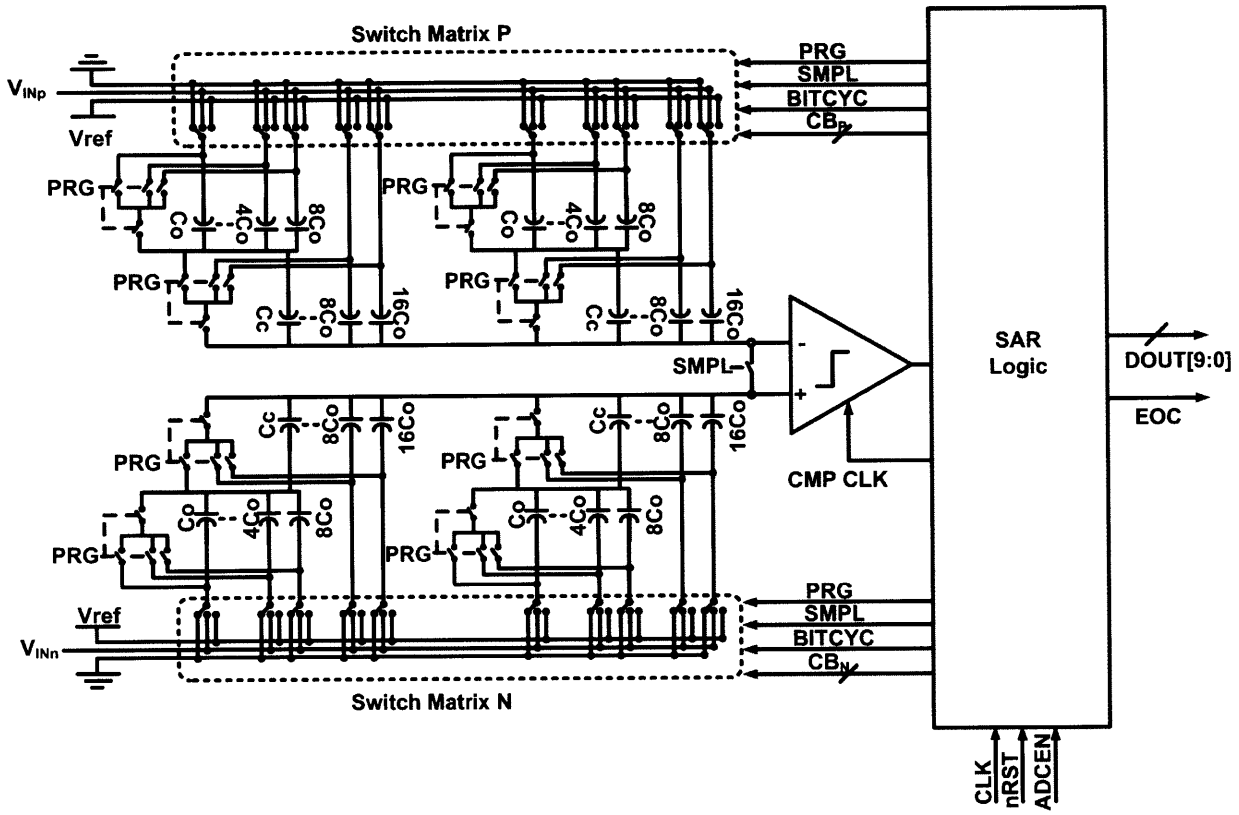


Figure 2-5: ADC architecture

As discussed in the previous section, all the capacitors are shorted to ground during the purging phase to reset the DAC. Figure 2-7 depicts the ADC during the sampling phase where the differential input signal is connected across the bottom plates of the capacitors of the DACp and DACn where $V_{DAC,P}$ and $V_{DAC,N}$ settles to the common mode voltage of the input signal as discussed before.

Since split capacitor array technique is utilized in the design, the operation during the bit-cycling phase slightly differs from conventional differential SAR ADC. The MSB capacitor is split into array identical to the rest of DAC capacitors. The bit-cycling phase starts by identifying the MSB bit as normal by connecting the bottom plates of the capacitors of DACp MSB array to V_{ref} while the rest of the capacitors to ground and the inverse is done to DACn as shown in Figure 2-8. If the MSB is 1, the differential input should be compared to $V_{ref}/2$ by connecting the bottom plate of the MSB-1 capacitor in DACp to V_{ref} while doing the inverse to DACn as shown

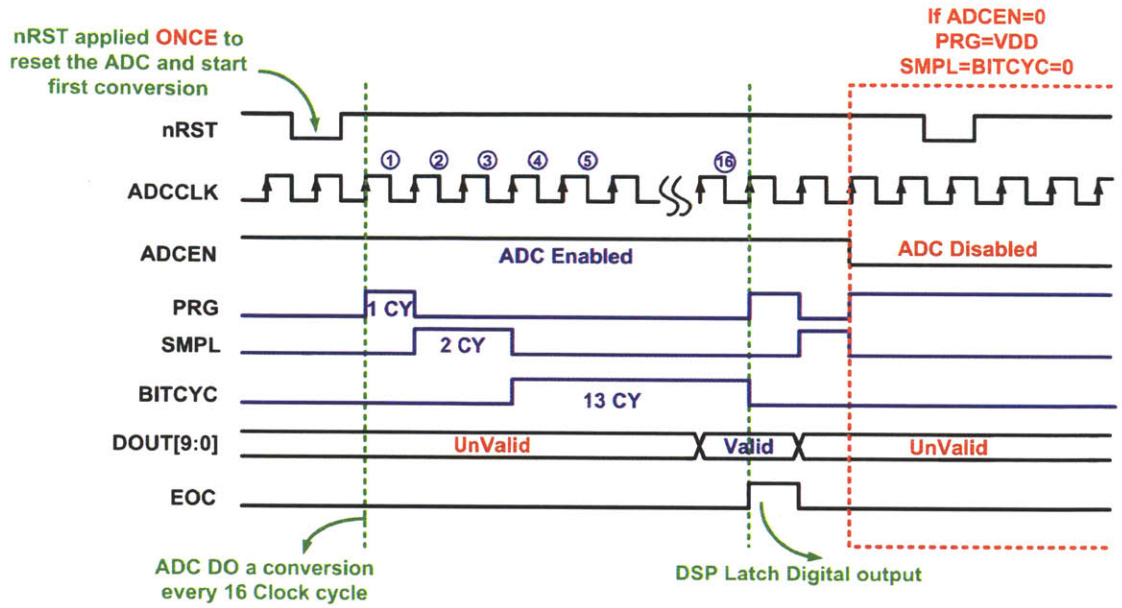


Figure 2-6: SAR ADC conversion plan

in Figure 2-9. On the other hand, if the MSB is zero, the differntial input should be compared to -$V_{ref}/2$. This is done using split-capacitor approach by connecting the bottom plate of the capacitor identical to MSB-1 in the DACp MSB array to ground while doing the inverse to DACn as shown in Figure 2-10.

It should be noted that as long as ADC enable (ADCEN) remains high, the ADC generates a digital word every 16 clock cycles despite the clock frequency used. It self-resets the registers at the end of each conversion to remove stored values. If ADCEN is equal to zero the capacitors bottom plates are connected to ground to disable the ADC from signal path. This feature is added to allow for individual testing of AFE in the whole system by isolating it from the ADC.

2.3 Capacitive DAC

The ADC designed in this work utilizes a fully differential capacitive DAC as shown in Figure 2-5. Its area and power consumption are reduced by combining both techniques of sub-DAC and split-capacitor array [10]. The DAC is composed of 6-bit main DAC and 4 bit sub-DAC where the MSB is built using capacitor array identical to the

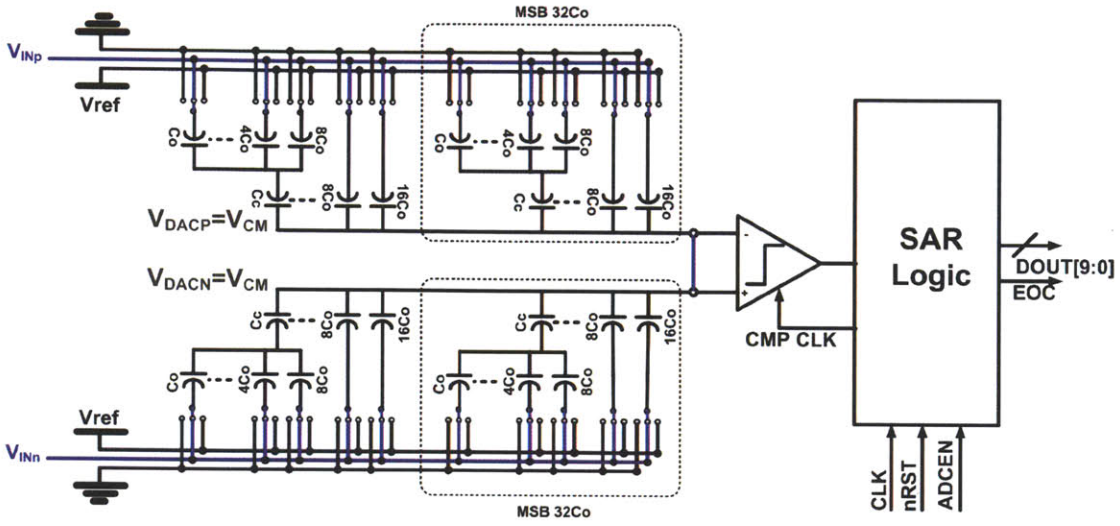


Figure 2-7: ADC during sampling phase (purging switches are not shown for clarity)

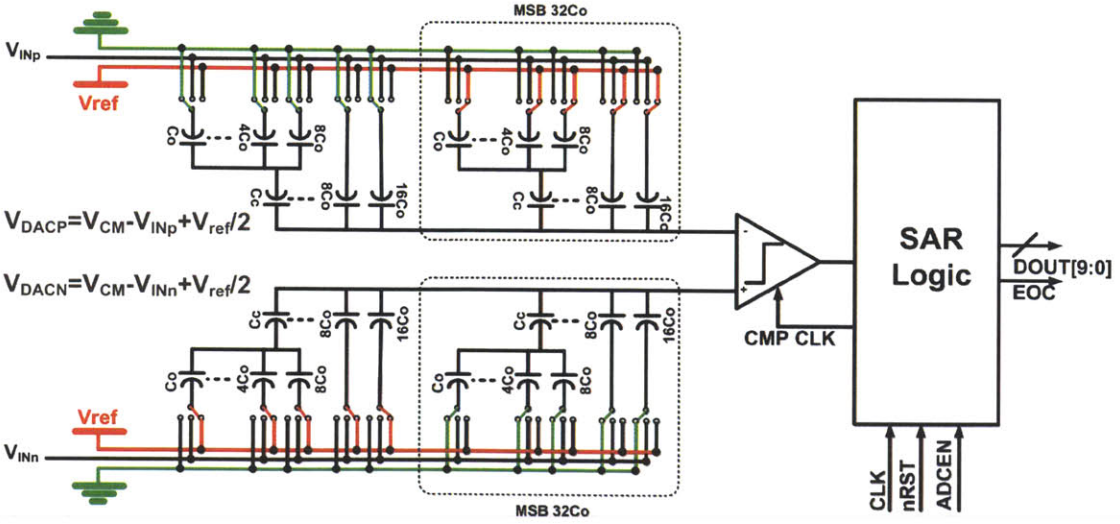


Figure 2-8: ADC during bit-cycling phase of MSB

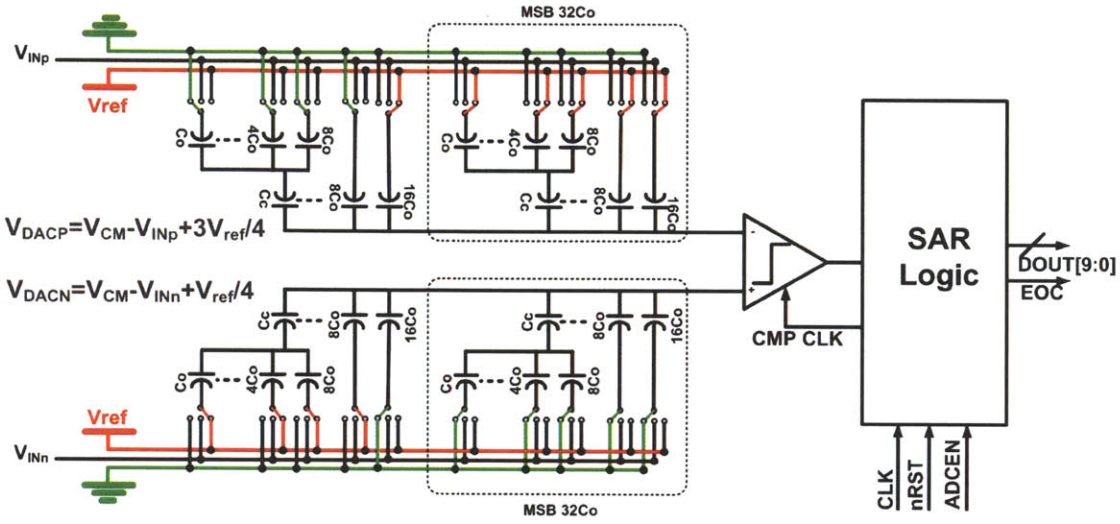


Figure 2-9: ADC during bit-cycling phase if MSB=1

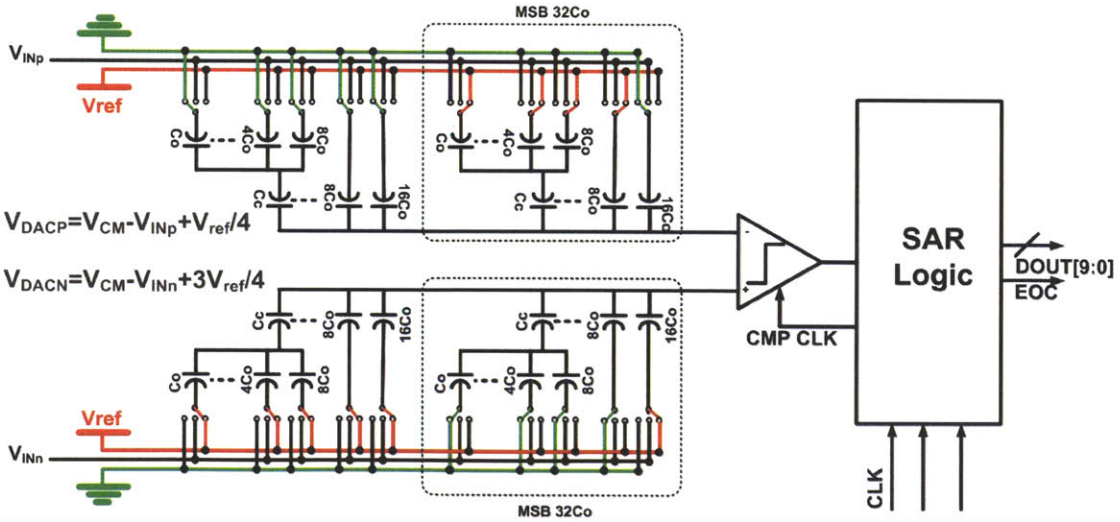


Figure 2-10: ADC during bit-cycling phase if MSB=0

rest of the DAC capacitors. The concepts of sub-DAC and split capacitor array are revised in the following subsections.

2.3.1 Sub-DAC Interpolation

The layout area of SAR ADC employing binary weighted capacitive DAC is usually dominated by the DAC area where the ratio of MSB to LSB capacitor is equal to 2^{N-1} (512 for 10 bit ADC). In order to reduce ADC area, the DAC can be divided into M-bit main-DAC and L-bit sub-DAC connected through a coupling capacitor [11], where the ADC resolution N=M+L. The net effective capacitance of the sub-DAC and coupling capacitor is equal to the unit capacitance used Co. Thus, the coupling capacitor should have a value of $\frac{2^L}{2^L-1}C_o$.

Figure 2-11 shows a single sided DAC split in 6 bit main-DAC and 4 bit sub-DAC. Superposition is applied to understand how each capacitor in main-DAC and sub-DAC affects the voltage V_{DAC}. Figure 2-12 depicts the effective capacitive divider while individually switching the bottom plate of each capacitor in the main-DAC to V_{ref} and the rest of capacitors to ground and assuming that V_{DAC} was initially zero. First, the bottom plate of the MSB capacitor (32Co) is connected to V_{ref}, a capacitive divider by two capacitors each is equal to 32 Co occurs and V_{DAC} is equal to half V_{ref}. If the capacitor 16Co is the one connected to V_{ref}, V_{DAC} is equal to quarter V_{ref} and so on.

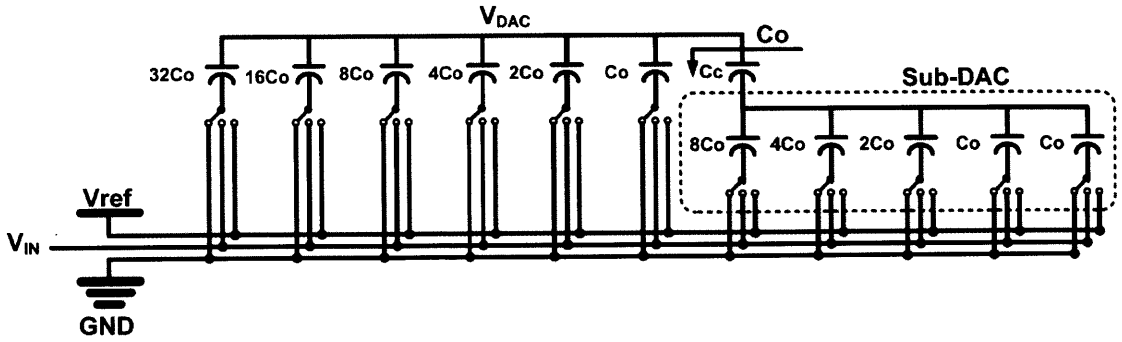


Figure 2-11: Binary weighted DAC with 6 bit main-DAC and 4 bit sub-DAC

Thevenin equivalent should be utilized to apply same procedure for the sub-DAC.

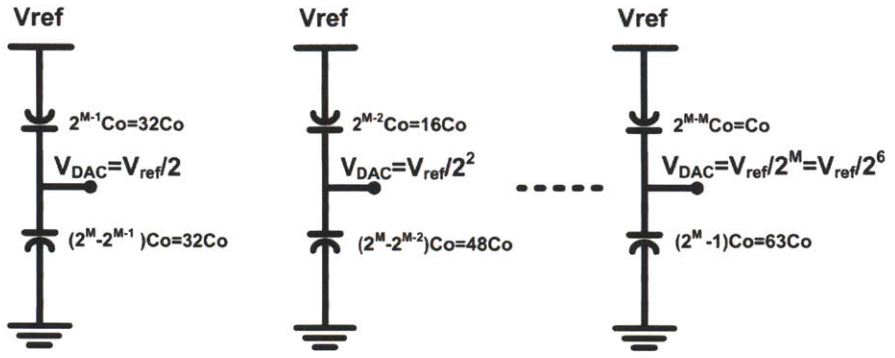


Figure 2-12: The DAC effective capacitive divider while individually connecting the bottom plate of each capacitor in the main-DAC to V_{ref} and the rest of capacitors to ground

Figure 2-13 shows the effective capacitive divider while connecting the bottom plate of the MSB capacitor of the sub-DAC to V_{ref} and the rest of capacitors to ground. The voltage V_{DAC} is equal to $V_{ref}/2$ divided by 2^M which is the half the value yielded by the LSB of the main-DAC. The same analysis can be applied to the rest of the capacitors of the sub-DAC. It should be noted that the thevenin capacitance is the same in all cases.

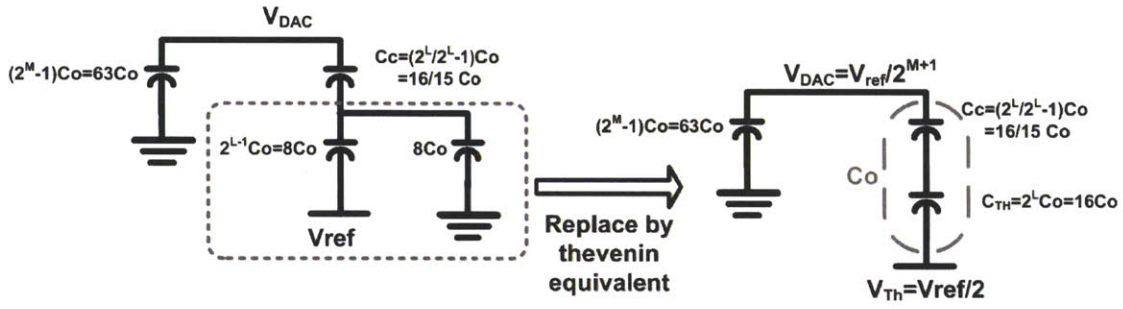


Figure 2-13: Thevenin equivalent circuit for analysing passive sub-DAC

The main problem with sub-DAC interpolation is its sensitivity to the parasitic capacitance from the top plate of sub-DAC capacitors to ground. This leads to INL/DNL errors due to the compression of transition steps by the sub-DAC. However, this problem can be minimized by increasing the size of the coupling capacitor to increase the effective weight of sub-DAC interpolation [11].

2.3.2 Split Capacitor Array

The split capacitor array provides an energy efficient charge recycling approach for the capacitive DAC. It reduces the average switching energy of the DAC by 37% compared to the conventional switching schemes [12]. Figure 2-14 shows an example of split capacitor array applied to 3 bit single-ended binary weighted capacitive DAC. The MSB capacitor ($4C_o$) is split into array identical to the rest of DAC capacitors.

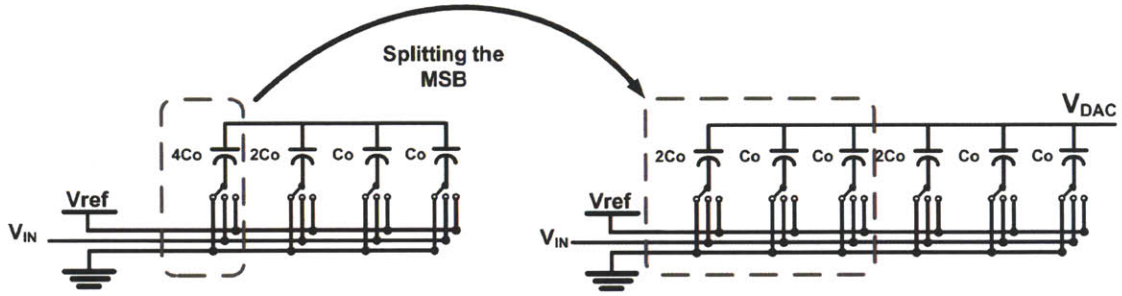


Figure 2-14: Applying split capacitor array technique to 3 bit binary weighted capacitive DAC

During the first step of bit-cycling, the bottom plates of the MSB array are connected to V_{ref} and rest of the capacitors to ground as shown in Figure 2-15 where the DAC top plate voltage settles to $-V_{in}+V_{ref}/2$. The energy drawn from the supply is equal to $2C_oV_{ref}^2$. If $V_{in}>V_{ref}/2$, the MSB bit is 1 and V_{in} should be compared to $3V_{ref}/4$ which is called an "up" transition. On the other hand, if $V_{in}<V_{ref}/2$ the MSB bit is 0 and V_{in} should be compared to $V_{ref}/4$ which is called a "down" transition.

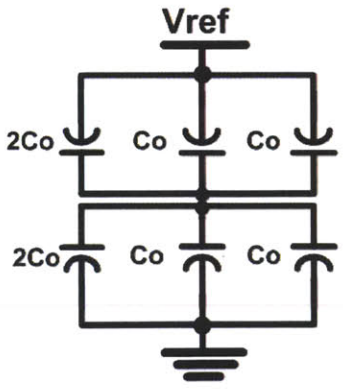


Figure 2-15: Step 1 of bit-cycling: Connecting the bottom plates of the MSB array to V_{ref} and the rest of the capacitors to ground

If the next transition is "up" the MSB-1 capacitor ($2C_o$) is connected to V_{ref} as shown in Figure 2-16 and the energy drawn is equal to $0.5C_oV_{ref}^2$ as given by equation 2.1 which is equal to the one required using conventional method.

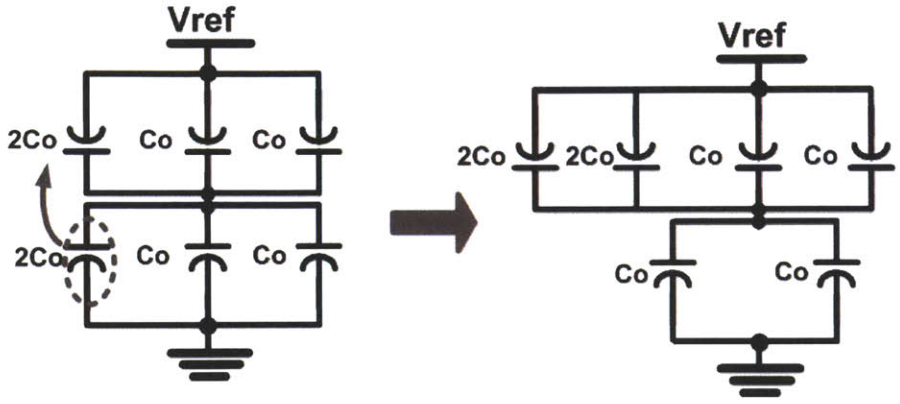


Figure 2-16: Up transition for a split capacitor array

$$E_{drawn}|_{up} = V_{ref}\left[2C_o\left(\frac{3V_{ref}}{4} - \frac{V_{ref}}{2}\right)\right] = \frac{1}{2}C_oV_{ref}^2 \tag{2.1}$$

However, both methods don't require the same energy during a "down" transition to turn the capacitors top plate voltage from $V_{ref}/2$ to $V_{ref}/4$. Figure 2-17 depicts the down transition using conventional switching method where the transition is performed by connecting the bottom plate of the MSB capacitor to ground and connecting the bottom plate of MSB-1 capacitor to V_{ref} where the energy drawn from the supply is equal to $2.5C_oV_{ref}^2$ as given by equation 2.2.

$$E_{drawn}|_{down-conv.} = V_{ref}\left[2C_o\left(\frac{3V_{ref}}{4} - \frac{-V_{ref}}{2}\right)\right] = \frac{5}{2}C_oV_{ref}^2 \tag{2.2}$$

In case of split capacitor array, "down" transition is accomplished by connecting the bottom plate of the capacitor $2C_o$ in the MSB array to ground as shown in Figure 2-18. The energy drawn from the supply is equal to $0.5C_oV_{ref}^2$ which is equal to the one required in case of "up" transition in this case. Energy is only utilized to derive the change in V_{DAC} while saving any energy for charging capacitors to V_{ref} [12].

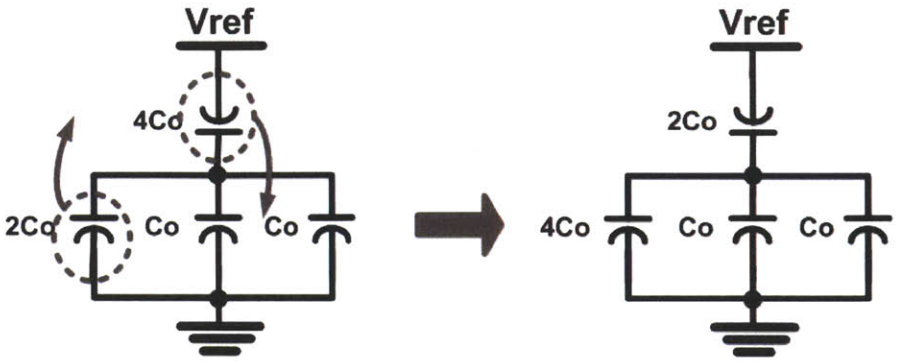


Figure 2-17: Down transition using conventional switching method

$$E_{drawn}|_{down-split} = V_{ref}\left[2C_o\left(\frac{3V_{ref}}{4} - \frac{V_{ref}}{2}\right)\right] = \frac{1}{2}C_oV_{ref}^2 \tag{2.3}$$

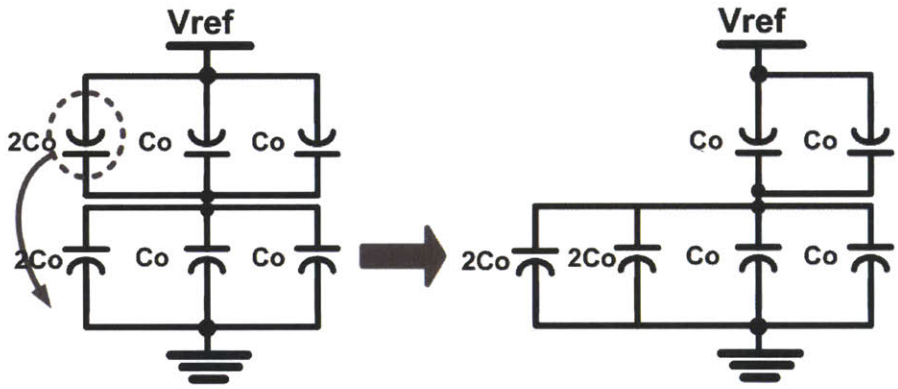


Figure 2-18: Down transition using split capacitor array

2.3.3 DAC Layout

The DAC is the most critical part of the ADC layout as it has a prominent impact on its linearity. Figure 2-19 depicts common-centroid layout of main-DAC and sub-DAC while surrounding them with dummy grounded capacitors. Since capacitors in the center of the array couple to neighbouring capacitors which are not at grounded, while those at the edge couple to the dummy capacitors, therefore the capacitor distribution is carefully made to target equal-edge ratio [11]. A grounded metal shield is used to decrease the coupling between the top and bottom plate routing [10].

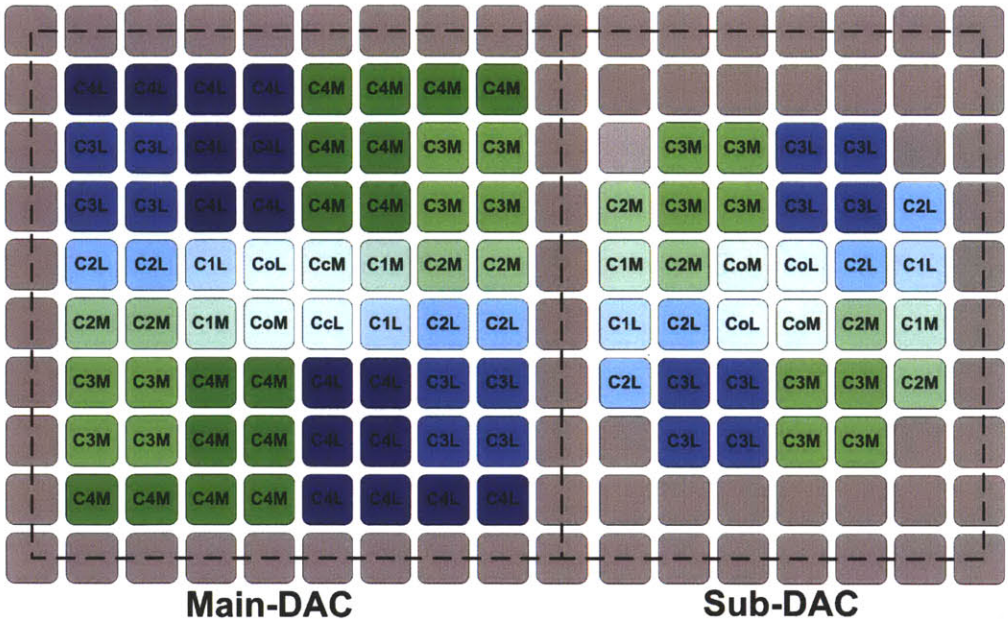


Figure 2-19: DAC common-centroid Layout with minimized edge effect

2.4 Comparator

Figure 2-20 depicts the dynamic latched comparator utilized in this work [10]. It enables ultra low power operation by eliminating the need for static bias current. When the CLK is high, all the internal nodes are grounded to eliminate any memory from previous comparisons. When the CLK turns low, the top PMOS transistor turns on and the input PMOS pair starts to pull-up the nodes OUT+ and OUT- at different rates depending on V- and V+ respectively. The cross coupled inverters latch when either OUT+ or OUT- reaches the inverter threshold.

Cross-coupled NAND gates are used as SR latch to store the output of the comparator then keep it fixed in the reset phase. Inverters are used in between to prevent output glitching while the comparator is latching. Figure 2-21 shows a sample of the transient waveforms of the comparator while using a 512 kHz clock.

This type of comparators suffers mainly from two main problems: the input-referred offset and kick-back noise. The transistors are sized to keep the 3σ of the offset close to 50 mV. Figure 2-22 depicts the histogram of the comparator offset while using 1000 monte carlo iterations where the standard deviation is equal to 17.5

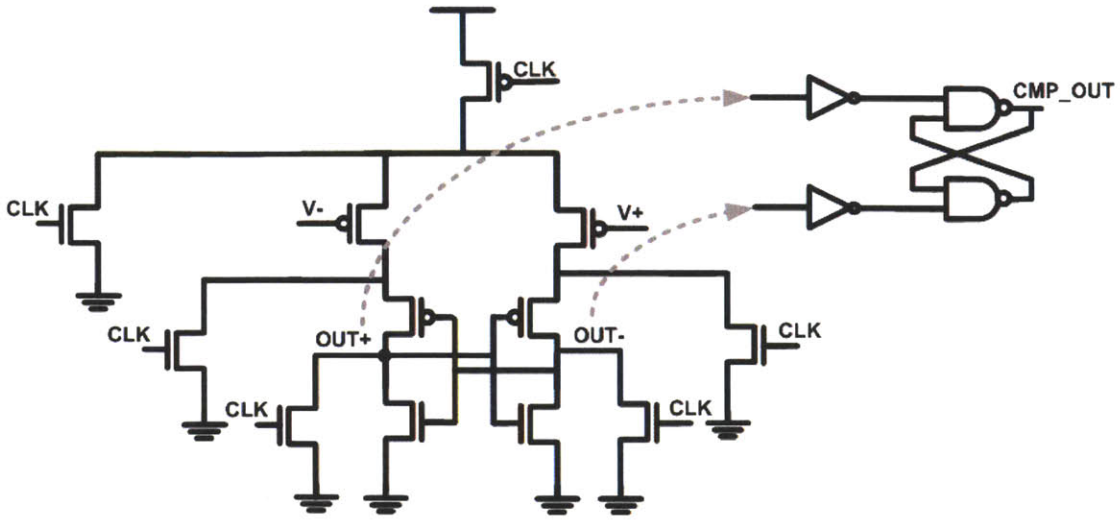


Figure 2-20: Schematic of dynamic latched comparator

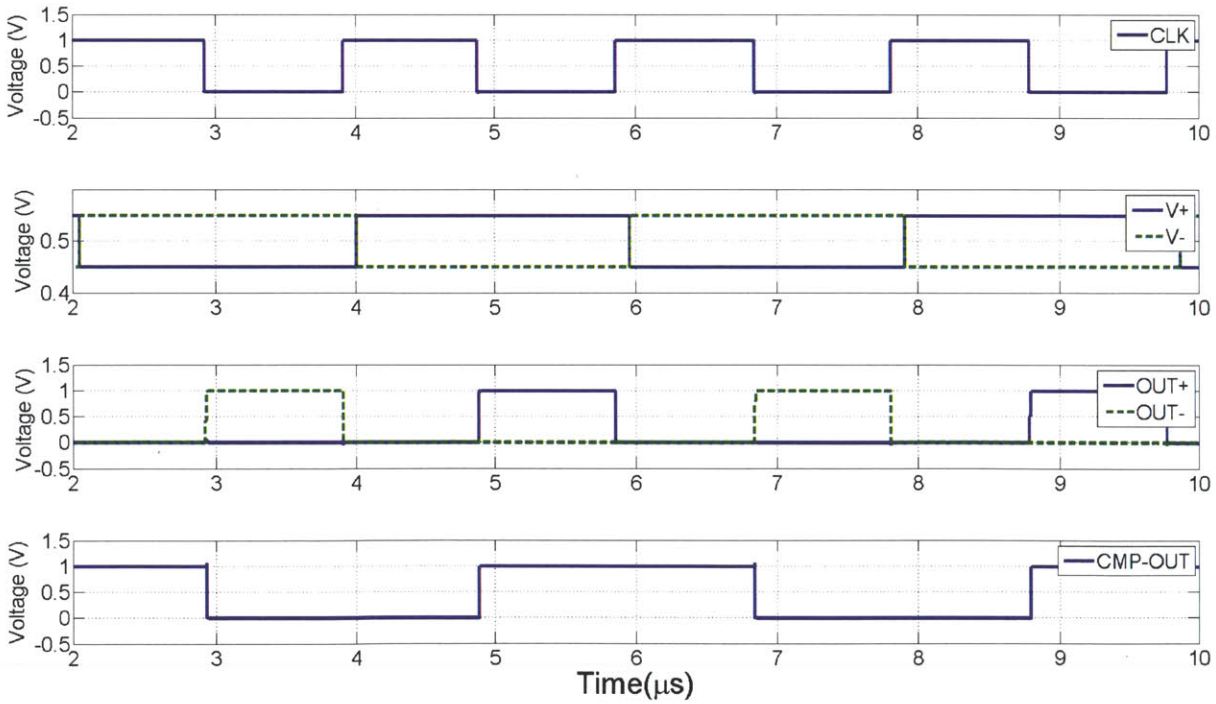


Figure 2-21: Comparator sample transient waveforms while using 512 kHz Clock

mV. Offset compensation is done with the aid of DBE for the ADC in the signal path by adding a fixed digital word, corresponding to the static offset of the ADC, to the output code. Kickback noise has little effect on the operation owing to the differential DAC where noise is roughly common mode when the output nodes begin to rise [10].

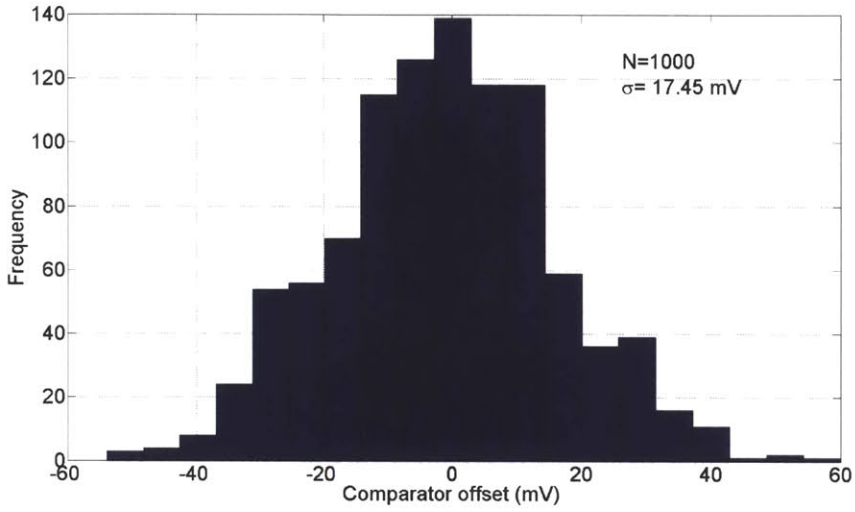


Figure 2-22: Histogram of the comparator input refered offset using 1000 monte carlo iterations

2.5 Switches

Switch matrices are used in SAR ADC for performing purging, sampling and bit-cycling. Figure 2-23 depicts the set of switches connected to the bottom plate of each capacitor. It includes NMOS switch for shorting the capacitors to ground during purging, CMOS transmission gate for sampling and NMOS and PMOS transistors for bit-cycling. Design considerations for each type of the switches are detailed in the following subsections.

2.5.1 Purging Switches

DAC purging is done by connecting the bottom plate of each capacitor to ground and shorting its top and bottom plates. When purging signal (PRG) is equal to V_{DD}, the

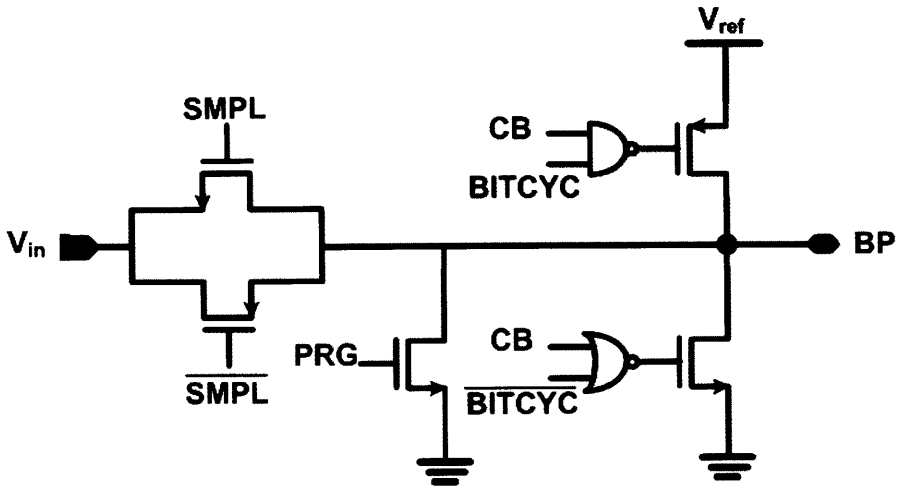


Figure 2-23: Switches connected to the bottom plate of each DAC capacitor

NMOS swich connected to the capacitor bottom plate should be turned on in addition to another switch in parallel with each capacitor. The impact of the parasitics due to purging switches can be minimized as the top plates of the capacitors of the main-DAC are all shorted. Figure 2-24 depicts the switches required for shorting the main-DAC where a single transistor is connected to the main-DAC top plate is in series with a set of transistors that are individually connected to the capacitors bottom plates [11]. The same procedure can be applied to the capacitors of the sub-DAC.

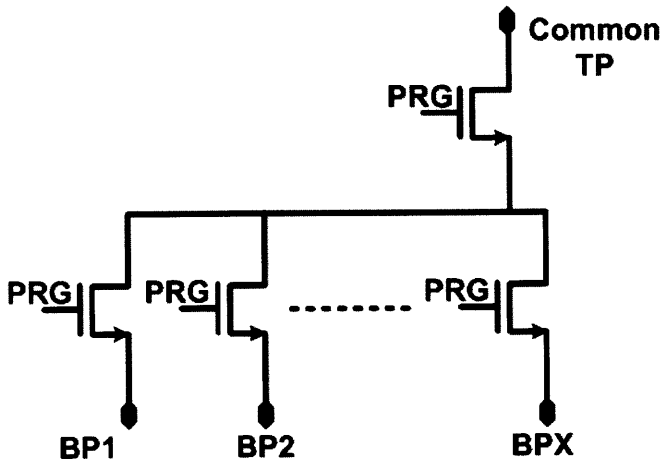


Figure 2-24: Purging switches for array of capacitors with common top plate (TP)

2.5.2 Sampling Switches

During the sampling phase, DACp and DACn top plates are shorted and the input analog signal is applied across the differential DAC through CMOS transmission gates as shown in Figure 2-26. The transistors should be sized such that the total harmonic distortion (THD) due to sampling switches is at least 10 dB better than the required SNDR at the desired input frequency range. Moreover, the switches worst case resistance should allow for 10 bit settling within the period of the sampling phase [10]. These requirements are achieved by properly sizing the PMOS, and boosting the control voltage of NMOS using charge pumps. Figure 2-25 depicts the voltage of V_{DACP} and V_{DACN} while enabling and disabling the charge pumps during the sampling of a differential input of 1 V with a common mode voltage of 0.5 V using 512 kHz clock. As shown in Figure, boosting the control voltage guarantees that transistors aren't driven in sub-threshold when the voltage at the source and drain of the transistors is close to mid-rail.

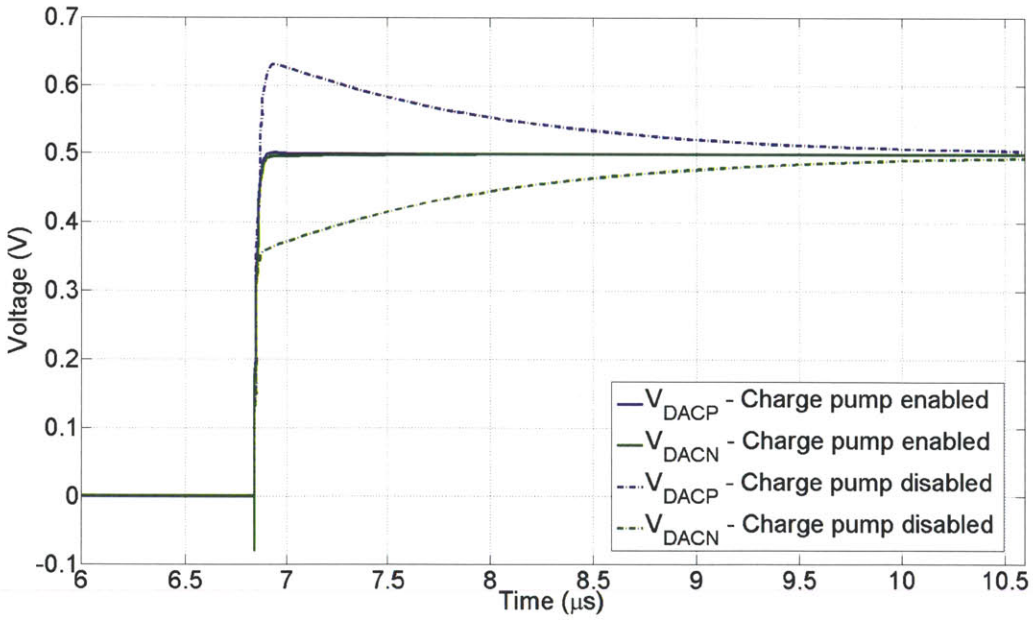


Figure 2-25: V_{DACP} and V_{DACN} while enabling and disabling the charge pumps during the sampling of a differential input of 1 V with a common mode voltage of 0.5 V using 512 kHz clock

It should be noted that the top-plate sampling switch must turn off before the input switches turn off. This help in minimizing the mismatch between the charge injected on the positive and negative arrays due to the top plate switch [11].

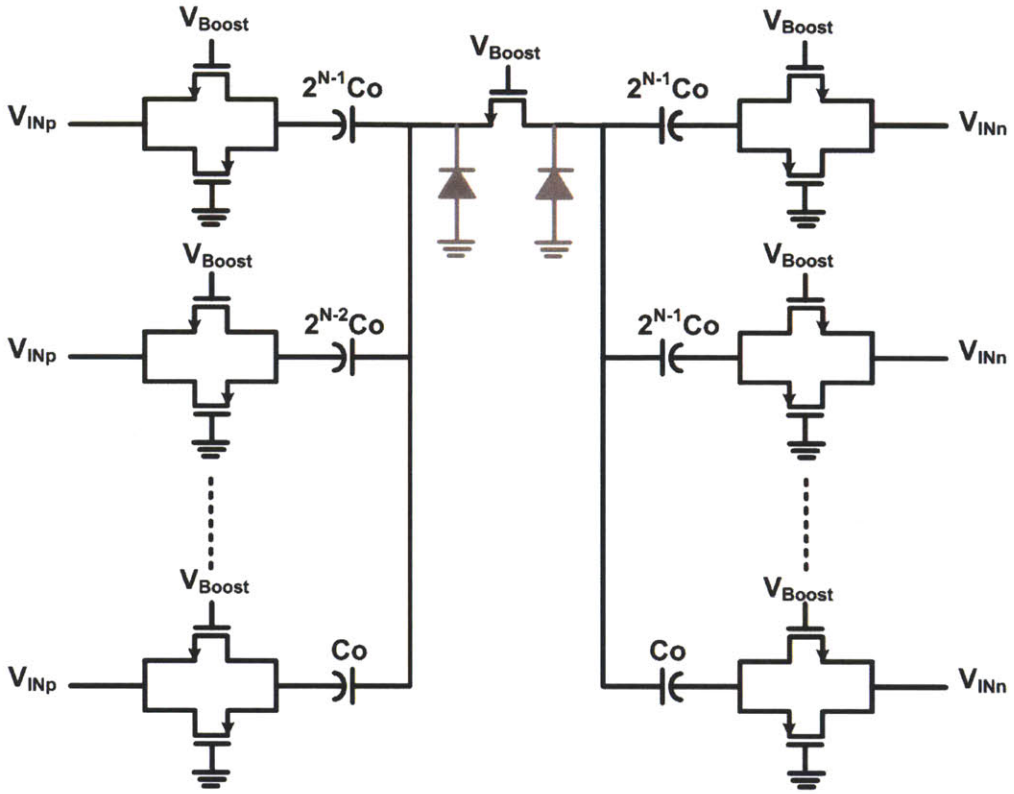


Figure 2-26: Binary DAC during sampling

2.5.3 Reference Switches

The reference switches are used to connect the bottom plate of the capacitors either to V_{ref} or ground during the bit-cycling phase. The major problem during the bit-cycling occurs due to the source-drain region of the top-plate sampling switch which introduces parasitic PN-junctions on the critical top-plate nodes as shown in Figure 2-26. Thus, when the sampling switches are open and the bottom plates are driven to V_{ref} or ground, the top plate voltage may undershoot instantly below zero specially while bit-cycling the MSB. This can forward bias the PN junctions yielding a loss in the top-plate charge. PMOS transistor should sized to be much stronger than NMOS

such that the top-plate voltage never undershoots below ground, and no charge is lost [11].

2.6 Charge Pump

Charge pumps are used to boost the control voltage of the NMOS sampling switches as discussed in the previous section. Figure 2-27 depicts the schematic of the charge pump utilized in this work while Figure 2-28 shows the voltage at various nodes during different phases of operation [13]. When the input voltage is zero, transistors MN1, MN2, MP2 are turned on and the capacitor C_{BS} is charged to V_{DD} which is equal 1 V. When input is switched to V_{DD}, transistors MP3, MP1 turn on while MN1, MN2 and MP2 are turned off and the output voltage goes up to $2V_{DD}$. Figure 2-29 depicts the input and output voltage which was boosted to 1.9 V only due to the charge sharing between capacitor C_{BS} and load capacitance.

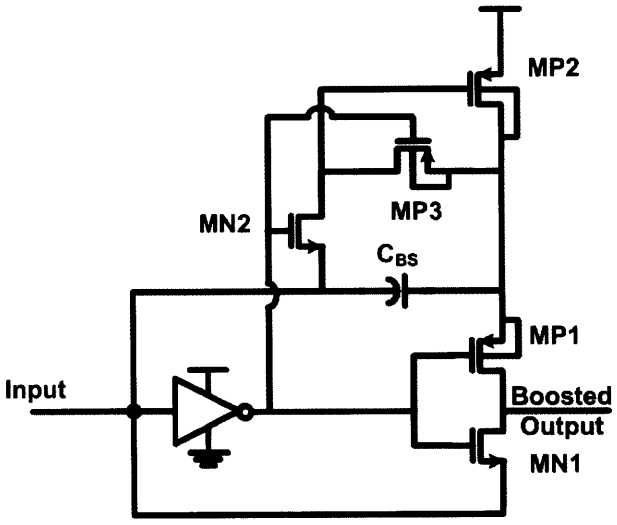


Figure 2-27: Schematic of the charge pump used to boost the input sampling switches

2.7 SAR Control Logic

The SAR logic is responsible for generating the control signals that govern the ADC conversion process every 16 clock cycles. It consists mainly of a sequencer for time

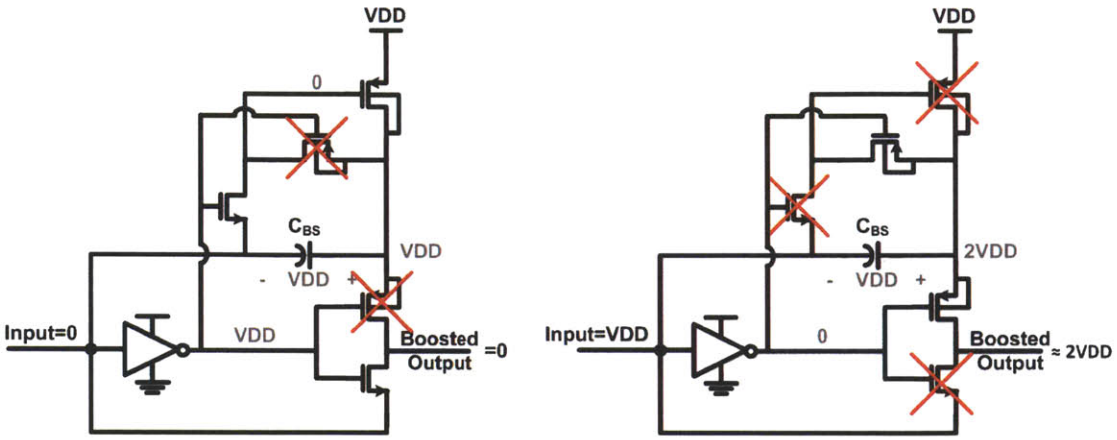


Figure 2-28: Charge pump operation

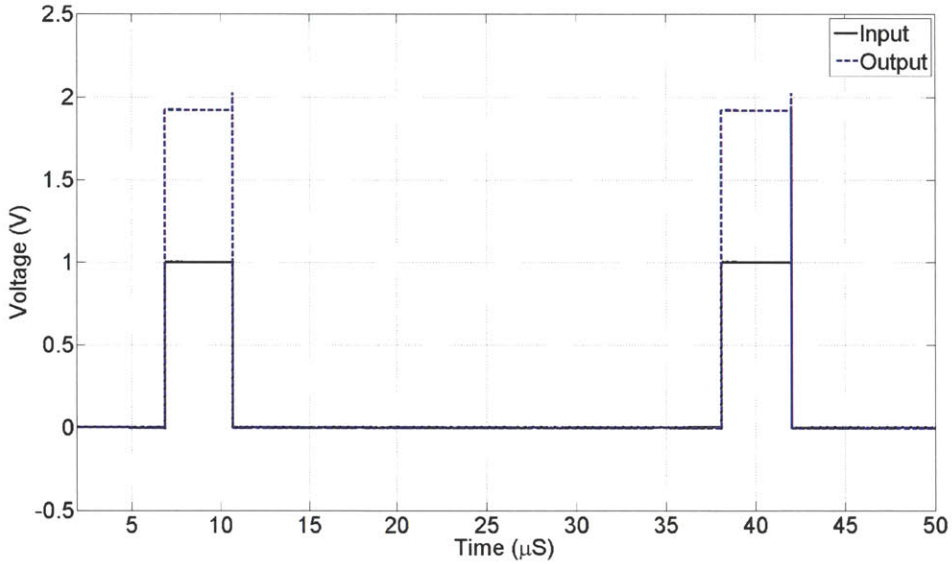


Figure 2-29: Simulation of the input and output voltage of charge pump

management and output data register [14].

The sequencer consists of a cascade of positive-edge triggered flip-flops where the input of the first register is tied to V_{DD} as shown in Figure 2-30. After the global reset of the registers, the outputs of the flip-flops go high sequentially as shown in Figure 2-31. The generated signals set the time length of ADC conversion phases in addition to triggering the data register to store the output of comparator.

Figure 2-30 depicts how the output of the sequencer control the purging, sampling

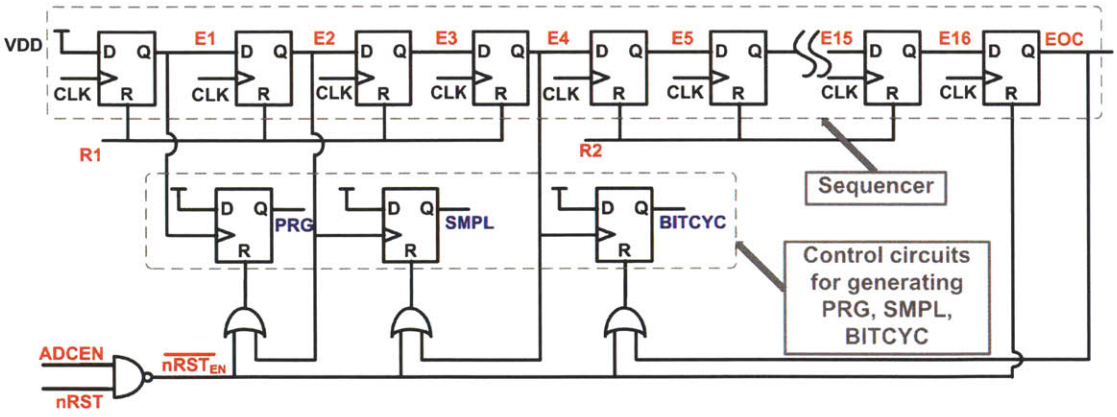


Figure 2-30: SAR sequencer and logic for generating PRG, SMPL and BITCYC

and bit-cycling with the aid of extra control circuits. When signal E1 goes high, purging signal goes and remains high till signal E2 goes from low to high. The same principal is used with signals E2, E4 to generate the sampling signal with a width of two clock periods while E4 and End of Conversion (EOC) are used for generating the bit-cycling signal.

It is important to ensure that PRG, SMPL and BITCYC aren't high simultaneously. This issue is critical while SMPL signal is going low and BITCYC is going high as the sampling switches are driven by slow charge-pumps [11]. Figure 2-32 depicts the circuit used to prevent the overlap of SMPL and BITCYC. If the effective SMPL signal out of the charge pump is high, the output $BITCYC_{op}$ of the NOR gate is forced to be low while the circuit just act as cascade of two inverters if SMPL is low.

The data register is used to store the output of digital comparator during the bit-cycling phase to form the digital output vector [14]. It consists of ten flip-flops whose inputs are tied to the output of the comparator and clocked by outputs of the sequencer as shown in Figure 2-33. The outputs of the data register [B9:B0] are initialized to zero during the sampling phase.

Figure 2-34 shows the timing diagram of the register during bit-cycling. As an example, when E6 goes high, the first flip-flop stores the output of the comparator which is the MSB bit. Two clock cycles are provided for the cycling of MSB and MSB-1 to relax settling time constraints.

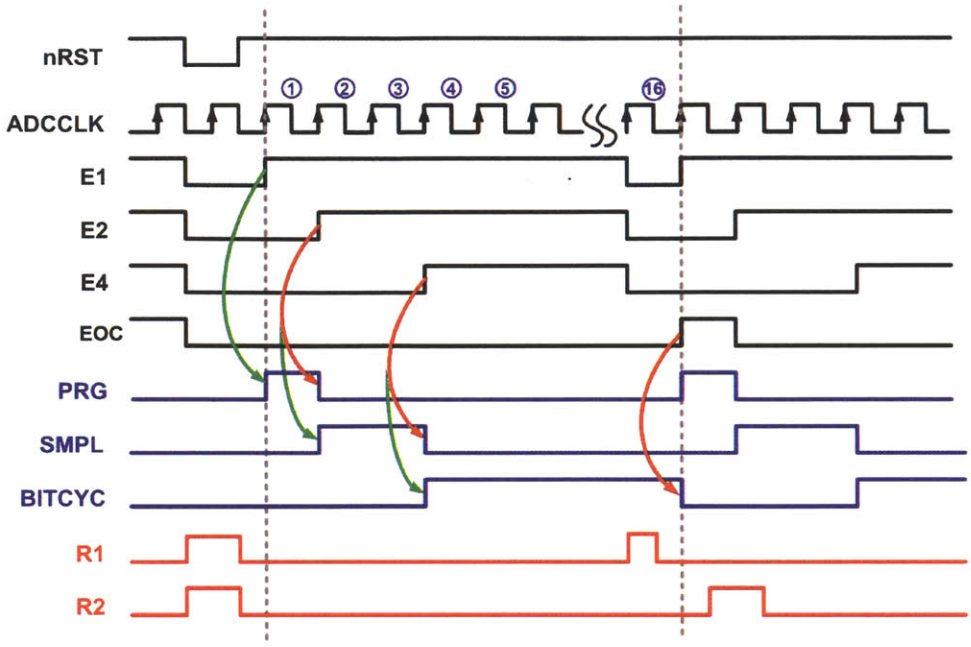


Figure 2-31: Sequencer timing diagram and overhead circuit to generate purging signal

Figure 2-32: overlap prevention of BITCYC and SMPL signal

The control signals of the MSB array and LSB array in both DACp and DACn are generated using the outputs of the sequencer and the data register during the bit-cycling phase as shown in Figure 2-33 [10]. While cycling the MSB, CB9[8:0] is set high while CB[8:0] is forced low due to the initialization of the registers. When E6 goes high, CB9[8] and CB[8] would be equal to the comparator output. Thus, if MSB=1 then CB9[8]=CB[8]=1 performing an transition while if MSB=0 then CB9[8]=CB[8] are set zero for a "down" transition. The same concept is applied for the rest of the DAC control signals. Delay elements are utilized to prevent glitching in CB9[8:0].

It should be noted that the comparator clock is gated using BITCYC signal as shown in Figure 2-35. During the purging and the sampling phase, the comparator CLK is forced to be high in order to keep the comparator in the reset phase.

At the end of each conversion cycle, the SAR logic self-resets itself using signals

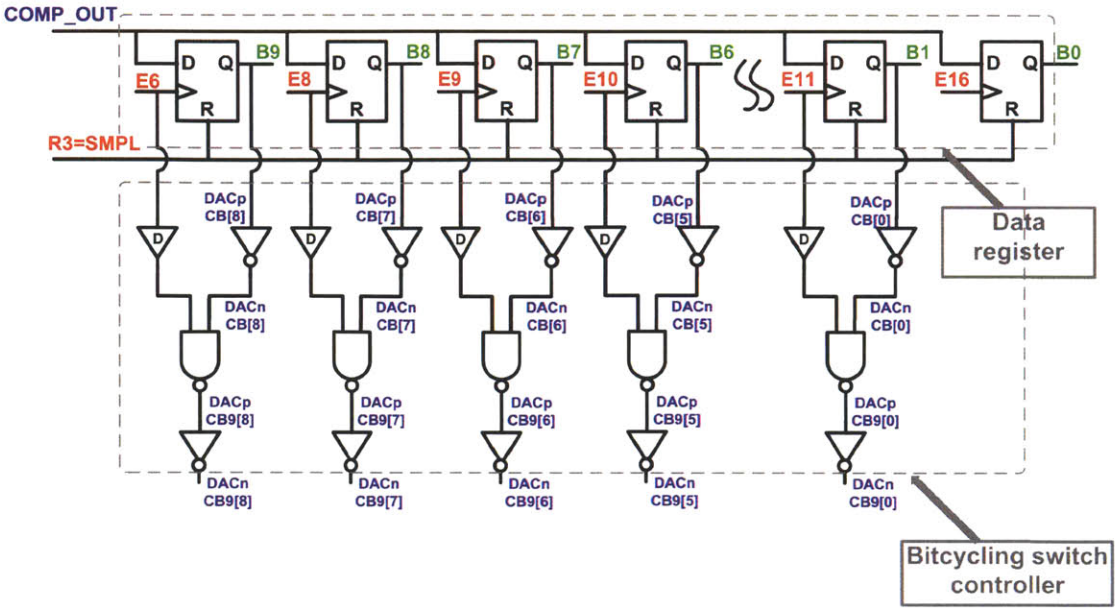


Figure 2-33: Data register for storing output of the comparator during bit-cycling and logic for generating the DAC control signals during bit-cycling

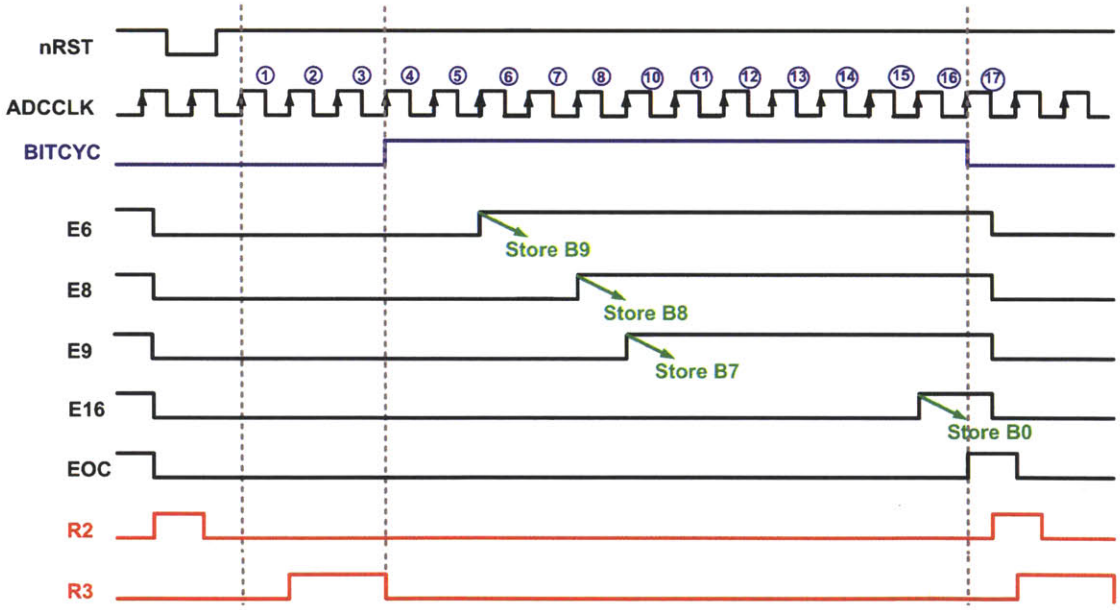


Figure 2-34: Data register timing diagram during bit-cycling

R1, R2, R3 to restart the conversion cycle while eliminating the need for external conversion signals. These signals are generated internally in an orderly fashion as shown in Figure 2-36 while R3 is the SMPL signal. The resetting of the sequencer

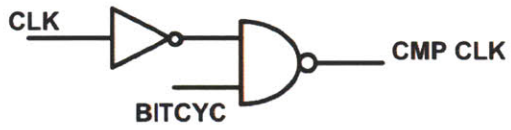


Figure 2-35: Generation of comparator clock

is carefully done on two stages as this process is running in parallel with the ADC conversion cycle which is time managed by the sequencer itself.

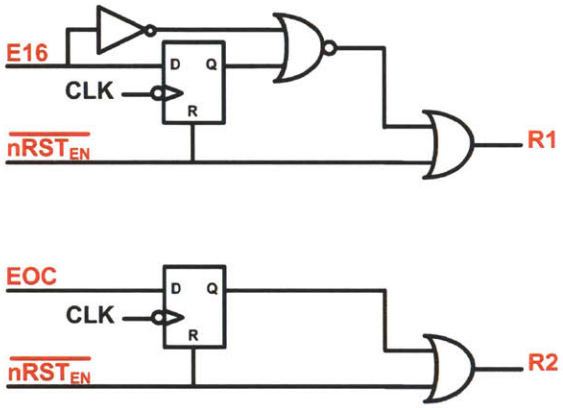


Figure 2-36: Generation of internal reset signals

The timing diagram of the reset strategy is shown in Figure 2-37. If the ADC is enabled and nRST signal is is low, R1 and R2 will go high to reset the sequencer and registers responsible for generating PRG, SMPL and BITCYC. When nRST signal is equal to 1, the outputs of the sequencer goes high sequentially as desired with the positive clock edge. When signal E16 makes transition from 0 to 1, signal R1 goes high to reset the first part of the sequencer responsible for generating E1 to E4. Signal R2 goes high by sampling the EOC signal with negative clock edge to reset the second half of the sequencer that is responsible for generating E5 to E16. By resetting E16, EOC turns low with the next positive clock edge and consequently R2 with the following negative clock edge. Signal R3 resets the data register during the sampling phase to remove any stored valued before bit-cycling.

If the ADCEN is equal to zero, the ADC should be disabled from the signal path and the DAC capacitors should be grounded. This condition is obtained by resetting the sequencer outputs as shown in Figure 2-30 while the effective purging signal is

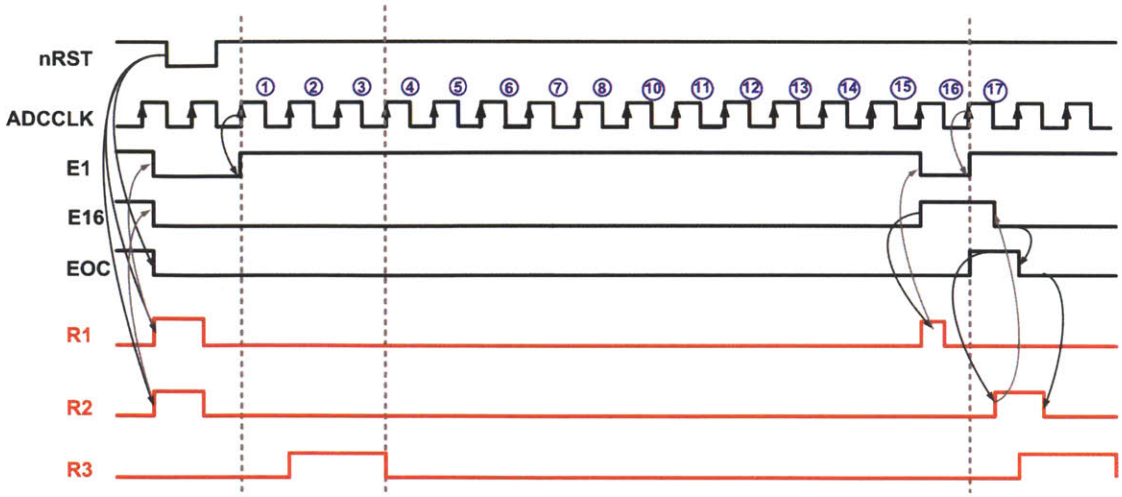


Figure 2-37: Timing diagram of reset strategy

obtained using the circuit shown in Figure 2-38.

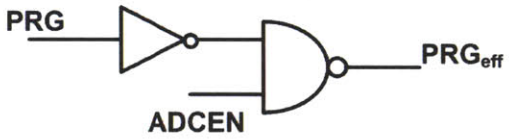


Figure 2-38: Generation of effective purging signal

2.8 Summary

This chapter presented the architecture and circuit design details of the ADC building blocks. Global architecture was presented along with the ADC conversion plan. A review of sub-DAC interpolation and split-capacitor array was provided. Transistor level implementation of the comparator was shown in addition to the sizing methodology of the switches. The design and operation of the charge pumps was also discussed. Finally, the SAR logic design was provided along with its self reset strategy.

Chapter 3

Testing and Characterization

The EEG SoC was designed and fabricated in 0.18 μm CMOS process. Figure 3-1 shows annotated micrograph of the entire EEG SoC which has an area of 5mm x 5mm. The chip incorporates two copies of the ADC, one in the signal path and a stand-alone ADC for characterization. This chapter presents the test setup and measurements results of the ADC designed in this work. The ADC performance parameters including offset, DNL/INL, SNDR , FOM and power consumption are summarized at the end of this chapter along with a comparison with the state-of-the art. Figure 3-2 shows annotated micrograph of the full ADC where it occupies a total area of 290μm x 330μm.

3.1 Test Setup

Figure 3-3 depicts the schematic of the ADC test setup. The Sinusoidal differential input is provided using Tektronix arbitrary function generator AFG3102. Discrete low pass filters where added on board to filter high frequency noise. Tektronix pattern generator and logic analyzer TLA7102 are used for generating the reset and clock signals and capturing the output of the ADC. The outputs of the pattern generator are level shifted to 1 V using on board resistive dividers. On chip serializer is used to capture the ADC output using one pin due to limitation of pads within the chip. Keithly 2400 sourcemeter is used to power the ADC while I/O and serializer are

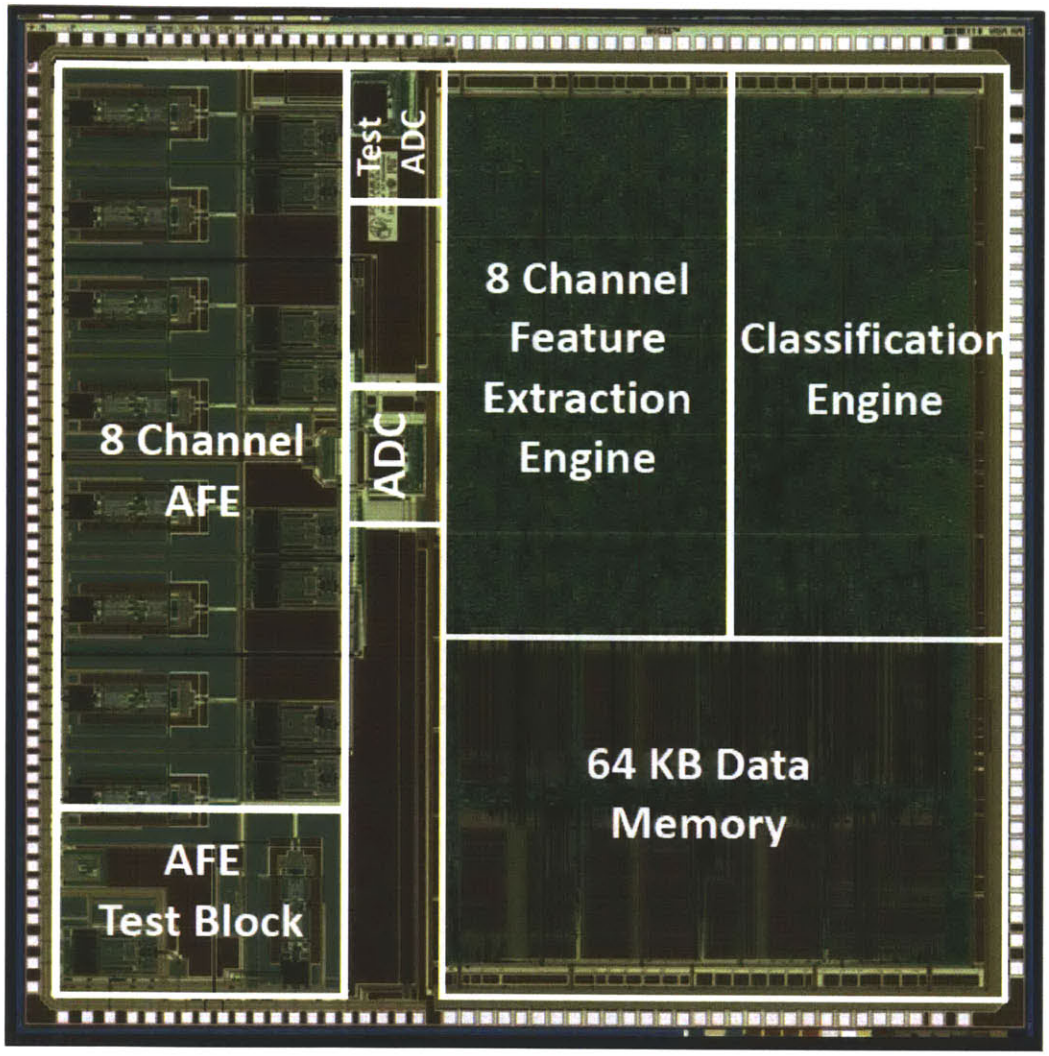


Figure 3-1: Micrograph of the full chip, courtesy of Prof. Jerald Yoo at Masdar Institute of Science and Technology

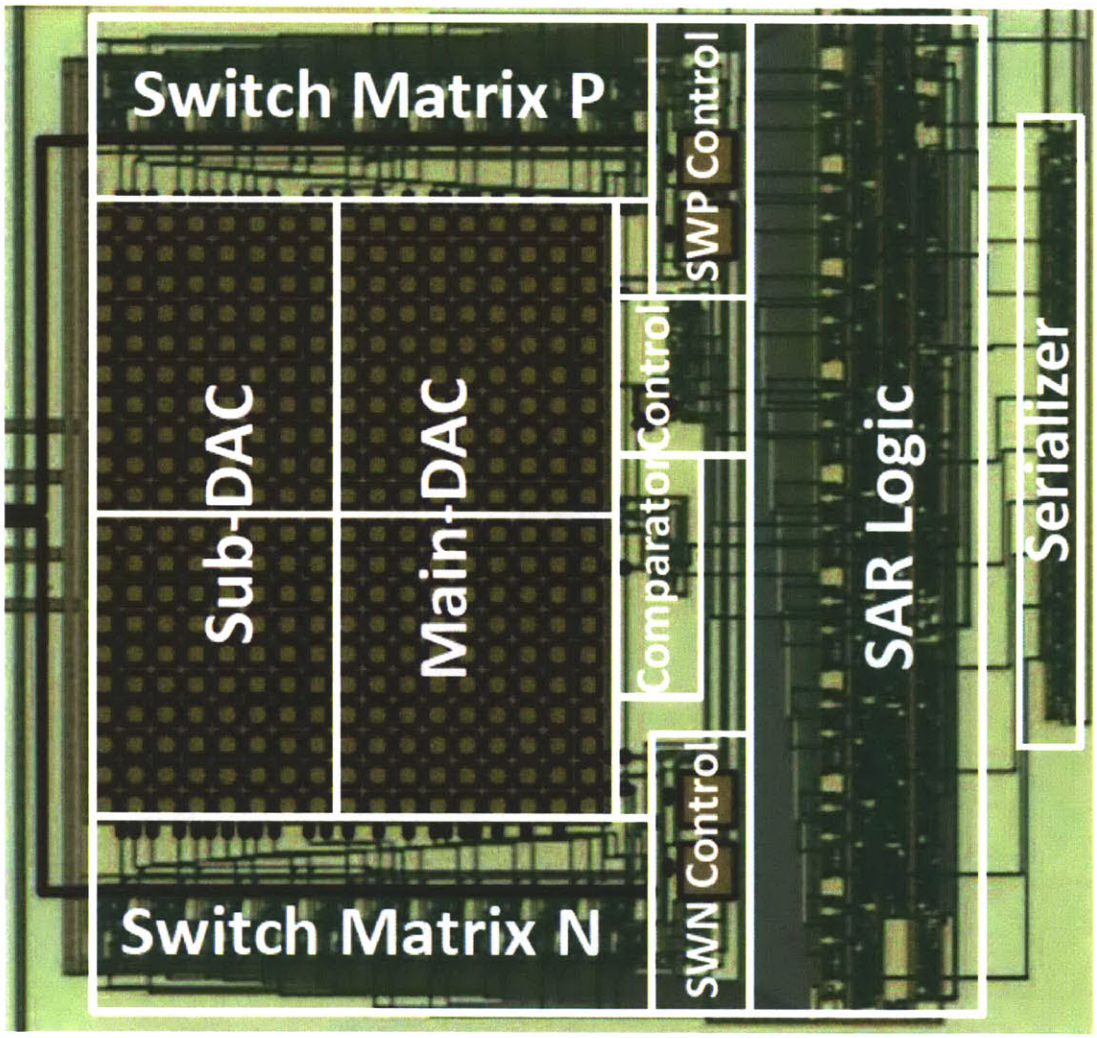


Figure 3-2: Micrograph of the full ADC and the serializer

powered separately so as not to disturb the ADC power measurements. Power supplies are decoupled on board as well as on chip. Figure 3-4 depicts photograph of the test board while a detailed schematic of the board partition for ADC testing is shown in Appendix A.

3.2 Characterization

This section describes the steps performed to evaluate the ADC performance parameters including offset, DNL/INL, SNDR and power consumption. Every test should start by applying the nRST signal to guarantee that all the registers are initialized properly. Results are presented at the end of each sub-section and a summary of performance parameters is also provided.

3.2.1 Static Linearity

The DNL/INL were extracted using code density test. First, a close to full-scale sine wave (but not clipping) was applied across the inputs of the ADC to determine the midcode. The ADC suffers from a static offset which resulted in midcode of 501 due to the mismatch in the digital comparator. Second, a sine wave is applied whose amplitude is slightly larger than the full-scale (2 V_{PP}) to clip the ADC slightly. For a 10 bit ADC, 1 million samples are at least required for 0.1 bit precisions with 99 percent confidence [15]. This test was conducted at a sampling rate of 32 kHz using a differential sinusoidal signal with frequency close to 100 Hz. More than 1.2 million samples were captured through 19 recording to establish the desired confidence level. The ADC raw data were processed using open source MATLAB code by MAXIM [16].

Figure 3-5 shows the code density histogram where no bins are empty highlighting that there are no missing codes. Figure 3-6 depicts the ADC DNL and INL versus output code. The maximum DNL is +0.55/-0.37 LSB while the maximum INL is +0.75/-0.68 LSB. The DNL has a sawtooth characteristic with a period of 32 code due to the imperfect sub-DAC interpolation. Abrupt transitions in the INL occurs with

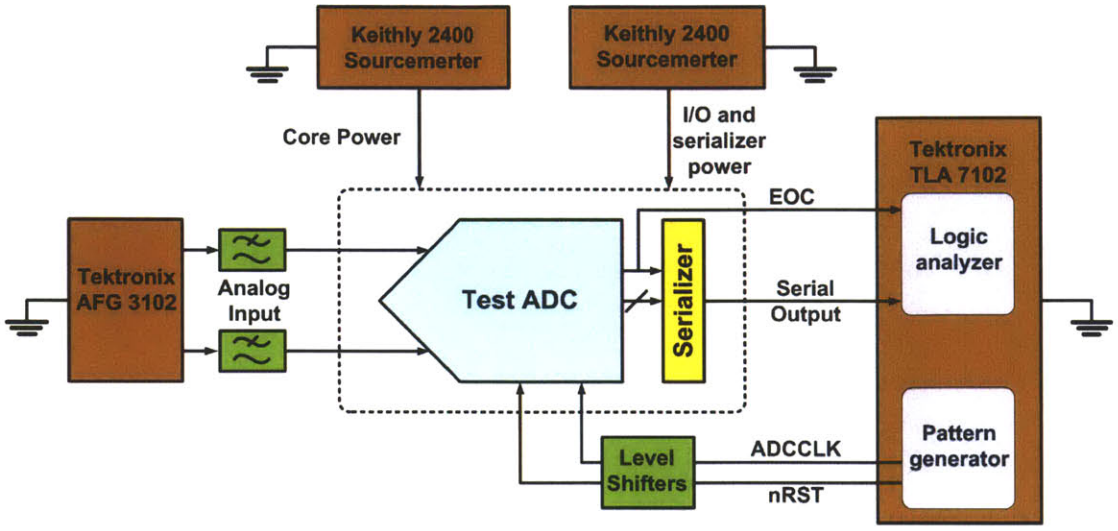


Figure 3-3: Schematic of the test setup

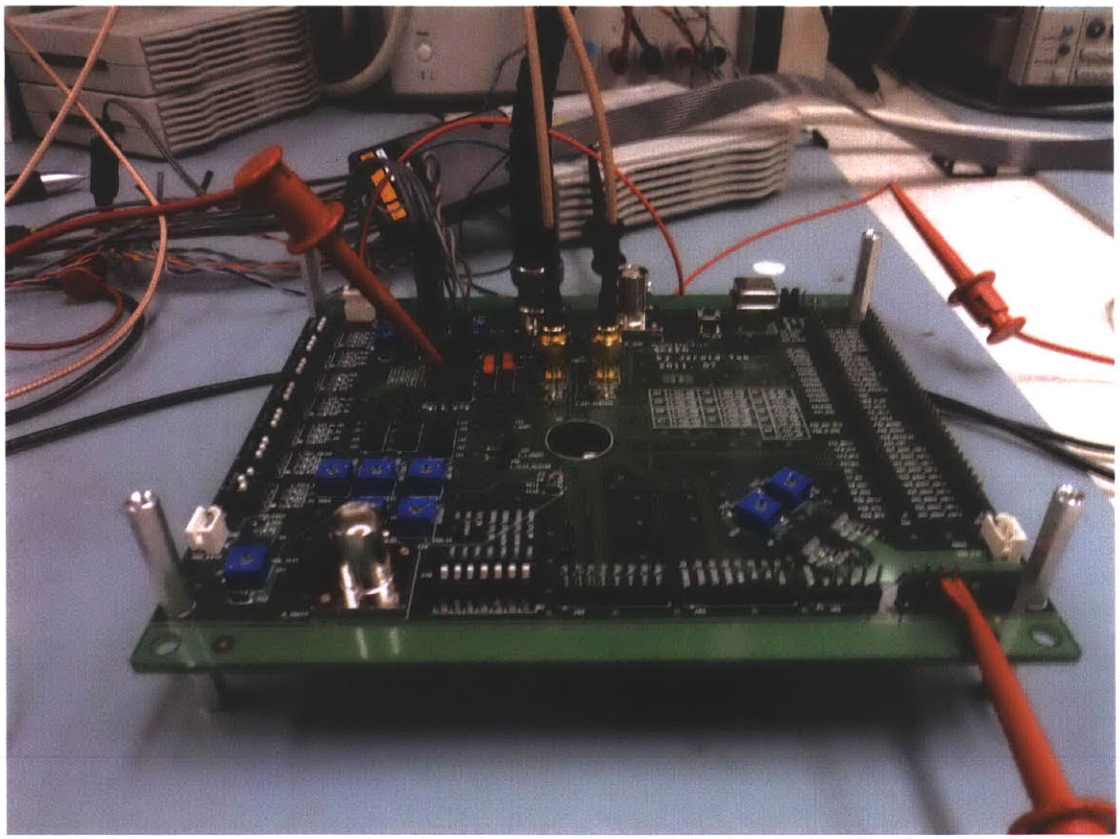


Figure 3-4: Test PCB photograph

a period of approximately 256 code indicating a mismatch in the MSB-1 capacitor. However, the INL of the ADC is still well within ± 1 LSB.

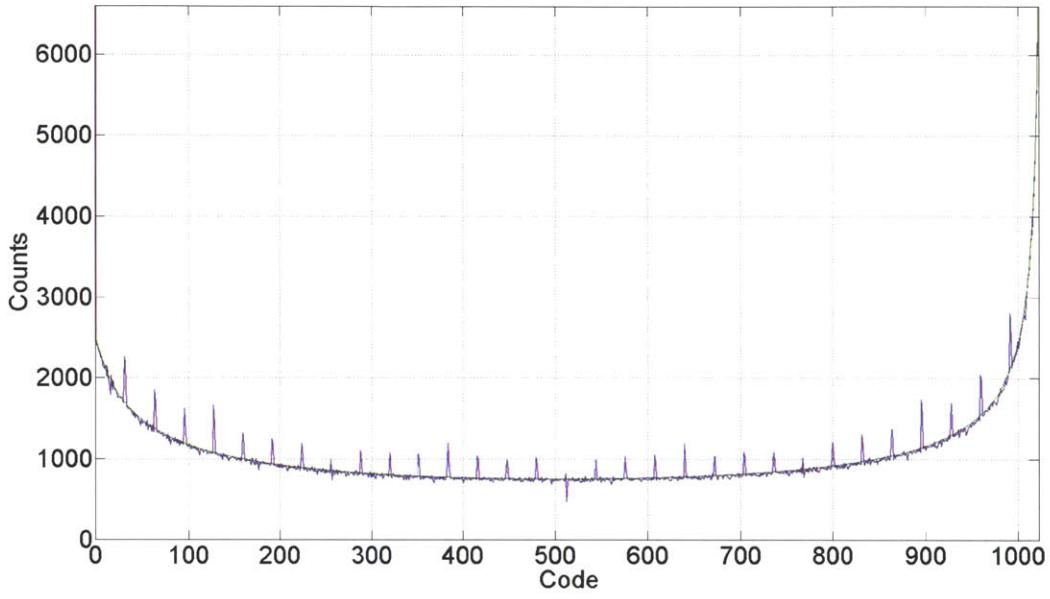
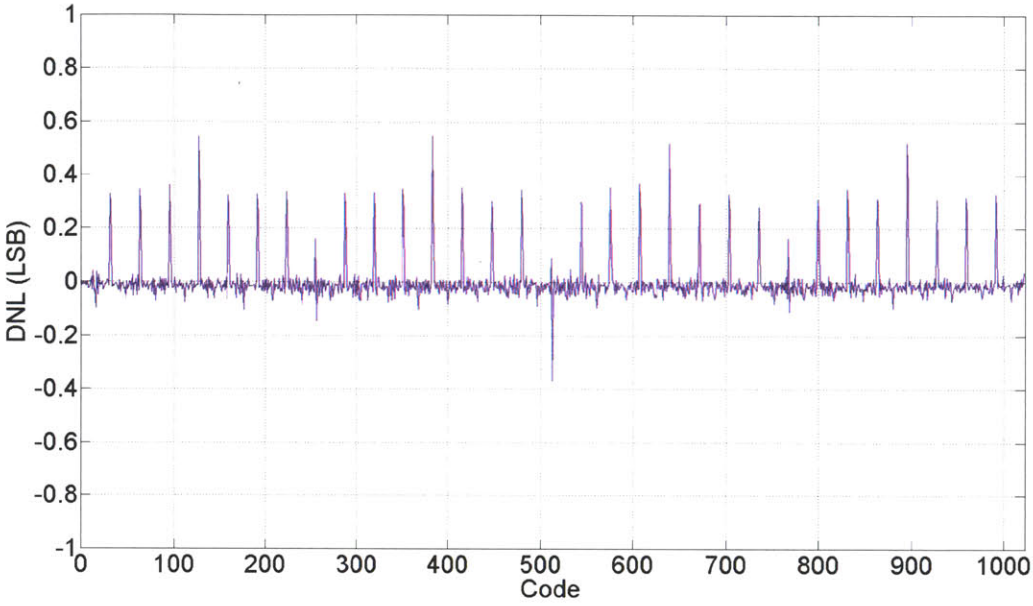


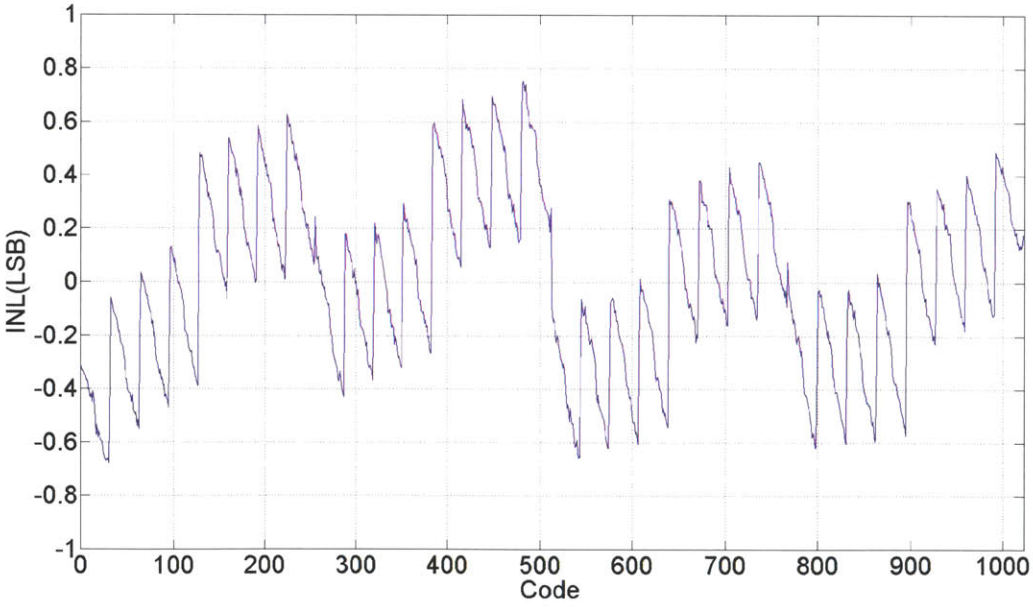
Figure 3-5: Code density histogram of the ADC

3.2.2 Dynamic Performance

The dynamic performance of the ADC is characterized using single-tone testing. A sine wave is applied whose amplitude is slightly smaller than the full-scale (1.96 V_{PP}) to avoid clipping the ADC output. The input signal frequency is varied from close to DC to one-half sampling rate. The SNDR was extracted by FFT-based analysis of the ADC output using MATLAB while utilizing Hanning window [17]. Figure 3-7 depicts the magnitude spectrum of the ADC output at 15.5 kHz input signal and 32 kHz sampling rate where the SFDR is 68.5 dB. Figure 3-8 depicts ENOB verus input signal frequency which is relatively constant to 9.32 bits over the input signal range.



(a) ADC DNL versus output code



(b) ADC INL versus output code

Figure 3-6: ADC Differential and Integral non-linearity versus output code

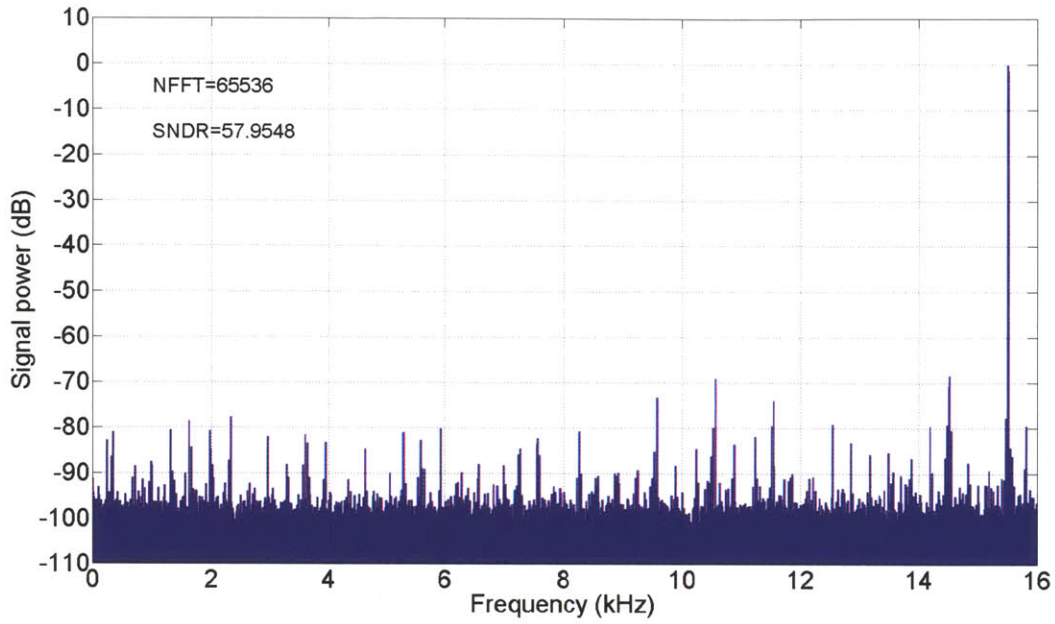


Figure 3-7: FFT of the ADC output with 15.5 kHz input signal

3.2.3 Power Consumption

The average current drawn by the ADC is measured using the Keithly source meter. Figure 3-9 depicts the ADC core power consumption versus the sampling rate. The total average power consumption excluding I/O is 1 μW at a sampling rate of 32 kHz and 1 volt supply.

Since the ADC adopts a highly digital architecture, the average power consumption of the ADC consists of a dynamic component proportional to the sampling rate and leakage component as given by equation 3.1 where α is a constant, f_{smpl} is the sampling frequency, V_{DD} is the supply voltage and $I_{leakage}$ is the leakage current which sets the minimum power consumption of the ADC.

$$\begin{aligned} P_{ADC} &= P_{dynamic} + P_{leakage} \\ &= \alpha f_{smpl} + V_{DD} I_{leakage} \end{aligned} \tag{3.1}$$

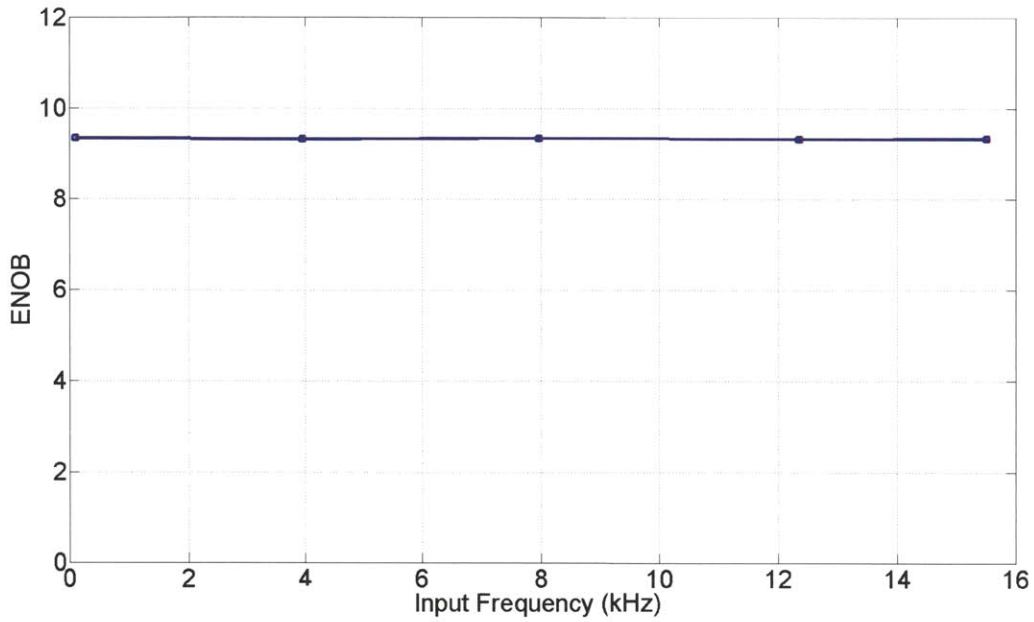


Figure 3-8: ENOB versus ADC input signal frequency at sampling rate of 32 kHz

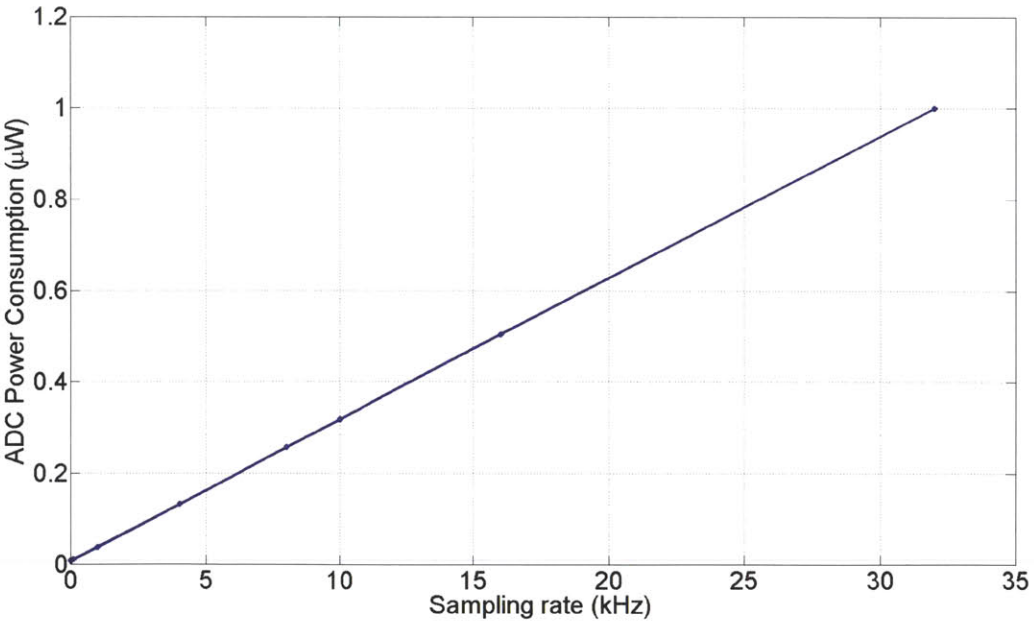


Figure 3-9: Average Power consumption of the ADC versus sampling rate

Figure 3-10 depicts a linear plot of the ADC power consumption versus the sampling rate below 1 kHz. As shown in the Figure, the power consumption plot follows the expected behaviour by equation 3.1 as a shifted straight line. The amount of shift is equal to the leakage power which is approximately 8 nW.

In order to identify the frequencies at which leakage dominates the power consumption, Figure 3-11 depicts the log-log plot of the ADC power consumption versus the sampling rate. The leakage component fully dominates the power consumption for sampling frequencies below 25 Hz i.e. leakage power is higher than 10 times of the dynamic power. The curve has a linear behaviour at relatively high sampling rates where the dynamic component of power dominates the power consumption.

3.3 Summary

The ADC performance parameters are summarized in Table 3.1. The entire ADC core consumes 1 μW from 1 V supply at a sampling rate of 32 kHz. The ADC has a maximum DNL and INL of 0.55 LSB and 0.75 LSB respectively. The SNDR and SFDR of the converter are measured at a sampling rate of 32 kHz and 15.5 kHz input tone to be 57.9 dB and 68.5 dBFS respectively. The ADC FOM is 51 fJ/Conv-Step while being calculated using equation 3.2 where P is the total power consumption, f_{in} is the input signal frequency [18]. Figure 2-20 shows a comparison of ADC to the state-of-the art where energy per Nyquist sample is plotted versus SNDR [19].

$$FOM = \frac{P}{2f_{in}2^{ENOB}} \tag{3.2}$$

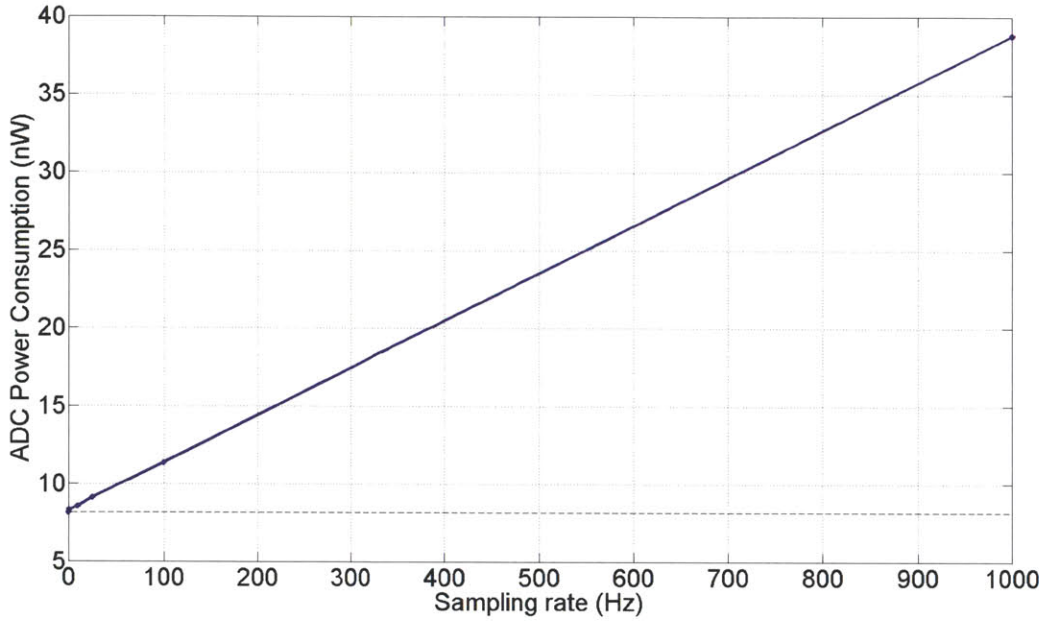


Figure 3-10: Linear plot of the power consumption of the ADC versus sampling rate below 1 kHz

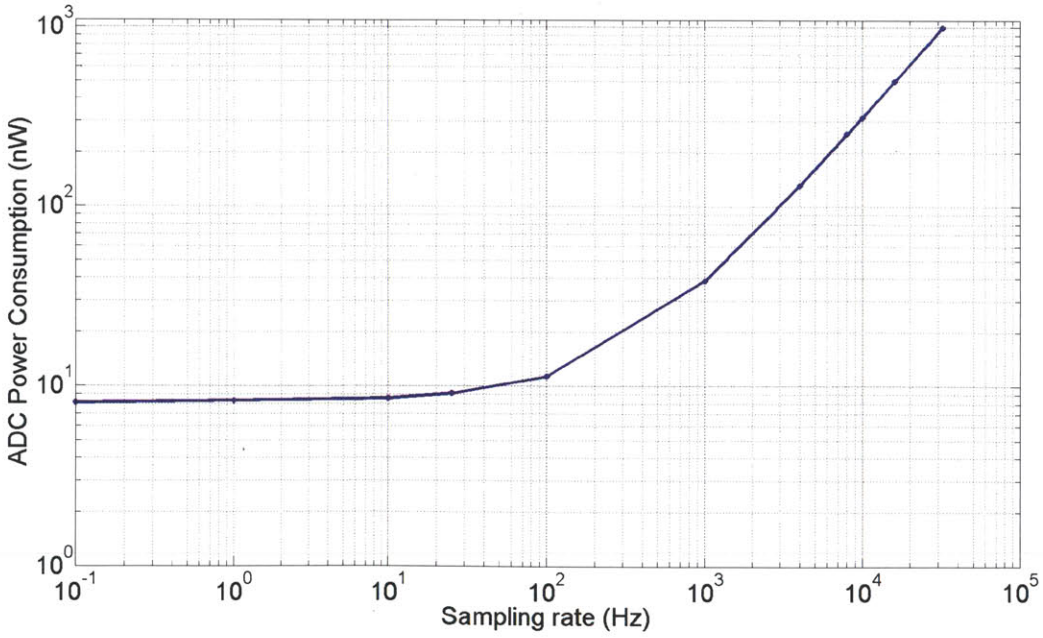


Figure 3-11: Log-log plot of the power consumption of the ADC versus sampling rate

Table 3.1: Summary of ADC performance parameters

Performance parameter	**Value**
SNDR	57.9 dB
ENOB	9.32 dB
SFDR	68.5 dBFS
Power consumption	1 μW @ f_s= 32 kHz
INL	0.75 LSB
DNL	0.55 dB
FOM	51 fJ/Conv-step

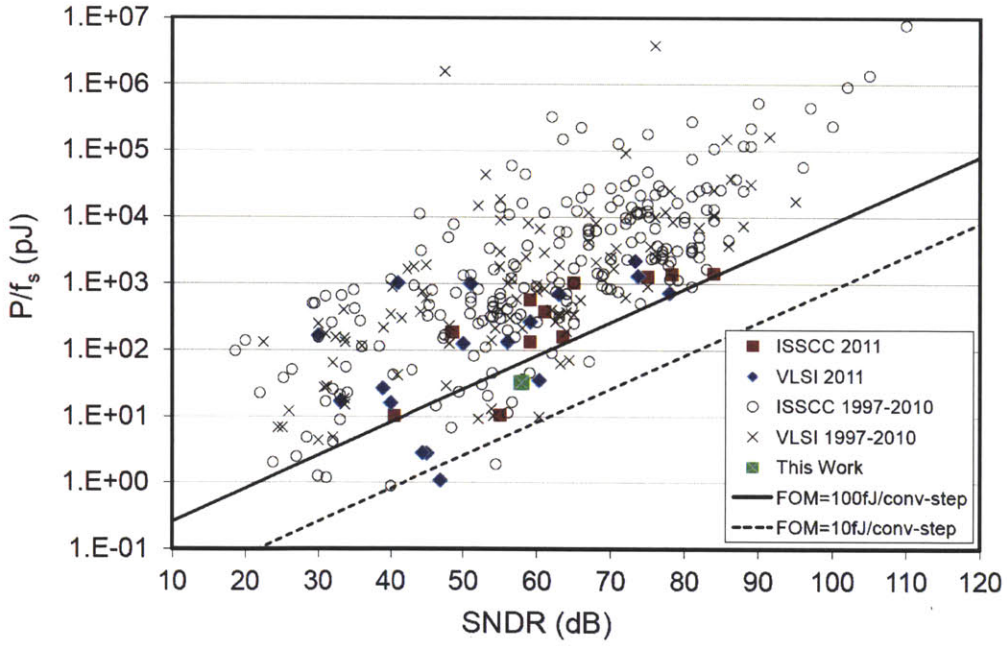


Figure 3-12: Comparison of the ADC to the state-of-the art (Data adopted from B. Murmann, "ADC Performance Survey 1997- 2010," http://www.stanford.edu/ murmann/adcsurvey.html)

Chapter 4

Conclusions and Future Work

This thesis presented the design of an ultra low power ADC to be integrated within SoC for ambulatory EEG recording and seizure detection. The full system can capture EEG signals through 1 up to 8 parallel differential channels that are time division multiplexed into a single ADC where the number of the operating channels in the AFE and corresponding ADC sampling frequency are controlled by the DBE. SAR ADC architecture was chosen for this design as it is highly energy efficient for medium to high resolution applications with low speed requirements. This chapter presents the conclusions and the future work that can be done to improve the performance of the ADC designed in this work.

4.1 Conclusions

The ADC was designed and fabricated in a 0.18 μm CMOS technology. The entire ADC operates from 1 V supply while bootstrapping is used internally. The ADC has a fixed resolution of 10 bits which is sufficient for extraction of bio-markers for seizure detection by DBE. The ADC has a scalable sampling rate that is controlled by the clock frequency to accommodate different number of channels in the EEG SoC. A sampling rate of 4 kHz/Channel was chosen to relax the roll-off of the anti-aliasing filters in the AFE while using a decimator in the DBE to down sample the ADC output.

A fully differential ADC architecture was adopted in this design. It enhances the common-mode rejection ratio and reduces the second order harmonics. This increases the robustness of the whole system at the expense of higher deign complexity and higher power consumption. Concepts of split-capacitor array and sub-DAC were combined to reduce the DAC area and power consumption. Charge pumps were used to boost the control voltage of sampling switches to decrease the THD. A self-resetting SAR logic was used to control the ADC conversion every 16 clock cycles. A digital comparator was used to avoid any static bias current and allow for low power consumption.

The entire ADC core consumes 1 μW from 1 V supply at a sampling rate of 32 kHz. The ADC has a maximum DNL and INL of 0.55 LSB and 0.75 LSB respectively. The SNDR and SFDR of the converter are measured at a sampling rate of 32 kHz and 15.5 kHz input tone to be 57.9 dB and 68.5 dBFS respectively. The ADC FOM is 51 fJ/Conv-Step.

4.2 Future Work

This section lists the future work that can be done to improve the performance of the ADC designed in this work.

1. Exploiting the correlation between samples of the EEG signal to predict the next code based on the previous conversion. This can allow for further power saving during the bit-cycling phase by using a more efficient search algorithm.

2. Auto-calibration of the offset of the comparator during start-up. Offset compensation can be done by digitally controlling the current supplied by input pair or a capacitor bank at the comparator outputs [10, 20].

3. The DAC presented in this work was divided into main-DAC and sub-DAC to reduce its overall area. Further savings can be obtained by splitting the sub-DAC using the same concept. However, top plate parasitics of each sub-DAC

will have a pronounced effect on DNL/INL and coupling capacitors should be carefully compensated to preserve the ADC linearity.

Appendix A

Test Setup

The whole EEG SoC was designed and fabricated in TSMC 0.18 μm CMOS technology. The chip includes two copies of the ADC, one in the signal path and a stand alone ADC for characterization. A custom 4-layer PCB was designed and fabricated for testing the whole system and the individual blocks. Figure A-1 depicts the partition of the schematic of the board used for the characterizing the stand alone ADC. The test board supports differential input using two SMA connectors. Digital inputs generated by Tektronix pattern generator are coupled to the ADC through header pins while resistive dividers are used to scale it down to V_{DD}. Digital outputs are captured using Tektronix logic analyzer through header pins also. The supply and reference are generated using Keithley SourceMeter2400 that has power measuring capabilities. Supplies are decoupled on board using a bank of four capacitors (10nF, 0.1 μF, 2.2 μF, 22 μF). Switches are used on board for connecting ADCEN and VMODE pins to either supply or ground. Table A.1 summarizes the stand alone ADC pin names and their description.

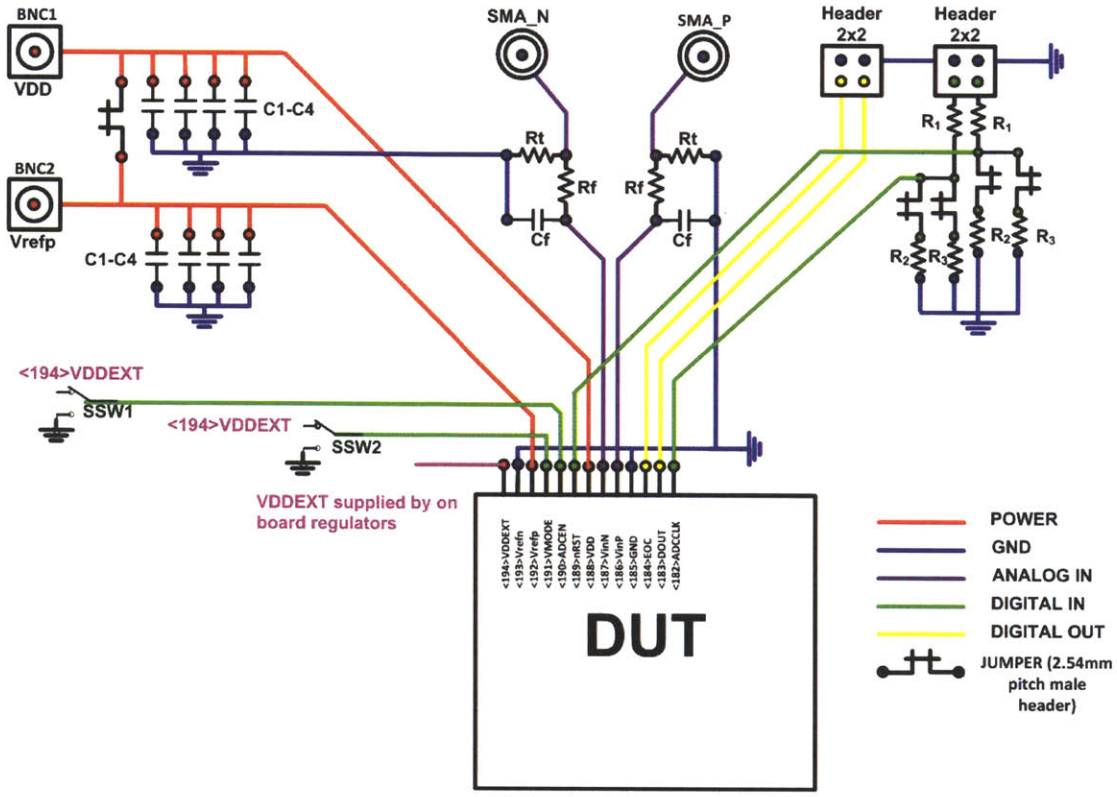


Figure A-1: Partition of the schematic of the board showing the necessary connections for the stand alone ADC

Table A.1: ADC pin definition

Pin name	Pin description
VDD	Supply of the core
GND	Ground
VinP, VinN	Differential analog input
ADCCLK	Clock
ADCEN	Enable
VMODE	Voltage mode
Vrefp	ADC positive reference (1V)
Vrefn	ADC negative reference
DOUT	Serial digital output
VDDEXT	Supply of I/O and serializer

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