

**Impact of Uniaxial Strain on
P-channel III-V Quantum-well Field Effect Transistors**

by

Ling Xia

B. S., Peking University (2003)

M. S., Peking University (2006)

**Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of**

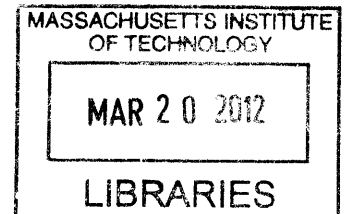
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Signature of Author _____

Department of Electrical Engineering and Computer Science
October 31, 2011

Certified by _____

Jesús A. del Alamo
Professor of Electrical Engineering
Thesis Supervisor

Accepted by _____

Leslie Kolodziejski
Professor of Electrical Engineering
Chairman, Department Committee on Graduate Thesis

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ABSTRACT

Continuous scaling of Si complementary metal-oxide-semiconductor (CMOS) technology requires a boost in carrier injection velocity. With the benefits of strained Si having been exhausted, n-channel III-V quantum-well field effect transistors (QW-FETs) show promising potential as a post-Si CMOS logic technology. To implement complementary circuits, achieving a high-performance p-channel III-V transistor remains one of the grand challenges. The key problem is the low hole mobility in these materials. In this thesis, we investigate a solution to this problem by exploring uniaxial strain as a means to improve hole mobility in III-V quantum-well structures.

We have fabricated Hall structures and QW-FETs on several III-V heterostructures. The channels of these heterostructures include n-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$, p-channel GaAs, $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$. We applied uniaxial strain to these devices by bending the III-V chips using a mechanical apparatus. Characteristics of these devices were measured while uniaxial strain was externally applied. Significant hole mobility enhancements were observed under uniaxial compressive stress parallel to the transport direction. Our analysis showed that strain-induced valence band deformation is the dominant mechanism. Nevertheless, two other strain effects were found relevant for QW-FET operations: Schottky barrier height change and the piezoelectric effect. Threshold voltage (V_T) and gate capacitance (C_G) of the QW-FETs were found to be changed by these two effects. For the first time, the piezoresistance coefficients for the three p-channel QWs were determined. A significant finding was that the combination of uniaxial strain with epitaxial biaxial strain appears to enhance the hole mobility in a superlinear way. With high piezoresistance coefficients and high hole mobility, InGaSb appears promising for high-performance p-channel QW-FETs for logic applications.

We also developed a device architecture for p-channel InGaAs FETs that incorporates uniaxial strain through a self-aligned dielectric stressor. For the first time, we demonstrated substantial enhancements in the transport characteristics of p-channel InGaAs FETs through the combination of compressive uniaxial strain and compressive epitaxially grown biaxial strain. Strain enhances both the intrinsic transconductance as well as the access resistances. The fabricated structure exhibits promising gate-length scalability and compatibility with self-aligned source/drain metal contacts. Our proposed device architecture holds promise to implement high-performance p-channel III-V FETs for future CMOS logic applications.

Thesis Supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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Chapter 1 Introduction

1.1 InGaAs QW-FET for post-Si logic technology

In the past four decades, logic technology based on silicon CMOS (complementary metal oxide semiconductor) has laid the foundation for the digital era bringing to human society revolutions in computation, communication and more. Innovations in logic technology have followed the so-called “Moore’s Law”. These innovations have made possible increases in computation power at the same time as cost reduction. Such a remarkable trend is desired to continue forever.

However, great challenges have emerged as Si CMOS continues to scale down the roadmap. For several decades, Si CMOS technology has relied on a gifted pair of materials: Si and SiO₂, for device channel and device gate dielectric, respectively. But at the 45 nm technology node, SiO₂ was replaced by a high- k dielectric with the goal of mitigating excessive gate leakage current due to continued scaling of SiO₂ thickness [1].

Now the time has come for a new channel material to replace Si. This is envisioned by the requirement of increasing virtual source injection velocity (v_{x0}) for scaled devices. [2-3] Khakifirooz and Antoniadis pointed out that in deeply scaled devices, the velocity (v_{x0}) at which carriers are injected into the channel at its source end is the driving factor for performance improvements in Si CMOS. Only if we can increase v_{x0} , while maintaining short-channel effects, can we counteract the penalty of ever-increasing parasitic capacitances in scaled devices. As the device scales below 10 nm technology node, the

v_{x0} that uniaxially strained Si can provide is not enough to deliver the required performance improvements. Figure 1-1 is taken from [4] of Khakifirooz and Antoniadis. This figure shows that a projected v_{x0} of 1.9×10^7 cm/s will be close to the ballistic velocity of electrons with 10 nm technology. This value of v_{x0} is hard to reach, considering that v_{x0} is only a portion (e.g. 0.65 for state-of-art Si MOSFETs) of the ballistic velocity.[4] Therefore, a new channel material that starts with a higher ballistic velocity and can provide intrinsically higher v_{x0} is required.

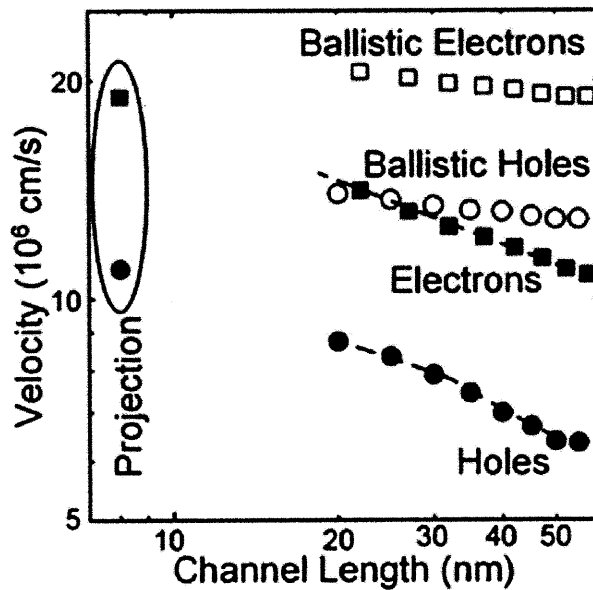


Figure 1-1. The extracted virtual source velocity (filled symbols) and calculated ballistic velocity (open symbols) vs. effective channel length. State-of-the-art MOSFETs operate at about 65% of their ballistic limit. (Figure taken from [4])

In this sense, $\text{In}_x\text{Ga}_{1-x}\text{As}$ ranks very high in the candidate list for new CMOS channel material. As a matter of fact, the $\text{In}_x\text{Ga}_{1-x}\text{As}$ high electron mobility transistor (HEMT) shows the highest cut-off frequency (f_T), a figure of merit of transistor's intrinsic speed, among all the FETs based on any materials in the world. [5] Recent experiments demonstrated that $\text{In}_x\text{Ga}_{1-x}\text{As}$ quantum wells possess up to 2x electron v_{x0} compared with

Si at less than half the operating voltage. [6] This is due to the fact that electrons in $\text{In}_x\text{Ga}_{1-x}\text{As}$ have intrinsically lower effective mass than in Si. A proxy to gauge the effective mass, the electron mobility in $\text{In}_x\text{Ga}_{1-x}\text{As}$ can be 20x higher than the bulk Si electron mobility at room temperature.

Other than the advantage in electron velocity, $\text{In}_x\text{Ga}_{1-x}\text{As}$ HEMTs can outperform state-of-art Si MOSFETs in short-channel effects, something that is essential for logic applications. [5] This is due to the ability of creating a very thin quantum well (few nm thick) also a few nanometers below the gate. [7] This type of FET, which we call quantum-well FET (QW-FET), is an excellent model system for studying new channel materials for CMOS applications. One noticeably drawback of the HEMT is that this type of device tends to have higher gate leakage current compared with well-behaved MOSFETs. This is because the bandgap of the barrier material is relatively low and carrier tunneling between gate and channel takes place. A future InGaAs FET needs to have a MOS gate structure, just like a MOSFET.

Overall, the advantages seen in the velocity as well as short-channel effects suggest that an $\text{In}_x\text{Ga}_{1-x}\text{As}$ quantum-well is the most promising candidate to substitute the Si channel in a future logic technology.

1.2 Critical issues in high-performance p-channel

III-V QW-FETs

To implement complementary logic circuits, high performance p-channel FETs are needed. As important as n-channel FETs are, p-channel FETs occur in equal numbers as n-channel FETs and greatly affect circuit performance. Figure 1-2 shows a vision for

integrating n- and p-FETs in a future CMOS technology in which both n- and p-FETs outperform state-of-art Si MOSFETs. Under such a vision, to choose a candidate material for pFETs to complement an $\text{In}_x\text{Ga}_{1-x}\text{As}$ nFET, two factors among many are considered first: hole mobility/velocity and readiness of integration with $\text{In}_x\text{Ga}_{1-x}\text{As}$ nFETs.

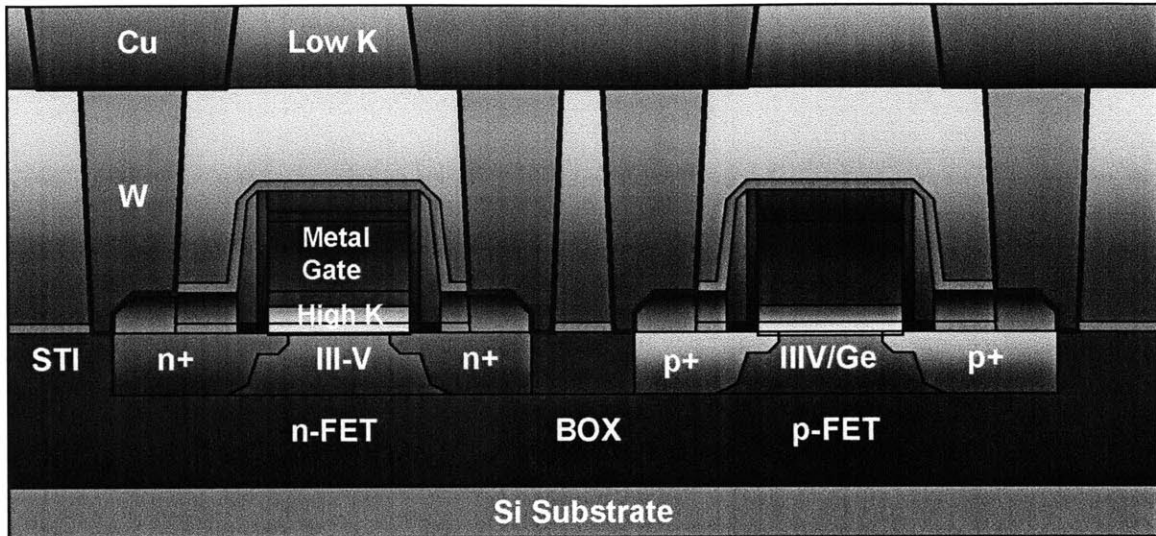


Figure 1-2. A conceptual architecture for a future complementary logic technology using an n-channel $\text{In}_x\text{Ga}_{1-x}\text{As}$ FET and a III/V or Ge p-channel FET. (www.sematech.org/meetings/archives/fep/20051204/)

One would like to start with a material that has a high hole mobility, so that the disparity between the selected pFET and $\text{In}_x\text{Ga}_{1-x}\text{As}$ nFET is not too great. In early bulk Si CMOS, the electron mobility can be several times higher than the hole mobility. This disparity between electron and hole mobilities requires extra chip area and effort when designing CMOS circuits. Typically, a larger transistor width is used for p-channel FETs to correct the n- and p-FET performance gap. While this disparity has been almost completely eliminated in recent CMOS generations due to strain, it could grow much worse with n-channel $\text{In}_x\text{Ga}_{1-x}\text{As}$ FETs. The electron mobility in $\text{In}_x\text{Ga}_{1-x}\text{As}$ can be as

high as $30,000 \text{ cm}^2/\text{V}\cdot\text{s}$, which easily dwarfs the hole mobility in most materials. Therefore, a p-channel FET with performance approaching an n-channel $\text{In}_x\text{Ga}_{1-x}\text{As}$ FET is highly desirable, but a suitable material is not readily available.

Among many candidate semiconductors, the hole mobility in $\text{Si}_x\text{Ge}_{1-x}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ stands out. The hole mobility reported in pure Ge channel inversion layers can be more than $2000 \text{ cm}^2/\text{V}\cdot\text{s}$ [8]; the hole mobility in $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ quantum well reaches $1500 \text{ cm}^2/\text{V}\cdot\text{s}$ [9]. These two values are reached by exploiting biaxial strain to enhance the hole mobility in the channel. This will be discussed in more detail in the next section. For p-channel $\text{In}_x\text{Ga}_{1-x}\text{As}$, unfortunately, the hole mobility is not much better than the value in Si. The highest reported value is $400 \text{ cm}^2/\text{V}\cdot\text{s}$. [10-11]

Nonetheless, regarding the readiness of integration with $\text{In}_x\text{Ga}_{1-x}\text{As}$ nFETs, the $\text{In}_x\text{Ga}_{1-x}\text{As}$ material system wins over $\text{Si}_x\text{Ge}_{1-x}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ alloys. It is easier to use the same material for both n- and p-channel FETs. Integrating two different materials will require providing two different lattice constants through appropriate buffer layers. Table 1-1 shows the lattice constants for the three groups of p-channel material candidates as well as InP, which is the substrate of the best $\text{In}_x\text{Ga}_{1-x}\text{As}$ nFETs so far [5]. Clearly, $\text{Si}_x\text{Ge}_{1-x}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ alloys have quite different lattice constants from $\text{In}_x\text{Ga}_{1-x}\text{As}$. This complicates the integration of any of these pairs of materials with InGaAs. One should also note additional buffer layer design constraints. It has to be thin for economic and thermal reasons. In addition, the buffer layer thicknesses have to be such that the resulting surface for both n- and p-FETs is planar so as to enable the fine-line lithography that is required to fabricate deeply scaled devices.

	Lattice constant (Å)	Lattice mismatch to Si
$\text{Si}_x\text{Ge}_{1-x}$	5.43 - 5.66	0% - 4.1%
$\text{In}_x\text{Ga}_{1-x}\text{As}$	5.65 - 6.05	4.1% - 11.4%
$\text{In}_x\text{Ga}_{1-x}\text{Sb}$	6.10 - 6.48	12.3% - 19.3%
InP	5.87	8.1%

Table 1-1. Relaxed lattice constants and mismatch with Si substrate for various p-channel candidates and InP substrate.

In short, there are challenges for all the three groups of materials as future p-channel materials to complement n-channel $\text{In}_x\text{Ga}_{1-x}\text{As}$ FETs. In this study, we will investigate the potential of III-V materials including $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ for pFETs. Our primary efforts will be on $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel FETs given it is more available and allows for systematic studies. These studies on $\text{In}_x\text{Ga}_{1-x}\text{As}$ FETs, however, were found to be relevant to other III-V channel FETs.

1.3 Hole mobility improvement by strain

It is highly desirable to improve the hole mobility in III-Vs to a level such that the pFET matches the performance of $\text{In}_x\text{Ga}_{1-x}\text{As}$ nFET. One approach to fundamentally improve the hole mobility is through the introduction of strain in the channel.

As early as in 1962, Hensel and Feher experimentally found that strain lifts valence band degeneracy and changes the hole effective masses in Si [12]. These effects inspired the demonstration in 1993 of the first strained Si pMOSFET with enhanced hole mobility. [13] After a decade of effort, strain engineering was incorporated into commercial Si CMOS at the 90 nm technology node [14]. In fact, the introduction of uniaxial strain has enhanced the p-MOSFET performance so much that the traditional advantage of the n-MOSFET has been almost completely erased at the 32 nm node [15].

Similar to Si [16], the hole mobility of III-V compounds is also responsive to strain [17]. Employing strain effects to enhance pFET performance in III-Vs was suggested theoretically to be feasible in a review article by O'Reilly [18]. In a relaxed bulk material (no strain), the valence band structure at the Γ point in the Brillouin zone consists of degenerate heavy-hole and light-hole bands. When strain is applied to III-V materials, the heavy-hole and light-hole bands split. In consequence, the holes will redistribute, and preferably occupy the band that has the highest electron energy. The band splitting by itself leads to reduced interband scattering and an increased mobility. Furthermore, when more holes occupy the light-hole band under certain types of strain, the overall effective mass of the holes is reduced. More mobility enhancement is then expected. In addition, strain induces valence band warping and consequently changes the conductivity effective mass. The combination of the three effects above can lead to a significant increase in the hole mobility. The underlying physics of these effects will be discussed in detail in Chapter 2.

On the experimental side, past efforts in strain engineered $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$ to modify hole transport were devoted to introducing biaxial strain into the channel through pseudomorphic epitaxial growth. [9, 11, 19-21] For $\text{In}_x\text{Ga}_{1-x}\text{Sb}$, compressive biaxial strain was experimentally found to be instrumental in enhancing the hole mobility on both GaSb [20] and InSb [21].

For $\text{In}_x\text{Ga}_{1-x}\text{As}$, we have compiled experimental hole mobility data in $\text{In}_x\text{Ga}_{1-x}\text{As}$ quantum wells grown on both GaAs and InP substrates. Two groups of experimental data are shown in Figure 1-3. One set is grown on GaAs ($0 < x < 0.35$) and another set on InP ($0.53 < x < 0.82$). [10-11, 19, 22-26] Within each of these two groups of data, the hole

mobility increases with the InAs mole fraction in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ alloy. However, the correlation between hole mobility and InAs mole fraction suggested by this figure is at first puzzling given the sharp discontinuity around 40-60% InAs composition. Interestingly, the hole mobility appears to correlate linearly with the biaxial strain in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ alloys, as shown in Figure 1-4. This correlation suggests that biaxial strain is a very significant factor affecting the hole mobility in $\text{In}_x\text{Ga}_{1-x}\text{As}$ quantum wells.

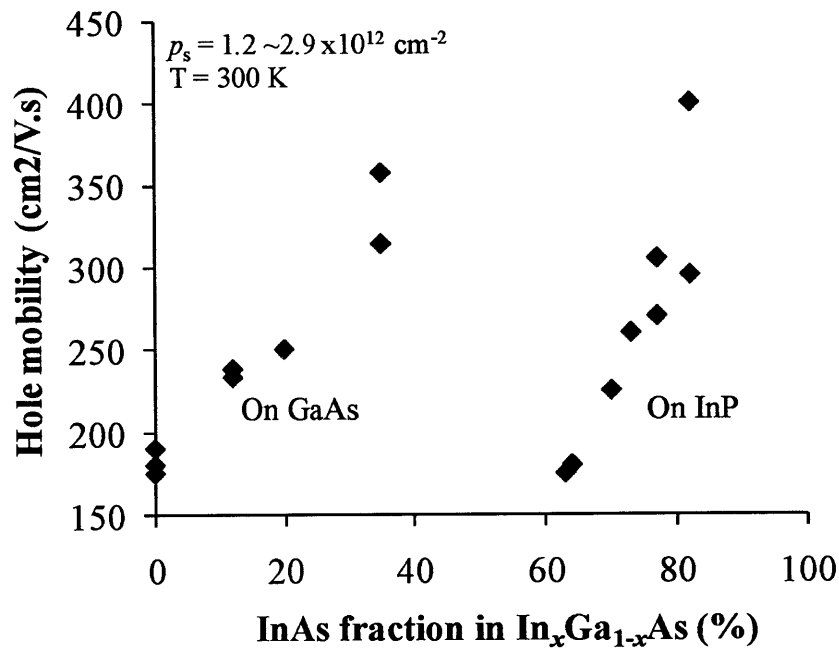


Figure 1-3. Experimental hole mobility in $\text{In}_x\text{Ga}_{1-x}\text{As}$ quantum wells as a function of InAs fraction in the channel. No definite correlation is observed for the entire range of $\text{In}_x\text{Ga}_{1-x}\text{As}$ alloys.

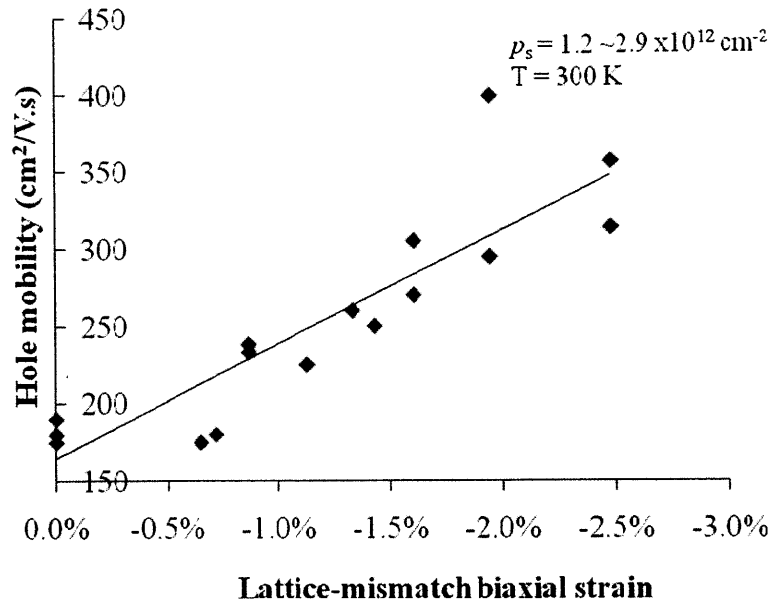


Figure 1-4. Hole mobility in $\text{In}_x\text{Ga}_{1-x}\text{As}$ quantum wells as a function of lattice-mismatch biaxial strain in the channel. The data is the same as in Fig. 1-3. A strong correlation appears between the hole mobility and biaxial strain.

Other than substrate-induced biaxial strain, uniaxial strain induced by process technology can also be an effective way to enhance hole mobility. In Si pMOSFETs, compressive uniaxial strain along $\langle 110 \rangle$ directions with $\langle 110 \rangle$ channels has turned out to be the most beneficial approach. [27] This is understood in the following way: Compressive uniaxial strain splits the valence bands so that the one with lighter in-plane effective mass has a higher electron energy and is preferably occupied. In addition, under $\langle 110 \rangle$ uniaxial strain, the band with the lighter in-plane mass has the heavier out-of-plane mass, so that the quantization of holes under high surface electric field does not cancel the effect of strain-induced band splitting. [28] As a result, the hole mobility enhancement in Si MOSFET under $\langle 110 \rangle$ uniaxial compressive strain reaches almost a factor of two under 2 GPa compressive stress. [29]

A comparison between hole mobility enhancement under $\langle 110 \rangle$ strain and biaxial

strain in a Si inversion layer can also be illustrated through Figure 1-5, obtained from simulations [30-31]. For a small amount of strain (usually within the range attainable by wafer-bending measurements) $\langle 110 \rangle$ compressive strain parallel to the channel direction increases the hole mobility while $\langle 110 \rangle$ tensile strain decreases the hole mobility. For large compressive strain, $\langle 110 \rangle$ uniaxial strain is significantly more effective in enhancing the hole mobility than compressive biaxial strain of the same magnitude. For large tensile strain, the biaxial strain changes the hole mobility in a non-monotonic way. This is because the subband splitting first decreases but then increases with tensile strain. [30] In addition simulations also suggest that $\langle 100 \rangle$ uniaxial strain is less effective than $\langle 110 \rangle$ uniaxial strain [30].

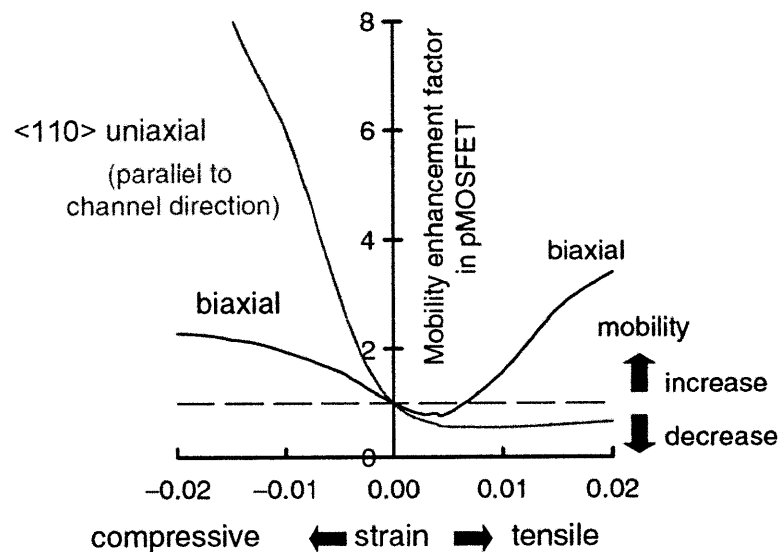


Figure 1-5. Calculated mobility enhancement factor for inversion-layer holes in Si p-channel MOSFETs with uniaxial compressive and biaxial tensile strain [30]. The value of E_{eff} is taken to be 1 MV/cm. (Figure taken from [31])

Recently, Gomez [32] found that in Ge, the combination of uniaxial strain with lattice-mismatch biaxial strain can be even more effective in improving hole mobility than

simply using uniaxial strain or biaxial strain separately. A factor of two improvement was observed in the $\langle 110 \rangle$ piezoresistance coefficient from Ge pMOS with 2.4% compressive strain compared with relaxed Ge pMOS. The amount of biaxial strain introduced through epitaxy is usually limited so that dislocation formation during growth does not cause severe crystal quality degradation. Adding uniaxial strain through device fabrication on top of a biaxially strained epitaxial layer appears to be an effective method to further enhance hole mobilities. The uniaxial piezoresistance increase in biaxially strained Ge reported by Gomez is very encouraging, in that it suggests that combining both sources of strain results in more than the algebraic sum of enhancements due to the two effects separately. A similar effect was also suggested by simulations in Si hole inversion layers. [33] This effect, however, has not been studied in III-Vs. If a similar effect exists, it could be effective in addressing the hole mobility problem.

In sum, strain has been demonstrated to be an effective approach to improve p-channel FET performance based on Si, Ge, $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$. The most appropriate configuration for obtaining the highest mobility enhancements and a mapping of the degree of enhancement under various conditions, nevertheless, requires an in-depth study. Among many possible configurations, uniaxial strain on $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$, especially combining uniaxial strain with biaxial strain in III-V quantum wells had not been studied by the time this thesis was launched. These strain configurations will be investigated through experiments in this thesis.

1.4 Thesis goals and outline

Replacing Si with III-V channel materials in CMOS faces many challenges. To name a few, large-scale Si wafer integration, high- k dielectrics for III-V MOS structures, and extrinsic device scaling are high in the list. In addition to these, developing a high-performance p-channel device remains a great challenge. The key problem is the low hole mobility of III-Vs as compared with n-channel $\text{In}_x\text{Ga}_{1-x}\text{As}$ FETs. This is true even for the candidate with the highest hole mobility. Therefore, fundamentally improving hole mobility through the introduction of strain to the device channel can be a feasible solution to this problem. This thesis focuses on exploring hole mobility improvement through the application of uniaxial strain as well as understanding other significant changes in other device characteristics associated with applied strain. The structures we study include $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ quantum wells.

Chapter 2 introduces theories of the most important physical effects related to strain effects in III-V transistors. The fundamentals of how strain changes the III-V band structure and therefore its transport properties are elaborated. In addition, two other effects, the piezoelectric effect and Schottky barrier height change, which affect transistor operation, are theoretically discussed. Chapter 3 presents an experimental methodology that we have developed to introduce uniaxial strain to III-V transistors in a controlled and measurable way. This is done through chip-bending experiments. The set-up that we built is described in Chapter 3. Chapter 4 presents experimental results on uniaxial strain effects on $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ quantum-well transistors. A detailed analysis of strain effects in different device designs is carried out. In Chapter 5, we extend our effort to introduce large-scale uniaxial strain through fabrication processes. A device

architecture employing self-aligned SiN stressors is developed to introduce uniaxial strain on a transistor structure with a channel under initial biaxial strain. Finally, the conclusions of this thesis are presented in chapter 6, together with suggestions for future work.

Chapter 2 Theoretical effects of uniaxial strain on III-V QW-FETs

2.1 Introduction

This chapter presents theories of the most significant physical effects that result from applying stress to III-V quantum wells. Individually, these effects have been studied in the past as properties of compound semiconductor materials. However, in our experimental transistors studies, we found that very often several effects come to play in the change of transistor characteristics as a result of applied stress. In the following discussion, we will uncover the physics of relevant stress effects including valence band (VB) dispersion, piezoelectric effect and band alignment shifts, as well as their manifestation on transistor characteristics.

2.2 Stress effect on valence band

Static stress changes the energy band dispersion because it affects the distance between semiconductor atoms. The deformation of crystals as a result of stress will be briefly introduced below; the band dispersion change will be discussed in the following subsections in detail.

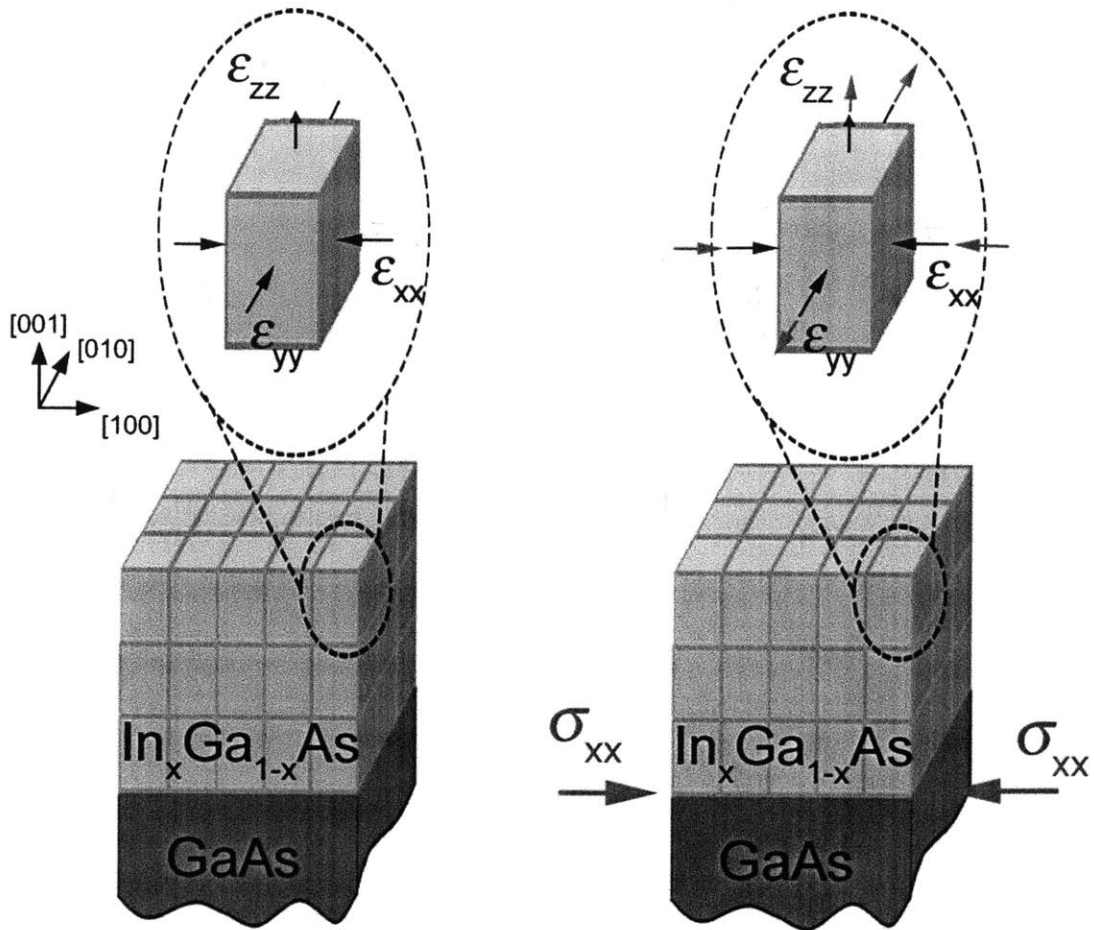


Figure 2-1. **(Left)** crystal deformation due to epitaxial **biaxial** strain. The crystal orientations for structures studied in this thesis are shown on the left. The arrows indicate the direction of the strain. The lattice mismatch between $\text{In}_x\text{Ga}_{1-x}\text{As}$ and GaAs induces biaxial compressive strain (ϵ_{xx} and ϵ_{yy}) in the film plane. An out-of-plane strain component (ϵ_{zz}) arises as a result of Poisson contraction. **(Right)** crystal deformation with in-plane compressive **uniaxial** stress (σ_{xx}) applied to the substrate and the epi-layer. The red arrows around the cubic unit cell indicate the strain components generated by σ_{xx} . Strain components along the same direction add linearly.

To consider strained quantum well structures, we first consider the mechanics of a pseudomorphically grown thin film on a lattice-mismatched substrate. Here, we describe the mechanics for a zinc-blende semiconductor grown along [001] direction, the growth direction for all the heterostructures (discussed in Chapter 3) used in this thesis. Figure

2-1 shows the deformation of a crystal lattice under epitaxial biaxial strain (left) and externally applied uniaxial strain (right). In this figure, $\text{In}_x\text{Ga}_{1-x}\text{As}$ on a GaAs substrate is used as an example. When a thin $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer is pseudomorphically grown on a GaAs substrate, in-plane biaxial strain (ε_{xx} and ε_{yy} in Figure 2-1) is induced, because the lattice constants of $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x > 0$) and GaAs are different. The in-plane strain is compressive, as $\text{In}_x\text{Ga}_{1-x}\text{As}$ has a larger lattice constant than GaAs and thus is compressed after the growth. The $\text{In}_x\text{Ga}_{1-x}\text{As}$ film also deforms in the growth direction, due to Poisson contraction of materials. For the growth induced biaxial strain, [34]

$$\varepsilon_{xx} = \varepsilon_{yy} \quad (2.1)$$

$$\varepsilon_{zz} = -\frac{C_{11}}{2C_{12}}\varepsilon_{xx} \quad (2.2)$$

The right figure in Figure 2-1 shows a scenario with a uniaxial stress (σ_{xx}) applied to the substrate and the epi-layer. This is similar to the mechanical settings in the bending experiments described in Chapter 3. In this case, three components of strain are generated along the major crystal directions:

$$\varepsilon_{xx_uniaxial} = \frac{\sigma_{xx}}{E} \quad (2.3)$$

$$\varepsilon_{zz_uniaxial} = \varepsilon_{yy_uniaxial} = -\nu \cdot \varepsilon_{xx_uni} \quad (2.4)$$

In the above equations, σ and ε are the stress and strain along the direction labeled by its subscript, the subscripts (xx , yy , zz) are used to denote axial components instead of shear components of stress/strain, ν is the Poisson ratio, E is Young's modulus, and C_{11} and C_{12} are elastic constants for cubic crystals. Notice that the total strain along a certain direction (xx , yy , zz) is simply the linear sum of all the components in that direction,

regardless of whether the components are generated by the epitaxial biaxial strain or externally applied strain, if any of these strain exists.

Besides the strain components along each direction, a hydrostatic strain component calculated as

$$\varepsilon_{hydro} = \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz} \quad (2.5)$$

is found to be relevant to study the strain-induced band alignment shifts discussed below.

The change in band dispersion fundamentally impacts the transport properties, among others. [35] This change in band dispersion is the foundation of the use of strain to improve transistor performance. In fact, energy band engineering by using strain has become a widely used technique in electronic devices. [18] A framework to study this is through the *k.p* method. [36] By using this framework, band dispersions with various strain configurations can be numerically calculated. In the following discussion, strain effects on valence band dispersion will be discussed accompanied with examples using *k.p* calculations.

2.2.1 Valence band in relaxed bulk materials

In unstrained bulk III-V compounds, the valence band at the Γ point in the Brillouin zone is two-fold degenerated (four-fold, if considering spin degeneracy), consisting of a heavy-hole (hh) band and a light-hole (lh) band. These two bands are named this way because they generally have different effective masses. Figure 2-2 shows an example of valence band dispersion from bulk relaxed $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ as calculated by the *k.p* method (by Nextnano³, www.nextnano.de). Each band is symmetric along equivalent orientations,

for example, [100], [010], and [001]; but is different along non-equivalent orientations, for example, [100] and [110]. Such bands usually are called non-spherical bands.

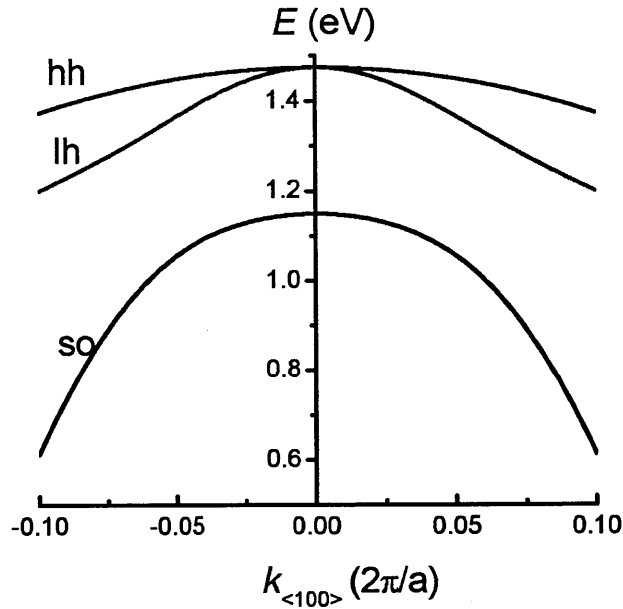


Figure 2-2. Dispersion relation along $\langle 100 \rangle$ direction for bulk relaxed $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$. The heavy-hole (hh) and light-hole (lh) bands are degenerate at $k = 0$ (the Γ point).

2.2.2 The role of quantization

This study considers quantum well devices. In quantum wells, carriers are confined along the growth direction, but are free to move in the quantum well plane. Quantization affects the energy levels of the band maxima of heavy-hole and light-hole bands. In addition, quantization also changes the valence band dispersion relation and therefore transport in the quantum well plane. To obtain the in-plane dispersion relation in a quantum well, self-consistent $k \cdot p$ and Schrodinger-Poisson calculations are necessary, which are more complicated and computationally intensive than the bulk dispersion relations mentioned above.

Figure 2-3 shows such a valence-band dispersion graph for 2DHG in a 9-nm $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well. In this calculation, no strain was incorporated. The lh and hh bands of the bulk semiconductor split into a series of subbands. The subbands are labeled with hh1, lh1, hh2, lh2, etc, as if the hh and lh bands in the bulk material were quantized to separate ladders of subbands. The rationale to do so is that the subband maxima appear to be close to the corresponding subband energy levels calculated by the conventional method for treating electron quantization, *i.e.*, the bulk effective masses perpendicular to the quantum-well plane are used as the quantization effective masses. [37] But in fact, each of the subbands in the range of nonzero wave vector consists of mixed states from the original hh, lh and so bands of the bulk materials. [37-38] The degree of band splitting depends on quantization: the thinner the QW, the higher the subband separation. It also depends on the original effective mass in the bulk material, the lighter it is, the stronger the quantization.

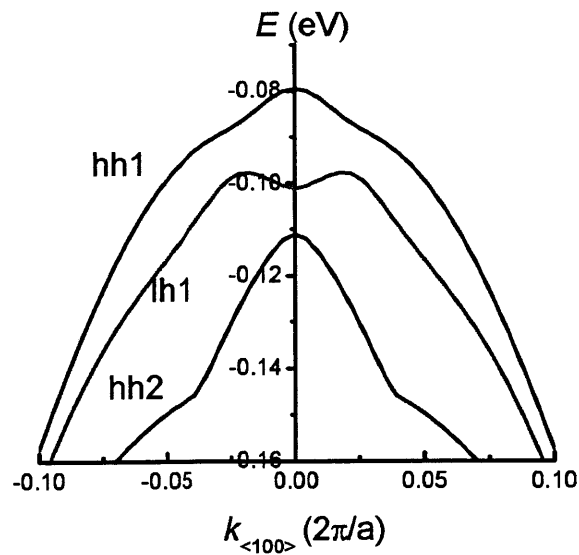


Figure 2-3. In-plane dispersion relation along $\langle 100 \rangle$ for a relaxed 9-nm thick $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well. The degeneracy is broken at the Γ point.

Figure 2-4 shows the 2D iso-energy contours of the hh1 band in

Figure 2-3. Each contour line represents the locus in k space of states with identical energy. The energy separation between contours is 20 meV. These 2D iso-energy contours show clearly the anisotropic valence band dispersion in the entire momentum space. This type of plot is useful when the bands are non-spherical or when the bands are affected in an anisotropic way. Such is the case in general for valence band under strain. In this type of in-plane dispersion relation graphs, the denser the iso-energy lines along a certain orientation are, the smaller the effective mass is along that orientation. It can be clearly seen in Figure 2-4 that the effective masses in hh1 band are highly anisotropic and also vary with energy.

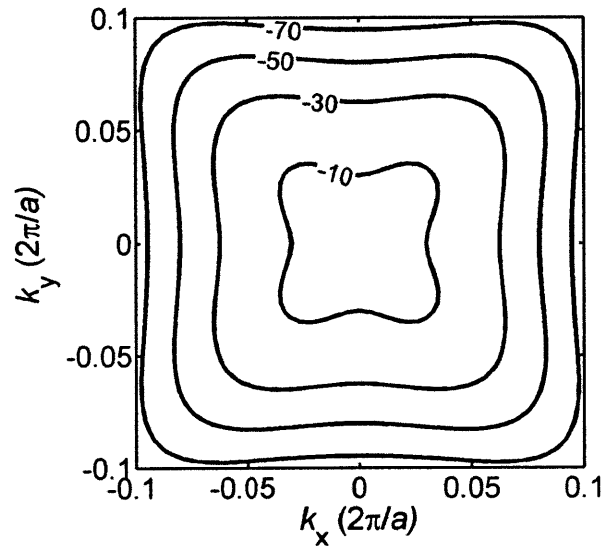


Figure 2-4. 2D iso-energy contours in the k -space for hh1 in Figure 2-3. Two adjacent curves are separated by 20 meV.

2.2.3 The role of strain

The valence band of compound semiconductors changes in several ways when strain is applied to quantum wells. The first effect is the split between the heavy- and light-hole bands. The maxima of these two bands are separated due to quantization in a 2D quantum well, as shown in Figure 2-3. When strain is applied, the maxima of the two bands will further split. The split magnitude can be about several tenths of meV when a biaxial strain of around 1% is applied. [18] Figure 2-5 shows the valence band dispersion when applying -1.7% compressive biaxial strain to the 9-nm $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well discussed above. Compared with Figure 2-3, the hh1 and lh1 bands in Figure 2-5 are separated by an additional 12 meV, due to the applied biaxial strain.

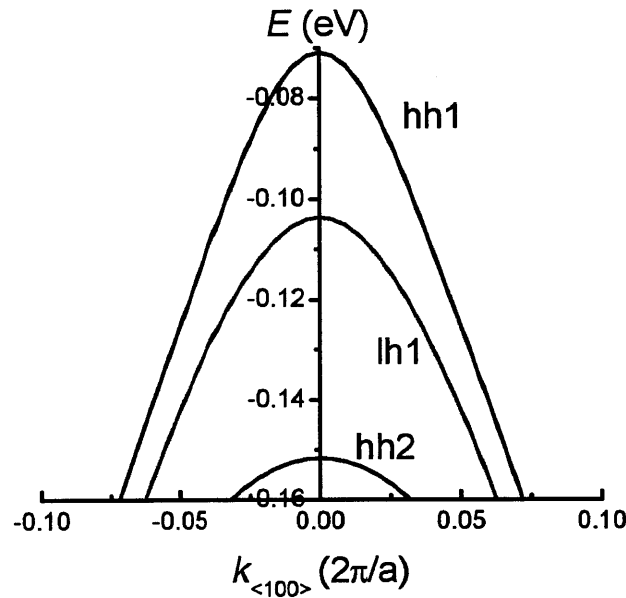


Figure 2-5. In-plane dispersion relation for a 9-nm $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well with -1.7% biaxial compressive strain.

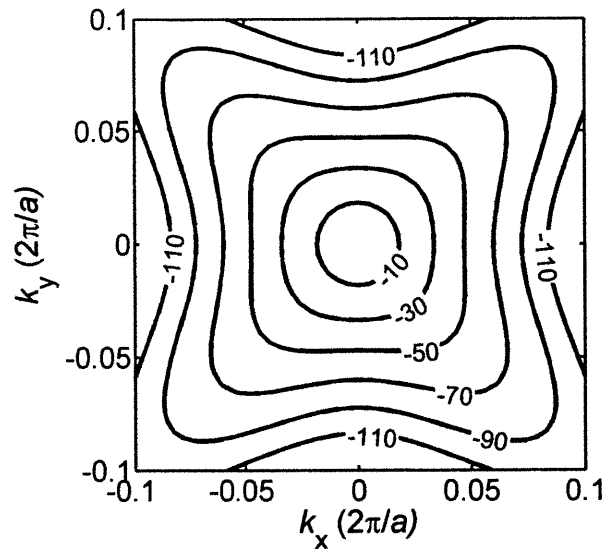


Figure 2-6. 2D iso-energy contours in the k -space for hh1 in Figure 2-5.

The second effect of strain is warping the bands. This can also be clearly seen in Figure 2-5. The curvatures of hh1 and lh1 subbands are increased, so that the effective masses of the bands are reduced. These top two bands are most important, as they are preferentially occupied by holes. The warping effect due to biaxial strain affects the valence band along all k orientations. This can be clearly seen if we compare Figure 2-4 and Figure 2-6. It is clear from this figure that the 2D iso-energy contours are compressed along all the directions causing a reduction in effective mass. This is a general effect of compressive biaxial strain. In fact, one general effect of compressive biaxial strain is to reduce the in-plane hole effective mass in the strain plane. Tensile biaxial strain has the opposite effect.

Uniaxial strain has a more subtle effect on the valence band structure than biaxial strain, just discussed. Specifically, applying uniaxial strain in the quantum well plane changes the in-plane dispersion in an anisotropic way. The change varies with the orientation of transport with respect to the strain orientation. In general, compressive uniaxial strain compresses the iso-energy contours along its direction and elongates them in the

perpendicular direction. Tensile uniaxial strain has the opposite effect. These effects have also been observed in Si [28] and Ge [39].

Table 2-1 summarizes hole effective mass changes along two orthogonal directions under uniaxial strain. The trend shown in this table is not only for $\langle 110 \rangle$ uniaxial strain but universal for uniaxial strain along other directions. This is also true regardless if the quantum well is under biaxial strain already. The prior presence or absence of biaxial strain is only of modifying the *magnitude* of the effective mass change.

	Tensile	Compressive
$m^*_{//}$	↑	↓
m^*_{\perp}	↓	↑

Table 2-1. Qualitative change of hole effective mass by uniaxial strain. The orientation of effective mass with respect to the uniaxial strain is labeled by parallel ($//$) and perpendicular (\perp).

As a specific example, we simulated the change in valence band structure due to uniaxial strain in the 9 nm InGaAs quantum well studied above, which already includes biaxial strain. Figure 2-7 shows the anisotropic change in the in-plane dispersion relation in response to the application of 0.1% compressive uniaxial strain along the $[-110]$ direction. In this figure, $k_{//}$ is along $[-110]$ and k_{\perp} is along $[110]$. It can be seen that the uniaxial strain increases the curvature of the $E-k$ curves along $k_{//}$, while decreases the curvature along k_{\perp} . The increase/decrease of the curvature indicates a decrease/increase of the effective mass along the corresponding k direction. We can more clearly see the anisotropic change of effective mass in the whole plane of the quantum well from the density changes of the 2D iso-energy contours of the valence band. Figure 2-8 shows

these changes of the hh1 band in the whole quantum well plane. In this figure, the changes parallel and perpendicular to the uniaxial strain agrees with the general effect discussed above. In between these two directions, only a little change is observed for the direction that is 45 degree rotated with respect to the strain direction.

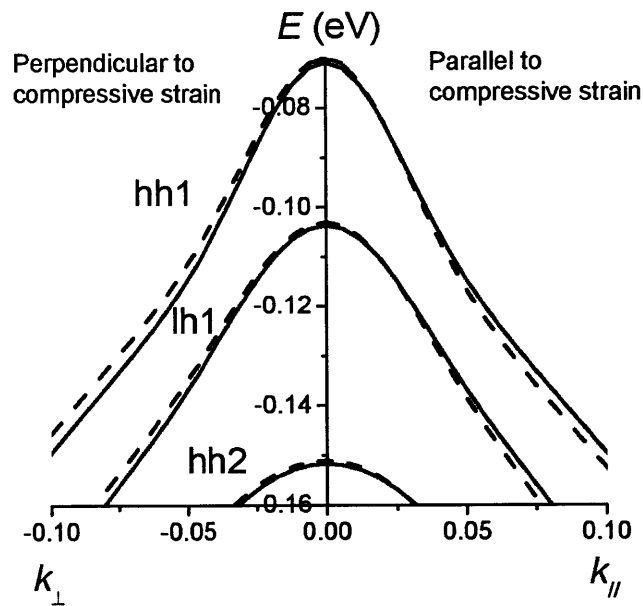


Figure 2-7. In-plane dispersion change under uniaxial compressive stress in a 9-nm $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well with -1.7% biaxial strain. The solid lines in red show the dispersion without uniaxial stress, while the blue dotted lines show the case with uniaxial stress.

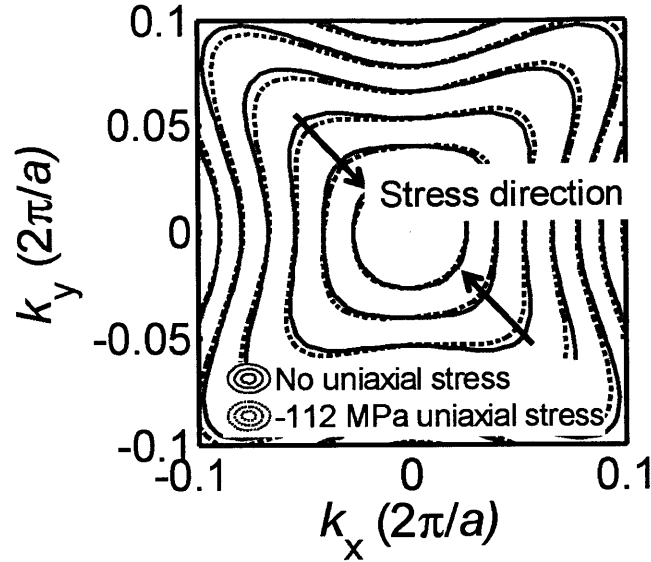


Figure 2-8. Changes of 2D iso-energy contours in k -space under uniaxial compressive stress in a 9-nm $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well with -1.7% biaxial strain. The solid lines in red show the dispersion without uniaxial stress, while the blue dotted lines show the case with uniaxial stress applied along the black arrows.

One final remark is that it is not possible to generalize whether the quantization effect on the VB dispersion is significant or marginal as compared with strain effects. The degree of the two effects matters. In some cases, for example, in strained Si pMOSFET with biaxial strain at high gate bias, the quantization can be so strong that the shift of the subband energy levels can increase the overall effective mass and cancel the mobility enhancement brought by the biaxial strain. In contrast, $\langle 110 \rangle$ strain in Si changes the valence band in a way such that the quantization effective mass of the band with a lighter in-plane transport effective mass gets increased by strain. Therefore, the band of lighter in-plane hole effective mass is less lifted by quantization and thus is still substantially occupied at high gate bias. In this case, the hole mobility enhancement is retained even at high gate bias. In fact, this is one of the reasons mentioned in Chapter 1 for $\langle 110 \rangle$ uniaxial strain to be the most effective for hole mobility enhancement in Si MOSFETs.

2.2.1 Hole effective mass approximation

In the above discussion, the effective mass is qualitatively interpreted as a parameter that depends on the curvature of the energy band or density of 2D iso-energy contours in k - space. More rigorously, the effective mass is usually calculated from the dispersion relation for a certain band in the following way:

$$m^* = \hbar^2 \left(\frac{d^2 E}{dk^2} \right)^{-1} \quad (2.6)$$

where \hbar is reduced Planck constant, E is energy and k is wave vector. Eq. (2.6) can be applied when the energy band is isotropic and quadratic. Such is the case near the conduction band minima in semiconductors.

For valence bands, even in relaxed bulk materials, simply applying Eq. (2.6) is meaningless. This is because the bands are non-spherical and non-parabolic. Therefore, no single value of m^* can be used to describe the E - k relationship at the top of the band, because the curvature varies with E and also along different k directions even for the same E . In fact, the curvature can even reverse sign within one single band, as for the hh1 band in the example of

Figure 2-3. The complex shape of the valence bands makes studying hole transport mathematically more complicated than electron transport. [16] Numerical rather than analytical calculations are needed.

An approximation to reduce the complexity of treating the non-parabolic valence bands was proposed based on an energy dependent m^* approach. [40-41] Instead of taking the 2nd derivative of the E - k relation as in Eq. (2.6), m^* is calculated as a function of E in the following way:

$$m_i^*(E, \vec{k}_i) = \frac{\hbar^2 |\vec{k}_i|^2}{2(E_{V_i} - E_i)} \quad (2.7)$$

where m_i^* is the effective mass for the i^{th} subband in the quantum well along a certain \vec{k}_i direction, E_{V_i} is the band maximum for the i^{th} subband, and E_i is the allowed energy in the i^{th} subband determined by the subband's dispersion relation. To obtain the effective mass for the whole valence band along the \vec{k}_i direction, m_i^* must be weighted by the carrier occupation in the corresponding i^{th} subband [41]:

$$m^*(\vec{k}) = \frac{\sum_i \int_{E_{V_i}}^{\infty} m_i^*(E, \vec{k}) f(E) g_i(E) dE}{\sum_i \int_{E_{V_i}}^{\infty} f(E) g_i(E) dE}$$

where $f(E)$ is Fermi-Dirac distribution, and $g_i(E)$ is the density of states in the i^{th} subband.

Applying Eqs. (2.7) and (2.8) to the valence band dispersion relation calculated by the $k.p$ method in the quantum well, we can obtain one single effective mass to characterize the valence band along a certain \vec{k} direction. As an example, the effective mass calculated by Eq. (2.8) for the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well along the $\langle 110 \rangle$ directions is shown in Figure 2-9. The quantum well is under 1.7% compressive biaxial strain. On top of that, three levels of uniaxial strain was applied along the y direction: zero strain, 0.1% tensile strain, and 0.1% compressive strain. The effective mass is plotted as a function of hole concentration. The results were calculated by varying the Fermi level across a certain range through the valence band. The effective mass increases almost linear with hole concentration. This linear dependence of m^* on p_s agrees with measurements in an $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ quantum well for holes [42]. Over the full range of p_s in Figure 2-9, tensile uniaxial strain increases $m^*_{//}$ while compressive uniaxial strain reduces $m^*_{//}$. The $m^*_{//}$ was

obtained along one of the two $\langle 110 \rangle$ directions. At this moment, $m^*_{//}$ along the two $\langle 110 \rangle$ directions are equal. The $m^*_{//}$ change was qualitatively expected from the band dispersion change, as shown in Figure 2-7.

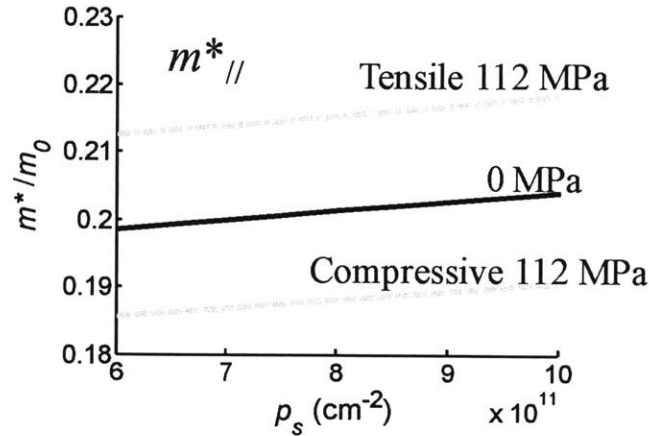


Figure 2-9. Effective mass ($m^*_{//}$) along uniaxial stress direction, $\langle 110 \rangle$, in the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well with 1.7% compressive biaxial lattice-mismatch strain. Three levels of uniaxial stress were applied 0, 112 and -112 MPa. These values correspond to no uniaxial strain, $\sim 0.1\%$ tensile strain and $\sim 0.1\%$ compressive strain.

Admittedly, the approximation to the calculation of the effective mass that is use here is rough if used for mobility calculations. This is more so the case because in a III-V quantum well, the scattering time is likely to be energy-dependent, inelastic and anisotropic. Nonetheless, this approach gives us a way to capture the change in the subband shape along a certain \vec{k} direction as well as the band splits due to applied strain and quantization. Insights on these changes are useful for understanding strain effects, especially when the strain range is small and a dominant portion of hole transport change can come from the change in the effective mass [16, 33]. In the following chapters, this approximation will be used to discuss strain effects on valence band and hole transport.

2.2.2 Mobility calculation

For spherical bands, conductivity m^* calculated by (2.6) can be neatly used to calculate carrier mobility (μ) using the equation below:

$$\mu = \frac{q\tau}{m^*} \quad (2.9)$$

where τ is scattering time and q is the Coulomb charge of an electron.

However, Eq. (2.9) cannot be directly applied to valence bands, because they are non-spherical as discussed above. A sophisticated approach to calculate hole mobility in inversion layers or quantum wells is discussed in [16]. This approach accounts for the detailed dispersion in k -space without resorting to extracting effective mass. Nevertheless, the effort to build the model and calculations in [16] is nontrivial. For the study in this thesis, we adapt the effective mass approximation mentioned above to capture the valence band changes. For simplicity, we also assume that changes in μ come from changes in m^* ; equivalently, the scattering time is assumed to be constant with strain. This assumption is still rough. However, it may allow us to capture the major part of $\Delta\mu$. This is because Fischetti [16] and Wang [33] pointed out that under small strain, changes in m^* account for a dominant portion (up to 85%) of $\Delta\mu$.

2.3 Piezoelectric effect

The piezoelectric effect occurs in polar materials. In particular, when unequal amount of uniaxial strain is applied along the two $\langle 110 \rangle$ directions to a zinc-blende III-V heterostructure with a [001] growth direction, a polarization field (P_z) is generated along the growth direction. [43-44] This is schematically shown in Figure 2-10.

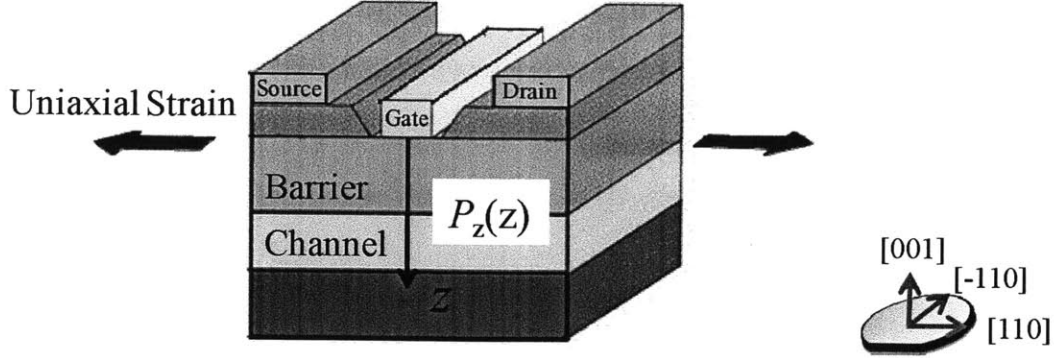


Figure 2-10. Schematics of piezoelectric effect in III-V QW-FETs with [001] growth orientation.

The polarization field is related to the $\langle 110 \rangle$ uniaxial strain by

$$P_z = \frac{1}{2} e_{14} \cdot (\epsilon_{[110]} - \epsilon_{[-110]}) \quad (2.10)$$

where e_{14} is the piezoelectric coefficient, $\epsilon_{[110]}$ and $\epsilon_{[-110]}$ are the strain along [110] and [-110], respectively.

The presence of a polarization field directly changes the device electrostatics, because the direction of P_z is exactly the direction of the gate electric field. As a consequence, two changes are expected: threshold voltage (V_T) shift and gate capacitance (C_G) shift.

The V_T shift occurs because P_z changes the electronic band bending along the growth direction. Mertens [45] modelled this change in V_T as a result of P_z in a double delta-doping high electron mobility transistors (HEMT):

$$\Delta V_T = - \int_0^{BC} \frac{P_z(z)}{\epsilon(z)} dz \quad (2.11)$$

where BC stands for the back channel-barrier interface, z is defined in Figure 2-10 as the distance from the gate contact along the growth ([001]) direction to a point in the heterostructure and $\epsilon(z)$ is the dielectric constant along z . The model in Eq. (2.11)

indicates that ΔV_T increases with the thickness of the barrier and channel. In addition, ΔV_T is also expected to be more pronounced in heterostructures with larger e_{14} , as Eq. (2.10) and (2.11) together suggest. One unique aspect of the piezoelectric effect seen in Eqs. (2.10) and (2.11) is that changing the uniaxial strain from [-110] to [110] directions reverses the direction of P_z and consequently the sign of ΔV_T . This is the unique signature of the piezoelectric effect.

The piezoelectric effect also causes a change in gate capacitance C_G . This shift originates from the displacement of 2 dimensional electron/hole gas (2DEG/2DHG) in the quantum well as its shape changes due to the appearance of P_z . C_G can be modelled as three capacitors connected in series (Figure 2-11 inset for an n-type quantum well structure): the insulator capacitor (C_{ins}), the centroid capacitor (C_{cent}), and the quantum capacitor (C_Q). The centroid capacitor comes from the fact that 2DEG/2DHG in the QW is usually centered at a distance away from the barrier-channel interface. The quantum capacitor originates from the limited density-of-states in the channel. As P_z changes the profile of the quantum well band, the wave function of the 2DEG/2DHG is changed. Therefore, the carrier distribution is also changed; C_{cent} increases or decreases depending on whether the carriers move toward or away from the gate.

Figure 2-11 depicts this C_{cent} change with an example simulation of the 2DEG shift in a QW induced by piezoelectric effect. In Figure 2-11, the change of overall C_G is $\sim 10\%$ with a strain change from -1% to 1%. The sensitivity of C_G to strain increases as the insulator thickness decreases.

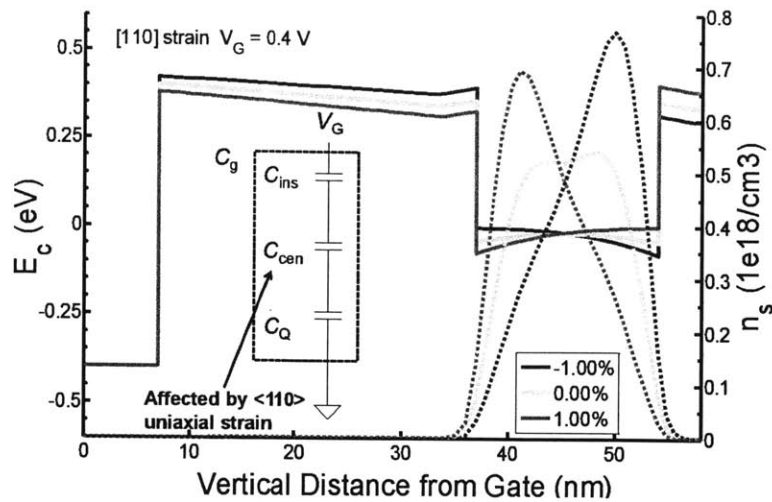


Figure 2-11. Gate capacitance (C_G) model and the piezoelectric effect on C_G . The 1D Schrodinger-Poisson simulation shows that the centroid of 2DEG is significantly shifted by uniaxial strain.

The aforementioned piezoelectric effect can be incorporated into Schrodinger-Poisson simulations (Nextnano³, www.nextnano.de). The QW profile obtained by such simulations can be used for bandstructure calculation using $k.p$ method for QWs. These Schrodinger-Poisson simulations as well as $k.p$ calculations will be used in the rest of this thesis.

2.4 Schottky barrier height change

Extensive research [46-49] suggests that there is a common reference level, a transition-metal impurity level, for band lineups and Schottky barrier height (ϕ_B) in compound semiconductors. This energy level falls constant with respect to the vacuum energy level across many materials. It is by lining up this level that conduction and band discontinuities between different semiconductors can be calculated [50].

When strain is applied to a semiconductor, the conduction band and valence band edge changes with respect to this reference energy level. In consequence, applying strain to a heterostructure will affect the conduction and band discontinuities between the various layers.

According to deformation potential theory [34, 51], the change of conduction minimum or valence band maximum at the Γ point in the Brillouin zone as a result of the application of stress is determined by the product of the hydrostatic component in Eq. (2.5), discussed at the beginning of this chapter, of applied strain and the deformation potential of the semiconductor:

$$\Delta(E_c - E_T) = a_c \cdot \varepsilon_{hydro} \quad (2.12)$$

$$\Delta(E_T - E_v) = a_v \cdot \varepsilon_{hydro} \quad (2.13)$$

where E_c and E_v are the band edge energies for conduction band and valence band, E_T is the transition-metal impurity level, a_c and a_v are the hydrostatic deformation potentials for conduction band and valence band at the Γ point. A survey of a_c and a_v values of various III-V compound semiconductors can be found in Vurgaftman's review article [52]. When strain is applied to a heterostructure, band offsets between the different material layers change. This is because the deformation potentials of these layers are different. The offset shift between a barrier and a channel can be calculated as

$$\left(a_{c/v_barrier} - a_{c/v_channel} \right) \cdot \varepsilon_{hydro} \quad (2.14)$$

But this offset change can be rather small for arsenides and antimonides. For example, $a_c(\text{In}_{0.15}\text{Ga}_{0.85}\text{As})$ is -6.11 eV; and $a_c(\text{Al}_{0.23}\text{Ga}_{0.77}\text{As})$ is -6.15 eV. Under 0.1% tensile hydrostatic strain, the conduction band offset between $\text{Al}_{0.23}\text{Ga}_{0.77}\text{As}$ and $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ decreases by 0.04 meV.

Another consequence of the strain-induced changes in the valence and conduction band edges is that the Schottky barrier height of a metal on a compound semiconductor also changes. The change in ϕ_B should not have any difference between the two $\langle 110 \rangle$ directions, as the hydrostatic strain for uniaxial stress along the two directions are equal. The sign of $\Delta\phi_B$ is determined by the signs of deformation potentials, as seen in Eqs. (2.12) and (2.13): for conduction band, $\Delta\phi_B$ is negative under tensile strain and positive under compressive strain; for valence band, the sign remains the same for in conduction band, but can be reversed in materials containing AlAs. Notice a_c and a_v are both negative for most of III-V materials [52], but a_v is positive for certain materials (e.g. AlAs) [53]. $\Delta\phi_B$ is usually more than one order of magnitude higher than the band offset shifts discussed in the previous paragraph. This is because usually $(a_{c/v_barrier} - a_{c/v_channel}) \ll a_{c/v_barrier}$ in our heterostructures. In the previous example with a $\text{Al}_{0.23}\text{Ga}_{0.77}\text{As}$ barrier and a $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ channel, $\Delta\phi_B$ is -6.11 meV under 0.1% tensile hydrostatic strain. This is two orders of magnitude larger than the conduction band offset under the same amount of strain calculated in the previous paragraph.

The expected Schottky barrier height change should translate directly to a threshold voltage shift (ΔV_T) in QW-FETs. The relationship is straightforward: $\Delta V_T = \Delta\phi_B$ [45]. This effect is included in Schrodinger-Poisson simulations for our heterostructures.

2.5 Summary

This chapter presents the three major effects produced by strain in III-V quantum-well structures that we have found relevant to our device experiments. These effects include strain-induced valence band change, piezoelectric effect induced by uniaxial strain, and

Schottky barrier height change. The valence band change is the core of applying strain engineering for improving device performances, whereas the later two effects can affect the electrostatics of devices in significant ways. The physics of these effects will be referred to in the following chapters. In the next chapter, we will discuss the experimental studies of strain effects on III-V QW-FETs, starting with an introduction of our experimental set-ups.

Chapter 3 Experimental methodology for measuring uniaxial strain effects

3.1 Introduction

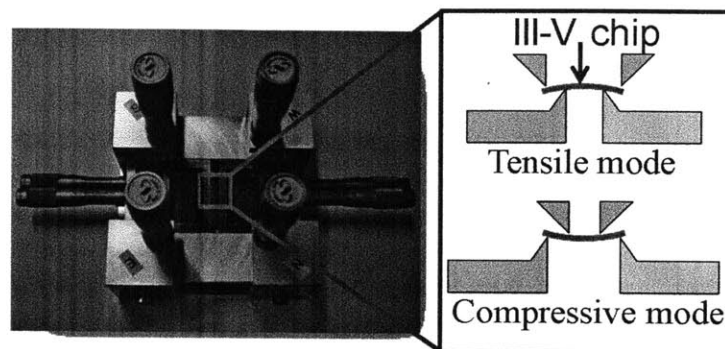
We have studied the effect of uniaxial strain on III-V p-channel quantum-well field effect transistors (QW-FETs) through chip-bending experiments. Measurements that apply external mechanical stress to devices by bending the substrates have been shown to be useful to bring insights into strain effects in Si and Ge devices. [28, 39] For Si or Ge devices, a large strip of a wafer rather than a chip with a few dies can be used for bending experiments. This is because the Si substrate is less expensive and more mechanically rugged compared with III-V substrates. In our study, a mechanical apparatus was designed and fabricated to accommodate relatively small as well as fragile III-V semiconductor chips and apply uniaxial stress to devices on the chips. While uniaxial stress was applied, a benign measurement suite was used to measure III-V QW-FETs and ungated Hall bars. This chapter presents in detail the design of the chip-bending apparatus, our semiconductor device structures and the electrical measurements performed in our devices.

3.2 Chip-bending apparatus

The chip-bending apparatus is pictured in Figure 3-1. The apparatus is able to perform four-point bending upon chips positioned between two pairs of jaws (Figure 3-1 a). The horizontal position of the jaws is controlled by four horizontal micrometers. Four vertical

micrometers are used to apply force on the upper pair of jaws. Either tensile or compressive stress can be applied to the top surface of the chips depending on the configuration of the jaws (Figure 3-1 a).

(a)



(b)

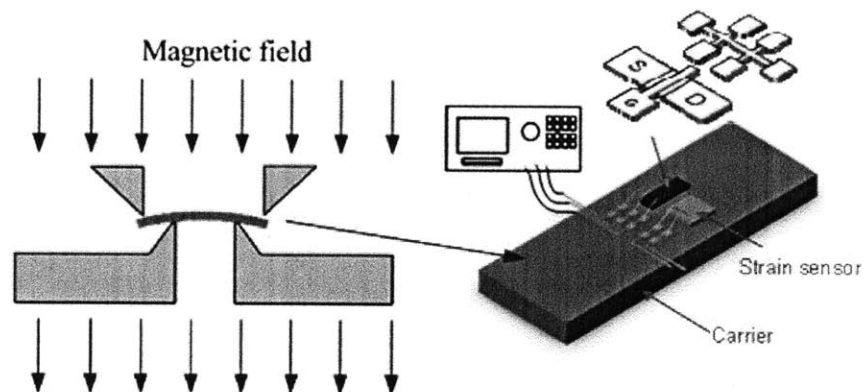


Figure 3-1 (a) Chip-bending apparatus and its working mechanism to introduce uniaxial stress to III-V chips. (b) Configuration of a magnetic field and electrical connections to a chip attached to an aluminum carrier.

Our experimental methodology has been optimized to apply large strain to III-V chips. This was accomplished by thinning the chips to around 100 μm by mechanical grinding and by attaching them to an aluminum carrier. In this way, we were able to introduce a strain level of $\pm 0.3\%$ to GaAs chips before they crack. This is about 5x the value that can

be attained by directly bending GaAs chips.

Hall measurements were enabled with a pair of permanent magnets that apply a magnetic field perpendicular to the chip surface (Figure 3-1 b). The strength of the magnetic field was measured to be 3465 ± 10 Gauss. The major body of the chip-bending apparatus is made of aluminum and demagnetized stainless steel. Therefore, the mechanical parts around the semiconductor sample do not affect the magnetic field distribution.

As shown in Figure 3-1 (b), in the course of our experiments, the strain was evaluated by a strain gauge attached beside the III-V chips each time the bending was changed. Strain transfer from the aluminum carrier to the mounted GaAs chip was checked by comparing the readings of two strain gauges: one on the aluminum surface and the other one on the GaAs chip surface. The difference between these two readings was found to be within 3.5%.

In our chip-bending experiments, we verified that the loading and unloading of strain is linear and has no hysteretic behavior. The level of strain in the experiments was kept below 0.1%, one third of the maximum strain that we have been able to attain (0.3%). This was in order to secure the samples for repeated measurements. This strain level is also below the yield point for the aluminum carrier so that the deformation of the carrier is elastic. Figure 3-2 shows an example of threshold voltage (V_T , defined below) change with applied stress. This example is from a p-channel GaAs QW-FET with [-110] channel and [110] applied stress. The fact that ΔV_T tracks closely the measured strain verifies that stress was successfully applied to the QW-FET and that the device remains pristine throughout the entire set of measurements.

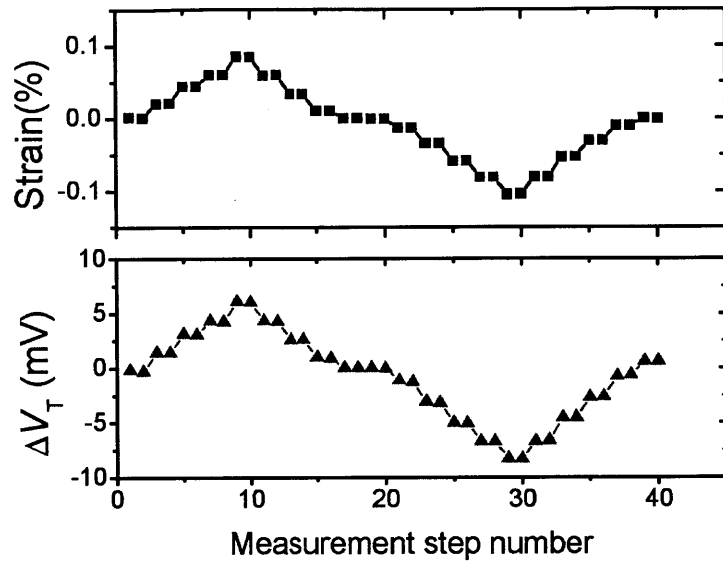


Figure 3-2. An example of sequential change of V_T with strain measured on the aluminum carrier. The strain and V_T data were taken from experiments of the p-channel GaAs sample with applied stress along [110] and QW-FET channel along [-110].

Since stress is usually used as the controlled variable in Si and Ge substrate-bending experiments, we converted the measured strain to stress by multiplying by the Young's Modulus of the channel material.

Table 3-1 lists the $\langle 110 \rangle$ Young's modulus of the channel materials used in this study along with the values for Si and Ge. The values for $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$, $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ are linearly interpolated from corresponding binary compounds (InAs, GaAs, InSb and GaSb). The values for these binaries as well as values of Si, and Ge can be found in [54].

Material	Si	Ge	GaAs	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$	$\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$
E (GPa)	168	137	122	115	112	78

Table 3-1. $\langle 110 \rangle$ Young's Modulus (E) of various channel materials.

The III-V chips were attached to the aluminum carrier by epoxy. The semiconductor devices were wire-bonded to metal pads attached to the aluminum carrier. (Figure 3-1 b) The metal pads were premade and attached to the aluminum carrier using the above epoxy. They are insulated from the carrier by a plastic film. The metal pads were then connected to a semiconductor parameter analyzer. By using wire-bonding, rather than probing, to connect our devices, any probing resistance variations can be eliminated in our measurements.

3.3 Devices

The devices studied in this work were fabricated from four different heterostructures. These are shown in Figure 3-3. The n-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ structure in Figure 3-3 (a) features a double silicon delta-doping below and above the channel. The p-channel GaAs structure (Figure 3-3 b) has a channel lattice-matched to the substrate and therefore free of biaxial strain. The p-channel $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ (Figure 3-3 c) and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ (Figure 3-3 d) structures feature -1.7% and -2.1% lattice-mismatch biaxial strain in the channel, respectively.

The device structures we chose to characterize include QW-FETs with a Schottky gate and ungated Hall bars. QW-FETs based on heterostructure (a) were provided by Mitsubishi Electric. These devices have a gate length of 1 μm . Electrons flow along the [-110] direction.

(a)

n ⁺ GaAs Cap	Si delta doping
Al _{0.23} Ga _{0.77} As	30 nm
In _{0.15} Ga _{0.85} As	17 nm
Al _{0.23} Ga _{0.77} As buffer	
S.I. GaAs	

(b)

p ⁺ GaAs Cap	30 nm	1.5x10 ¹² cm ⁻² Carbon doping
Al _{0.42} Ga _{0.58} As	21 nm	
GaAs	40 nm	
Al _{0.42} Ga _{0.58} As	30 nm	
Al _{0.33} Ga _{0.67} As/GaAs buffer		
S.I. GaAs		

(c)

p ⁺ GaAs Cap	30 nm	1.5x10 ¹² cm ⁻² Carbon doping
Al _{0.42} Ga _{0.58} As	21 nm	
In _{0.24} Ga _{0.76} As	9 nm	
Al _{0.42} Ga _{0.58} As	30 nm	
Al _{0.33} Ga _{0.67} As/GaAs buffer		
S.I. GaAs		

(d)

InAs Cap	2 nm
In _{0.2} Al _{0.8} Sb	4 nm
Al _{0.8} Ga _{0.2} Sb	10 nm
In _{0.41} Ga _{0.59} Sb	7.5 nm
Al _{0.8} Ga _{0.2} Sb	1.5 μm
S.I. GaAs	

Figure 3-3. Schematic of the four heterostructures studied in this thesis by chip-bending experiments: (a) n-channel In_{0.15}Ga_{0.85}As structure, (b) p-channel GaAs structure, (c) p-channel In_{0.24}Ga_{0.76}As structure and (d) p-channel In_{0.41}Ga_{0.59}Sb structure.

Structure (d) in Figure 3-3 was provided by Naval Research Laboratory. This structure is characterized by a Hall mobility of 1500 cm²/V.s and a sheet hole density (p_s) of 6.6×10¹¹ cm⁻². This mobility is the highest for holes in III-V compounds so far. The channel is under 2.1% biaxial compressive strain, which contributes to the high hole mobility. [9] The fabricated QW-FETs have a 0.2 μm gate length. Holes flow in the channel of these devices along the [110] direction. Other electrical characteristics of these devices are given in [55].

P-channel arsenide devices based on heterostructures (b) and (c) in Figure 3-3 were fabricated by this author at MIT on samples grown at Prof. S. Oktyabrsky's lab at SUNY Albany. The fabrication process for the p-channel arsenide devices is briefly described next.

The process starts with mesa etching by a $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1:1:25) solution (Figure 3-4 (a)). After this, ohmic contacts were formed by electron-beam evaporated Ni/Au/Zn/Au (10 nm/10 nm/30 nm/200 nm) and rapid thermal annealing (RTA) at 440 °C for 30 s (Figure 3-4 b). Next, gate recess for the FETs was performed by a citric acid/ H_2O_2 (4:1) solution [56]. The GaAs cap layer was selectively etched. Ti/Pt/Au (20 nm/20 nm/200 nm) was evaporated to form the gate. (Figure 3-4 c) The ungated Hall bars were recessed at the same time but were covered during gate metal evaporation. Finally, Ti/Au (20 nm/200 nm) was evaporated to form contact pads. (Figure 3-4 d)

Typical output characteristics of a finished p-channel QW-FET based on the structure in Figure 3-3 (b) are shown in Figure 3-5. This QW-FET has a gate length (L_G) of 2 μm and a gate width of 50 μm , showing satisfactory working properties. Figure 3-6 and Figure 3-7 show the transfer and subthreshold characteristics of the fabricated QW-FET. The performance of this device are comparable to what has been reported in literature [57-58] for similar devices with a similar L_G .

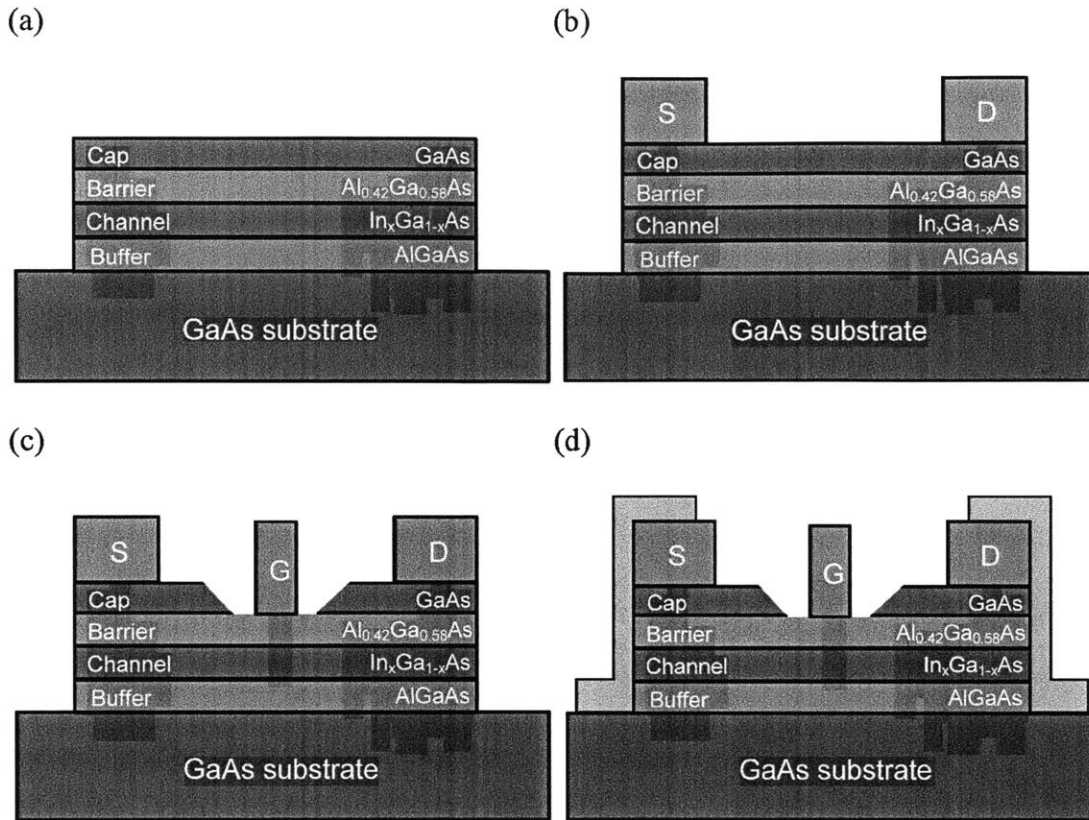


Figure 3-4. Schematic view of the fabrication processes for p-channel arsenide QW-FETs: (a) Mesa isolation; (b) Ohmic contact formation; (c) Gate recess process and gate metallization; (d) Probing pad formation.

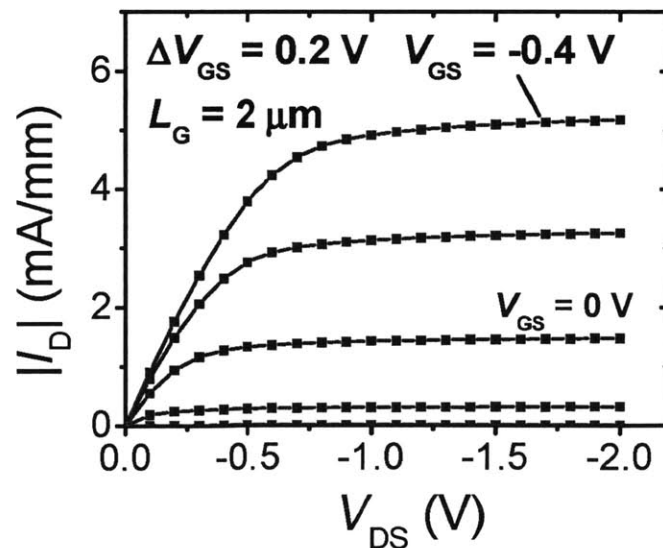


Figure 3-5. Typical output characteristics of a QW-FET with $L_G=2 \mu\text{m}$. The starting heterostructure of this QW-FET is shown in Figure 3-3 (b).

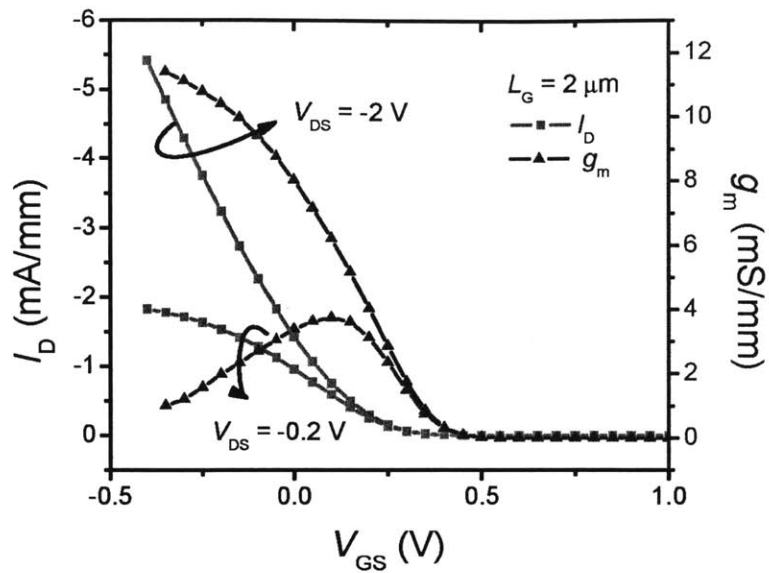


Figure 3-6. Transfer characteristics in linear and saturated regimes of the fabricated GaAs QW-FET with $L_G = 2 \mu\text{m}$.

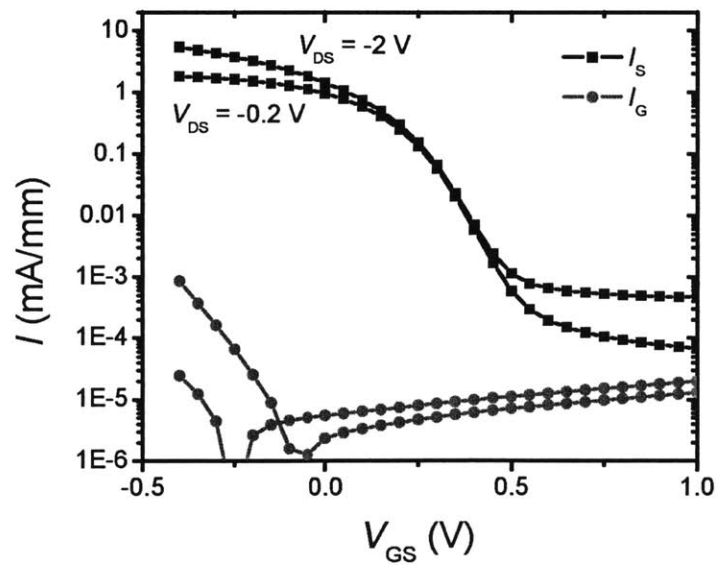


Figure 3-7. Subthreshold characteristics of the fabricated GaAs QW-FET with $L_G = 2 \mu\text{m}$.

3.4 Measurement suite and strain configurations

Two separate measurement suites were developed to characterize QW-FETs and Hall bars under stress. Automation of these measurement suites was achieved through an Agilent VEE program and a 4155B semiconductor parameter analyzer.

For QW-FETs, the transfer characteristics were measured at a drain-to-source voltage, $|V_{DS}|$ of 50 mV, which is low enough to avoid heating effects and significant parasitic ohmic drops. We chose to study the strain dependence of threshold voltage (V_T) as a proxy for the electrostatics, and linear-regime drain current (I_{Dlin}) or the intrinsic transconductance (g_{mi}) as proxy for transport. V_T was extracted at a constant drain current ($I_D = 1$ mA/mm for n-channel device and $I_D = -0.05$ mA/mm for p-channel devices) near the sub-threshold regime where I_D changes exponentially with V_{GS} . I_{Dlin} was extracted at a constant gate overdrive ($V_{GS} - V_T$) for each structure. The intrinsic transconductance was determined following the method in [59], which requires the knowledge of extrinsic transconductance, output conductance and source/drain resistances. The output conductance was obtained from the output characteristics measurements. The source/drain resistances were extracted using the gate-current-injection method [60].

The measurement suites were verified to be benign to the devices, so that the measurements themselves do not change the device characteristics. This was established by monitoring both V_T and I_{Dlin} for 50 measurements with a 1-min interval between two sequential measurements. The variation in V_T is < 0.5 mV and in I_{Dlin} is $< 0.5\%$. This verification is critical because the measurements were conducted at each stress level and therefore were repeated for many times for each device under test. Also, the changes induced by strain were at times rather small.

For ungated Hall bars, Hall measurements were conducted with a 5-terminal contact configuration. The geometry of a Hall bar is shown in Figure 3-8. The two end terminals (5 and 6) were used for current injection. Three out of four side terminals (1 to 4) were used for voltage measurements. The redundant side terminal can be used as a backup in the wire-bonding process. At each stress level, measurements with current injected from 5 and 6, and magnetic field pointing up and down were conducted in sequence (four measurements in total). The results of these measurements were averaged to eliminate variations due to any inhomogeneity of the fabricated Hall bars. This averaging technique is commonly adapted in Hall measurements[61]. The typical current level is $< 10^{-3}$ mA/mm. No self-heating effect is expected in these measurements.

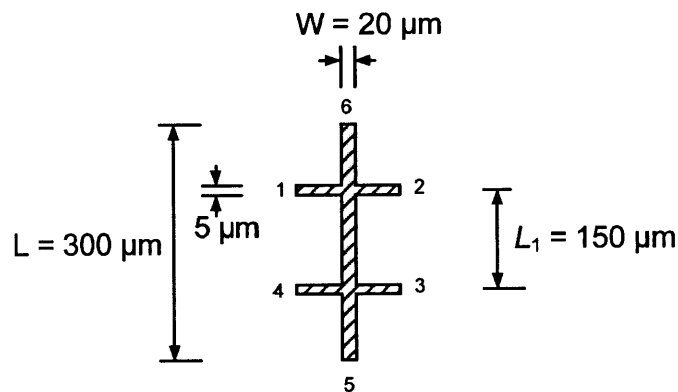


Figure 3-8. Geometry of a typical Hall bar used in this study. Terminals 5 and 6 are used for current injection. Three terminals out of terminals 1 to 4 are used for voltage monitoring.

The two types of measurements on QW-FETs and Hall bars have their own advantages. QW-FETs characterization provides straight-forward measurements on strain effects on figures of merits relevant to FET operation. In a complementary way, Hall bar measurements offer a means to separate carrier mobility and carrier concentration. These Hall measurements are used to obtain insights that C-V measurements can also provide.

C-V measurement is a desirable and commonly-used method to extract gate capacitance (C_G) and carrier concentration (n_s or p_s) in MOSFETs. However, in our Schottky-gate QW-FETs, the gate leakage current is substantial and prevents performing accurate C-V measurements. One uncertainty in comparing the mobility measured by Hall effects and C-V measurements is the Hall scattering factor (r_H). [35] This factor is the ratio of the Hall mobility to drift mobility. The value of r_H is of the order of unity. While assuming $r_H = 1$ in III-Vs usually does not lead to serious error, r_H can differ from 1. [62] For example, r_H for holes in GaAs was measured to be 0.93 ± 0.12 . [63]

The directions of the applied stress and the devices require some elaboration. In our experiments, if available, we characterized devices with transport direction oriented along the two cleaving crystallographic directions on the (100) surface ([110] and [-110]). For these types of devices, measurements were carried out with uniaxial stress applied along the same two directions. This is mainly due to the fact that in zincblende III-V crystals, the two $\langle 110 \rangle$ crystalline directions are known to be asymmetric as discussed in Chapter 2. This is unlike the diamond-type Si or Ge crystals. Figure 3-9 defines the directions of QW-FETs, Hall bars and stress. In this work, the stress is named with two subscripts: the first one indicates the relative direction between stress and device current flow (parallel or perpendicular), and the second one indicates the absolute crystallographic direction of the stress ([110] or [-110]). The color convention of Figure 3-9 (blue for stress parallel to transport direction, red for perpendicular) is also used throughout this thesis when graphing experimental data.

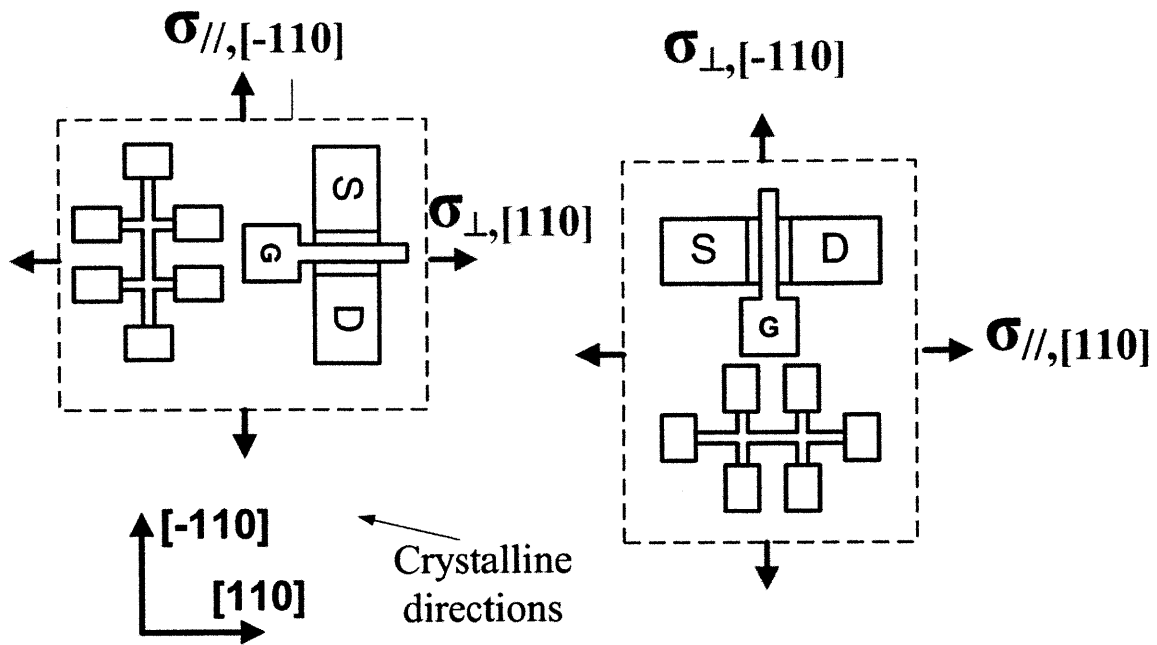


Figure 3-9. Schematic illustration of directions of test structures and applied stress and notation used for stress. The wafer crystallographic directions are indicated on the bottom left. The wafer surface is (100).

3.5 Summary

This chapter describes the experimental setup constructed to study uniaxial strain effects on III-V quantum well devices, as well as the epitaxial and device structures we used in this study. Our mechanical setup is able to introduce uniaxial strain up to 0.3% in III-V chips. With our suites of electrical measurement, repeatable characterization of QW-FETs and Hall bars can be performed as a function of applied stress. The experimental results are discussed in the next chapter.

Chapter 4 Results and analysis of chip-bending experiments

4.1 Introduction

This chapter presents results of chip-bending experiments on devices made from the four heterostructures introduced in Chapter 3. First, The study on n-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ QW-FET is introduced, with the emphasis on impact of strain on the electrostatics of QW-FETs. Second, the results from p-channel GaAs QW-FETs and Hall bars are discussed including a detailed comparison between results from these two types of structures. After this, results on biaxially-strained channel based on $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.49}\text{Ga}_{0.51}\text{Sb}$ are discussed. At the end of this chapter, performance enhancements in p-channel III-V materials through substrate-bending experiments are compared.

4.2 N-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ QW-FET

The device structure was introduced in Chapter 3. Figure 4-1 shows an example of the change in subthreshold characteristics of this device with different level of applied uniaxial stress along the [-110] direction. Significant shift of the device characteristics was observed. As discussed in Chapter 3, for these devices, we use threshold voltage (V_T , defined at $I_D = 1 \text{ mA/mm}$) and intrinsic transconductance (g_{mi}) as the proxies to map the role of uniaxial strain on electrostatic and transport, respectively.

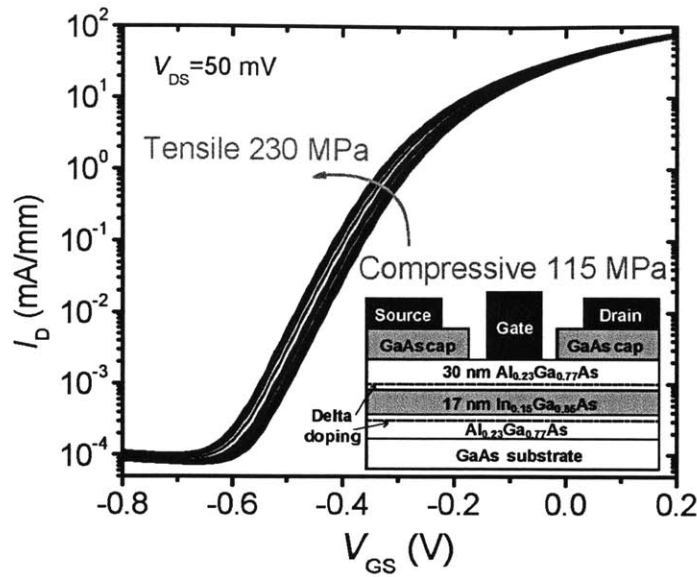


Figure 4-1. Measured subthreshold characteristics of devices as a function of [-110] stress. A cross section of the device is shown in the inset.

Figure 4-2 summarizes the change of threshold voltage (ΔV_T) under both [-110] and [110] stress. The stress along the two different $\langle 110 \rangle$ directions reverses the sign of ΔV_T . This is the unique signature of the piezoelectric effect, as discussed in Chapter 2. From Equations (2.10) and (2.11), it can be seen that alternating uniaxial stress from [-110] to [110] directions reverses the direction of polarization field (P_z) and consequently the sign of ΔV_T . This ΔV_T sign reversal predicted by Equations (2.10) and (2.11) is consistent with the data in Figure 4-2.

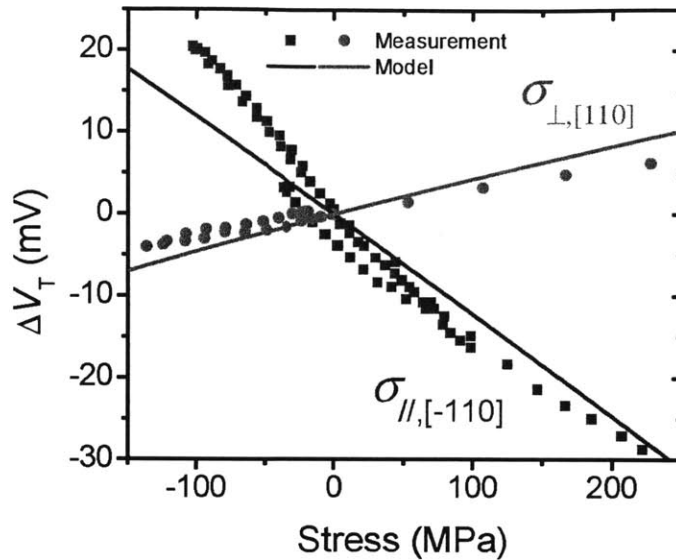


Figure 4-2. Change of V_T as a function of $\langle 110 \rangle$ strain. Data are well explained by the model (solid lines) that includes the piezoelectric effect and Schottky barrier height change. The channel is along $[-110]$.

Equations (2.10) and (2.11) also predict that the absolute value of ΔV_T should be the same for the two $\langle 110 \rangle$ directions. However, Figure 4-2 shows that $|\Delta V_T|$ under $[-110]$ stress is nearly 3x larger than that under $[110]$ stress. This suggests that there is another mechanism in action here.

Previously, an asymmetric directional dependence was observed in both GaAs metal semiconductor field effect transistors (MESFET) [44] and InP HEMTs [64], but this was not fully understood. Asbeck [44] suspected that in GaAs MESFETs subjected to dielectric passivation stress, this asymmetrical dependence originated in the spatial distribution of piezoelectric charge under the gate. In the study of hydrogen-induced piezoelectric effect in InGaAs/InP HEMTs, Blanchard [64] speculated that proton penetration into the semiconductor caused a solid shift of ΔV_T observed for $[110]$, $[-110]$ and $[010]$ directions. However, no clear evidence was further reported of these

hypotheses in these two studies.

We postulate that the asymmetric directional dependence of ΔV_T that we observe arises from a strain-induced change in the Schottky barrier height (ϕ_B), as discussed in Chapter 2. Figure 4-3 shows $\Delta\phi_B$ extracted using a thermionic-emission model for the I-V characteristics of the gate-source diode. Strain changes ϕ_B without any directional dependence. This is consistent with the discussion of Chapter 2. In fact, we extracted the hydrostatic deformation potential (a_c) from our measurements for $\text{Al}_{0.23}\text{Ga}_{0.77}\text{As}$. The value of a_c is -11.6 eV, which is well within the reported range in the literature (-5.0 to -15.4 eV) [65]. Since $\Delta\phi_B$ directly adds to ΔV_T , this non-directional change superimposes on the directional change due to the piezoelectric effect leading to the overall ΔV_T pattern shown in Figure 4-2.

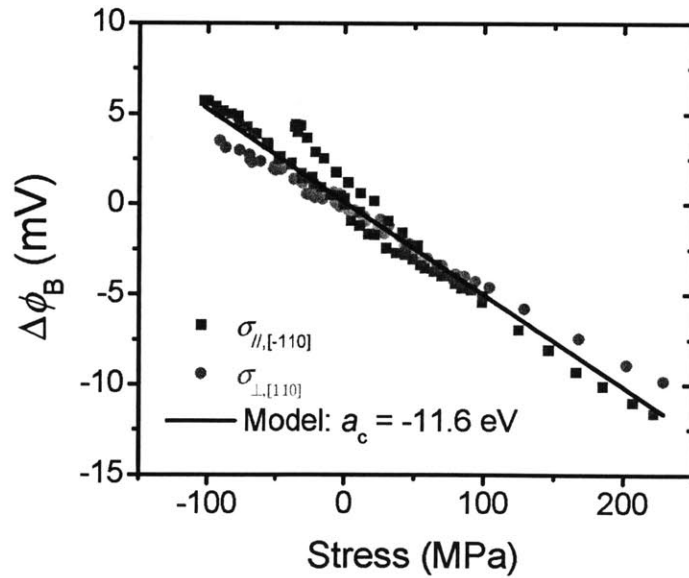


Figure 4-3. Change of Schottky barrier height as a function of uniaxial strain parallel and perpendicular to the channel direction [110]. The slope of a linear fitting (solid line) to the data determines the deformation potential (a_c).

By incorporating the piezoelectric and $\Delta\phi_B$ effects into a 1D Schrödinger-Poisson (SP)

simulator, the 2 dimensional electron gas (2DEG) charge concentration (n_s) as a function of gate voltage can be calculated. Extracting V_T as the gate voltage when n_s equals to 10^{11} cm^{-2} , we found that the experimental data can be well explained by the simulation results (dashed lines in Figure 4-2). The piezoelectric constants used in the simulation were $e_{14}(\text{GaAs}) = -0.16$ C/m^2 , $e_{14}(\text{InAs}) = -0.044$ C/m^2 , $e_{14}(\text{AlAs}) = -0.29$ C/m^2 . A brief discussion for these coefficients can be found in Section 2.3 of Chapter 2.

To investigate the impact of strain on transport, we extracted the linear regime intrinsic transconductance (g_{mi}) as a function of applied uniaxial strain. g_{mi} was obtained from extrinsic transconductance by removing the impact of parasitic source and drain resistance. Care needs to be exercised when doing this because these parasitic resistances are also affected by strain. To the first order, a well-extracted linear regime g_{mi} is independent on V_{GS} which we verified, if mobility or gate capacitance do not change with V_{GS} . Thus, the effect of strain-induced V_T change can be appropriately separated. Furthermore, we extracted g_{mi} at a certain gate overdrive ($V_{\text{GS}} - V_T = 0.4$ V) to fully offset the effect of gate-field-induced QW profile change as discussed in Chapter 2, even though this effect is minor. Figure 4-4 shows the extracted g_{mi} for both [110] and [-110] strain. Sign reversal and asymmetric Δg_{mi} pattern are seen for the two $\langle 110 \rangle$ strain directions.

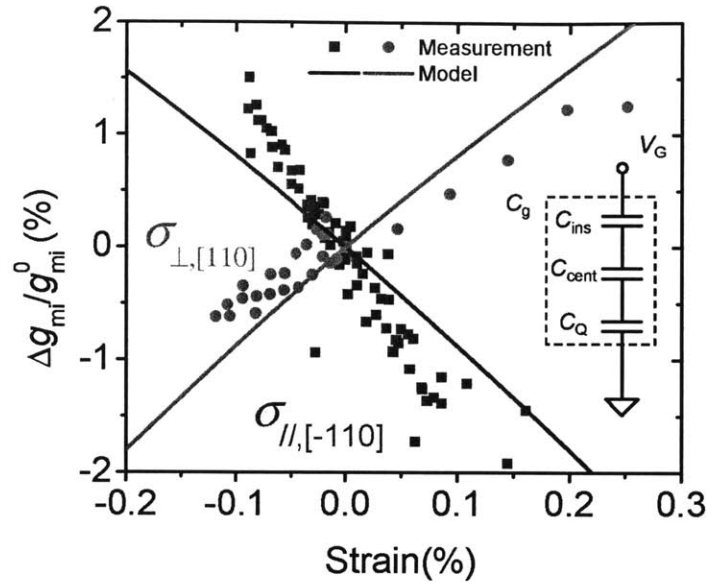


Figure 4-4. Relative change of intrinsic transconductance of n-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ HEMT under $\langle 110 \rangle$ stress. Simulation results that account for the piezoelectric effect and changes in ΔE_c and quantization are shown by the solid lines. The inset shows the equivalent-circuit model for overall gate capacitance. Channel direction is $[-110]$.

Theoretically, the change of g_{mi} consists of a combination of change in gate capacitance (C_G) and electron mobility (μ_e). The model for C_G (Figure 4-4 inset) has been introduced in Section 2.3 of Chapter 2. SP simulations of this $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ QW-FET reveal that C_{cent} is changed significantly by uniaxial strain in a manner that again suggests a dominant role for the piezoelectric effect. This can be explained through the modifications that the strain-induced polarization field imposes on the QW profile. In essence, the centroid of 2DEG moves either closer to or farther from the gate, depending on the direction of the polarization field. In a relatively thick channel, this movement can be significant. In addition, a non-directional component of ΔC_{cent} arises from the change in band discontinuity (ΔE_c) at the barrier-channel interface and its impact on sub-band quantization. The SP simulation shows that the $\Delta C_{cent}/C_{cent}$ can be as high as -14% with 0.4% strain. The $\Delta C_Q/C_Q$ due to effective mass change [66] is estimated to be in the order

of -3.5% with 0.4% strain. The capacitance of C_{ins} is set by the barrier thickness. Considering that C_{Q} is around 2x larger than C_{cent} in our HEMT, the change of C_{g} is dominated by the change in C_{cent} . SP simulation results of the overall $\Delta C_{\text{g}}/C_{\text{g}}$ with polarization field incorporated is shown by the continuous lines in Figure 4-4. In the SP model, the gate capacitance is determined by the differential increase of n_{s} over V_{G} at $V_{\text{G}} - V_{\text{T}} = 0.4$ V. Interestingly, the impact of uniaxial strain on C_{G} nearly fully accounts for all the observed change in g_{mi} .

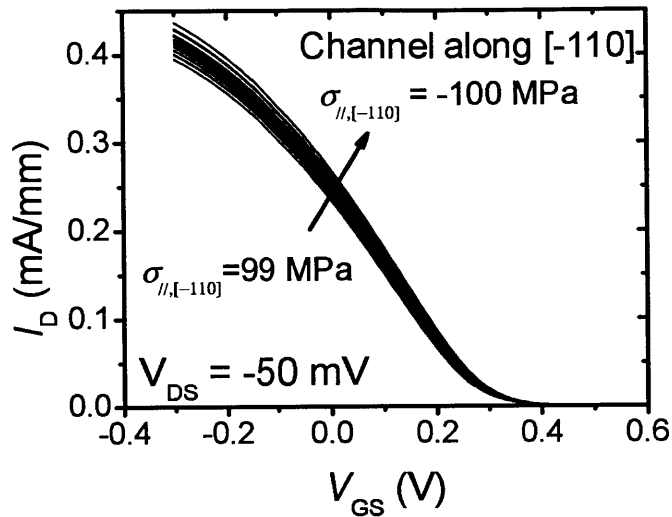
The agreement between model and experiments obtained in Figure 4-4 suggests that strain does not affect μ_{e} significantly in these devices. Theoretically, μ_{e} should increase with tensile strain and decrease with compressive strain due to conduction band warping [66]. This is precisely contrary to what is observed in our experiments in the non-directional component of Δg_{mi} which decreases for tensile strain. Consistent with our experimental results, the reported experimental Hall mobility change for electrons in GaAs due to strain is not significant, the value is in the $\pm 1\%$ range for strain up to -0.4%. [67] Thus, we conclude that the observed Δg_{mi} in our experiments is dominated by the change in C_{cent} .

4.3 P-channel GaAs quantum well

The device structure for the QW-FETs in this section has been introduced in Chapter 3. Figure 4-5 shows a representative example of the shift of the linear regime transfer characteristics of a p-channel GaAs QW-FET under uniaxial stress. In this particular example, the stress is along [-110] and parallel to the channel direction. Linear regime drain current (I_{Dlin}) measured with $V_{\text{DS}} = 50$ mV and $V_{\text{GS}} = -0.3$ V increased 10.4% as σ_{\parallel} ,

$[-110]$ changes from tensile 99 MPa to compressive 100 MPa. The threshold voltage, V_T , is also seen to be affected by the applied strain.

(a)



(b)

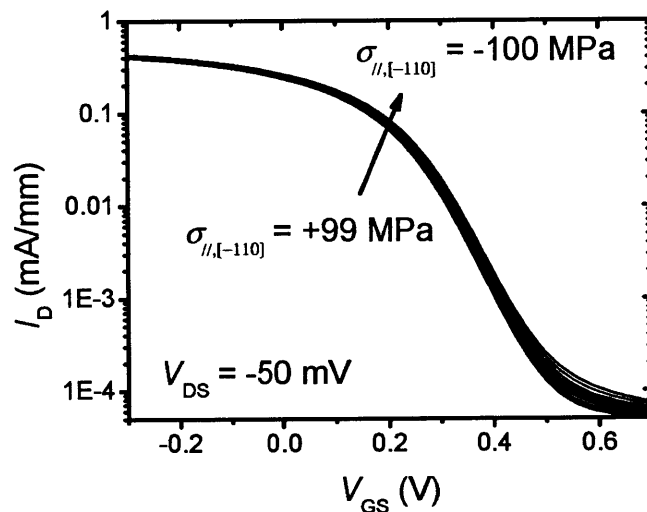


Figure 4-5. Transfer characteristics in linear scale (a) and semi-logarithmic scale (b) of a GaAs QW-FET as a function of $[-110]$ uniaxial stress. Both channel and stress are aligned with the $[-110]$ crystalline direction in this example.

Extracting the hole mobility change from the change in I_{Dlin} is not straightforward. In

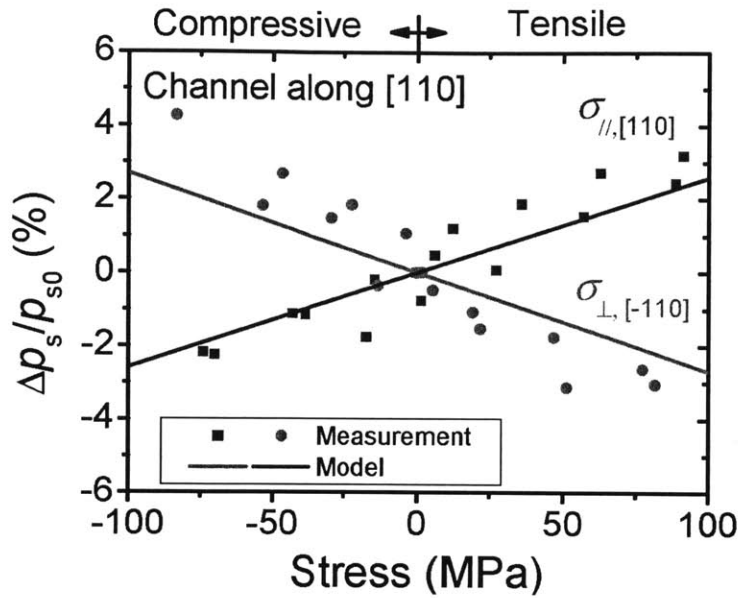
Section 4.2, we showed that $\langle 110 \rangle$ uniaxial stress changes the 2D electron concentration in a n-channel III-V QW-FET through the piezoelectric effect by shifting the threshold voltage (V_T) and the gate capacitance (C_G). Similarly, ΔI_{Dlin} in the present devices likely consists of not only a change in μ_h , but also a change in the 2DHG concentration p_s .

In this study on the GaAs heterostructure, Hall bars were fabricated and were used to separate the changes in μ_h and p_s by Hall measurements. Figure 4-6 summarizes the measured relative change of p_s with $\langle 110 \rangle$ uniaxial stress (symbols). Here we found that Δp_s depends almost solely on the absolute alignment between stress and crystallographic direction. The directions of transport in the Hall bar have little effect on Δp_s , as observed if we compare Figure 4-6 (a) and (b). This behavior of Δp_s suggests that, similar to the situation in Section 4.2, the piezoelectric effect dominates the change in p_s .

Δp_s can be predicted by 1D SP simulations with piezoelectric effect, as shown by the solid lines in Figure 4-6. The piezoelectric coefficients used in the simulations are $e_{14}(\text{GaAs}) = -0.16 \text{ C/cm}^2$, $e_{14}(\text{InAs}) = -0.044 \text{ C/m}^2$ and $e_{14}(\text{AlAs}) = -0.25 \text{ C/cm}^2$. The value of e_{14} for $\text{Al}_{0.42}\text{Ga}_{0.58}\text{As}$ was linearly interpolated from $e_{14}(\text{GaAs})$ and $e_{14}(\text{AlAs})$.

The impact of stress on μ_h measured from Hall measurements is shown in Figure 4-7. $\Delta \mu_h$ also changes with stress in an anisotropic way. However, unlike for Δp_s , the direction of the Hall bar determines the sign of $\Delta \mu_h$. In particular, μ_h increases with compressive $\sigma_{//}$ and tensile σ_{\perp} , whereas it decreases with tensile $\sigma_{//}$ and compressive σ_{\perp} . This suggests that this effect is due to the impact of stress on the valence band dispersion relation and therefore hole transport. Similar effects have been widely observed in Si and Ge [68].

(a)



(b)

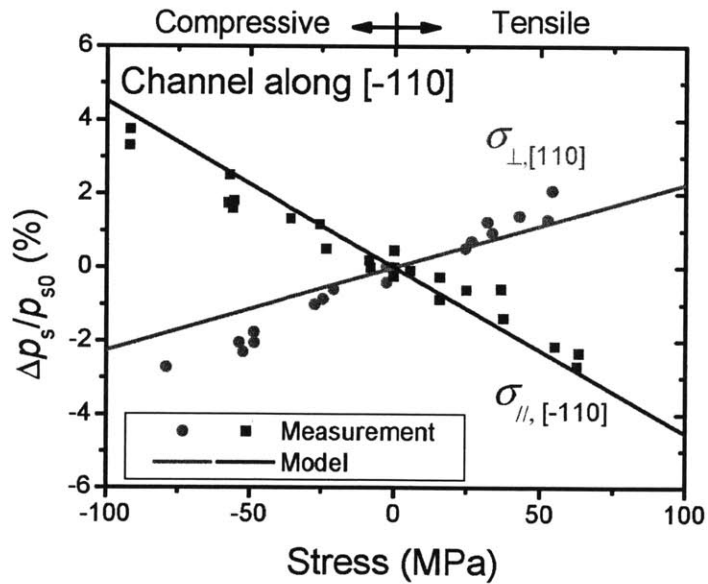
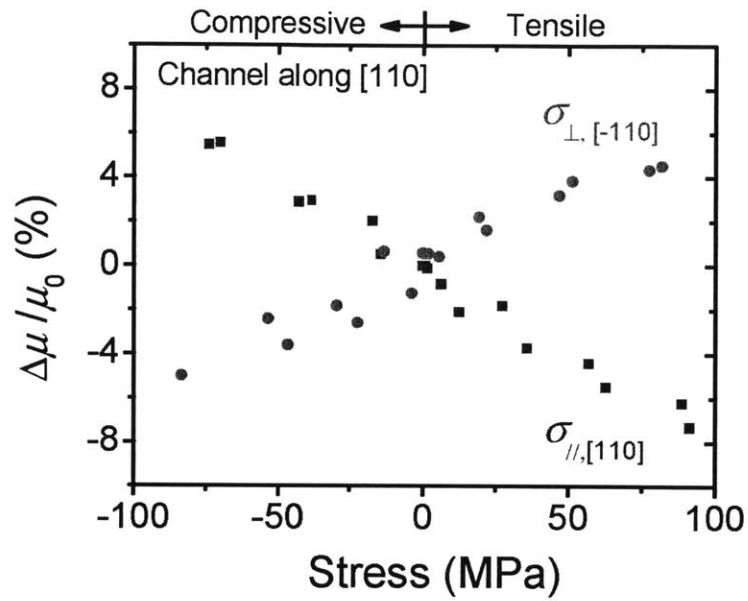


Figure 4-6. Normalized change of sheet hole concentration (p_s) as a function of $\langle 110 \rangle$ stress (symbols). Results from ungated Hall bars along $[110]$ and $[-110]$ are shown in (a) and (b) respectively. The solid lines are Δp_s predicted by Schrodinger-Poisson simulations.

(a)



(b)

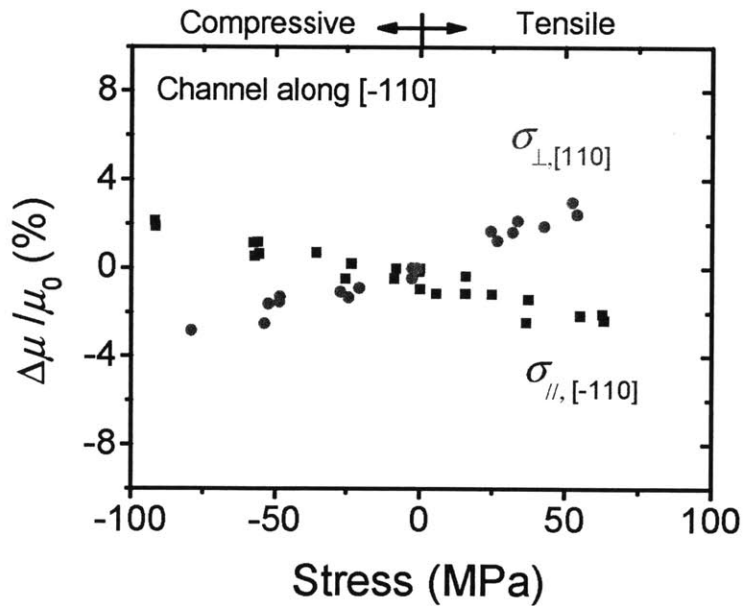


Figure 4-7. Normalized change of hole mobility as a function of $\langle 110 \rangle$ stress. Results from Hall bars along [110] and [-110] are shown in (a) and (b) respectively.

In addition to the valence band change, the change in p_s that was noted above may also be affecting μ_h . As we can see in Figure 4-7, the slopes of $\Delta\mu_h$ versus stress with the same

relative stress directions (e.g. $\sigma_{//[110]}$ and $\sigma_{//[-110]}$) are quite different, i.e. the crystalline directions affect the sensitivity of μ_h to uniaxial stress. This effect is likely due to the dependence of μ_h on p_s . As discussed in [9-10], an increase/decrease of p_s can lead to a decrease/increase in μ_h . This has also been seen in separate experiments by other authors [69]. A change in p_s enhances the sensitivity of μ_h to stress ($//$ or \perp) when the channel is along [110], whereas it weakens the sensitivity when the channel is aligned to [-110]. This is the reason why the apparent sensitivities of μ_h to either $\sigma_{//}$ or σ_{\perp} are different when the channel is aligned to the different crystalline directions.

To extract the dependence of μ_h on applied stress excluding the change of μ_h due to Δp_s , we note that:

$$d\mu = \left. \frac{\partial \mu}{\partial \sigma} \right|_{p_s} d\sigma + \left. \frac{\partial \mu}{\partial p_s} \right|_{\sigma} dp_s = \left. \frac{\partial \mu}{\partial \sigma} \right|_{p_s} d\sigma + \left. \frac{\partial \mu}{\partial p_s} \right|_{\sigma} \frac{dp_s}{d\sigma} d\sigma \quad (4.1)$$

Therefore:

$$\frac{d\mu}{d\sigma} = \left. \frac{\partial \mu}{\partial \sigma} \right|_{p_s} + \left. \frac{\partial \mu}{\partial p_s} \right|_{\sigma} \frac{dp_s}{d\sigma} \quad (4.2)$$

Following the expected power-law dependence of μ on p_s in [16], let us assume that:

$$\mu_{//} \propto p_s^{\alpha_{//}} \quad (4.3)$$

$$\mu_{\perp} \propto p_s^{\alpha_{\perp}} \quad (4.4)$$

As the change of p_s in our experiments is very small, employing constant power indices, α , is appropriate. Assuming two α constants for parallel and perpendicular

directions respectively means that the dependence of μ_h on p_s is determined by the relation ($//$ or \perp) between the directions of μ_h and stress σ , but is insensitive to the crystalline direction of σ ($[110]$ or $[-110]$). The underlying physics is that the responses of valence band dispersion are asymmetric to $\sigma_{//}$ and σ_{\perp} , but this asymmetry is not affected by the crystalline direction of stress. This assumption has been verified by $k.p$ simulations of valence band dispersion in the studied quantum well with the piezoelectric effect included. Values of α between 0 and -1, depending on hole concentration, are commonly seen at room temperature. [16, 70]

Traditionally, piezoresistance coefficient (π) in bulk semiconductors has been used to represent the relative change of resistivity with respect to applied stress [71]:

$$\pi = \frac{\Delta\rho}{\rho} \frac{1}{\sigma} \quad (4.5)$$

where ρ is resistivity. In studies of strain effects on FETs, π was extracted from the change of mobility in FETs with respect to applied stress under constant carrier density [39, 72]:

$$\pi = -\left. \frac{\partial\mu}{\partial\sigma} \right|_{p_s} \cdot \frac{1}{\mu_0} \quad (4.6)$$

Following this definition, and by inserting Eq. (4.3), (4.4) and (4.6) into (4.2), we can obtain a set of four equations for stress with various combinations of relative and crystalline directions:

$$\frac{d \ln \mu_{[110]}}{d \sigma_{//[110]}} = -\pi_{//} + \alpha_{//} \cdot \frac{d \ln p_s}{d \sigma_{//[110]}} \quad (4.7)$$

$$\frac{d \ln \mu_{[-110]}}{d \sigma_{//[110]}} = -\pi_{//} + \alpha_{//} \cdot \frac{d \ln p_s}{d \sigma_{//[110]}} \quad (4.8)$$

$$\frac{d \ln \mu_{[-110]}}{d \sigma_{\perp,[110]}} = -\pi_{\perp} + \alpha_{\perp} \cdot \frac{d \ln p_s}{d \sigma_{\perp,[110]}} \quad (4.9)$$

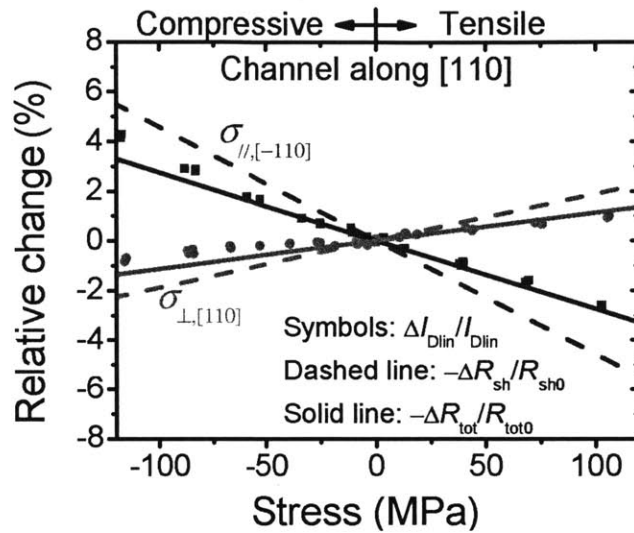
$$\frac{d \ln \mu_{[110]}}{d \sigma_{\perp,[-110]}} = -\pi_{\perp} + \alpha_{\perp} \cdot \frac{d \ln p_s}{d \sigma_{\perp,[-110]}} \quad (4.10)$$

The values of $d \ln p_s / d \sigma$ and $d \ln \mu / d \sigma$ can be obtained from Figure 4-6 and Figure 4-7, respectively. Therefore, solving Eqs. (4.7) and (4.8) yields $\pi_{//}$ and $\alpha_{//}$, while π_{\perp} and α_{\perp} can be obtained from Eq. (4.9) and (4.10). Following this procedure, we obtain the piezoresistance coefficients $\pi_{//} = 54 \text{ cm}^2/\text{dyn}$ and $\pi_{\perp} = -50 \text{ cm}^2/\text{dyn}$. $\alpha_{//}$ and α_{\perp} are extracted to be -0.7 and -0.2.

Interestingly, the Δp_s and $\Delta \mu_h$ measured from Hall measurements are consistent with the changes observed in QW-FET characteristics. We chose the normalized change of I_{Dlin} at $V_{GS} = 0 \text{ V}$ ($\Delta I_{Dlin} / I_{Dlin}$) and ΔV_T extracted at $I_D = -0.05 \text{ mA/mm}$ as the two figures of merit of QW-FETs. Figure 4-8 summarizes measured $\Delta I_{Dlin} / I_{Dlin}$ in two orthogonal GaAs QW-FETs as a result of uniaxial stress application (symbols). $\Delta I_{Dlin} / I_{Dlin}$ essentially reflects the change of the total resistance of the FETs ($\Delta R_{tot} / R_{tot0}$). Similar to the case in [73], $R_{tot0} = R_{sh0} \cdot L_G / W_G + R_p$, where R_p is a fixed parasitic resistance. Considering both the change in sheet resistance ($\Delta R_{sh} / R_{sh0}$) measured from the ungated Hall bars and R_p obtained by transmission line method (TLM), we found that $\Delta I_{D0} / I_{D0}$ follows well the expected $-\Delta R_{tot} / R_{tot0}$ of the FETs. This is also shown in Figure 4-8: the dotted lines show

the measured relative change in R_{sh} ; and the dashed lines show $-\Delta R_{tot}/R_{tot0}$ which includes the effect of the fixed parasitic resistance.

(a)



(b)

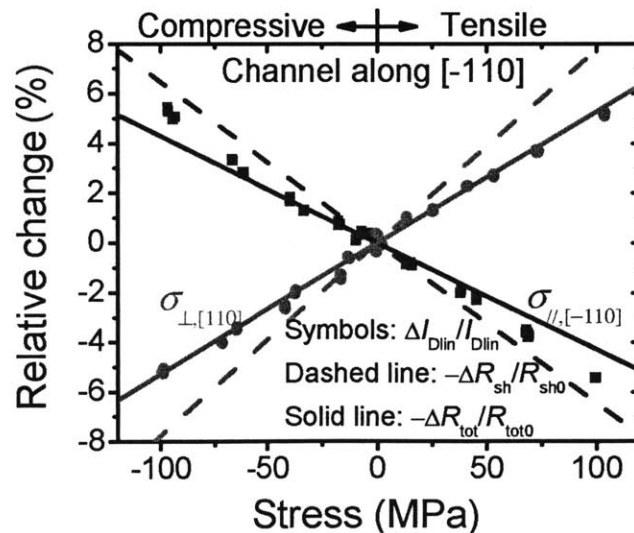


Figure 4-8. Normalized change in linear regime drain current of FETs (symbols) as a function of applied $\langle 110 \rangle$ uniaxial stress. The channel direction is along [110] in (a) and [-110] in (b). The dashed lines are the relative change in sheet resistance ($-\Delta R_{sh}/R_{sh0}$) measured in ungated Hall bars. The solid lines are estimations of $-\Delta R_{tot}/R_{tot0}$ that include both fixed parasitic resistances and $-\Delta R_{sh}/R_{sh0}$. Good agreement between the solid lines and symbols were found.

We also extracted the V_T in the GaAs QW-FETs, as shown in Figure 4-9. The anisotropic pattern of ΔV_T again suggests the possible presence of piezoelectric effect, similar to the scenario in n-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ HEMT in Section 4.2. On top of the piezoelectric effect, we postulate that the change in μ_h observed in Figure 4-7 also impacts ΔV_T . [73]

Since we extract V_T at a constant current in the subthreshold regime, anything that affects the subthreshold current (I_{Dsub}) can propagate into an apparent change in V_T . Theoretically, carrier transport in the subthreshold regime of an FET follows a diffusion process [74]. Therefore, I_{Dsub} depends on μ_h through the Einstein relation and the difference in p_s at the source and drain edges of the gate. Approximately, p_s depends linearly on the effective 2D density of states (DOS), and exponentially on V_{GS} . [75] Therefore, for $V_{GS}-V_T \gg kT/q$,

$$I_{Dsub} \propto \mu_h \exp\left(\frac{-q(V_{GS} - V_T)}{nkT}\right), \quad (4.11)$$

where n is the ideality factor, k is Boltzmann constant, T is temperature, and V_T is the threshold voltage which, from a theoretical point of view, we define as the condition in which the Fermi level lines up with the top of the 1st subband in the channel.

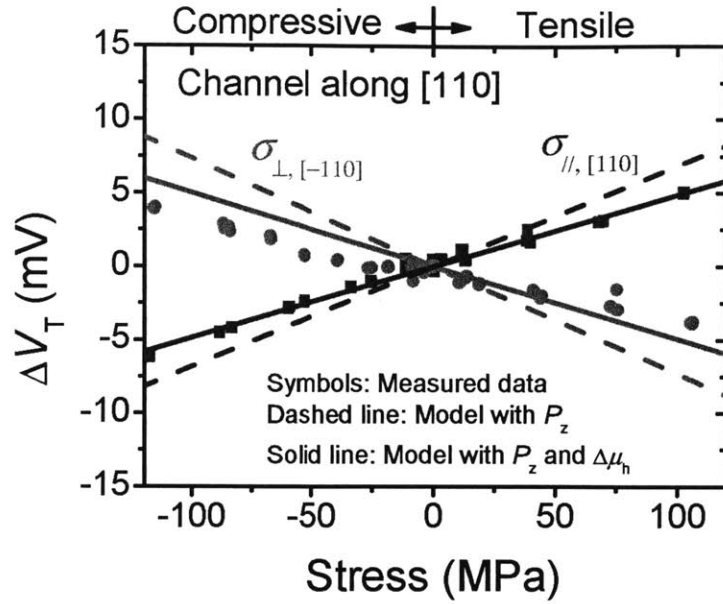
This model suggests that I_{Dsub} is linearly proportional to μ_h . The proportionality constant in Eq. (4.11) contains the 2D DOS. 8×8 $k \cdot p$ simulations suggest that changes to the DOS due to strain are negligible for our level of stress and only lead to $|\Delta V_T| < 0.5$ mV. The parameters used in these simulations are according to [52]. In consequence, the change in apparent V_T measured at constant subthreshold current (ΔV_T^{app}) is indeed a shift of V_{GS} in the following way:

$$\Delta V_T^{app} = \Delta V_T^{elec} + \frac{nkT}{q} \ln\left(1 + \frac{\Delta\mu_h}{\mu_h}\right) \quad (4.12).$$

where ΔV_T^{elec} , as the shift of V_{GS} for a constant p_s (10^{11} cm^{-2}) was extracted from the same set of 1D Schrodinger-Poisson simulations that generated the $\Delta p_s/p_{s0}$ values in Figure 4-6. We calculated the 2nd term on the right hand side of Eq. (4.12), using $\Delta\mu_h/\mu_h$ from the Hall measurement data in Figure 4-7. The ideality factor, n , was extracted from the subthreshold slope at $V_{GS} = V_T$ in the measured transfer characteristics.

Changes measured in QW-FET V_T can be well explained by considering the piezoelectric effect and the impact of $\Delta\mu_h$ in Eq. (4.12). The overall ΔV_T^{app} (dashed lines) agree well with the measured ΔV_T in QW-FET with applied $\langle 110 \rangle$ stress (symbols), as shown in Figure 4-9. The excellent agreement among measurements in FETs and Hall bars as well as simulations gives great credibility to our extraction methodology and our identification of the relevant physics.

(a)



(b)

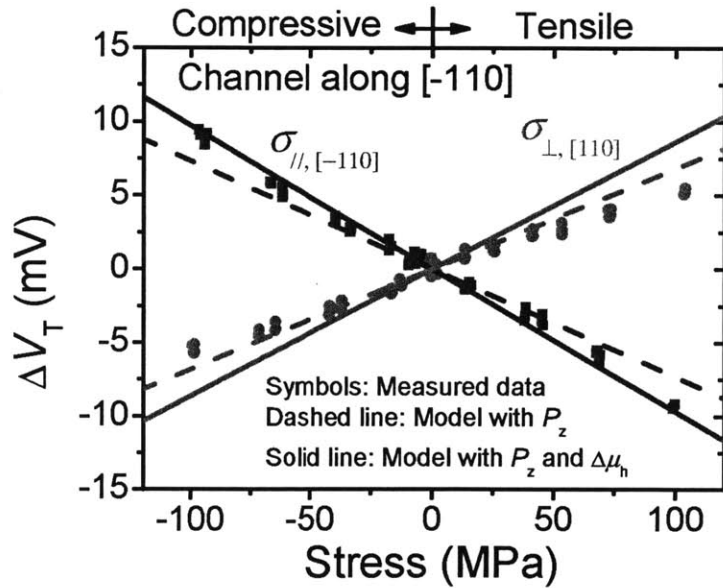


Figure 4-9. Change of threshold voltage as a function of stress. Results from QW-FET (symbols) with channel along [110] and [-110] are shown in (a) and (b) respectively. The dashed lines are ΔV_T predicted by SP simulations considering electrostatic change in the quantum well as a result of applied stress. The solid lines are ΔV_T predicted by Eq. (4.12) that includes ΔV_T due to both electrostatic and mobility change induced by stress.

4.4 P-channel In_{0.24}Ga_{0.76}As quantum well

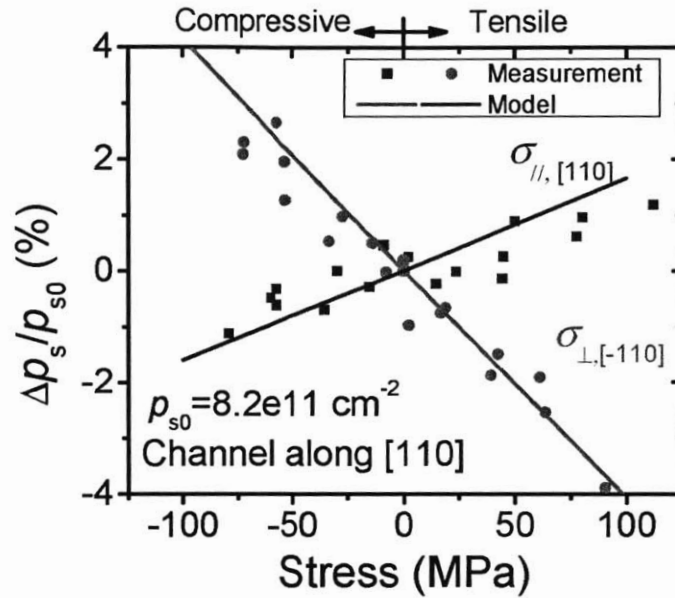
Chip-bending experiments were carried out on ungated Hall bars based on the In_{0.24}Ga_{0.76}As quantum well introduced in Chapter 3. The as-fabricated ungated Hall bars shows $p_{s0} = 8.2 \times 10^{11} \text{ cm}^{-2}$ and $\mu_{h0} = 265 \text{ cm}^2/\text{V.s}$ for [110] orientation and $p_{s0} = 7.8 \times 10^{11} \text{ cm}^{-2}$ and $\mu_{h0} = 293 \text{ cm}^2/\text{V.s}$ for [-110] orientation.

Figure 4-10 shows the change of sheet hole concentration (Δp_s) measured as a function of applied $\langle 110 \rangle$ uniaxial stress. The orientation dependence of the measured Δp_s is similar to what we found in the GaAs quantum well. This suggests again the dominant role of the piezoelectric effect. When adding Schottky barrier height change due to strain, good agreement with experiments is predicted by SP simulations (solid lines in Figure 4-10).

Figure 4-11 shows μ_h change due to applied $\langle 110 \rangle$ stress in the In_{0.24}Ga_{0.76}As quantum well. The anisotropic orientation dependence of μ_h on $\langle 110 \rangle$ stress is again similar to the results in Section 4.3 for the GaAs quantum well. The signs of the sensitivities of $\Delta \mu_h$ to stress are identical for every configuration of stress and Hall bar orientations, if we compare the GaAs (Figure 4-7) and In_{0.24}Ga_{0.76}As (Figure 4-11) quantum well data. However, the magnitudes of these sensitivities are different. $|\Delta \mu / \sigma_{//}|$ increased 3 times along [-110], while decreased 40% along [110]. $|\Delta \mu / \sigma_{\perp}|$ increased 20% along [-110] and 26% along [110]. These differences are partly due to the substantially different valence band structure in the GaAs and In_{0.24}Ga_{0.76}As quantum wells. The valence band structure in the later one is substantially affected by the -1.7% biaxial lattice mismatch strain, as

shown in Chapter 2. Therefore, it is not surprising that the quantitative sensitivities of $\Delta\mu_h$ to applied stress differ significantly in the two quantum well structures.

(a)



(b)

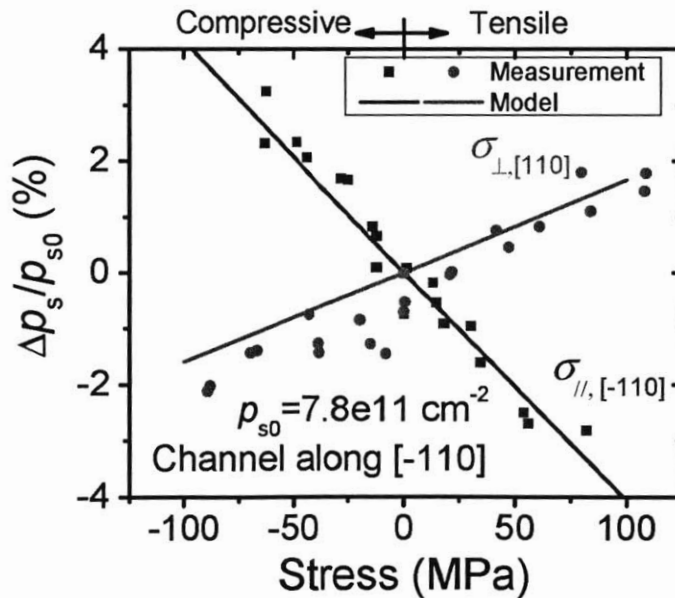
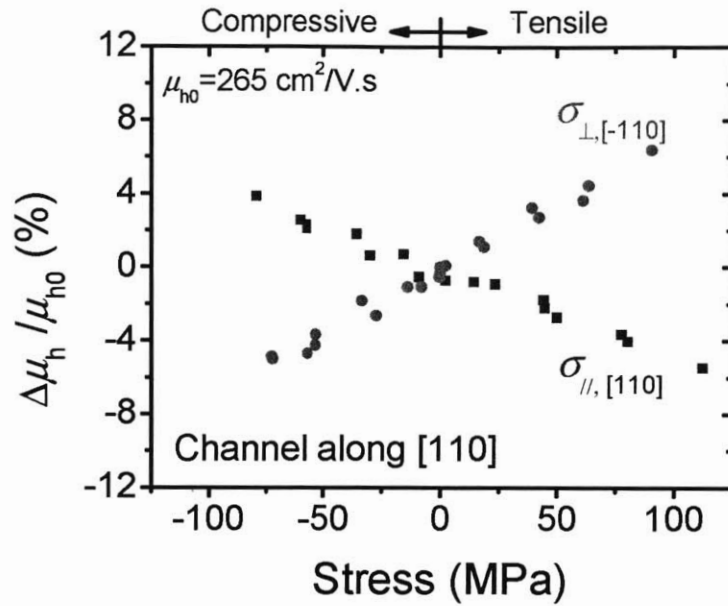


Figure 4-10. Sheet hole concentration change with $\langle 110 \rangle$ uniaxial stress in (a) [110] and (b) [-110] Hall bars of the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ heterostructure. Solid lines are SP simulation results for this $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well.

(a)



(b)

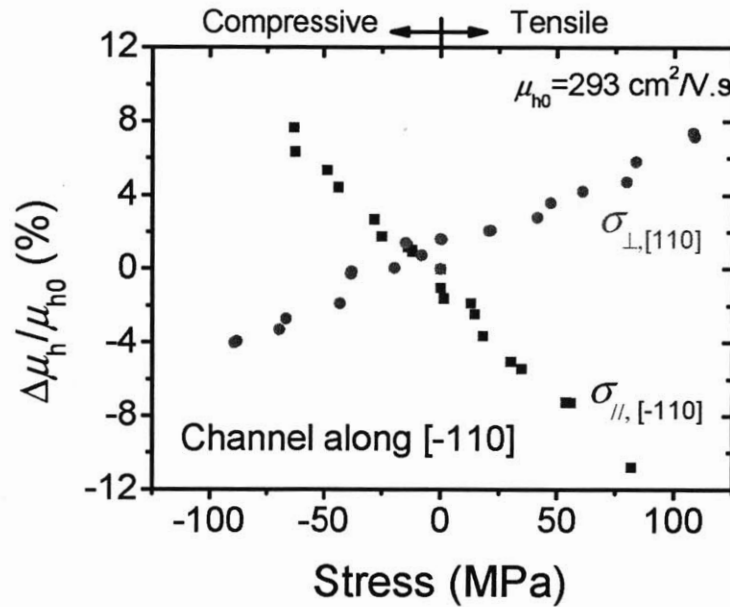


Figure 4-11. Hole mobility change with $\langle 110 \rangle$ uniaxial stress in (a) [110] and (b) [-110] Hall bars of the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ heterostructure.

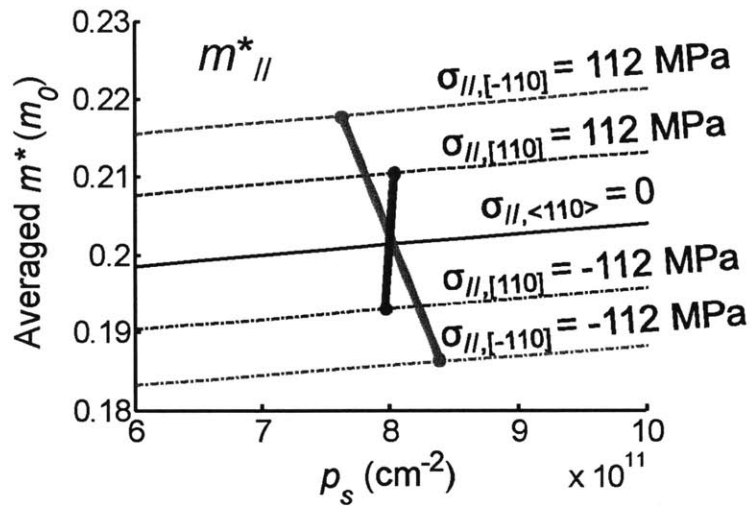
One unforeseen point worth noting is the effect from Δp_s on the $\Delta\mu_h$ sensitivities. When we follow the same procedure to separate the effect of Δp_s on $\Delta\mu_h$ using Eq. (4.7) to (4.10)

and extract $\pi_{//}$ and π_{\perp} of the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well, we obtained a positive α for the data with stress parallel to channel ($\sigma_{//}$). Contrary to our expectations, the positive α seemingly means that $\mu_{h//}$ increases with p_s . However, this phenomenon is very unlikely in our quantum well with p_s close to 10^{12} cm^{-2} at room temperature. Zhang [70] calculated the room-temperature hole mobility of $\text{In}_x\text{Ga}_{1-x}\text{As}$ considering nonpolar acoustic/optical phonon scattering, surface roughness scattering, remote phonon scattering, longitudinal optical phonon scattering, and alloy scattering. The calculation clearly shows a decreasing trend of μ_h with p_s . A possible explanation for our experimental observation is that the effect of Δp_s on $\Delta\mu_h$ persists as in the GaAs quantum well case (μ_h decreases with increasing p_s); but other mechanisms induce an asymmetric responses of μ_h to $\sigma_{//, [-110]}$ and $\sigma_{//, [110]}$ and overwhelm the Δp_s effect. Therefore, unlike the GaAs quantum well, the effect of Δp_s on $\Delta\mu_h$ in this can not explain the difference between $\Delta\mu_h/\sigma$ along the two $\langle 110 \rangle$ directions in this $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well.

A mechanism that might explain this could be the change in the valence band dispersion relation as a result of the change in quantization in the QW [76]. In our quantum well, band bending due to P_z changes the quantization and therefore the VB dispersion relation. Using the $k \cdot p$ method, we simulated the VB structure in our QW including the external uniaxial strain, built-in biaxial strain and P_z . We calculated the averaged transport effective mass (m^*), a key factor that impacts μ_h , by following the treatment of nonparabolic bands discussed in Section 2.2 of Chapter 2. The results are shown in Figure 4-12. The black solid lines show the m^* in the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well with no uniaxial strain applied. The colored dashed lines are showing the results with uniaxial strain applied along $[-110]$ and $[110]$ directions. In addition, two pairs of

thick solid lines in red and blue are used to connect the m^* values with p_s following the change observed in Hall measurements (Figure 4-10) due to piezoelectric effect. Each of the thick colored lines is used for stress along one of the $\langle 110 \rangle$ directions.

(a)



(b)

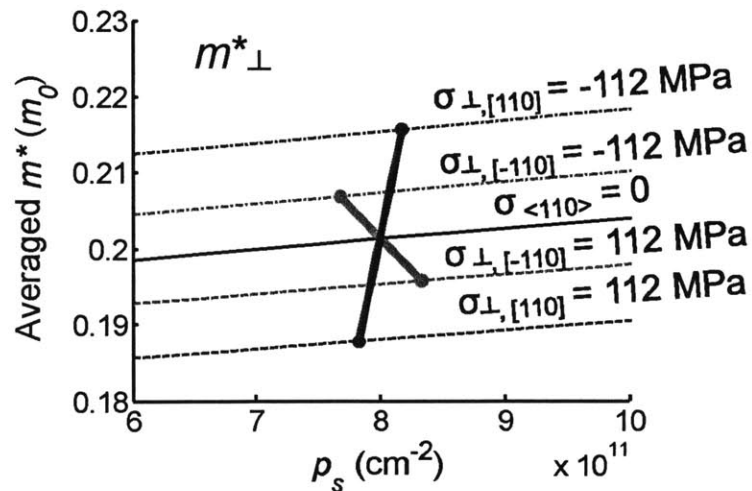


Figure 4-12. Change in averaged transport m^* parallel (a) and perpendicular (b) to applied $\langle 110 \rangle$ uniaxial stress as a function of p_s . m^* calculated as in Ch. 2. The thick solid lines in red (for $[-110]$) and blue (for $[110]$) represent the trajectory of Δm^* with stress expected in experiments. It combines both the change of p_s and the change in dispersion relation.

A pronounced difference between the effect of uniaxial strain along the two $\langle 110 \rangle$ directions can be seen in Figure 4-12, as shown by the bold red and blue solid lines. We found that this is due to the presence of the polarization field (P_z). In the absence of P_z , uniaxial strain along the two $\langle 110 \rangle$ directions changes m^* in the same way, as shown in Figure 2-9. Strain-induced P_z gives rise to additional changes in m^* . For example, P_z induced by $[110]$ compressive strain increases $m^*_{//}$, whereas P_z induced by $[-110]$ compressive strain reduces $m^*_{//}$. The P_z -induced Δm^* opposes or enhances the stress-induced Δm^* depending on the crystalline orientation of stress. In agreement with our data, the simulation predicts that $m^*_{//}$ is more sensitive to $\sigma_{[-110]}$ than to $\sigma_{[110]}$. (Figure 4-13).

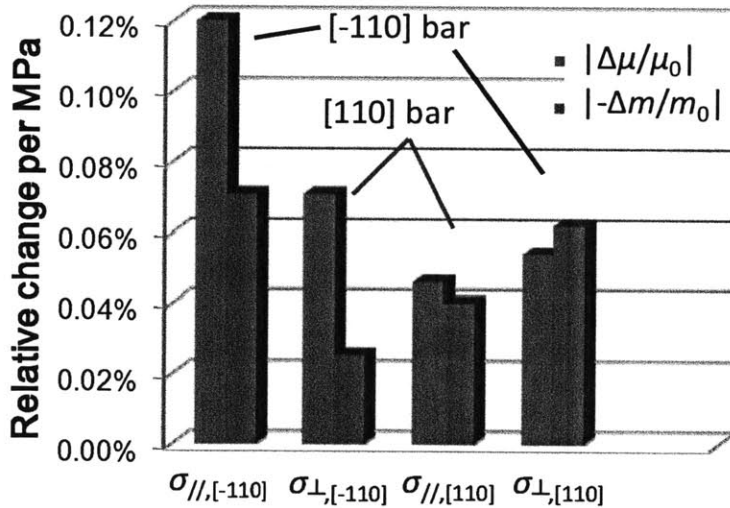


Figure 4-13. Comparison between experimental mobility changes and simulated effective mass changes with uniaxial stress.

Figure 4-13 shows the comparison between relative changes in μ_h measured in experiments and m^* calculated above. Here we assumed that the scattering time remains constant in the range of applied strain. Fischetti [16] and Wang [33] suggested that with

low range of strain applied, m^* change may account for a large portion (as high as 85%) of change in μ_h . The results in Figure 4-13 show that anisotropic changes in μ_h along the two $\langle 110 \rangle$ directions are expected.

Nevertheless, discrepancies exist in Figure 4-13 between the experiment and simulation of the piezoresistance coefficients. Possible sources of the discrepancies include neglecting scattering, as already mentioned, and other sources for structural anisotropy.

Harris [77] pointed out that the scattering time (τ) is anisotropic for polar optical phonon scattering, one of the most important scattering mechanisms for compound semiconductors at room temperature. The scattering time depends on not only the transport effective mass in longitudinal direction ($m^*_{//}$), but also the ratio of $m^*_{//}$ over the effective mass in the transverse direction (m^*_{\perp}). This anisotropy will probably give rise to different values of τ parallel and perpendicular to the direction of applied uniaxial stress in our quantum well, where the $m^*_{//}/m^*_{\perp}$ ratios for these two τ are different (exactly reciprocal and are different from unity). The underlying mechanism is due to valence band anisotropy as a result of the applied uniaxial stress, as discussed in Chapter 2.

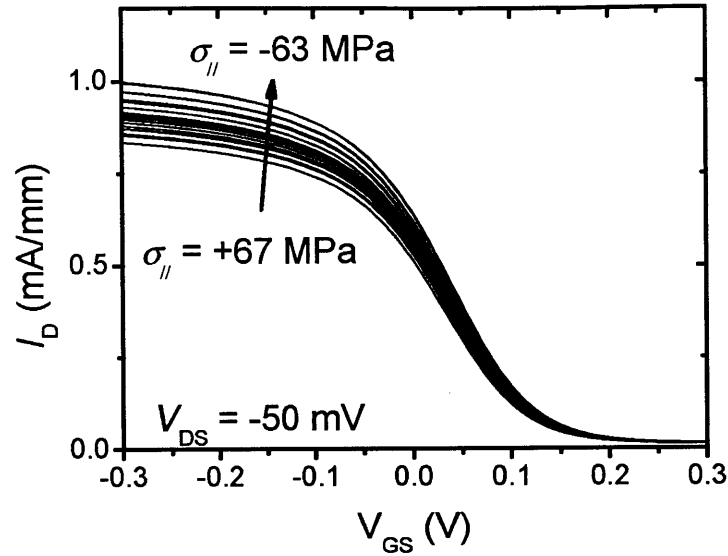
In addition to neglecting scattering time, anisotropic structural properties along the $\langle 110 \rangle$ directions have been reported for InGaAs quantum wells. Preferential strain relaxation along $[110]$ direction in $\text{In}_x\text{Ga}_{1-x}\text{As}$ has been observed in experiments. [78-80] In addition, indium composition in the quantum well plane can change in a periodic fashion along $[110]$. [81] These asymmetric strain field and/or composition anisotropy can result in asymmetric valence band structures along the two $\langle 110 \rangle$ directions in our quantum well. Therefore, the response of the valence band along those two $\langle 110 \rangle$ directions to uniaxial strain are likely to be different.

In short, it is not surprising that hole mobility enhancements differ under various configurations of stress and transport orientations. There exists a preferred crystal direction of stress for μ_h enhancement in this $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well: our experiments suggest this direction is $[-110]$ with $\pi_{//} = 1.2 \times 10^{-10} \text{ cm}^2/\text{dyn}$ and $\pi_{\perp} = 0.7 \times 10^{-10} \text{ cm}^2/\text{dyn}$. The $\pi_{//}$ coefficient may be even slightly underestimated due to p_s changing in a way that mitigates the μ_h enhancement.

4.5 P-channel $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ QW-FET

The transfer characteristics of this QW-FET were measured at low V_{DS} (-50 mV). A maximum of 0.08% strain parallel and perpendicular to the channel was sequentially applied to the same FET by rotating the chip by 90 degrees. The stress is calculated using an interpolated $\langle 110 \rangle$ Young's Modulus (78 GPa) for the $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ channel. Figure 4-14 shows a representative example of the change in the transfer characteristics of an InGaSb QW-FET with stress applied along the channel direction ($\sigma_{//}$). A significant increase in I_{Dlin} with compressive stress ($\sigma < 0$) was observed.

(a)



(b)

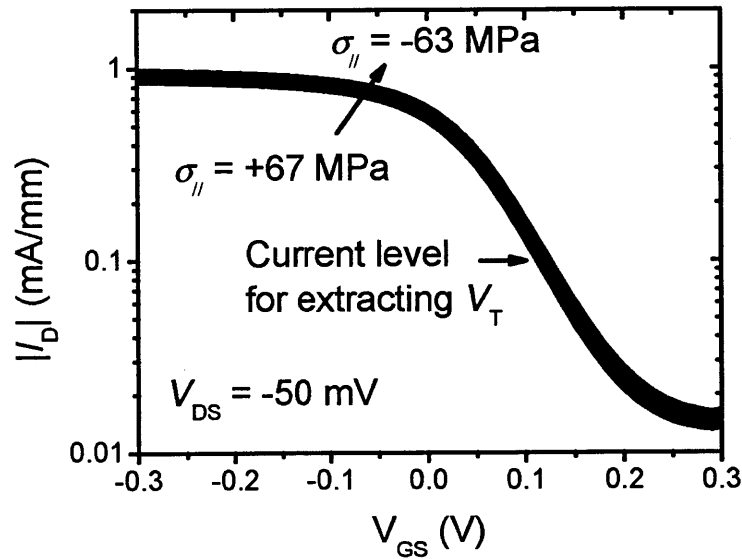


Figure 4-14. Measured transfer characteristics in linear scale (a) and semi-log scale (b) of the $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ QW-FET as $\sigma_{||}$ changes. The device channel is oriented along the $[110]$ direction.

We focused on the two figures of merit: linear-regime drain current (I_{Dlin} , extracted at $V_{\text{GS}} - V_{\text{T}} = -0.2$ V) and threshold voltage (V_{T} , extracted at $I_{\text{D}} = 0.1$ mA/mm).

Figure 4-15 summarizes the change of I_{Dlin} at $V_{\text{GS}} - V_{\text{T}} = -0.2$ V measured with both

stress parallel ($\sigma_{//}$) and perpendicular (σ_{\perp}) to the channel. Significant anisotropic effects are seen: the magnitude of ΔI_{Dlin} under $\sigma_{//}$ is $\sim 6\times$ higher than under σ_{\perp} ; the signs are also opposite for ΔI_{Dlin} with $\sigma_{//}$ and σ_{\perp} . For higher gate overdrive (-0.2 V to -0.4 V, the maximum in this study), the measured $\Delta I_{\text{Dlin}}/I_{\text{Dlin}}$ is found to be independent of V_{GS} and stays the same as the data shown in Figure 4-15. This is because at high gate overdrive, the intrinsic resistance (R_{int}) becomes small compared with that of the S/D regions (R_{ext}). Therefore, $\Delta I_{\text{Dlin}}/I_{\text{Dlin}}$ under high gate overdrive is dominated by $\Delta R_{\text{ext}}/R_{\text{ext}}$, and is independent of V_{GS} .

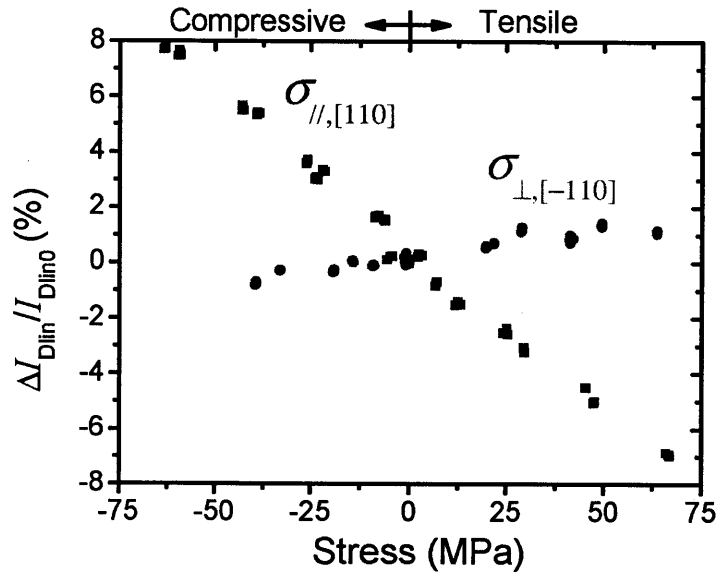


Figure 4-15. Relative change of linear-regime drain current at $V_{\text{GS}} - V_{\text{T}} = -0.2$ V as a function of $\langle 110 \rangle$ stress. The transport direction is along $[110]$.

As $\Delta I_{\text{Dlin}}/I_{\text{Dlin}}$ essentially reflects the change of the total resistance of the FETs ($\Delta R_{\text{tot}}/R_{\text{tot0}}$), we also need to isolate the impact from fixed parasitic resistance R_{p} . This is similar to the discussion in the GaAs QW-FET experiments. The total channel resistance of our FET can be written as $R_{\text{ch}} = 2R_{\text{c}} + 2R_{\text{ext}} + R_{\text{int}}$, where R_{c} is the contact resistance

between ohmic metal and the 2DHG underneath it, R_{ext} is the resistance of the ungated semiconductor portion between the gate and the S/D contact metals, and R_{int} is the resistance of the intrinsic region under the gate. $2R_c$ measured by the TLM method is ~ 4 $\Omega\cdot\text{mm}$. This is $<6\%$ of R_{total} (~ 68 $\Omega\cdot\text{mm}$) at the bias of the I_{Dlin} extraction. R_{ext} is considered to be governed by similar strain effects as to R_{int} , except for a fixed 2DHG concentration of 6.6×10^{11} cm^{-2} . Therefore, any impact from a fixed parasitic resistance arises only from $2R_c$, which can be safely neglected.

Similar to our previous studies on n- and p-channel InGaAs/GaAs QW-FETs, connecting the change in I_{Dlin} to a change of μ_h requires considering any possible change in p_s . On this particular chip, we do not have Hall bars that allow us to conduct experiments as we did for the GaAs QW. However, in the current InGaSb QW-FET, changes of p_s due to the piezoelectric effect are estimated to be negligible. Our 1D SP simulations show that Δp_s or ΔC_G due to the piezoelectric effect in this $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ structure is $25\times$ smaller than the observed ΔI_{Dlin} . The reason is the tight confinement of 2DHG by the extremely thin quantum well (7.5 nm) and the small piezoelectric constants of the materials involved [82]. Therefore, we can conclude that the observed ΔI_{Dlin} is dominated by changes in μ_h .

The piezoresistance coefficients ($\pi = -\Delta\mu/\mu\sigma$) of the $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ 2DHG parallel and perpendicular to $\langle 110 \rangle$ uniaxial stress can then be calculated from the data in Figure 4-15. They are found to be $\pi''_{\langle 110 \rangle} = 1.17 \times 10^{-10}$ cm^2/dyn and $\pi^{\perp}_{\langle 110 \rangle} = -1.9 \times 10^{-11}$ cm^2/dyn . Compared with $\pi''_{\langle 110 \rangle}$ for Si pMOS at a similar hole concentration (6.6×10^{11} cm^{-2}) [83-84], $\pi''_{\langle 110 \rangle}$ of the $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ 2DHG is $1.5\times$ higher. This value is also $1.4\times$ higher than the $\pi''_{\langle 110 \rangle}$ found in an $\text{In}_{0.35}\text{Ga}_{0.65}\text{Sb}$ MOSFET in [85]. Nevertheless, $\pi''_{\langle 110 \rangle}$ in [85] was

probably measured at higher p_s ($> 10^{12} \text{ cm}^{-2}$), which might decrease its value.

As suggested by Eq.(4.12), the measured change in V_T (Figure 4-16) should also reflect the change in μ_h . Under the conditions of the present study, we estimated that the impact of the piezoelectric effect and Schottky barrier height changes on ΔV_T^{elec} are $< 0.5 \text{ mV}$ and $< 0.6 \text{ mV}$, respectively. Therefore, we neglect the component of ΔV_T^{elec} and consider ΔV_T^{app} dominated by $\Delta\mu_h$. As shown in Figure 4-16, calculations of ΔV_T^{app} using the 2nd term on the right hand side of Eq. (4.12) broadly agree with our experiments. The solid lines show the projected ΔV_T^{app} as a result of $\Delta\mu_h$ extracted from ΔI_{Dlin} . The projected ΔV_T^{app} matches relatively well with the apparent ΔV_T extracted from the subthreshold regime. The residual gap in Figure 4-16 between the model and the data may be attributed to a larger $\Delta\mu_h/\Delta\sigma$ in the subthreshold regime than in the linear regime. This effect is akin to the observed decrease in the piezoresistance coefficients in p-type Si with increased carrier concentration [86].

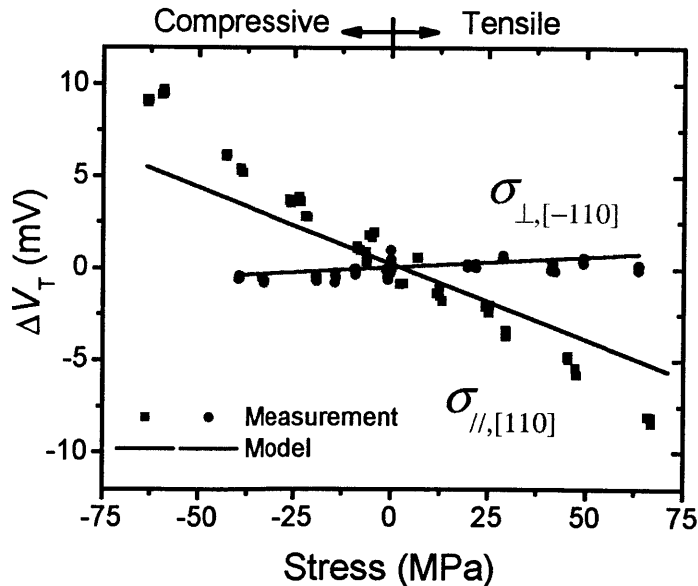


Figure 4-16. Change of measured or apparent threshold voltage as a function of $\langle 110 \rangle$ stress. The solid lines represent ΔV_T^{app} projected from $\Delta\mu_h$ according to Eq. (4.12).

The anisotropic behavior of the piezoresistance coefficients of $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ qualitatively agrees with the trend seen in Si [27]. This is partly due to the anisotropic response of the valence band to $\langle 110 \rangle$ uniaxial strain as seen in our $k \cdot p$ simulations in Chapter 2. More sophisticated calculations [16] are needed to theoretically quantify the change in hole mobility. A final remark is that the piezoresistance coefficients are measured for $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ channel with 2.1% compressive biaxial strain and quantum confinement. These coefficients could be different under other built-in biaxial strain or confinement conditions.

4.6 Piezoresistance coefficients comparison

Figure 4-17 compares the piezoresistance coefficients determined experimentally in p-channel FETs with various channel materials including Si [28, 83], Ge [39], and strained Ge [32]. The fact that piezoresistance coefficients of III-V materials are comparable to or even larger than the Si channel value suggests that uniaxial strain is also a feasible path to enhance p-channel QW-FET performance for logic applications. In addition, we observed high $\langle 110 \rangle$ piezoresistance coefficients in various biaxially strained materials. This suggests that biaxial lattice-mismatch strain may fundamentally enhance the sensitivity of hole mobility to additive uniaxial strain. To understand this phenomenon, we believe that comprehensive simulations considering impact of uniaxial strain on both valence band dispersion as well as carrier scattering are necessary. This is discussed in more detail in Section 2.2.5.

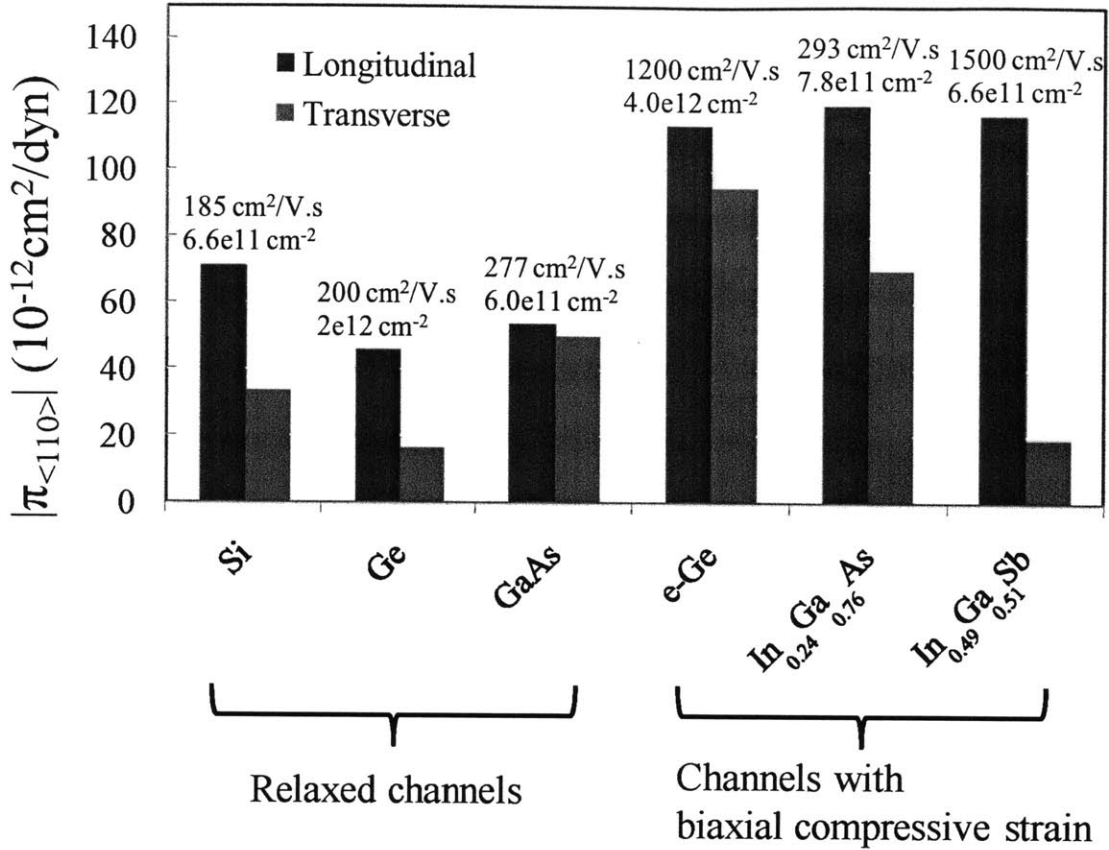


Figure 4-17. Comparison between p-type piezoresistance coefficients in inversion layers or 2DHG of various materials measured from substrate-bending experiments. In all situations, the sign of longitudinal coefficients (π_{\parallel} , shown by left columns) is positive, whereas the sign of transverse coefficients (π_{\perp} , shown by right columns) is negative. The as-fabricated hole mobility and the hole concentration at which the mobility was extracted are labeled above corresponding columns. The strained Ge (e-Ge), $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$, and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ channels have -2.4%, -1.7% and -2.1% biaxial compressive strain, respectively. The values for Si, Ge and e-Ge are from [28, 32, 39, 83]. The values for GaAs, $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ are from this work.

4.7 Summary

This chapter presents experimental results of the impact of $\langle 110 \rangle$ uniaxial stress on various QW-FET structures. In the n-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ HEMT, $\langle 110 \rangle$ uniaxial stress affects the electrostatics through a combination of piezoelectric effect, Schottky barrier

height change, and quantum well profile change. These effects are much more significant than any impact of strain on electron mobility. These electrostatic changes were found to also happen in p-channel QW-FETs. As a consequence, hole concentration can change at the same time with hole mobility as a result of applied stress. This is clearly seen through our Hall measurements on GaAs and $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum wells. Through an in-depth analysis, we isolated the hole concentration changes and determined the piezoresistance coefficients that reflect the sensitivity of the hole mobility change with respect to $\langle 110 \rangle$ stress. These coefficients for GaAs, $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ 2DHG were reported for the first time. Compared with coefficients in Si and Ge pMOS, the piezoresistance coefficients of these III-V channel 2DHGs suggest that uniaxial strain engineering is expected to benefit p-channel III-V QW-FET significantly. In addition, we observed increased and high piezoresistance coefficients in biaxially-strained channels. A fundamental mechanism related to strain effects on valence band dispersion and hole scattering time may exist. Understanding this will require a more sophisticated modeling than what we did in Chapter 2.

Chapter 5 Performance enhancement in InGaAs pFET by process-induced uniaxial strain

5.1 Introduction

Our results in Chapter 4 suggest that by combining uniaxial strain and biaxial strain, μ_h in InGaAs inversion layers can be significantly enhanced, even more effectively than in Si. To fully explore the potential of this new concept for improving the performance of p-channel InGaAs FETs, we pursue the fabrication of devices through a process that incorporates uniaxial strain on a heterostructure in which, as grown, the channel is under biaxial strain. This chapter presents simulations for determining an effective approach for strain introduction, as well as results and analysis on QW-FETs fabricated following the strain-introduction scheme.

5.2 Mechanical simulations and target structure

Initially, we considered a few options for introducing uniaxial strain to the channel of $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ QW-FETs. These options were conceived in a way such that modifications to our established QW-FET processes are as simple as possible. Through 3D mechanical simulations, we also considered the possibility of introducing large-scale strain as well as preliminary gate-length scalability. These considerations will be discussed in this section.

5.2.1 Gate-metal-induced stress

The first option was to use gate-metal-induced stress for channel strain. The target structure is sketched in Figure 5-1. A tensile-stressed gate metal film induces compressive stress in the area underneath it including the channel. This enhances hole mobility in the channel.

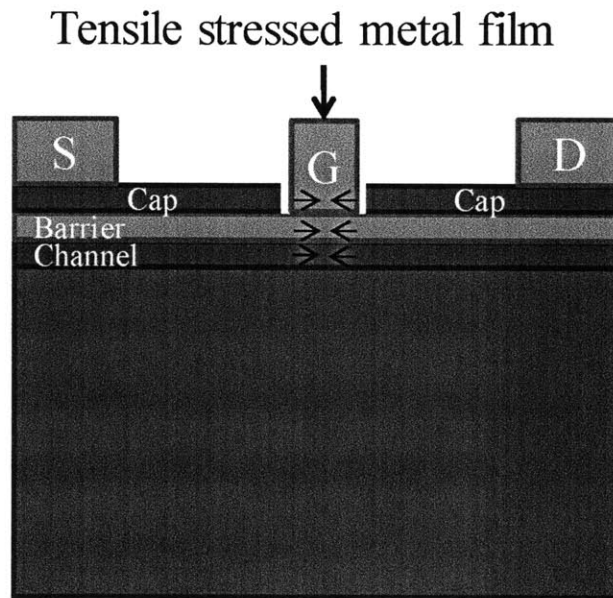


Figure 5-1. The schematic of gate-induced stress method. The arrays of arrows indicate the direction of strain relaxation in the stressed gate and the direction of deformation in the heterostructure.

A possible implementation of a tensile-stressed gate is by incorporating silicide in the gate metal. Specifically, silicides can be created with internal stress of over 1 GPa. [87] The major source of the stress is thermal expansion mismatch between the silicide and proximate layers. At the annealing temperature above the forming temperature of the silicide film, the film becomes lattice-matched to the substrate. As the film cools down from the annealing temperature, the difference between the thermal expansions of the substrate and the film causes stress in the film. [87]

Thermal mismatch is also expected between GaAs and certain silicides (e.g. PtSi). The coefficients of thermal expansion (CTE) at room temperature of GaAs and PtSi are 5.6×10^{-6} (K^{-1}) [88] and 14×10^{-6} (K^{-1}) [89], respectively. The stress in the film at room temperature is $\sigma = (\text{CTE}_{\text{film}} - \text{CTE}_{\text{substrate}}) \cdot (T_{\text{annealing}} - T_{\text{room}}) \cdot E$, where E is the Young's Modulus of the film. As a result, a tensile stress is expected in the silicide film as the film cools down from the annealing temperature, given that $\text{CTE}_{\text{film}} > \text{CTE}_{\text{substrate}}$. The forming temperature for PtSi can be as low as 194 °C [90]. The annealing temperature for our QW-FETs can be above 400 °C, as long as it does not degrade the ohmic contacts or the epitaxial layers. With this annealing temperature, a practical stress as large as 500 MPa can be induced in the PtSi films on GaAs substrate. The final stress under the gate is proportional to this stress and the PtSi thickness.

This process using silicide in the gate stack may only require 2 new materials and a thermal step after metal deposition in addition to the conventional QW-FET process shown in Chapter 3. Furthermore, a variety of metal silicides are conductive, so that the gate electrode should also remain conductive. Therefore, this process appears straightforward to implement.

Figure 5-2 shows 3D simulation results of stress distribution in the gate area for a structure with a tensile-stressed metal film on a GaAs substrate. In this simulation, we used the material properties of PtSi for the gate. The internal stress of the silicide was set to tensile 2 GPa. This value was set to the same value as we chose in the next stress scheme, for a direct comparison between the two schemes. The thickness of the gate (H_G) was 200 nm. The gate length was set to 2 μm . Clearly, compressive stress (blue) was

introduced into the area underneath the gate film. The compressive stress can be as high as -350 MPa in the example in Figure 5-2.

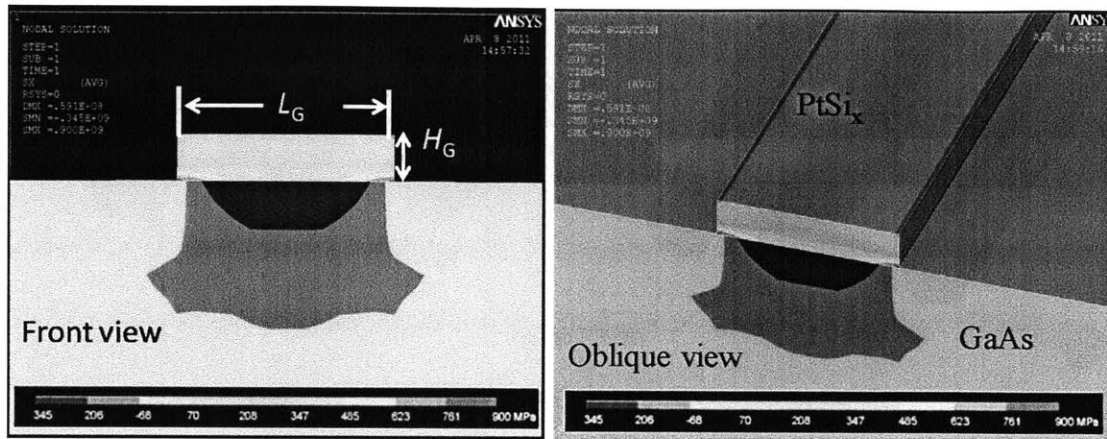


Figure 5-2. Stress distribution in a structure with tensile-stressed PtSi_x on GaAs substrate. The color bar is coded with blue as the compressive extreme and red as the tensile extreme.

Figure 5-3 shows both the longitudinal and transverse stress distribution extracted along a line across the center of the gate region (Figure 5-3 left). It can also be seen in Figure 5-3 that two tensile stress peaks are near the gate edges. These peaks are not favorable for access resistances because they are expected to decrease the mobility of 2DHG in the access region and therefore increase the local resistance. In Figure 5-3, the transverse stress is also compressive but of marginal value. However, the magnitude of the transverse stress depends rather on the gate width, which in this example is wide ($50 \mu\text{m}$). In case the gate width narrows, the transverse stress will increase, as the center of the gate is closer to the edge of the gate metal in the width direction.

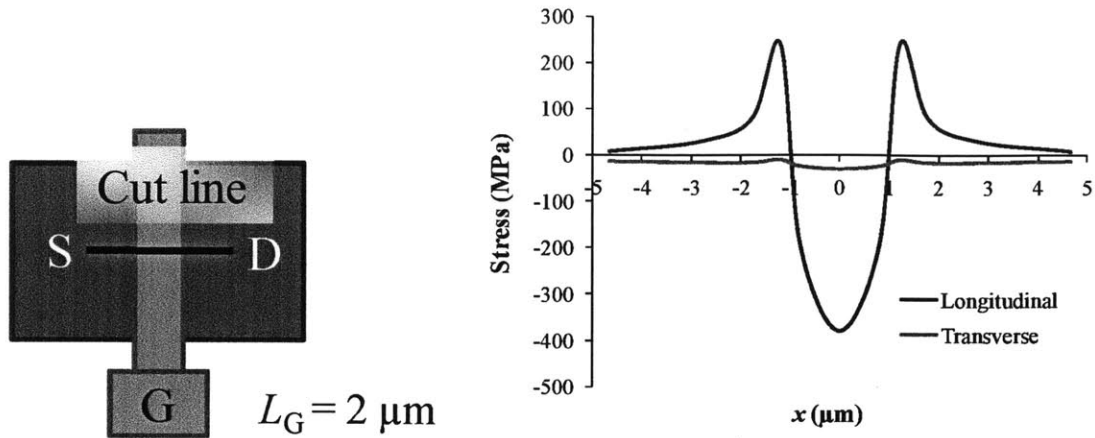


Figure 5-3. Stress distribution along a line underneath the gate. The position to take the distribution is shown on the left. Longitudinal and transverse stress distributions are shown on the right. The thickness of the gate film is 200 nm. The gate internal stress was set to 2 GPa.

We have also investigated the gate-length (L_G) dependence of the stress introduced to the channel. Figure 5-4 shows the center stress dependence on the gate length. We found that this option using gate-induced stress is not suitable for scaled QW-FETs. By varying L_G from 20 μm to 125 nm, we obtained the dependence of the peak compressive stress (the maximum compressive stress in Figure 5-3 right) in the channel as a function of L_G . This is shown in Figure 5-4. The longitudinal stress, which is the most effective in enhancing hole mobility, peaks with L_G around 1 μm , but then decreases quickly as L_G scales down. While the L_G at which the stress peaks probably depends on the gate film thickness as well as the mechanical properties of the film and the substrate, the trend of stress evolution with L_G is expected to be general. Hence, this approach utilizing gate-induced-stress is of little interest for our study.

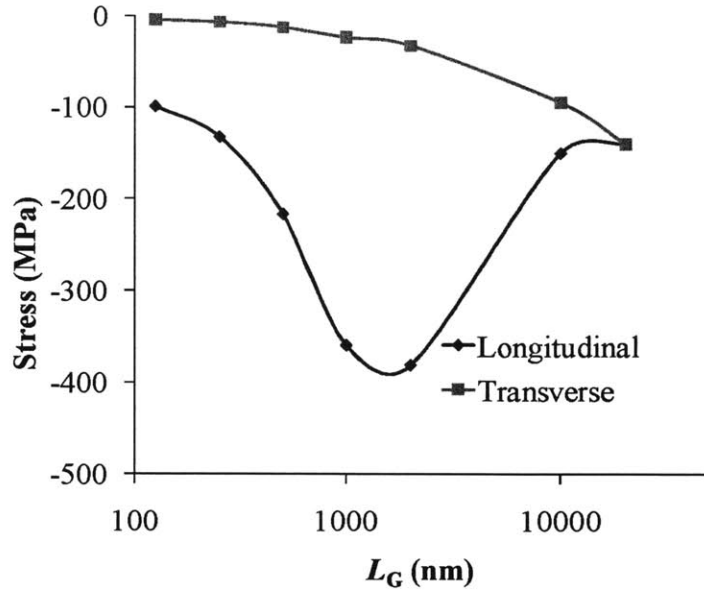


Figure 5-4. Gate-length dependence of the peak stress in the channel with tensile-stressed gate film.

5.2.2 Dielectric-overlay-induced stress

The second option is to use dielectric overlay stress. A possible structure is shown in Figure 5-5. In this design, a compressively stressed dielectric is deposited on top of the gate area. After an opening of the dielectric is cut using the gate lithography pattern, the stress near the edge of the dielectric compresses the region under the gate, as the dielectric tends to expand. The edge stress of a dielectric pattern has been extensively studied in Si technology [91]. Also, a variety of dielectric films with compressive stress can be selected depending on process availability. The highest compressive stress reported reaches 11 GPa in diamond-like carbon films [92]. Examples of using these carbon films in QW-FET structures have been reported [93].

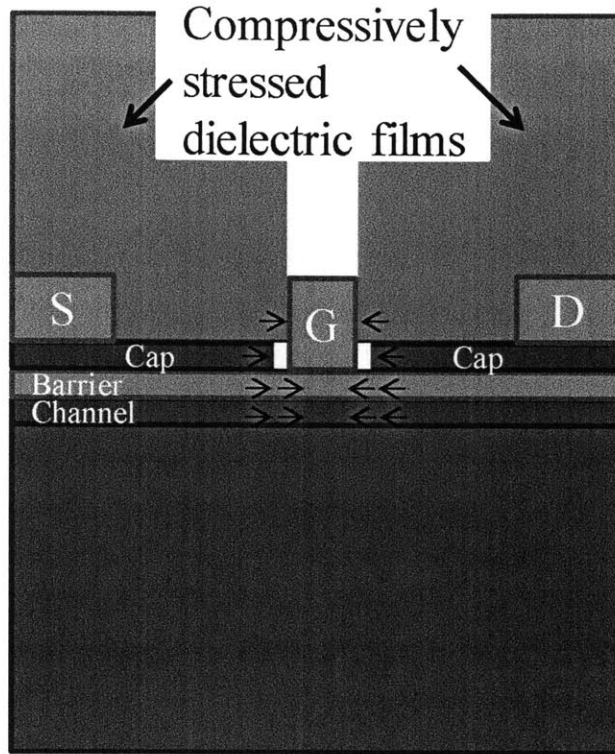


Figure 5-5. Schematic of the QW-FET with stressed dielectric overlay. The arrays of arrows indicate the direction of strain relaxation in the stressed dielectric and the direction of deformation in the heterostructure.

Our simulations for this structure (Figure 5-6) reveal that stress concentrates at the cut edge of the dielectric and decreases with increasing distance from the edge. The structure simulated in Figure 5-6 has a gate opening (L_G) of 1 μm and a film thickness of 200 nm. The stress distribution can be better seen in Figure 5-7, which shows the stress distribution along a line cutting through the center of the gate. Also illustrated in Figure 5-7, the stress perpendicular to the gate length direction (transverse) is 2 to 3 times smaller than the stress parallel to gate length (longitudinal), and with an opposite sign (tensile). The fact that the transverse stress is tensile is also desirable, as the negative

transverse piezoresistance coefficient obtained in Chapter 4 suggests μ_h can be further enhanced with tensile transverse stress.

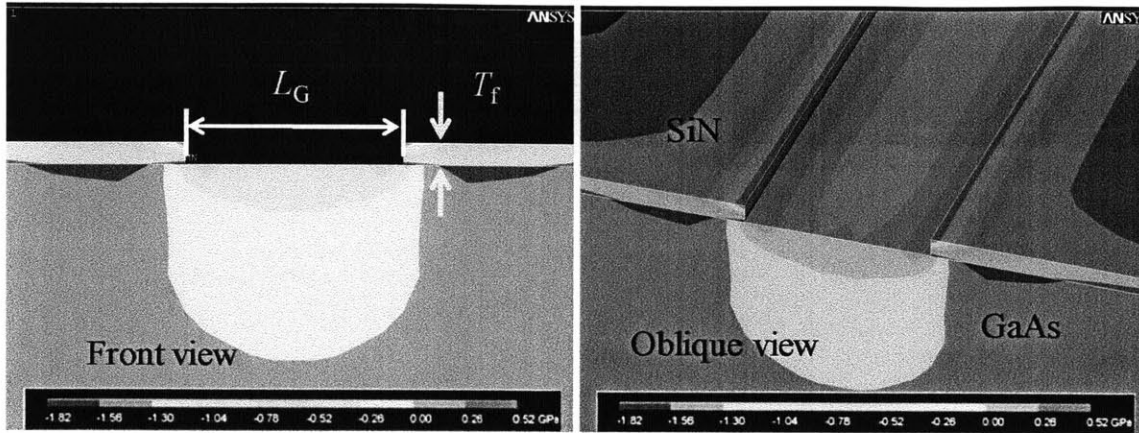


Figure 5-6. Stress distribution in a structure with compressively-stressed SiN overlay on GaAs substrate. The color bar is coded with blue as the compressive extreme and red as the tensile extreme. In this simulation, $L_G = 2 \mu\text{m}$ and $T_f = 200 \text{ nm}$.

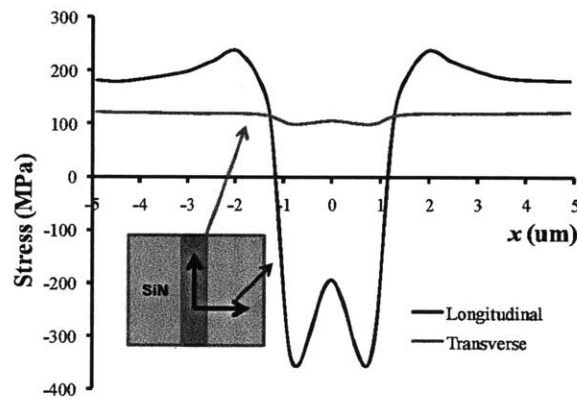


Figure 5-7. Stress distribution along a line underneath the gate with compressive dielectric. The position to take the distribution is shown in the inset. Longitudinal and transverse stress distributions are shown. The thickness of the gate film is 200 nm. The internal stress of the dielectric was set to -2 GPa.

This stressed dielectric approach scales appropriately. Figure 5-8 shows the stress in the channel at the center of the gate ($x = 0$ in Figure 5-7) as a function of L_G . It can be clearly seen that the stress increases rapidly as the gate length scales down. The stress can

be over 2 GPa when $L_G < 100$ nm. This behavior not only suggests that this dielectric overlay approach is suitable for scaled QW-FETs but also that it can be an effective way for studying large strain effects in QW-FETs. Therefore, we pursue this approach in the following experimental studies of this chapter.

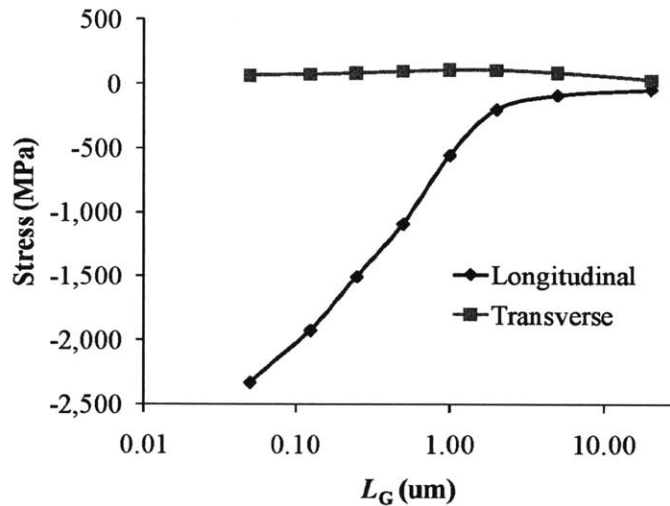


Figure 5-8. Gate-length dependence of the stress at the center of channel.

The selected structure is similar to the stressor liner techniques widely used in advanced Si nMOS. A question to ask is if this scheme is pitch scalable [94]. In particular, as the distance between gate electrodes shrinks together with gate length, the volume of stressors is limited. Therefore, the effective stress that stressors can exert on the channel can shrink in deeply scaled Si nMOS. [95] For our p-channel QW-FET structure with a stressor, this topic also requires attention. A detailed study seems more appropriate when a complete nanometer scale device structure emerges.

5.3 Fabrication process and structural analysis

Figure 5-9 summarizes the process flow for the QW-FET with SiN stressor. Figure 5-10 shows two key cross-sections after ohmic metallization of the device with the process flow of Figure 5-9. The steps before ohmic contact formation have been presented in Chapter 3.

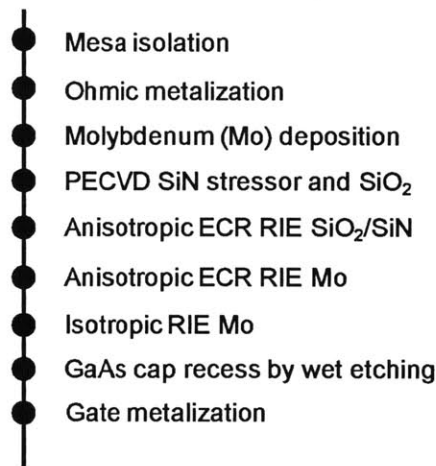


Figure 5-9. Process flow for p-channel $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ QW-FET with built-in stressor.

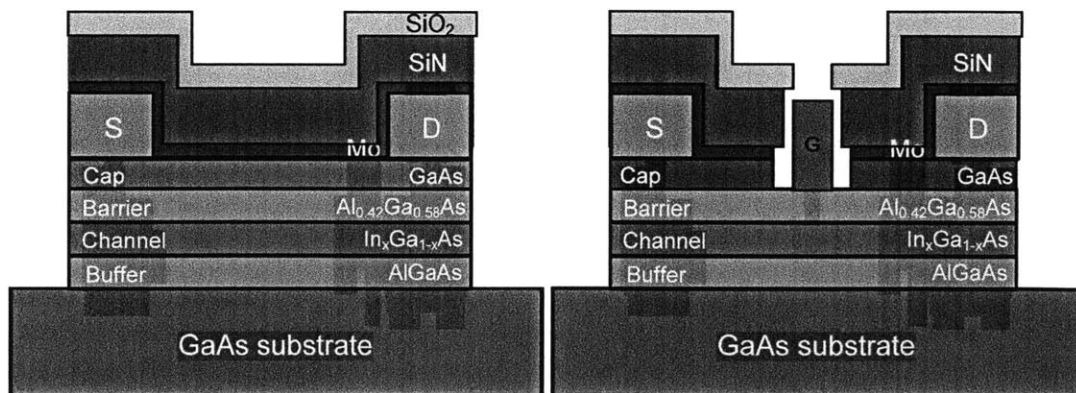


Figure 5-10. Cross sections after stressor deposition (left) and the finished device (right). This process yields a refractory contact metal layer and SiN stressor that are both self-aligned to the gate edge.

In our target structure (Figure 5-10 right), uniaxial strain is introduced through a

plasma enhanced chemical vapor deposition (PECVD) SiN layer with internal compressive stress. An opening in this film to accommodate the gate in a self-aligned way exerts compressive stress in the semiconductor underneath the gap near the film edge. Below the SiN, a Mo film is introduced to prevent p-type dopant (carbon) passivation during PECVD [96]. With better metal selection, this metal film could behave as a self-aligned ohmic contact to the transistor. Above the SiN stressor, a SiO₂ layer is used as a hard mask for the gate metal and prevents shorting with the Mo film. In our process, the Mo and SiN were pulled back from the gate edge in a self-aligned way. This allows the stressor to be placed very closely to the FET channel. In our experiments, two types of SiN were deposited in our experiments: one with -2.1 GPa compressive stress and a reference one with nearly zero stress.

Figure 5-11 shows a cross-section SEM example of a processed FET. After the gate recess process, the distance between the gate and the GaAs cap is found to be ~400 nm. This distance can be shrunk by reducing the process time of the isotropic SiN and Mo RIE. No side etch of the GaAs cap under the Mo layer is observed. This feature is useful for future self-aligned ohmic metal contact.

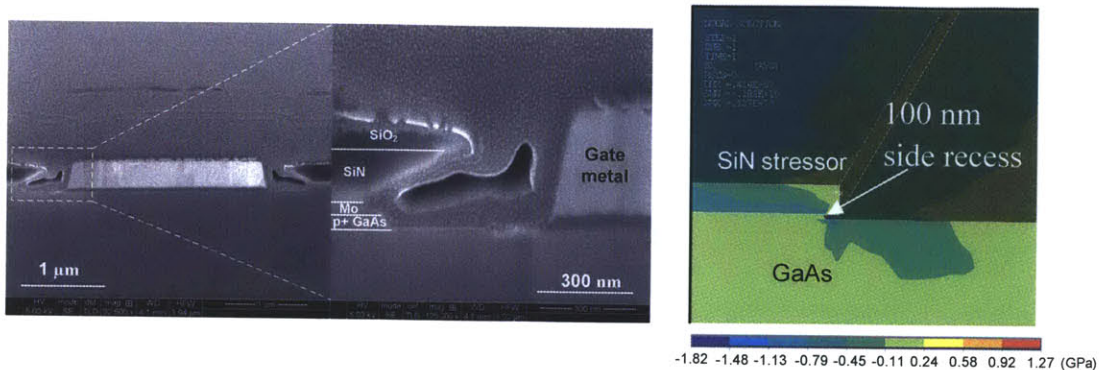


Figure 5-11. (Left) Cross section SEM of a p-channel QW-FET. (Right) Spatial distribution of the stress along gate length direction by 3D finite-element mechanical simulations. A side-recessing distance of 100 nm for GaAs cap was considered in the simulations.

We performed mechanical simulations (Figure 5-11 right) including the side-recess gap that is formed in our structures. These simulations are used to evaluate the impact of the air gap on the magnitude of stress under the gate. For simplicity, the mechanical properties of GaAs were used for the Mo layer. To the first order, this should only affect to a small extent the stress distribution in the gate region, as long as this layer is elastic. In addition, at this moment, we are not investigating the stress distribution in the Mo layer.

Figure 5-12 shows the simulated values for stress taken at the center of the recessed gap as a function of L_G . The longitudinal stress increases markedly with decreasing L_G . There are three regimes of stress sensitivity to L_G that are determined by the relative dimensions of L_G , side recess length and stressor thickness. The first regime is with L_G much larger than stressor thickness. In this regime, the stress under the gate (center stress) increases slowly with decreasing L_G . The second regime is with L_G comparable to the stressor thickness. In this regime, the center stress increases sharply with decreasing

L_G . The 3rd regime is with L_G comparable to the side-recess length. The rate of increase of the center stress decreases. The pFETs in this work fall in the first slow-increase segment due to L_G being much larger than the SiN thickness. As L_G scales down to the sub-50 nm range, up to -1.2 GPa stress is expected in the FET following our proposed process. Assuming a linear relationship between stress and mobility enhancement, a greater than 160% enhancement in μ_h is expected as devices scale down to $L_G < 50$ nm. Greater enhancements are possible with structure optimization. For devices fabricated in the following section, which have $L_G > 2 \mu\text{m}$, we expect to see an improvement of μ_h less than 25%. These calculations did not consider the effect of non-uniform stress distribution, which is expected to present in fabricated devices. This non-uniform effect is likely to result in larger enhancements than our current calculations, because the stress value we chose for the present calculations are the lowest across the channel.

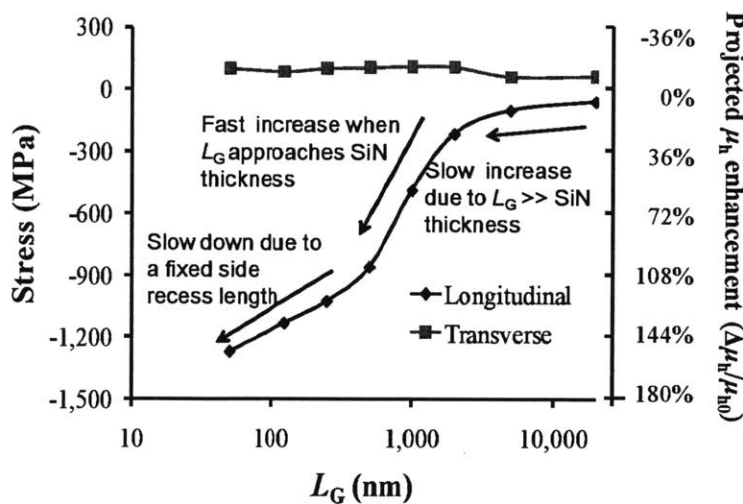


Figure 5-12. Center stress (left y-axis) scaling with L_G and projected μ_h enhancement (right y-axis). The center stress was simulated following the structure in Figure 5-11. The μ_h enhancement was projected assuming a linear relationship between μ_h and stress and using the piezoresistance coefficients obtained in Chapter 4.

5.4 QW-FET results and analysis

We fabricated two types of QW-FETs: one with -2.1 GPa SiN stressor, another with zero stress SiN stressor. Gate lengths of QW-FETs on these chips were varied from 8 μm to 2 μm . For each gate length, devices with channel aligned with 4 directions, [-110], [110], [010], and [100] were fabricated side by side.

In the fabricated devices, significant improvements in device performance were found when uniaxial strain was introduced. Figure 5-13 compares the output characteristics of two devices with high- and zero-stress SiN, $L_G = 2 \mu\text{m}$ and channel along [-110]. A significant increase in the drain current was observed. Figure 5-14 shows the subthreshold characteristics of the two devices. They both have similar gate current characteristics and subthreshold swing.

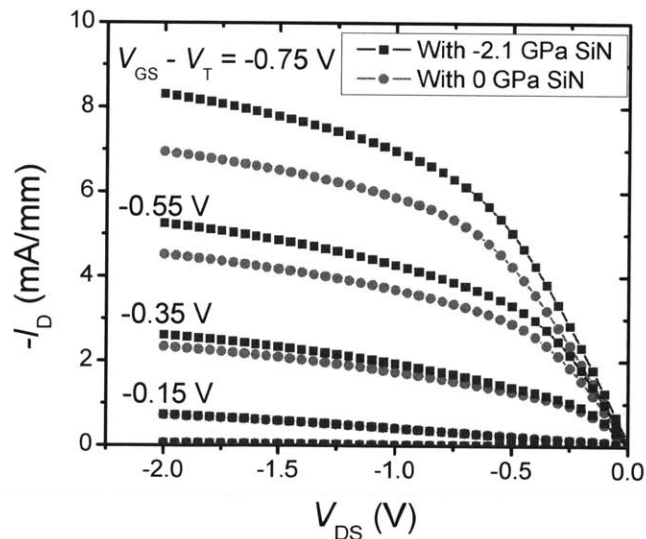


Figure 5-13. Comparison between output characteristics of QW-FETs with high-stress and zero-stress SiN films. $L_G = 2 \mu\text{m}$. Channel aligns with [-110] direction.

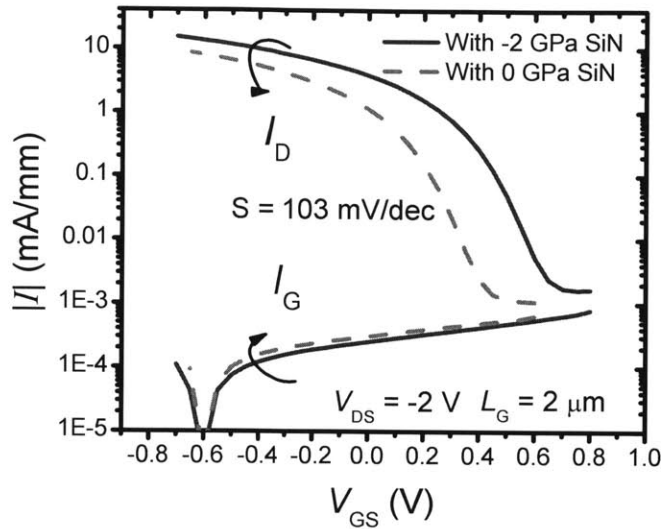


Figure 5-14. Comparison between subthreshold characteristics of FETs with high-stress and zero stress SiN films. $L_G = 2 \mu\text{m}$. Channel aligns with $[-110]$ direction.

In Figure 5-14, it can also be seen that the V_T of the high-stress device is 0.2 V more positive than the zero-stress device. This difference (including sign and magnitude) was observed for all L_G we obtained and devices with all the orientations. We suspect that this difference is because the recessed $\text{Al}_{0.42}\text{Ga}_{0.58}\text{As}$ barrier is slightly thinner in the zero-stress sample. During the PECVD SiN process, the thickness of the zero-stress SiN film was ~ 50 nm thinner than the high-stress SiN. Thereafter, these two samples experienced same ECR RIE processes, as shown in Figure 5-9. The anisotropic ECR RIE process for the SiN films was targeted with 50% over etch for the thicker film. In consequence, the GaAs cap in the devices with thinner SiN film (zero-stress) were exposed during dry etch for a longer time than in the devices with high-stress film. Even though the chemicals used for SiN etch are not supposed to react with GaAs, physical bombardment may have happened to the GaAs cap making it thinner for the zero-stress devices (a DC bias of -50 V was applied to implement anisotropic etch). After the RIE, this thickness difference in the GaAs cap is partially transferred to the AlGaAs barrier during wet gate recess, given

that the selectivity between GaAs and AlGaAs by the recess etchant is finite. Therefore, V_T in the zero-stress devices shifted negatively compared with the high-stress devices.

This barrier thickness difference may make the gate capacitance in the zero-stress devices somehow higher than in the high-stress devices in theory. This is likely to counteract a portion of the μ_h enhancement in the high-stress devices. However, the gate capacitance difference between the two types of samples is unlikely to be significant, given that the gate leakage current of these two samples are not too different.

The extrinsic resistance between the gate edge and the Mo edge is probably not affected by the thickness difference in the two samples. The reason is because the thickness difference is mainly limited to the gate area defined by the anisotropic RIE.

Performance improvements are particularly visible in the transconductance (Figure 5-15) with high (-2 V) and low (-0.2 V) drain bias. The intrinsic transconductance (g_{mi}) was extracted from the extrinsic transconductance (g_{mext}) using source/drain resistance (R_S/R_D) measured by the gate current injection method.

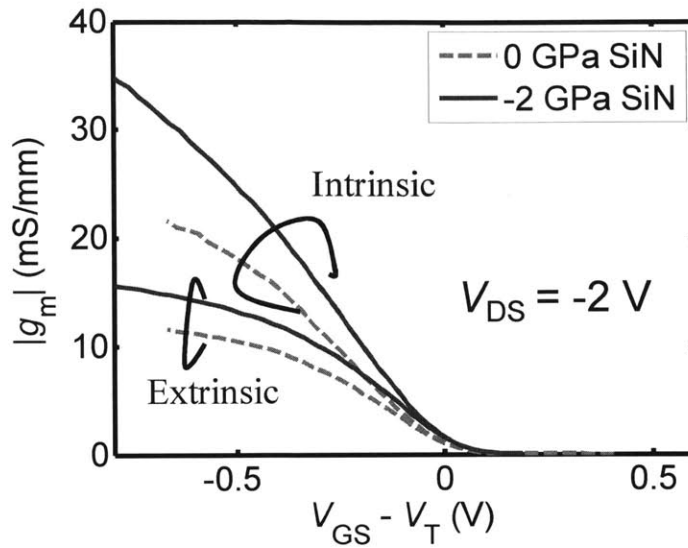


Figure 5-15. Comparison between transconductance at $V_{DS} = -2$ V of FETs with high-stress and zero stress SiN films. $L_G = 2$ μm . Channel aligns with $[-110]$ direction.

It is also found that R_S and R_D are significantly smaller in the high-stress sample with a maximum reduction of $\sim 25\%$ along $[-110]$. (Figure 5-16) This is most likely due to a reduction of the resistance in the side-recess regions next to the gate due to compressive strain. The stress level in these regions is higher than under the gate, as suggested by our simulations, for example, in Figure 5-7. The enhancements in g_{mi} and reduction in R_S and R_D consistently show the signs expected from μ_h enhancement under compressive stress.

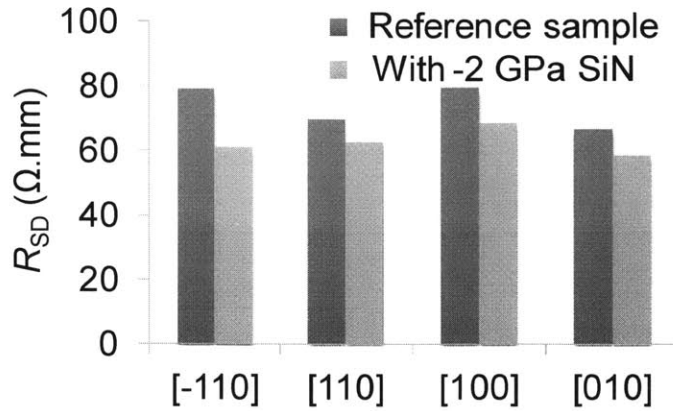


Figure 5-16. Source-drain resistance extracted by gate current injection method for four major crystal orientations. Decrease of R_{SD} was seen in all four cases. Best results obtained in the [-110] orientation.

We also investigated the dependences of the g_{mi} enhancement on crystal orientation. As shown in Figure 5-17, we found that the effect of uniaxial stress is not isotropic. Particularly, the enhancement for stress parallel to hole transport is the highest when the channel is along [-110] direction. The magnitude of Δg_{mi} can be 3 times larger than in a device with the channel along [110]. The $\langle 100 \rangle$ direction channel devices showed similar response to the applied uniaxial strain, as expected. The $\langle 110 \rangle$ anisotropy of enhancement agrees with what we found in chip-bending measurements on this heterostructure: μ_h increases 12% per -100 MPa with [-110] channel, but increases 4.6% per -100 MPa with [110] channel [3]. Similar improvements in g_{mi} were found for the two $\langle 100 \rangle$ directions.

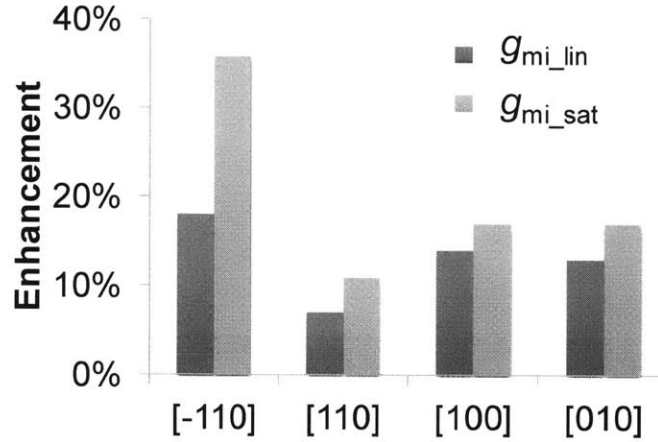


Figure 5-17. Increase of intrinsic transconductance in linear regime (g_{mi_lin}) and saturation regime (g_{mi_sat}) for pFETs with $L_G = 2 \mu\text{m}$ along the four major crystal orientations. Best results obtained along [-110] orientation.

Following the method discussed in Chapter 2, we simulated the valence band structure (Figure 5-18 left) in our QW including the external uniaxial strain, built-in biaxial strain and piezoelectric effect; and calculated the averaged transport effective mass (m^*), a key factor that impacts μ_{hs} , following the procedure outlined in Chapter 2. The calculated m^* exhibits a similar anisotropic behavior as observed in the experiments. (Figure 5-18 right) For the effective mass along the strain direction, the change is the largest in [-110] direction, followed by <100> directions and the smallest in [110] direction. The magnitude of enhancements along <110> directions were also discussed in Chapter 4. One additional remark is that <100> directions have a lower Young's Modulus (78 GPa), compared with 112 GPa in <110> orientations. As a result, the same magnitude of stress may generate higher strain in <100> directions compared with <110> orientations. This mechanical difference gives <100> directions an advantage of around 40% for the effective mass change per unit stress.

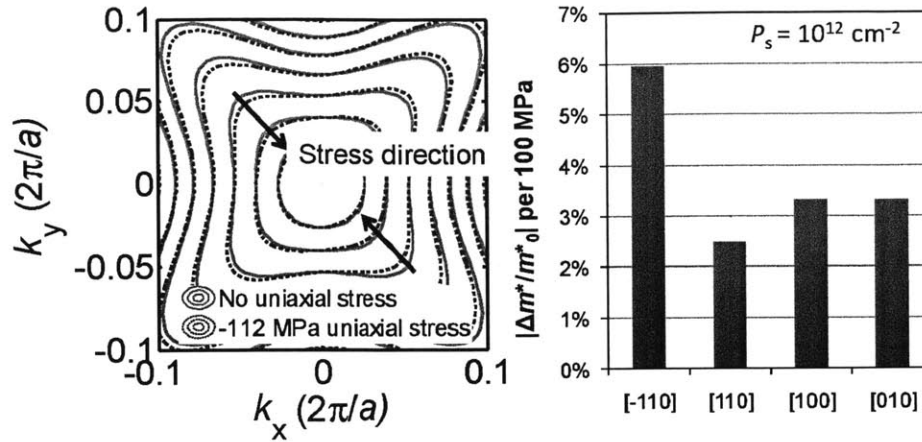


Figure 5-18. (Left) $k.p$ simulation showing anisotropic change of valence band with uniaxial stress. (Right) Change of average in-plane effective mass following a nonparabolic multi-band treatment, for $\langle 110 \rangle$ and $\langle 100 \rangle$ orientations. The maximum change in the effective mass along strain direction is calculated to occur along the $[-110]$ direction.

We have also studied the performance enhancement of QW-FETs as a function of L_G . We found that it increases with shorter L_G . Figure 5-19 shows that $\Delta g_{mi}/g_{mi}^0$ becomes more pronounced as L_G decreases. This agrees with theory in Figure 5-12, *i.e.*, the center stress in the device increases as L_G decreases, indicating an increase of overall strain in the device channel.

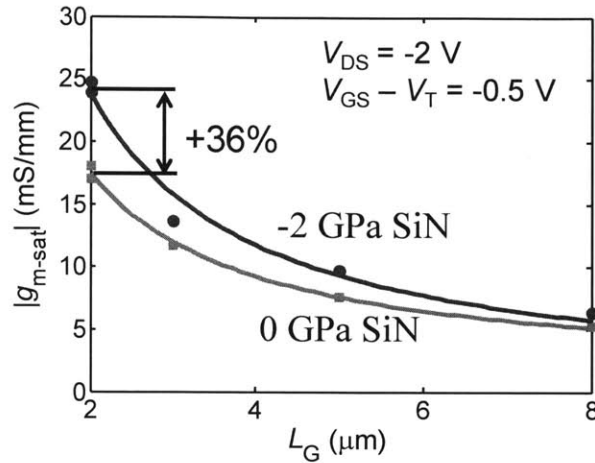


Figure 5-19. Gate length dependence of peak intrinsic saturation-regime transconductance for high-stress and zero-stress samples along $[-110]$. The dots are measured data. The solid lines are least-square-fitted models.

5.5 Summary

In this chapter, we have developed a device architecture for p-type InGaAs FETs that incorporates uniaxial strain through a self-aligned dielectric stressor. For the first time, we demonstrate substantial enhancements in the transport characteristics of p-type InGaAs FETs through the combination of compressive uniaxial strain and compressive epitaxially grown biaxial strain. Strain enhances both the intrinsic transconductance as well as the access resistances. A maximum of 36% increase in the intrinsic transconductance in QW-FETs with $L_G = 2 \mu\text{m}$ was observed. The structure exhibits promising gate-length scalability, as the enhancements are expected in theory as well as demonstrated in our experiments to increase with gate length scaling down. In addition, the structure is compatible with self-aligned source drain metal contacts. Our proposed device architecture holds promise to implement high-performance p-channel III-V FETs for future CMOS logic applications.

Chapter 6 Conclusions and suggestions for further research

6.1 Summary

In this thesis, we devote our efforts to improve hole mobility in III-Vs and p-channel QW-FET performance for post-Si complementary logic technology. We studied the effect of applying uniaxial strain to III-V quantum well FETs both theoretically and experimentally.

From a theoretical point of view, the valence band change is the fundamental reason for the hole mobility enhancement induced by strain. In general, applied strain splits the heavy-hole and light-hole band degeneracy at the Γ point in the momentum space (k -space). Simultaneously, the curvature of the bands is changed. In consequence, the interband scattering and in-plane transport effective mass of holes can be reduced. When uniaxial strain is applied, an anisotropic change of the effective mass on the plane of hole transport takes place. Uniaxial strain changes the effective masses parallel and perpendicular to its direction in opposite ways.

Connecting hole effective mass and mobility requires substantial efforts in numerical calculations, because the hole bands are highly non-parabolic. We followed an approximate treatment for non-parabolic bands that allowed us to obtain energy- and directional dependent effective masses for the valence bands and furthermore obtain an overall effective mass along any given direction averaged by carrier occupation. This approach helped us to quantitatively capture the effect of strain on valence band and

effective mass. Our analysis shows that the biggest reduction in effective mass due to uniaxial strain is obtained when compressive strain is applied along the [-110] direction with hole transport parallel to strain.

Other than modifications to the valence band, Schottky barrier height change and the piezoelectric effect were also found to be relevant in III-V QW-FET operation. Band alignment shifts for conduction and valence band due to hydrostatic component of the applied strain give rise to a shift in Schottky barrier height and threshold voltage. This shift appears the same for strain along [110] and [-110]. The piezoelectric effect changes the electrostatics of QW-FETs along the growth direction as a result of strain-induced piezoelectric charges in the heterostructure. This electrostatics change also induces a threshold voltage shift in QW-FETs. In contrast with the ΔV_T induced by Schottky barrier height change, the change induced by the piezoelectric effect shows a unique signature – the sign of ΔV_T is reversed when strain changes from [110] to [-110]. In addition to the shift in V_T , the piezoelectric effect is also expected to change the gate capacitance of a QW-FET. This is because the piezoelectric effect changes the quantum well profile and therefore the quantum confinement of the carriers in the quantum well. This affects the centroid capacitance of the 2DHG. The magnitude of the piezoelectric effect depends on the thicknesses of barrier and channel layers. Because of this, it tends to become less significant as devices scale down.

In experiments, a series of studies were carried out by introducing uniaxial strain to III-V quantum wells through four-point bending. The quantum well materials that were examined include n-channel $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ and p-channel GaAs , $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$.

The n-channel QW-FET is found to be dominated by Schottky barrier height change and the piezoelectric effect. Combining these two effects, we found that threshold voltage shifts in the QW-FET can be well predicted by Schrodinger-Poisson simulations. One particular interesting effect is that change in the intrinsic transconductance due to strain, which in general reflects the combined change due to electron mobility and QW-FET gate capacitance, actually has a sign that is opposite to what is expected from the electron mobility shift. In fact, the change in intrinsic transconductance can be well explained by the gate capacitance shift induced by the piezoelectric effect.

In the p-channel GaAs quantum well, the hole mobility and concentration are found to change at the same time due to $\langle 110 \rangle$ strain. The underlying mechanisms include strain induced transport change and electrostatics change (similar to the n-channel QW). The effect of mobility change was extracted from Hall measurements. For the first time, the $\langle 110 \rangle$ piezoresistance coefficients of GaAs 2DHG have been determined. The changes of hole mobility and concentration manifest themselves as changes in the linear-regime drain current and threshold voltage of the QW-FETs.

To explore the effect of combining uniaxial strain with biaxial strain, we carried out bending experiments on $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ quantum wells. The two channels have biaxial strain of -1.7% and -2.1%, respectively. In these devices, we found that the piezoresistance coefficients parallel to hole transport are both ~ 1.6 x of the Si piezoresistance value. In addition, the parallel piezoresistance coefficients in the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well is >3 x the GaAs value. While the InAs fraction in the two materials are not drastically different, this result suggests that applying uniaxial strain on

top of biaxial strain may be fundamentally more effective in enhancing hole mobility than pure uniaxial strain can do. This agrees with a recent study by Gomez [32].

Among the results of the above experiments, the piezoresistance coefficients for 2DHG are determined for the first time in the GaAs, $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ quantum wells. The values are summarized in the last figure in Chapter 4. The sign of these coefficients agrees with the theoretical change in mobility due to applied uniaxial strain. These coefficients all suggest that compressive strain along the hole transport direction is preferred over any other direction for enhancing p-channel QW-FET performance.

To extend the efforts of introducing uniaxial strain to p-channel QW-FETs, we developed a device architecture that incorporates compressive SiN stressors self-aligned to the gate. In these experiments, the $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ quantum well was used, which has the highest parallel piezoresistance coefficient measured in previous experiments. With a 170 nm thick SiN with 2 GPa compressive strain, we obtained up to 36% improvement in a 2- μm -long device transconductance. The structure exhibits promising gate-length scalability and compatibility with self-aligned source drain metal contacts. Our proposed device architecture holds promise to implement high-performance p-channel III-V FETs for future CMOS logic applications.

6.2 List of contributions

The main contributions of this thesis have been summarized in the previous section. Here they are listed in bullet format:

- Developed a measurement set-up for bending III-V chips and electrically characterizing transistors and Hall structures on the chips.

- Theoretically interpreted strain effects on III-V QW-FETs with expected material properties in response to the strain. These effects include valence band change, piezoelectric effect and Schottky barrier height change.
- For the first time, experimentally observed and verified these relevant effects in n- and p-channel QW-FETs fabricated on various materials.
- For the first time, determined the piezoresistance coefficients for 2DHG in GaAs, $\text{In}_{0.24}\text{Ga}_{0.76}\text{As}$ and $\text{In}_{0.41}\text{Ga}_{0.59}\text{Sb}$ quantum wells.
- Demonstrated a device architecture that uses SiN stressor self-aligned to the gate to introduce uniaxial strain into the device channel. Significant scalable improvements in device performance were observed.

6.3 Suggestions for future work

Developing a high-performance p-channel FET to complement an n-channel $\text{In}_x\text{Ga}_{1-x}\text{As}$ FET is a grand challenge for post-Si CMOS technology. The work in this thesis is a modest step toward addressing this challenge. Further research is required before the most suitable choice can be identified. Key issues are:

- Study the virtual source injection velocity in the p-type quantum wells mentioned in this thesis, as well as strain effects on improving this velocity. This is the most important transport related figure of merit of relevance to performance.
- Carry out a more in-depth theoretical analysis for the impact of the combination of uniaxial and biaxial strain on hole transport characteristics.

A proper approach seems to be the one used for studying Si and Ge inversion layer hole mobility in [16].

- Scale down the gate length in the device structure with SiN stressor and explore the limit of performance improvement in $\text{In}_x\text{Ga}_{1-x}\text{As}$ pFETs.
- Apply the stressor scheme of Ch. 4 to $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ QW-FETs and demonstrate high-performance pFETs. With high hole mobility and high piezoresistance coefficients, $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ looks promising for high-performance p-channel FETs for post-Si CMOS technology.
- Extend strain studies to p-channel III-V MOSFET devices and study how interface roughness scattering affects the strain effects.

References

- [1] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, *et al.*, "A 45nm logic technology with high- k + metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *IEDM Tech. Dig.*, 2007, pp. 247–250.
- [2] A. Khakifirooz and D. A. Antoniadis, "MOSFET performance scaling - Part I: Historical trends," *IEEE Transactions on Electron Devices*, vol. 55, pp. 1391-1400, 2008.
- [3] A. Khakifirooz and D. A. Antoniadis, "MOSFET Performance Scaling - Part II: Future Directions," *IEEE Transactions on Electron Devices*, vol. 55, pp. 1401-1408, 2008.
- [4] A. Khakifirooz and D. A. Antoniadis, "Transistor Performance Scaling: The Role of Virtual Source Velocity and Its Mobility Dependence," in *IEDM Tech. Dig.*, 2006, pp. 1-4.
- [5] D.-H. Kim and J. A. del Alamo, "30 nm E-mode InAs PHEMTs for THz and future logic applications," in *IEDM Tech. Dig.*, 2008, pp. 719-722.
- [6] D.-H. Kim and J. A. del Alamo, "Extraction of virtual-source injection velocity in sub-100 nm III-V HFETs," in *IEDM Tech. Dig.*, 2009, pp. 861-864.
- [7] D.-H. Kim, J. A. del Alamo, L. Jae-Hak, and K.-S. Seo, "Logic Suitability of 50-nm In_{0.7}Ga_{0.3}As HEMTs for Beyond-CMOS Applications," *IEEE Transactions on Electron Devices*, vol. 54, pp. 2606-2613, 2007.
- [8] T. Irisawa, S. Tokumitsu, T. Hattori, K. Nakagawa, S. Koh, and Y. Shiraki, "Ultrahigh room-temperature hole Hall and effective mobility in Si_{0.3}Ge_{0.7}/Ge/Si_{0.3}Ge_{0.7} heterostructures," *Applied Physics Letters*, vol. 81, pp. 847-849, 2002.
- [9] R. Bennett, M. G. Ancona, J. B. Boos, and B. V. Shanabrook, "Mobility enhancement in strained p-InGaSb quantum wells," *Applied Physics Letters*, vol. 91, p. 042104, 2007.
- [10] A. M. Kusters, A. Kohl, V. Sommer, R. Muller, and K. Heime, "Optimized double heterojunction pseudomorphic InP/In_xGa_{1-x}As/InP (0.64< x <0.82) p-MODFETs and the role of strain in their design," *IEEE Transactions on Electron Devices*, vol. 40, pp. 2164-2170, 1993.
- [11] A. M. Kusters, A. Kohl, K. Heime, T. Schapers, D. Uhlisch, B. Lengeler, *et al.*, "Low- and high-field transport properties of pseudomorphic In_xGa_{1-x}As/InP (0.73< x <0.82) p-type modulation-doped single-quantum-well structures," *Journal of Applied Physics*, vol. 75, pp. 3507-15, 1994.
- [12] J. C. Hensel and G. Feher, "Cyclotron Resonance Experiments in Uniaxially Stressed Silicon: Valence Band Inverse Mass Parameters and Deformation Potentials," *Physical Review*, vol. 129, p. 1041, 1963.
- [13] K. Nayak, J. C. S. Woo, J. S. Park, K. L. Wang, and K. P. MacWilliams, "High-mobility p-channel metal-oxide-semiconductor field-effect transistor on strained Si," *Applied Physics Letters*, vol. 62, pp. 2853-2855, 1993.
- [14] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, *et al.*, "Delaying forever: Uniaxial strained silicon transistors in a 90nm CMOS technology," in *VLSI Symp. Tech. Dig.*, 2004, pp. 50-51.

- [15] S. Natarajan, M. Armstrong, M. Bost, R. Brain, M. Brazier, C. H. Chang, *et al.*, "A 32nm logic technology featuring 2nd-generation high- k + metal-gate transistors, enhanced channel strain and 0.171 μm^2 SRAM cell size in a 291Mb array," in *IEDM Tech. Dig.*, 2008, pp. 941-943.
- [16] M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, "Six-band k,p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness," *Journal of Applied Physics*, vol. 94, pp. 1079-1095, 2003.
- [17] T. Y. Wang and G. B. Stringfellow, "Strain effects on $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{InP}$ single quantum wells grown by organometallic vapor-phase epitaxy with $0 \leq x \leq 1$," *Journal of Applied Physics*, vol. 67, pp. 344-352, 1990.
- [18] P. O'Reilly, "Valence band engineering in strained-layer structures," *Semiconductor Science and Technology*, vol. 4, p. 121, 1989.
- [19] R. A. Kiehl, H. Shtrikman, and J. Yates, "Parallel and perpendicular hole transport in heterostructures with high AlAs mole-fraction barriers," *Applied Physics Letters*, vol. 58, pp. 954-956, 1991.
- [20] R. Bennett, M. G. Ancona, J. B. Boos, C. B. Canedy, and S. A. Khan, "Strained GaSb/AlAsSb quantum wells for p-channel field-effect transistors," *Journal of Crystal Growth*, vol. 311, pp. 47-53, 2008.
- [21] M. Radosavljevic, T. Ashley, A. Andreev, S. Coomber, G. Dewey, M. Emeny, *et al.*, "High-performance 40nm gate length InSb p-channel compressively strained quantum well field effect transistors for low-power ($V_{\text{CC}} = 0.5$ V) logic applications," 2008, pp. 727-730.
- [22] M. Kudo, H. Matsumoto, T. Tanimoto, T. Mishima, and I. Ohbu, "Improved hole transport properties of highly strained $\text{In}_{0.35}\text{Ga}_{0.65}\text{As}$ channel double-modulation-doped structures grown by MBE on GaAs," *Journal of Crystal Growth*, vol. 175-176, pp. 910-914, 1997.
- [23] M. Kudo, T. Mishima, H. Matsumoto, I. Ohbu, and T. Tanimoto, "Highly strained $\text{In}_{0.35}\text{Ga}_{0.65}\text{As}/\text{GaAs}$ layers grown by molecular beam epitaxy for high hole mobility transistors," *Journal of Electronic Materials*, vol. 25, pp. 944-947, 1996.
- [24] R. A. Kiehl, S. Tiwari, S. L. Wright, and M. A. Olson, "P-channel quantum-well heterostructure MI3SFET," *Electron Device Letters, IEEE*, vol. 9, pp. 309-311, 1988.
- [25] R. Hsu, Tay, W. Hsu, Chou, J. Wang, Shiun, *et al.*, "Study of Zinc-Delta-Doped Strained Quantum Well InGaAs/GaAs p-Channel Heterostructure Field-Effect Transistors," *Japanese Journal of Applied Physics*, vol. 35, p. 2085, 1996.
- [26] P. Nagaiah, V. Tokranov, M. Yakimov, and S. Oktyabrsky, "Strained Quantum Wells for p-Channel InGaAs CMOS," *Proc. Mater. Res. Soc. Symp.*, vol. 1108, p. A12-01, 2008.
- [27] S. E. Thompson, S. Guangyu, C. Youn Sung, and T. Nishida, "Uniaxial-process-induced strained-Si: extending the CMOS roadmap," *IEEE Transactions on Electron Devices*, vol. 53, pp. 1010-1020, 2006.
- [28] S. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in *IEDM Tech. Dig.*, 2004, pp. 221-224.

- [29] L. Washington, F. Nouri, S. Thirupapuliur, G. Eneman, P. Verheyen, V. Moroz, *et al.*, "pMOSFET with 200% mobility enhancement induced by multiple stressors," *IEEE Electron Device Letters*, vol. 27, p. 511, 2006.
- [30] M. Uchida, Y. Kamakura, and K. Taniguchi, "Performance Enhancement of pMOSFETs Depending on Strain, Channel Direction, and Material," *International Conference on Simulation of Semiconductor Processes and Devices, 2005. SISPAD 2005*. pp. 315-318.
- [31] A. Dimoulas, E. Gusev, P. C. McIntyre, and M. Heyns, *Advanced Gate Stacks for High-Mobility Semiconductors*: Springer Publishing Company, Incorporated, 2007.
- [32] L. Gomez, C. Ni Chléirigh, P. Hashemi, and J. L. Hoyt, "Enhanced Hole Mobility in High Ge Content Asymmetrically Strained-SiGe p-MOSFETs," *IEEE Electron Device Letters*, vol. 31, pp. 782-784, 2010.
- [33] X. Wang, P. Matagne, L. Shifren, B. Obradovic, R. Kotlyar, S. Cea, *et al.*, "Physics of Hole Transport in Strained Silicon MOSFET Inversion Layers," *IEEE Transactions on Electron Devices*, vol. 53, pp. 1840-1851, 2006.
- [34] S. Adachi, *Physical properties of III-V semiconductor compounds: InP, InAs, GaAs, GaP, InGaAs and InGaAsP*, New York: Wiley, (1992).
- [35] M. Lundstrom, *Fundamentals of Carrier Transport*, 2 ed.: Cambridge University Press, 2000.
- [36] P. Y. Yu and M. Cardona, *Fundamentals of Semiconductors - Physics and Materials Properties (3rd Edition)*, 3 ed.: Springer - Verlag, 2011.
- [37] R. Eppenga, S. Colak, and M. F. H. Schuurmans, "Effects of band mixing on the radiative properties of a quantum well," *Fiber and Integrated Optics*, vol. 7, pp. 57-67, 1988/01/01 1988.
- [38] P. A. Chen, C. Y. Chang, and C. Juang, *Analysis of differential gain in GaAs/AlGaAs quantum well lasers* vol. 76: AIP, 1994.
- [39] O. Weber, T. Irisawa, T. Numata, M. Harada, N. Taoka, Y. Yamashita, *et al.*, "Examination of additive mobility enhancements for uniaxial stress combined with biaxially strained Si, biaxially strained SiGe and Ge channel MOSFETs," in *IEDM Tech. Dig.*, 2007, pp. 719-722.
- [40] M. De Michielis, D. Esseni, Y. L. Tsang, P. Palestri, L. Selmi, A. G. O'Neill, *et al.*, "A Semianalytical description of the hole band structure in inversion layers for the physically based modeling of pMOS transistors," *IEEE Transactions on Electron Devices*, vol. 54, pp. 2164-2173, 2007.
- [41] M.-J. Chen, C.-C. Lee, and K.-H. Cheng, "Hole effective masses as a booster of self-consistent six-Band k,p simulation in inversion layers of pMOSFETs," *IEEE Transactions on Electron Devices*, vol. 58, pp. 931-937, 2011.
- [42] S.-Y. Lin, H. P. Wei, D. C. Tsui, and J. F. Klem, "Cyclotron mass of two-dimensional holes in strained-layer GaAs/In_{0.20}Ga_{0.80}As/GaAs quantum well structures," *Applied Physics Letters*, vol. 67, pp. 2170-2172, 1995.
- [43] H. Booyens, J. S. Vermaak, and G. R. Proto, "Dislocations and the piezoelectric effect in III-V crystals," vol. 48, ed: AIP, 1977, pp. 3008-3013.
- [44] P. M. Asbeck, C. P. Lee, and M. C. F. Chang, "Piezoelectric effects in GaAs FET's and their role in orientation-dependent device characteristics," vol. 31, ed, 1984, pp. 1377-1380.

- [45] S. D. Mertens and J. A. del Alamo, "A model for hydrogen-induced piezoelectric effect in InP HEMTs and GaAs PHEMTs," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1849-1855, 2002.
- [46] L.-A. Ledebro and B. K. Ridley, "On the position of energy levels related to transition-metal impurities in III-V semiconductors," *Journal of Physics C: Solid State Physics*, vol. 15, p. L961, 1982.
- [47] J. Tersoff, "Schottky barrier heights and the continuum of gap states," *Physical Review Letters*, vol. 52, p. 465, 1984.
- [48] J. Tersoff, "Schottky barriers and semiconductor band structures," *Physical Review B*, vol. 32, p. 6968, 1985.
- [49] J. Tersoff and W. A. Harrison, "Transition-metal impurities in semiconductors: Their connection with band lineups and Schottky barriers," *Physical Review Letters*, vol. 58, p. 2367, 1987.
- [50] G. Van de Walle, "Band lineups and deformation potentials in the model-solid theory," *Physical Review B*, vol. 39, p. 1871, 1989.
- [51] D. Nolte, W. Walukiewicz, and E. E. Haller, "Band-edge hydrostatic deformation potentials in III-V semiconductors," *Physical Review Letters*, vol. 59, p. 501, 1987.
- [52] Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III-V compound semiconductors and their alloys," *Journal of Applied Physics*, vol. 89, pp. 5815-5875, 2001.
- [53] S.-H. Wei and A. Zunger, "Predicted band-gap pressure coefficients of all diamond and zinc-blende semiconductors: Chemical trends," *Physical Review B*, vol. 60, p. 5404, 1999.
- [54] S. Adachi, *Handbook on Physical Properties of Semiconductors*: Springer-Verlag, 2004.
- [55] B. Boos, B. R. Bennett, N. A. Papanicolaou, M. G. Ancona, J. G. Champlain, Y.-C. Chou, *et al.*, "Sb-based n- and p-channel heterostructure FETs for high-speed, low-power applications," *IEICE Trans. Electronics*, vol. E91-C, pp. 1050-1057, 2008.
- [56] D. Gregory, F. T. Wen, and C. James, "Etch rates and selectivities of citric acid/hydrogen peroxide on GaAs, $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, and InP," *J. Electrochem. Soc.*, vol. 139, pp. 831-835, 1992.
- [57] M. Hirano, K. Oe, and F. Yanagawa, "P-channel AlGaAs/GaAs heterostructure FETs employing two-dimensional hole gas," vol. 23, ed, 1984, pp. L868-L870.
- [58] Chien-Ping, H. T. Wang, G. J. Sullivan, N. H. Sheng, and D. L. Miller, "High-transconductance p-channel InGaAs/AlGaAs modulation-doped field effect transistors," *IEEE Electron Device Letters*, vol. 8, pp. 85-87, 1987.
- [59] S. Y. Chou and D. A. Antoniadis, "Relationship between measured and intrinsic transconductances of FETs," *IEEE Transactions on Electron Devices*, vol. 34, pp. 448-450, 1987.
- [60] R. Greenberg and J. A. del Alamo, "Nonlinear source and drain resistance in recessed-gate heterostructure field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 43, pp. 1304-1306, 1996.
- [61] J. V. d. Pauw, "A method of measuring specific resistivity and Hall effect of discs of arbitrary shape," *Phillips Res. Rep.*, vol. 13, p. 1, 1958.

- [62] A. Anderson and N. Apsley, "The Hall effect in III-V semiconductor assessment," *Semiconductor Science and Technology*, vol. 1, p. 187, 1986.
- [63] C. Look, C. E. Stutz, J. R. Sizelove, and K. R. Evans, "On Hall scattering factors for holes in GaAs," *Journal of Applied Physics*, vol. 80, pp. 1913-1915, 1996.
- [64] R. R. Blanchard, J. A. del Alamo, S. B. Adams, P. C. Chao, and A. Cornet, "Hydrogen-induced piezoelectric effects in InP HEMT's," *IEEE Transactions on Electron Devices*, vol. 20, pp. 393-395, 1999.
- [65] Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III-V compound semiconductors and their alloys," *Journal of Applied Physics*, vol. 89, pp. 5815-5875, 2001.
- [66] C. Kopf, H. Kosina, and S. Selberherr, "Physical models for strained and relaxed GaInAs alloys: Band structure and low-field transport," *Solid-State Electronics*, vol. 41, pp. 1139-1152, 1997.
- [67] Y. Liu, Z. L. Rang, A. K. Fung, C. Cai, P. P. Ruden, M. I. Nathan, *et al.*, "Uniaxial-stress dependence of Hall effect in an AlGaAs/GaAs modulation-doped heterojunction," *Applied Physics Letters*, vol. 79, pp. 4586-4588, 2001.
- [68] L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 97, p. 011101, 2005.
- [69] M. Kudo, H. Matsumoto, T. Tanimoto, T. Mishima, and I. Ohbu, "Improved hole transport properties of highly strained In_{0.35}Ga_{0.65}As channel double-modulation-doped structures grown by MBE on GaAs," *Journal of Crystal Growth*, vol. 175-176, pp. 910-914, 1997.
- [70] Y. Zhang, M. V. Fischetti, B. Soree, and T. O'Regan, "Theory of hole mobility in strained Ge and III-V p-channel inversion layers with high-k insulators," *Journal of Applied Physics*, vol. 108, p. 123713, 2010.
- [71] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Physical Review*, vol. 94, p. 42, 1954.
- [72] S. Suthram, J. C. Ziegert, T. Nishida, and S. E. Thompson, "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (~1.5 GPa) channel stress," *IEEE Electron Device Letters*, vol. 28, pp. 58-61, 2007.
- [73] L. Xia, J. B. Boos, B. R. Bennett, M. G. Ancona, and J. A. d. Alamo, "Hole mobility enhancement in In_{0.41}Ga_{0.59}Sb quantum-well field-effect transistors," *Applied Physics Letters*, vol. 98, p. 053505, 2011.
- [74] S. M. Sze, *The Physics of Semiconductor Devices*. New York: Wiley, 1981.
- [75] S. Karmalkar, "A new equivalent MOSFET representation of a HEMT to analytically model nonlinear charge control for simulation of HEMT devices and circuits," *IEEE Transactions on Electron Devices*, vol. 44, pp. 862-868, 1997.
- [76] T. M. Lu, Z. F. Li, D. C. Tsui, M. J. Manfra, L. N. Pfeiffer, and K. W. West, "Cyclotron mass of two-dimensional holes in (100) oriented GaAs/AlGaAs heterostructures," *Applied Physics Letters*, vol. 92, p. 012109, 2008.
- [77] J. Harris and B. K. Ridley, "Hot electrons in nonparabolic bands with acoustic and polar optical phonon scattering," *Journal of Physics and Chemistry of Solids*, vol. 34, pp. 197-207, 1973.

- [78] B. Bennett and J. A. del Alamo, "Orthorhombic distortion of mismatched $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{InP}$ heterostructures," *Journal of Electronic Materials*, vol. 20, pp. 1075-1079, 1991.
- [79] B. R. Bennett and J. A. d. Alamo, "Optical anisotropy in mismatched InGaAs/InP heterostructures," *Applied Physics Letters*, vol. 58, pp. 2978-2980, 1991.
- [80] K. Rammohan, D. H. Rich, R. S. Goldman, J. Chen, H. H. Wieder, and K. L. Kavanagh, "Study of μm -scale spatial variations in strain of a compositionally step-graded $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}(001)$ heterostructure," *Applied Physics Letters*, vol. 66, pp. 869-871, 1995.
- [81] J. A. Wilson, M. MacKenzie, S. MacFadzean, T. McMullen, S. Hamill, P. Stopford, *et al.*, "Electron transport anisotropies in pseudomorphic InGaAs channel materials and their structural origin," vol. 203, ed, 2006, pp. 628-637.
- [82] G. Arlt and P. Quadflieg, "Piezoelectricity in III-V compounds with a phenomenological analysis of the piezoelectric effect," *Physica Status Solidi (b)*, vol. 25, pp. 323-330, 1968.
- [83] S. E. Thompson, S. Suthram, Y. Sun, G. Sun, S. Parthasarathy, M. Chu, *et al.*, "Future of strained Si semiconductors in nanoscale MOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 1-4.
- [84] K. Uchida, R. Zednik, L. Ching-Huang, H. Jagannathan, J. McVittie, P. C. McIntyre, *et al.*, "Experimental study of biaxial and uniaxial strain effects on carrier mobility in bulk and ultrathin-body SOI MOSFETs," in *IEDM Tech. Dig.*, 2004, pp. 229-232.
- [85] A. Nainani, T. Irisawa, Z. Yuan, Y. Sun, T. Krishnamohan, M. Reason, *et al.*, "Development of high-k dielectric for Antimonides and a sub 350°C III-V pMOSFET outperforming Germanium," in *IEDM Tech. Dig.*, 2010, pp. 138-141.
- [86] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Transactions on Electron Devices*, vol. 29, pp. 64-70, 1982.
- [87] J. T. Pan and I. A. Blech, "In situ study of film stress and kinetics of platinum silicide formation on silicon," *Thin Solid Films*, vol. 113, pp. 129-134, 1984.
- [88] T. Soma, J. Satoh, and H. Matsuo, "Thermal expansion coefficient of GaAs and InP," *Solid State Communications*, vol. 42, pp. 889-892, 1982.
- [89] J. Angilello, F. d'Heurle, S. Petersson, and A. Segmuller, "Observations of stresses in thin films of palladium and platinum silicides on silicon," *Journal of Vacuum Science and Technology*, vol. 17, pp. 471-475, 1980.
- [90] G. Colgan, "Activation energy for Pt_2Si and PtSi formation measured over a wide range of ramp rates," 1995.
- [91] S. M. Hu, "Stress-related problems in silicon technology," *Journal of Applied Physics*, vol. 70, pp. R53-R80, 1991.
- [92] J. Fallon, V. S. Veerasamy, C. A. Davis, J. Robertson, G. A. J. Amaratunga, W. I. Milne, *et al.*, "Properties of filtered-ion-beam-deposited diamondlike carbon as a function of ion energy," *Physical Review B*, vol. 48, p. 4777, 1993.
- [93] X. Liu, B. Liu, E. K. F. Low, W. Liu, M. Yang, L.-S. Tan, *et al.*, "Local stress induced by diamond-like carbon liner in AlGaN/GaN metal-oxide-semiconductor high-electron mobility transistors and impact on electrical characteristics", *Applied Physics Letters*, vol. 98, p. 183502, 2011.

- [94] K. J. Kuhn, "Moore's law past 32nm: Future challenges in device scaling," *13th International Workshop on Computational Electronics, 2009. IWCE '09.*, 2009, pp. 1-6.
- [95] A. Oishi, O. Fujii, T. Yokoyama, K. Ota, T. Sanuki, H. Inokuma, *et al.*, "High performance CMOSFET technology for 45nm generation and scalability of stress-induced mobility enhancement technique," in *IEDM Tech. Dig.*, 2005, pp. 229-232.
- [96] A. Nakajima, K. Nagata, and T. Makimura, "Passivation of P-Type Dopants in GaAs by Process Induced Hydrogenation and Reactivation by Thermal Annealing," *Japanese Journal of Applied Physics*, vol. 31, p. L1704, 1992.