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Mimicking of pulse shape - dependent learning rules with a quantum dot memristor

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We present the realization of four different learning rules with a quantum dot memristor by tuning the shape, the magnitude, the polarity and the timing of voltage pulses. The memristor displays a large maximum to minimum conductance ratio of about 57000 at zero bias voltage. The high and low conductances correspond to different amounts of electrons localized in quantum dots, which can be successively raised or lowered by the timing and shapes of incoming voltage pulses. Modifications of the pulse shapes allow altering the conductance change in dependence on the time difference. Hence, we are able to mimic different learning processes in neural networks with a single device. In addition, the device performance under pulsed excitation is emulated combining the Landauer-Büttiker formalism with a dynamic model for the quantum dot charging, which allows explaining the whole spectrum of learning responses in terms of structural parameters that can be adjusted during fabrication such as gating efficiencies and tunneling rates. The presented memristor may pave the way for future artificial synapses with a stimulus-dependent capability of learning.

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I. INTRODUCTION

Memristors are fundamental passive circuit elements proposed by L. Chua in 1971.[1] The fingerprint of memristors is a pinched hysteresis loop in the current-voltage-plane showing a state-dependent conductance.[2] The state of a memristor is determined by previous charge flow through the device.[3] Hence, the conductance can be precisely controlled by voltage pulses with different widths, amplitudes and shapes,[4-6] which allows artificially mimicking synaptic functionalities.[7-10] Synapses and the modification of their strength are crucial for learning and memory in neural networks.[11,12] A model called spike-timing-dependent plasticity (STDP) relates this modification to the time difference between incoming pre- and postsynaptic action potentials,[13-16] which allows to detect the coincidence of two or more input signals.[17,18] Various modifications as a function of pulse timing have been reported for different synapses.[19-21] For example, in hippocampal neurons, potentiation (increase) of the synaptic strength is observed when the post- follows the presynaptic pulse, while depression (decrease) occurs when the pre- follows the postsynaptic pulse (asymmetric Hebbian learning).[16] This functionality can be successfully emulated with memristors[4,22-26] and, empirically, it is described with exponential functions.[14,27] Depending on the synapse type (excitatory or inhibitory), potentiation and depression can also occur for a reversed order of the pre- and postsynaptic pulses (asymmetric anti-Hebbian learning). The symmetric Hebbian and symmetric anti-Hebbian learning rules allow potentiation or depression to occur irrespectively of the relative timing of pre- and postsynaptic pulses.[19] Recently, it was found that pattern completion in network models is most effective for symmetric learning rules.[28] The different types of learning essentially depend on the synapse type and/or the computational task. Hence, the symmetric and asymmetric learning rules are beneficial for pattern completion and the recalling and storing of temporal sequences of action potentials, respectively.[28,29] The four different learning rules were artificially emulated by varying electrical input signals in chalcogenide[23,30,31] and metal oxide memristors[32], and by varying optical input signals of metal-sulphide microfibers.[33]

We present the emulation of four learning rules with a quantum dot memristor where the conductance change corresponds to charge transfer between quantum dots (QDs) and a two-dimensional electron gas (2-DEG). The localized charge in the QDs can be controlled by tuning shapes, magnitudes and timing of voltage pulses. The large ratio of maximum to minimum conductance of 57000 at zero bias voltage provides high sensitivity and efficiency and allows reducing the relative effects of undesirable readout noise. A model describing the device performance and the charging and discharging processes when applying pulses within a critical voltage and time window is introduced. Hence, the conductance modification can be correlated to device parameters such as gate efficiencies and critical voltages for charging and discharging.

II. DEVICE CHARACTERISTICS

An electron microscope image of the device with the corresponding circuit diagram is shown in Fig. 1(a). A GaAs/AlGaAs heterostructure is grown by molecular beam epitaxy with site-controlled QDs positioned in a narrow channel. A detailed description of the fabrication techniques is given in Ref. 34. Short circuiting the drain contact with lateral gates provides the memristive operation.[35-37] The pre- (V_{pr}) and postsynaptic (V_{po}) voltage pulses are applied to the drain and source contacts and emulate the input signals of pre- and postsynaptic neurons, respectively. A resistance with 1 MΩ is used in series to the channel and the measurements are conducted at 4.2 K in the dark. The current-voltage-characteristic in Fig. 1(b) shows a pinched hysteresis loop with memductances of $G_{\mathrm{h}} = 0.8$ and $G_{\mathrm{l}} = 1.4\mathrm{x}10^{-5}$ µS around zero bias voltage. The Coulomb interaction of localized electrons with the nearby wire leads to the memductance ratio of around 57000.[36] Thus the state variable of the present device corresponds to the amount of localized electrons.[38] For voltage differences between the two terminals $\Delta V = V_{\mathrm{pr}} - V_{\mathrm{po}}$ that exceed the threshold voltages for charging $V_{\mathrm{c}} \approx -1.9$ V and discharging $V_{\mathrm{d}} \approx 3.9$ V, the amount of charges is raised and lowered, respectively.[39] The switching between high and low conductances (see Fig. 1(b)) is comparable to other memristor realizations, e.g. the Al_2O_3/TiO_{2-x} memristors reported in Ref. 32. The steep current increase at V_d occurs due to a fast discharging mechanism, while below V_d the device operates in a slow discharging regime of the QDs. The two discharging regimes (above and below V_d) have different timescales and are beneficial to perform arithmetic operations in tunable bases with more gradual conductance changes occurring at voltage pulse slightly below V_d.[39]

III. PULSE SHAPE - DEPENDENT STDP

Fig. 1(c) shows the voltage pulses that are required and used to emulate the four learning rules and applied to the drain (red) and source (blue) contacts. The corresponding voltage differences between the pre- and postsynaptic pulses for positive time differences ($\Delta t_p > 0$) are illustrated in Fig. 1(d). For different shapes of the pulses, the threshold voltages for charging or discharging can be exceeded. Emulating asymmetric Hebbian and anti-Hebbian learning is realized with pulses consisting of a positive and a negative amplitude. Shapes with amplitudes of different polarities with respect to the resting potential (zero for the presented shapes) are also observed in biological systems.[40] The shape with positive and negative spikes allows controlling the voltage across the memristor solely by varying the time difference Δt_p between the pulses. Similar pulses were used to emulate asymmetric Hebbian learning with other memristor realizations.[26,30] Different pulse shapes are applied to investigate the emulation of input-dependent learning. Note that the pulses to mimic symmetric learning rules are symmetric in time, thus charging and discharging the QDs should not depend on the temporal order of the pulses, but on the absolute value of the time difference. The width of the pulses is 10 ms and the amplitudes are listed in Table 1. All pulse pairs are followed by a read-out pulse to determine the conductance of the device. The implementation of the learning rules with different pulse shapes is motivated by biological systems, where varying shapes carry information about stimulus history[41] or can be used to encode information[42] or to classify neurons.[43]

Fig. 2(a) shows the conductance G versus pulse number N for different Δt_p and the pulses that emulate asymmetric Hebbian learning (see Fig. 1(c)). Before the measurements, the system is set to the same initial conductance $G(N=0) = G_0 \approx 1.0\ \mu\mathrm{S}$ which corresponds to a specific amount n_0 of charges in the QDs. Tuning the time difference allows to increase or decrease the conductance by discharging the QDs for $\Delta t_\mathrm{p} = +2.4$ ms and charging the QDs for $\Delta t_\mathrm{p} = -4.0$ ms, respectively. In Fig. 1(d), the voltage difference for the considered pulses exceeds V_d for positive time difference leading to the discharging.[39] For negative time differences, $|\Delta V|$ exceeds $|V_\mathrm{c}|$.

Fig. 2(b) depicts the conductance versus N for different negative time differences and the same experimental configuration as in Fig. 2(a). The conductance after 10 pulses is lower for larger time differences. Thus the state variable for $N = 10$ is controlled by the time difference between pre- and postsynaptic pulses. During programming (QD charging for negative time difference), the voltage difference across the memristor controls the maximum number of localized electrons in the QDs. In the range between -4.4 and -2.0 ms, the minimum value of ΔV is lowered for larger time differences and consequently more electrons can be localized. The conductance after 10 pulses, G_{10}, as a function of the time difference is illustrated in Fig. 2(c). Within a critical range, G_{10} is strongly influenced by the time difference. After the application of 10 pulses with $\Delta t_\mathrm{p} < -2.5$ ms, the conductance is non-zero and varying time differences allow programming different memductance states, which may be exploited to realize multilevel memories.[44,45] The horizontal lines in Fig. 2(c) indicate eight different states that can be programmed solely by tuning the time difference between pre- and postsynaptic pulses in step sizes of

0.2 ms. The data in Fig. 2(a) shows that intermediate values can also be realized leading to the storage of more than eight levels.

Fig. 3(a) displays the relative conductance change $\Delta G = (G_1 - G_0) / G_0$ under the asymmetric Hebbian learning configuration (see Fig. 1(c)) corresponding to the data in Fig. 2(a), with G_1 being the conductance after the first pulse. For a pulse separation of more than five milliseconds, the relative conductance change is zero. Note that the critical time window for conductance modifications ranges from -4 to +2 ms. For small $|\Delta t_p|$, G is enhanced for positive and lowered for negative time differences. An inversion of the voltage pulses in combination with larger negative amplitude of the presynaptic pulse of -2.8 V corresponds to the asymmetric anti-Hebbian learning configuration (see Fig. 1(c)) and leads to positive and negative values of ΔG for $\Delta t_p < 0$ and $\Delta t_p > 0$, respectively, as depicted in Fig. 3(b). The voltage difference across the device for positive Δt_p is displayed in Fig. 1(d) and, under the asymmetric anti-Hebbian learning configuration, exceeds the threshold voltage for charging. In turn, for negative time differences (not shown in Fig. 1 (d)), ΔV exceeds V_d.

So far, the ΔG vs Δt_p dependencies that emulate asymmetric learning rules show transitions from depression to potentiation when inverting the temporal order of the pulses. To mimic symmetric learning rules, which are independent on the temporal order (symmetric Hebbian and symmetric anti-Hebbian learning), time-symmetric pulses, as displayed in Fig. 1(c), are applied. The relative conductance change in Fig. 3(c) is positive around zero and negative for large values of $|\Delta t_p|$. Thus, the conductance change depends exclusively on the time difference between the pulses and not on the order of their arrival. In neuroscience, comparable observations of the synaptic strength versus Δt_p are described by the symmetric Hebbian learning rule and were observed in GABAergic synapses.[46] In turn, applying the pulses sketched in the inset of Fig. 3(d), the relative conductance change is negative for small time differences and zero for large magnitudes of Δt_{p}.

The amplitudes of the voltage pulses in Fig. 1(c) are tuned in a way to realize large absolute conductance changes for small time differences. This enables the emulation of fast learning processes (only small amounts of repetitions are required to enhance the conductance). To emulate more subtle changes of synaptic strength, the voltage difference between the two pulses can be tuned slightly above or below the threshold voltages for charging and discharging, which allows the gradual increase or decrease of the conductance under a sequence of hundreds of pulses. With the experimental results presented in Fig. 3, the device is suitable to emulate different learning rules in dependence on the input signals (stimulus). The electronic properties of the device further allow simulating the signal transduction governed by the QD charge in a comprehensive way.

IV. MODELLING OF LEARNING RULES

Applying the voltage difference ΔV to the memristor, the current can be determined within the Landauer-Büttiker formalism that assumes

$$I(\Delta V) = \frac{e}{2\pi}\int_{-\infty}^{\infty} v_n\left[H(v_n) f_{FD}\left(E, \mu_{pr}\right) + H(-v_n) f_{FD}\left(E, \mu_{po}\right)\right] dk, \tag{1}$$

with $\mu_{pr} - \mu_{po} = e\Delta V, v_n = 1/\hbar(\partial E/\partial k)$, the elementary charge e, the Fermi-Dirac-distribution f_{FD}, the step function H, and $E = E^0 + \frac{\hbar^2 k^2}{2m^*}$, where k denotes the electron wave vector, and m^* is the electron effective mass. In the limit of low voltage differences, $\mu_{pr} \approx \mu_{po} \equiv \mu$, the current for the electrical configuration in Fig. 1(a) can be approximated by

$$I = \frac{e^2}{2\pi\hbar} f_{FD}(E_i, \mu)(\Delta V - I \cdot R). \tag{2}$$

Thus, the conductance is reduced to

$$G(n,\mu)=\frac{\left(\exp\left[\frac{E_i(n)-\mu}{kT}\right]+1\right)^{-1}}{1+R\frac{e^2}{2\pi\hbar}\left(\exp\left[\frac{E_i(n)-\mu}{kT}\right]+1\right)^{-1}}. \tag{3}$$

T is the temperature and R the resistance in series with the wire. The transverse subband energies $E_i(n)=E_i^0+\gamma n+\eta\Delta V$ are determined by the efficiencies γ and η, and by the number, n, of electrons in the QDs. The rate equation determining the QD charge is given by

$$\frac{dn}{dt}=\begin{cases}-\alpha_c\Delta V & for\ \ \Delta V<V_c<0\\ -\alpha_d\Delta Vn & for\ \ \Delta V>V_d>0\end{cases}. \tag{4}$$

Here α_c and α_d are the efficiencies that control the QD charging and discharging, respectively. These efficiencies depend on device parameters as the gate wire distance and the tunneling distance.[47,48] Thus when the QDs become charged, starting from an initial charge n_0, the number of electrons is determined by

$$n=n_0-\alpha_c\int(\Delta V-V_c)dt, \tag{5}$$

according to the first line of Eq. (4). For discharging processes, the number of localized electrons follows from the second line of Eq. (4) with

$$n=n_0\exp[-\alpha_d\int(\Delta V-V_d)dt]. \tag{6}$$

The QD-localized charge is mainly governed by the shape of the applied pulses. Note that the active part of pulse combination that controls either the charging or discharging in Eqs. (5) and (6) is determined by the pulse action defined as $S_{c(d)}=\int\left(\Delta V\left(\Delta t_p\right)-V_{c(d)}\right)dt$, corresponding to the shaded areas in Fig. 1(d).

The theoretical relative conductance change as a function of Δt_p is displayed in Fig. 4. The four panels are arranged in the same sequence as Fig. 3 and are obtained by using exactly the same input pulses as in the experiments. Simulations with the pulses shown in Fig. 1(c) lead to ΔG vs Δt_p dependencies that enable the emulation of asymmetric Hebbian learning in Fig. 4(a), asymmetric anti-Hebbian learning in Fig. 4(b), symmetric Hebbian learning in Fig. 4(c), and symmetric anti-Hebbian learning in Fig. 4(d). Note in Figs. 4(a) and (b) that the model predicts non-zero relative conductance changes for $|\Delta t_p|>5$ ms. Here, the presynaptic pulse is sufficient to charge the QDs, because its amplitude exceeds $|V_c|$. In Fig. 4(c), the limit $\Delta G \rightarrow -1$ for large $|\Delta t_p|$ corresponds to totally charged QDs which reduces G_1 to zero. The slight asymmetry of positive ΔG, when inverting the temporal order, is explained by the non-commutativity of charging and discharging in Eq. (4). This is also evident in the experimental results (see Fig. 3 (c)). The asymmetry of the ΔG-vs-Δt_p-curve in Fig. 4(c) with respect to Δt_p originates from the asymmetry of the charging and discharging processes due to their different time scales. In Fig. 3(c), both charging and discharging processes occur within a single pulse sequence, which, due to their non-commutativity, leads to slight asymmetric ΔG-vs-Δt_p-curves with respect to Δt_p.

Modelling the device performance for different α_c allows correlating the conductance change to the device layout. Smaller efficiencies for charging can be realized by increasing the tunneling distance or the gate wire distance. The ΔG vs Δt_p dependencies in Fig. 4 show that charging is boosted for enhanced α_c, leading to larger time intervals for charging. In addition, the time window for discharging in Fig. 4(c) is reduced for enhanced α_c. Thus, tuning the device geometry, e.g. the gate wire distance, enables control of the time windows for conductance modifications, which may be beneficial to realize artificial synapses with different sensitivities regarding time difference. For small gate wire distances, the conductance can only be tuned within a narrow time window allowing the implementation of high specialization and selectivity. Larger gate wire distances lead to broader time windows for learning and hence a large spectrum of time differences tunes the conductance.

The presented model further allows assessing the ΔG vs Δt_p dependence in terms of the pulse shapes. According to Eq. (3), the conductance can be expressed in general terms as $G(n) = [A \cdot exp(B \cdot n) + \rho]^{-1}$, thus $\Delta G(n) = A[exp(B \cdot n_0) - exp(B \cdot n)][A \cdot exp(B \cdot n) + \rho]^{-1}$, where A, B and ρ are fixed parameters defined by the system configuration (e.g. subband energies, gate efficiencies, temperature). When discharging the QDs, in the limit of low values of *n*, ΔG can be approximated by

$$\Delta G(n, \Delta t_p) \rightarrow \Delta G_d(n, \Delta t_p) = \frac{AB}{A+\rho}(n_0 - n) = \frac{AB}{A+\rho}\left[1 - \exp\left(-\alpha_d S_d(\Delta t_p)\right)\right] > 0. \tag{7}$$

In turn, for charging, in the limit of large values of *n*, the relative conductance tends to

$$\Delta G(n, \Delta t_p) \rightarrow \Delta G_c(n, \Delta t_p) = \exp[B(n_0 - n)] - 1 = \exp\left(-B\alpha_c S_c(\Delta t_p)\right) - 1 < 0. \tag{8}$$

All the information of the pulse shape is contained in either S_c or S_d. For the pulse shapes used in this analysis, the pulse action for both charging and discharging can be well described up to second order in Δt_p as $\alpha_{c(d)} S_{c(d)} \sim \sum_{i=0}^{2} a_i \Delta t_p^i$. The experimental data in Fig. 3 are fitted according to the exponential laws obtained in Eq. (7), with $\frac{AB}{A+\rho} = 3$, and Eq. (8), for positive and negative values of ΔG, respectively. The expressions used for the corresponding pulse actions are listed in Table 2. Exponential ΔG vs Δt_p dependencies as observed in Figs. 3(a) and (b) were also determined in hippocampal neurons.[27,49] The expression used in Fig. 3(c) is comparable to the one used in Ref. 28 to empirically describe the symmetric Hebbian learning rule. Note in this case that according to Eq. (8), for $|\Delta t_p| \gg 0$, $\Delta G_c \rightarrow -1$. The small discrepancy with the experiment in this limit is ascribed to unavoidable leakage (partial discharge) during the charging process. The data in Fig. 3(d) is fitted according to one exponential function and represents the symmetric anti-Hebbian learning rule. The exponential fit functions include the actions S_d and S_c, in Eqs. (7) and (8) respectively, and hence explicitly relate the relative conductance changes with the pulse shapes.

V. DISCUSSION

The presented data demonstrate the ability to realize pulse shape - dependent learning rules based on the mature III-V-semiconductor platform. It is worth noting that the low operation temperature of the device corresponds to the small energetic confinement of the electrons in the QDs which is about 0.4 eV. Because of this confinement, the maximum operation temperature of the device is 165 K, as was reported in Ref. 36. Room temperature operation may be realized by tuning the material compositions of the QDs and the surrounding layers.[50] Hence for the desired room temperature operation, devices based on other material compositions (different Al contents etc.) need to be designed, fabricated and tested. However, the presented results are expected to be directly transferable. Pulse shape - dependent learning rules were also obtained in Refs. 30 and 31 with a chalcogenide memristor, which has the advantage of short time windows for learning. In contrast to the previous proposals, the presented device is based on the mature III-V semiconductor platform that enables optical conductance control with low power light pulses.[39] Thus the memductance state can be controlled either by optical or electrical pulses or by combinations of both, which allows the integration with photodetectors as sensory neurons. The conductance control is further sensitive to the wavelength of incoming light[51], which was also demonstrated with other memristors[52] and memcapacitors[53] and enables encoding information in the wavelength. For the present device, the light sensitivity leads to varying learning processes in the dark and under illumination, which is the key advantage compared to other memristor realization with large on/off ratios of up to 10^{12},[54] low switching times in the sub-nanosecond range[55] or high endurance (10^{12} cycles).[56] More complex functionalities as recognition and classification tasks were performed with memristor crossbars that offer high scalability.[57] Scalability of quantum wires as key element of the presented memristor was demonstrated with the realization of a full adder.[58]

In Ref. 39, the relative conductance change $\Delta G/G_0$ of the present device for the asymmetric Hebbian learning rule was found to be independent on G_0 for depression, but shows a maximum at medium G_0 conductance values for potentiation. A dependency of the learning rules on the initial conductance was also presented for an Al_2O_3/TiO_{2-x} memristor in Ref. 32. Finally, the present device allows controlling the time window for conductance modifications by tuning the device layout. In Eqs. (7) and (8), the relative conductance changes tend faster to zero for larger charging and discharging efficiencies, which may be exploited to realize artificial synapses for high specialization (narrow time window for learning) and basic learning (broader time window for learning).

VI. CONCLUSION

In summary, we are able to artificially emulate four learning rules of neural networks with a quantum dot memristor. Analogous to synaptic strength in neural networks, the conductance is controlled by changing the time difference between pre- and postsynaptic voltage pulses. The conductance of the device is tuned by localizing electrons in quantum dots, which depends sensitively on the shape, magnitude and timing of pre- and postsynaptic voltage pulses. The presented pulse shape - dependent learning rules may pave the way to the realization of activity-dependent learning with a single device in future artificial neural networks.

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Figure captions:

FIG. 1. (a) Electron microscope image of the memristor. The pre- and postsynaptic voltage pulses are applied to the drain and source contacts, respectively. The positions of the QDs are highlighted in yellow. (b) Current-voltage-characteristic of the memristor. A pinched hysteresis loop is observed. The QDs are charged and discharged when the voltage exceeds V_c and V_d, respectively. Inset: Zoom in of low conductance state around zero bias voltage. (c) Schemes of the pre- (red) and postsynaptic (blue) voltage pulses versus time. If the difference $\Delta V = V_{pr} – V_{po}$ in (d) exceeds V_c or V_d (see orange areas), the amount of localized charges is enhanced or reduced, respectively. The pulses from left to right are applied to investigate the emulation of asymmetric Hebbian, asymmetric anti-Hebbian, symmetric Hebbian and symmetric anti-Hebbian learning, respectively. (d) Voltage difference for the pulses in panel (c) and $\Delta t_p > 0$.

FIG. 2. (a) Conductance versus pulse number for various time differences and the pulse shapes to emulate asymmetric Hebbian learning in Fig. 1(c). Depending on the temporal order of the pulse, G can be enhanced or lowered. (b) G versus N for the same experimental setup as in (a) but different Δt_p. For varying time difference, the conductance after 10 pulses is changed. (c) Conductance after 10 pulses versus Δt_p. For $\Delta t_p < 2.5$ ms, the conductance depends sensitively on the time difference. The horizontal lines indicate eight different levels that may be stored by tuning Δt_p in step sizes of 0.2 ms.

FIG. 3. Relative conductance change versus Δt_p for the pulse shapes in Fig. 1(c). In each panel, the corresponding pulse shapes are sketched with red (V_{pr}) and blue (V_{po}) lines. The presented ΔG vs Δt_p dependencies allow the emulation of asymmetric Hebbian learning in (a), asymmetric anti-Hebbian learning in (b), symmetric Hebbian learning in (c), and symmetric anti-Hebbian learning in (d).

FIG. 4. Simulation of the relative conductance change versus time difference. The figure is arranged in analogy to Fig. 3. The corresponding pulse shapes for the panels (a) to (d) are shown from left to right in Fig. 1(c). Panels (a) and (b) show the asymmetric and (c) and (d) the symmetric learning rules. The resilience is investigated by tuning the efficiency for charging.

Learning rule	V_{pr} (V)	V_{po} (V)
Asymmetric Hebbian	-3.0, +4.2	-2.0, +2.0
Asymmetric anti-Hebbian	+4.2, -2.8	+2.0, -2.0
Symmetric Hebbian	-3.8, +3.8, -3.7	-2.0
Symmetric anti-Hebbian	-2.4	+2.4

Table 1: Amplitudes of the voltage pulses in Fig. 1(c). The positive and negative voltages correspond to the maximum and minimum values for increasing time, respectively.

Fig.	ΔG_d	ΔG_c
3(a)	$\alpha_d S_d = -0.17\Delta t_p^2 + 0.34\Delta t_p + 0.34$	$B\alpha_c S_c = -0.24\Delta t_p^2 - 0.864\Delta t_p + 0.9$
3(b)	$\alpha_d S_d = -0.08\Delta t_p^2 + 0.96$	$B\alpha_c S_c = -0.1\Delta t_p^2 + 0.18$
3(c)	$\alpha_d S_d = -0.2\Delta t_p^2 + 0.2$	$B\alpha_c S_c = -0.2\Delta t_p^2$
3(d)	---	$B\alpha_c S_c = -0.1\Delta t_p^2 + 0.65$

Table 2: Pulse actions used to fit the experimental data in Fig. 3.

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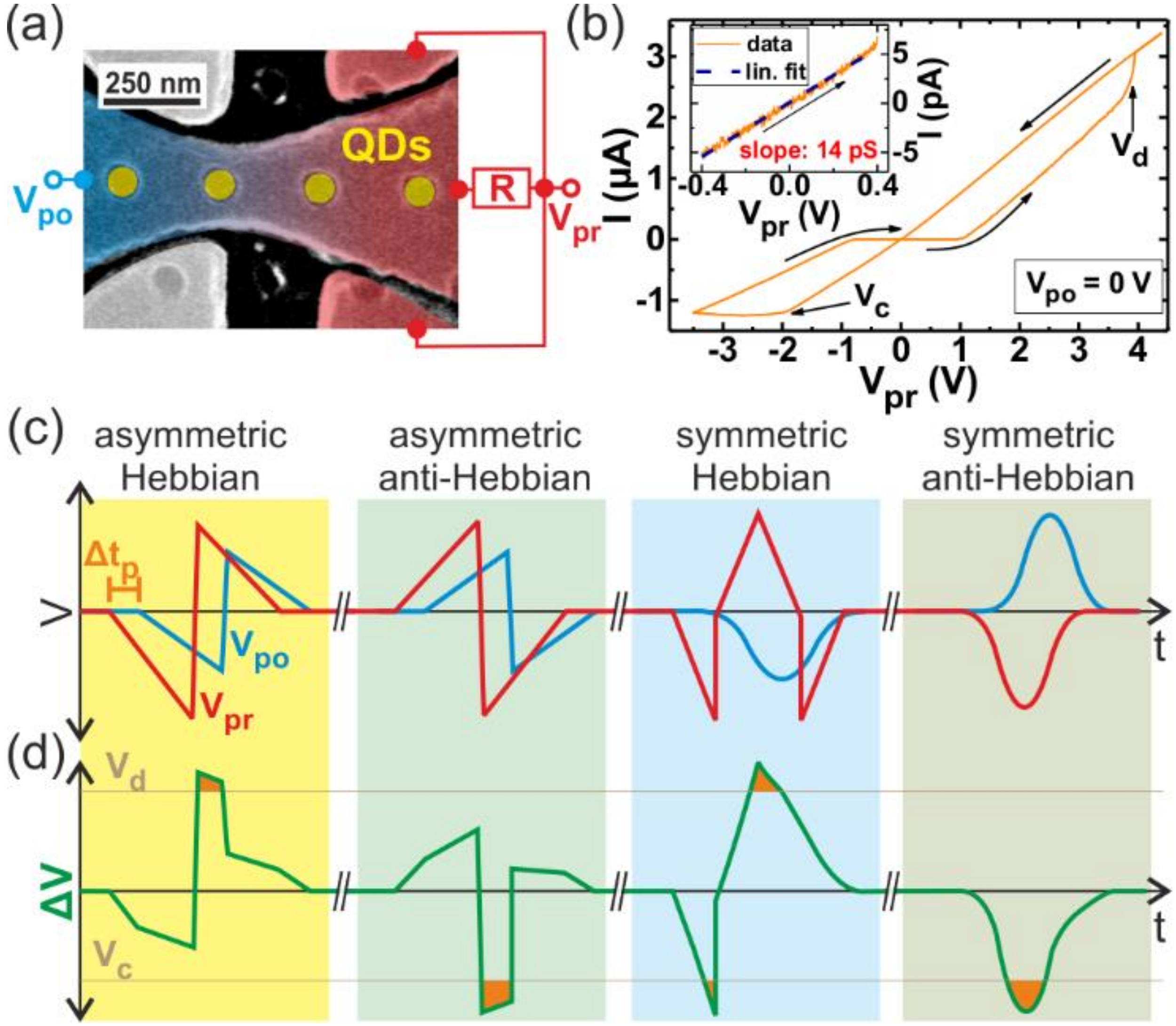
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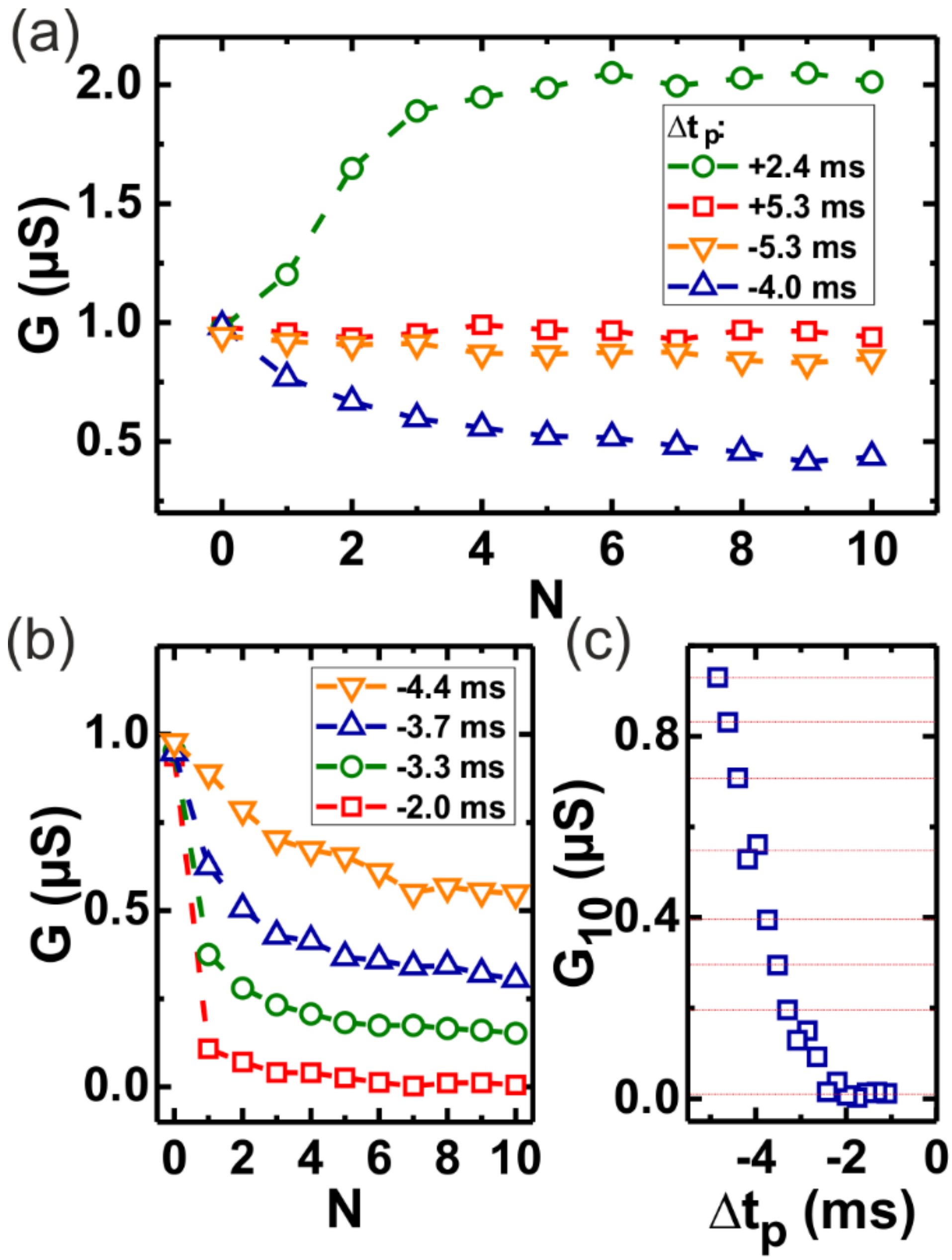(a)
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(b)
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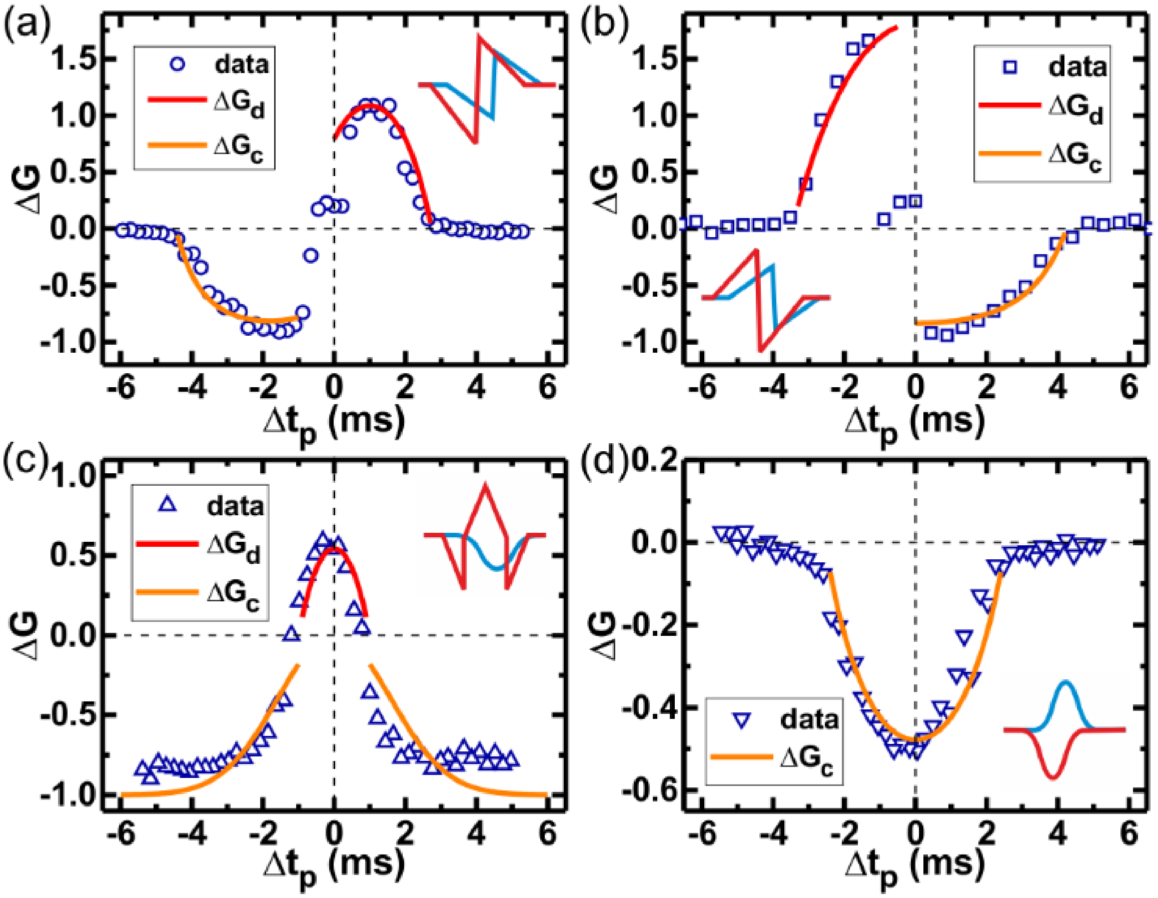
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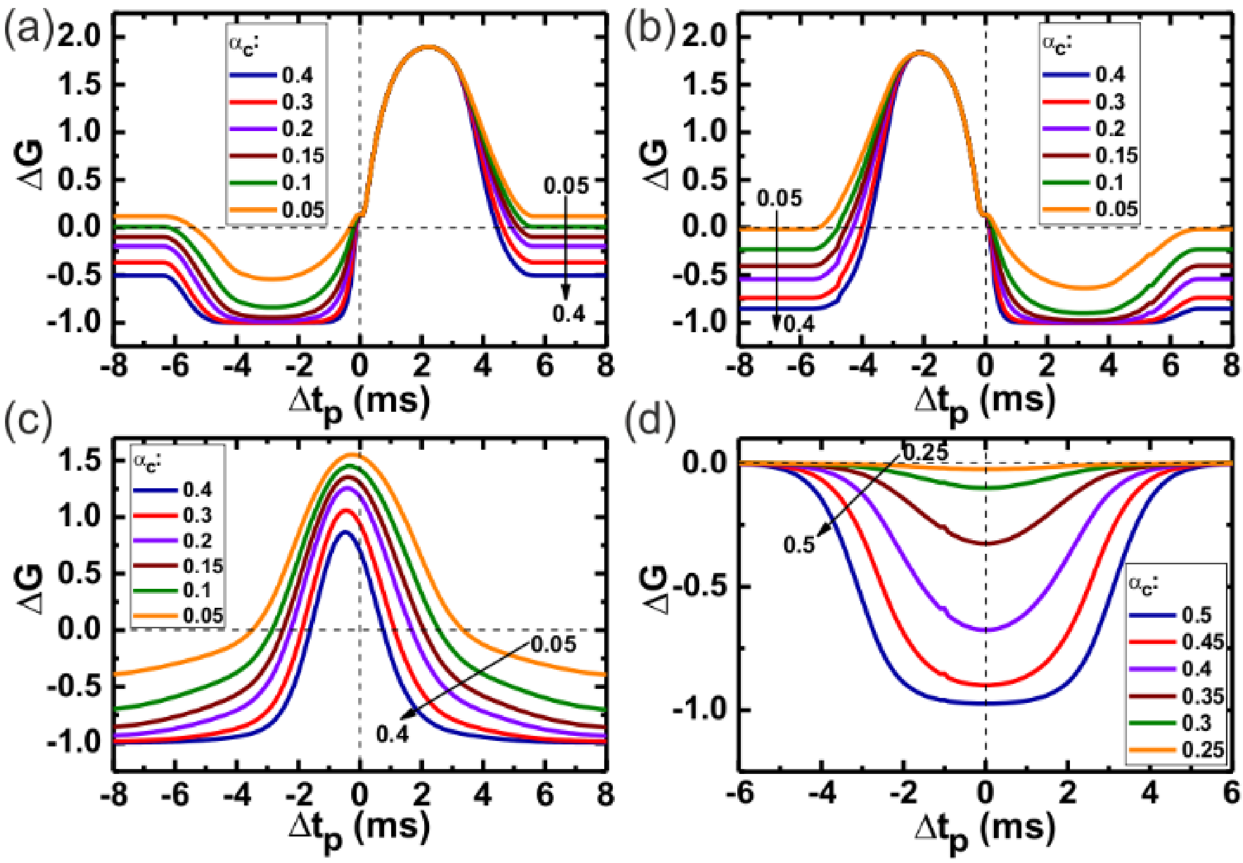
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