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Introduction

The static induction transistor (SIT) was invented by Professor Junichi Nishizawa of Tohoku University in 1950. One of the main advantages of the SIT device is its high speed switching characteristics. Since no carriers are injected from the gate, switching can be performed at an extremely high speed (without storage effects) and a small gate resistance (r_g) is used for minimum high frequency signal loss. SITs have high input impedance and are voltage controlled devices, and therefore only a low drive power is required at the gate. SiC has very high voltage breakdown (2MV/cm), thermal conductivity (4.8W/cm-K), and saturation velocity ($2x10^7$ cm/s) compared to Si devices. Thus, SiC SITs are highly suited for high power applications (Lostetter, 2003).

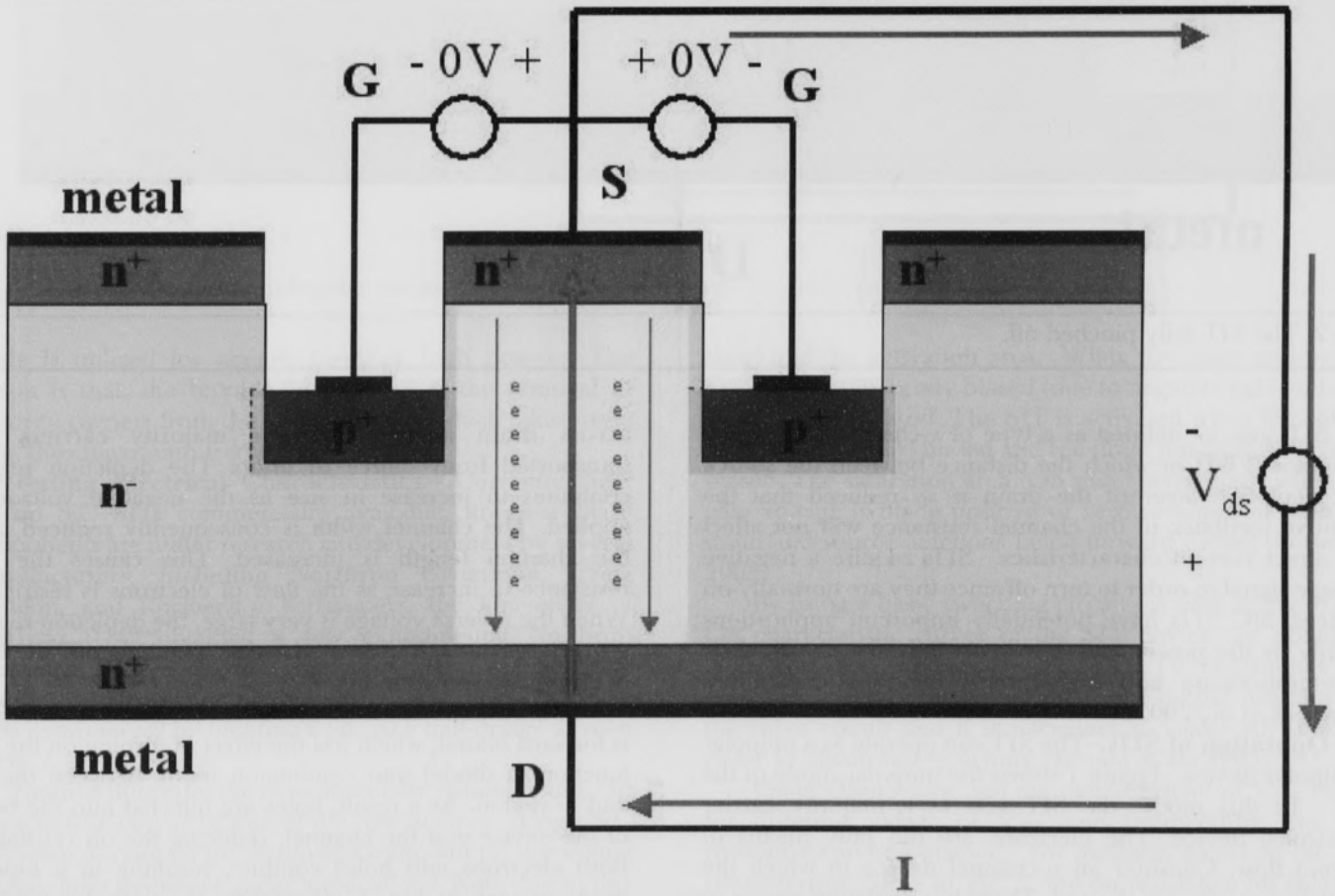

Fig. 1. The SIT operating in a unipolar forward conduction mode.

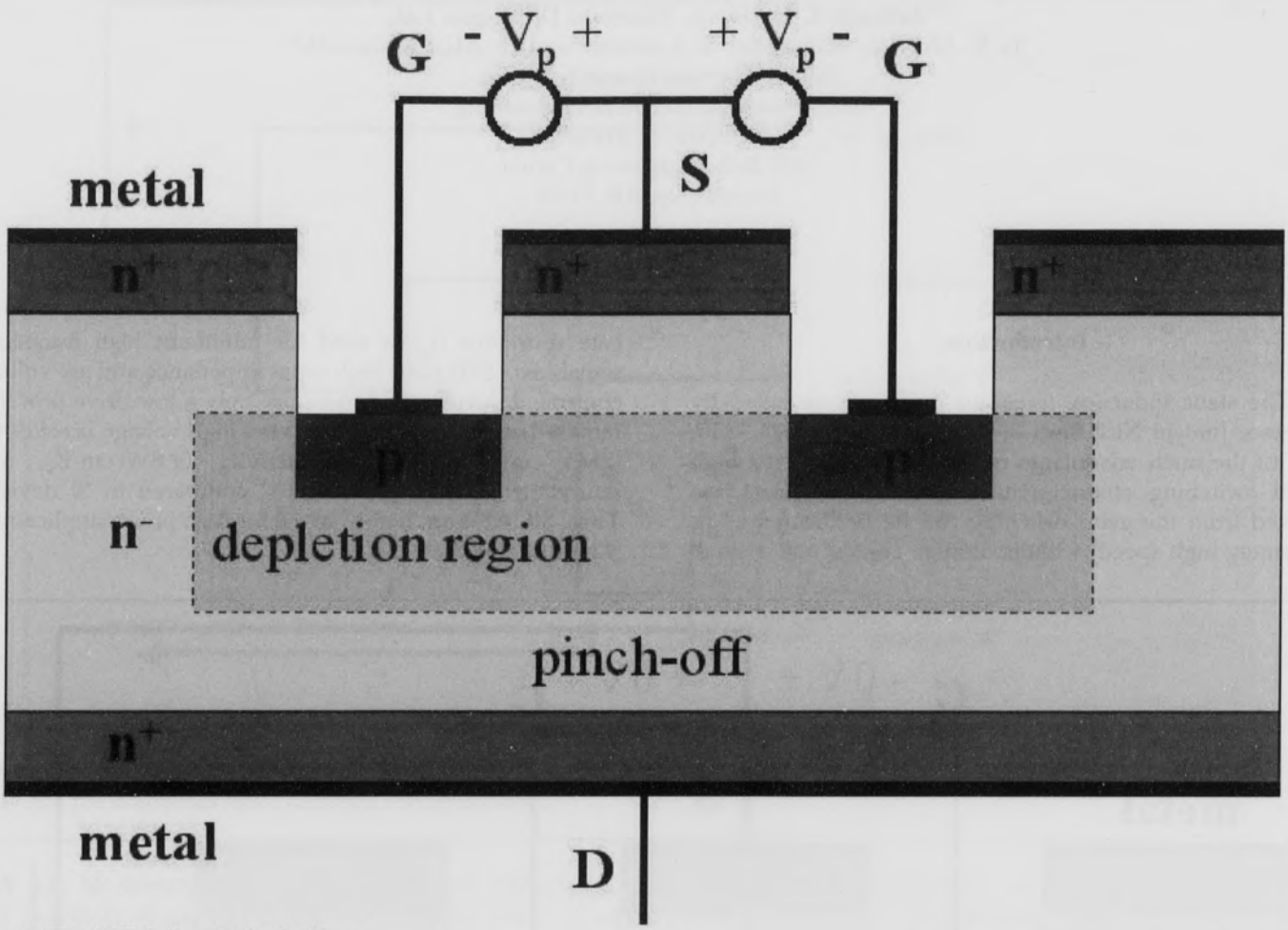

Fig. 2. The SIT fully pinched-off.

SITs can be defined as a type of v-channel field effect transistor (FET) in which the distance between the source and depletion layer of the drain is so reduced that the negative feedback of the channel resistance will not affect the direct current characteristics. SITs require a negative voltage signal in order to turn off since they are normally-on devices. SiC SITs have potentially important applications mainly in the power and aerospace industry due to their high-temperature and high-current handling capabilities (Neudeck et al., 2002).

Operation of SITs.--The SIT can operate as a unipolar or bipolar device. Figure 1 shows the unipolar mode of the SIT. In this mode, the SIT acts as a majority carrier (electrons) device. The electrons are the only means of current flow. Consider an n-channel device in which the drain and source are shorted. There is a depletion region in the gate-source interface and when a voltage is applied across drain and source, the majority carriers are transported from source to drain. The depletion region continues to increase in size as the negative voltage is applied. The channel width is consequently reduced, and the channel length is increased. This causes the on-resistance to increase as the flow of electrons is restricted. When the reverse voltage is very large, the depletion region grows large enough to meet, thereby "pinching off" the flow of current as shown in Fig. 2.

In the bipolar mode of operation, the gate-source region is forward biased, which has the effect of turning on the p-n junction (a diode) into conduction mode between the p^+ and n- region. As a result, holes are injected into the body of the device and the channel, reducing the on resistance. Both electrons and holes conduct, resulting in a bipolar mode as seen in Fig. 3. Generally, the unipolar mode is used for high frequency applications whereas the bipolar

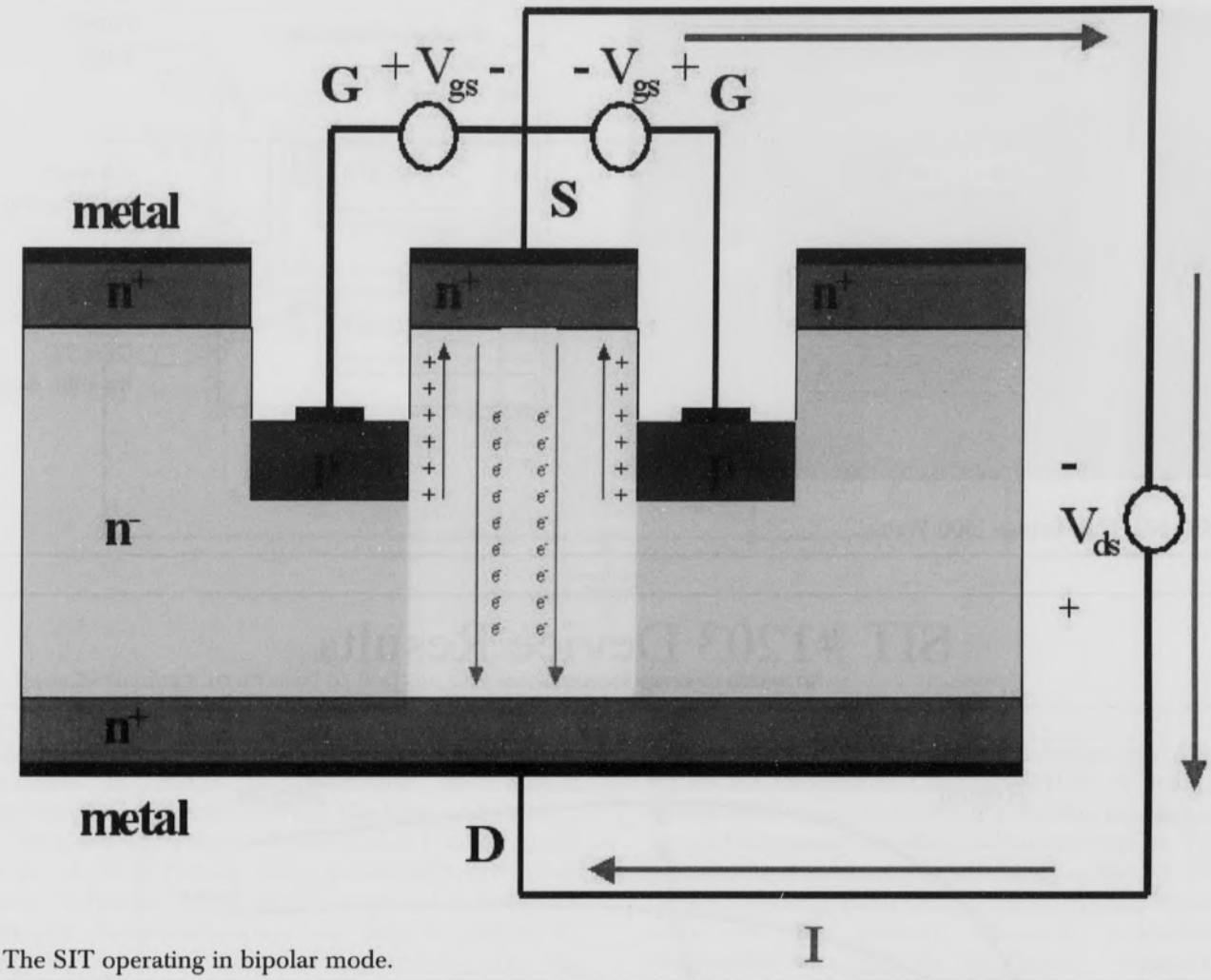

Fig. 3. The SIT operating in bipolar mode.

mode is utilized for circuits handling high power. The reason is that, the bipolar mode requires the removal of minority carriers from the bulk substrate, which takes more time, thus maximum frequency is reduced.

Testing Electrical Characteristics.-- Currently there are no SiC SITs commercially available, however these components are under research and development by several manufacturers, including Northrop Grumman, Cree, Infineon, and Rockwell. Fortunately, the University of Arkansas (UA) obtained a few experimental Northrop Grumman static induction transistors and Cree Schottky diodes. The UA Silicon Carbide group has begun to utilize these components by building a SiC SIT half-bridge as seen in Fig. 4.

Figure 5 illustrates the experimentally obtained turn-On characteristic curves of one of the SIT devices. These SiC SITs were developed by Northrop Grumman for use in low voltage, high frequency radar applications. Note that in this figure the transition region consists of the cut-off area (Off state) and the activation area. When the drain and source junctions are inversely biased (due to negative gate voltage), the SIT device is off. The SIT is activated when the source junction is forward biased and the drain junction is reversed biased. The saturation area (On state) takes place when the gate voltage is made positive or zero resulting in both the drain and source junctions being forward biased (Lostetter, 2003).

By using a basic switching circuit (as seen in Fig. 6) the On characteristic curves of the SIT device are obtained. Note that the driving circuit in Fig. 6 determines the switching speed of the circuit. RS is the output resistance in the drive circuit and it is necessary to make RS small in order to obtain fast switching (Tatsuta et al., 1995).

Using Ohm's Law and the measurement of V_{DS} vs. ID for different values of V_{GS} and temperature, the on-resistance can be obtained. For instance, based on the ON characteristic curve in Fig. 5, the on-resistance for this SIT device at room temperature will be 2Ω. Theoretically, the

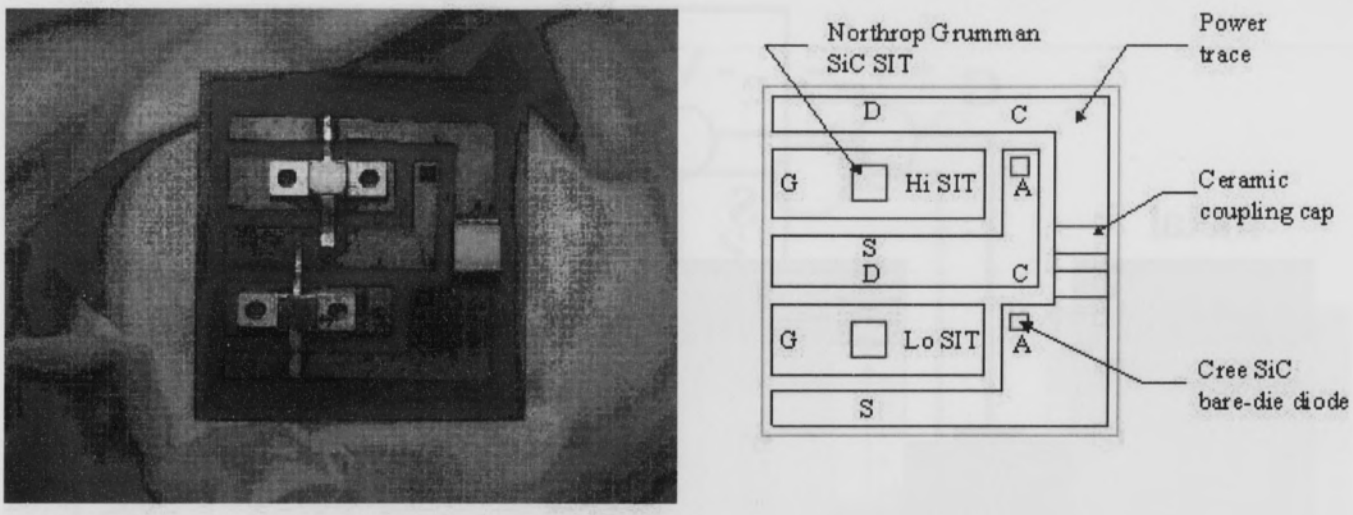

Fig. 4. SiC SIT Half-Bridge (500 Watts).

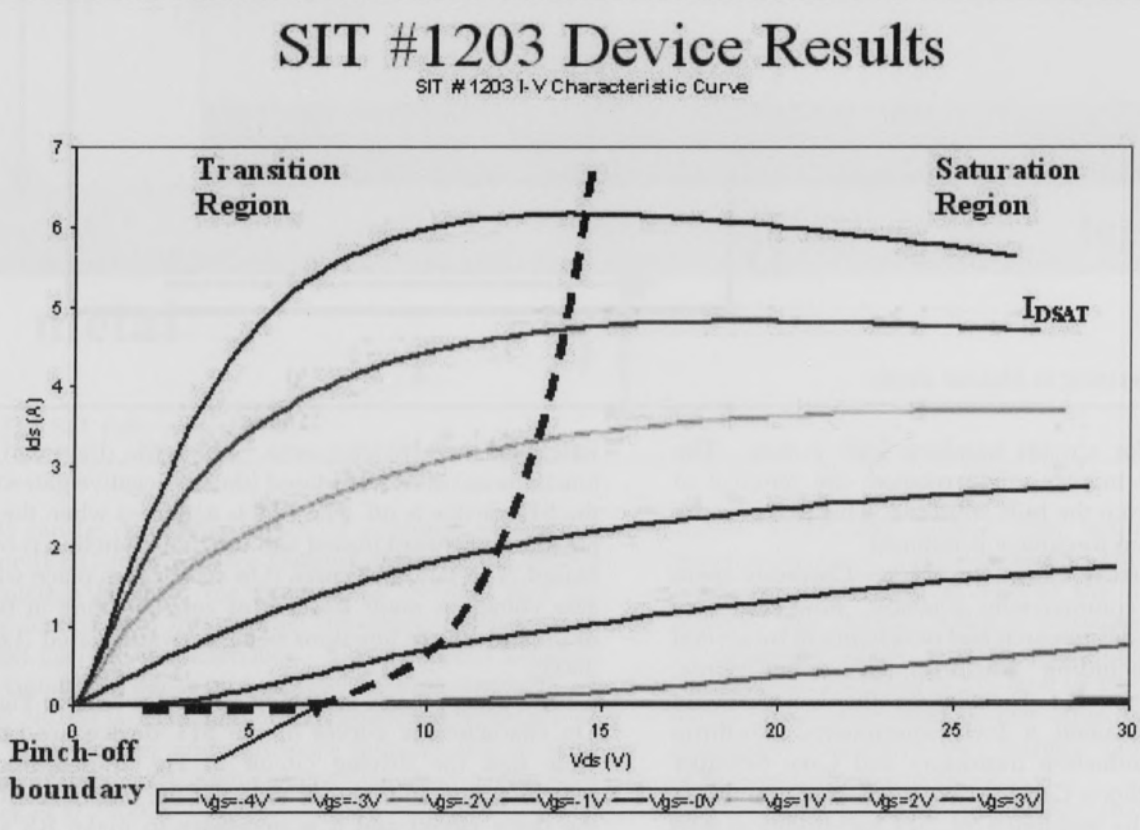

Fig. 5. SIT #1203 I-V ON characteristic curve.

on resistance will go down as temperature increases because of the negative current/temperature characteristics.

The voltage amplification ratio (μ) is the ratio of the potential change of V_{DS} and V_{GS}.

$$\mu = \left| \frac{V_{DS}}{V_{GS}} \right|$$

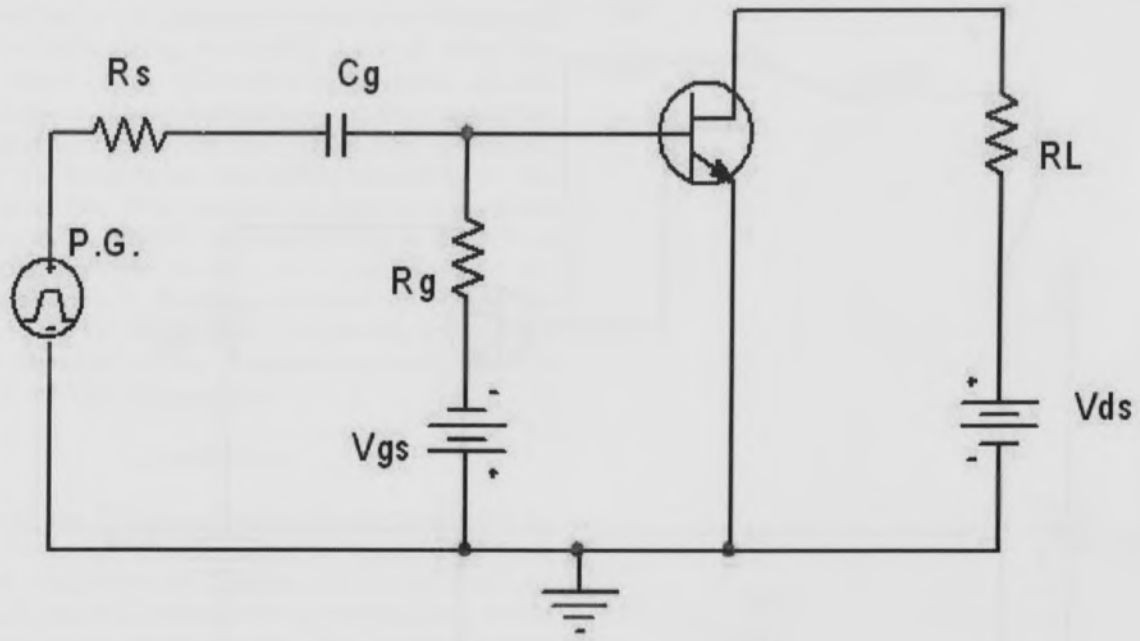

Fig. 6. Basic Switching Circuit used to find the ON resistance of the SIT.

Another basic circuit, as seen in Fig. 7, is under construction in order to determine the mutual transconductance of the SIT device. The drain current, I_{D1}, can be obtained when Switch 1 is placed at Position 1, and Switch 2 is placed in Position 2; I_{D2} is obtained when Switch 1 is placed at Position 2, and Switch 2 is placed at Position 1. The mutual transconductance can then be found by applying the measured values of I_{D1} and I_{D2} into the following formula:

$$g_m = \frac{I_{D1} - I_{D2}}{\Delta V_{GS}}$$

The SIT's response time (that is, delay time, rise time, storage time, and fall time) can be obtained by examining the measured input current and voltage versus the output. The delayed time is the time required for the output to reach 10% of the maximum amplitude starting at the time of the application of the input pulse. The rise time is the time required for the output to go from 10% to 90% of the maximum amplitude. The storage time is the time required for the output to decrease to 90% of the maximum amplitude after the input pulse disappears. Finally, the fall time is the time required for the output to decrease from 90% to 10% of the maximum amplitude.

Modeling Characteristics.--Given the increasing popularity of SiC devices, compact circuit simulation models are in great demand so that commercial simulators can include them in their model libraries. The MSCAD Laboratory at the University of Arkansas uses the MAST Hardware Description Language (HDL) (Vlach., 1992) to model these devices. MAST is a flexible language that can be used to generate excellent behavioral models. The model parameters and means of extraction for the SiC SITs have been identified (Scozzie et al., 1994). As stated previously, some of the primary electrical parameters are transconductance (g_m), the drain/source saturation current (I_{DSS}), the threshold voltage (V_t), the lumped resistance parameter (r_s), gate-source junction capacitance at zero bias (c_{gs}), and gate-drain junction capacitance at zero bias (c_{gd}). The term gm is defined as the maximum transconductance at zero gate voltage and uses a value of I_{DSS} that is the average of the current in the saturation region of the device for zero gate voltage. Figure 8 shows the equivalent circuit for the SIT model that can be used for analyses. V_t was extracted from the data using the square-root of the I_D vs. V_{GS} curve, in which the slope of the curve is extrapolated to the x-axis, and V_t is defined as the intercept. V_t is the externally applied voltage to achieve pinch-off. The lumped resistance parameter (r_s) will be modeled using the EMPEROR technique (Wen et al., 1992). The characteristic equations that are used to model the SIT are as follows:

Cut-off region $(V_{GS}-V_{to} \le 0) : i_d = 0$

Linear region $(0<V_{DS}<V_{GS}-V_{to}): i_d = g_{ml} V_{DS} * [2(V_{GS}-V_{to})-V_{DS}]$

Saturation region $(0< V_{GS}-V_{to} \le V_{DS}): i_d = g_{ms} * [V_{GS}-V_{to}]2 * [1+ \zeta V_{DS}]$

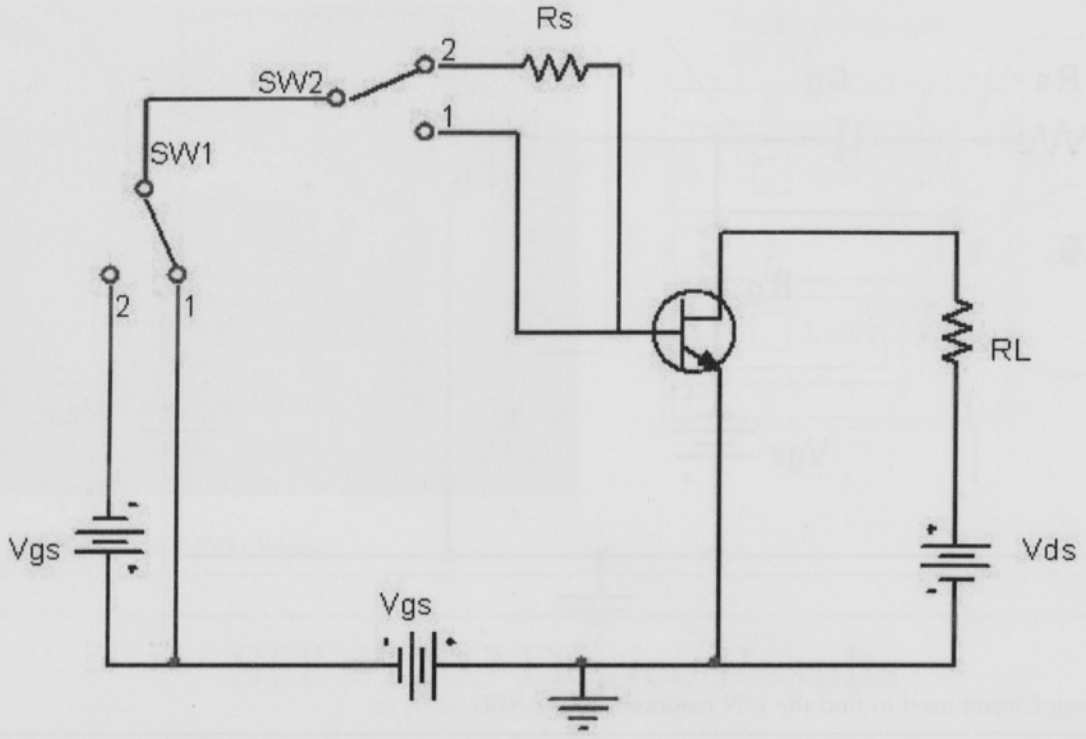

Fig. 7. Basic switching circuit used to find the mutual transconductance of the SIT.

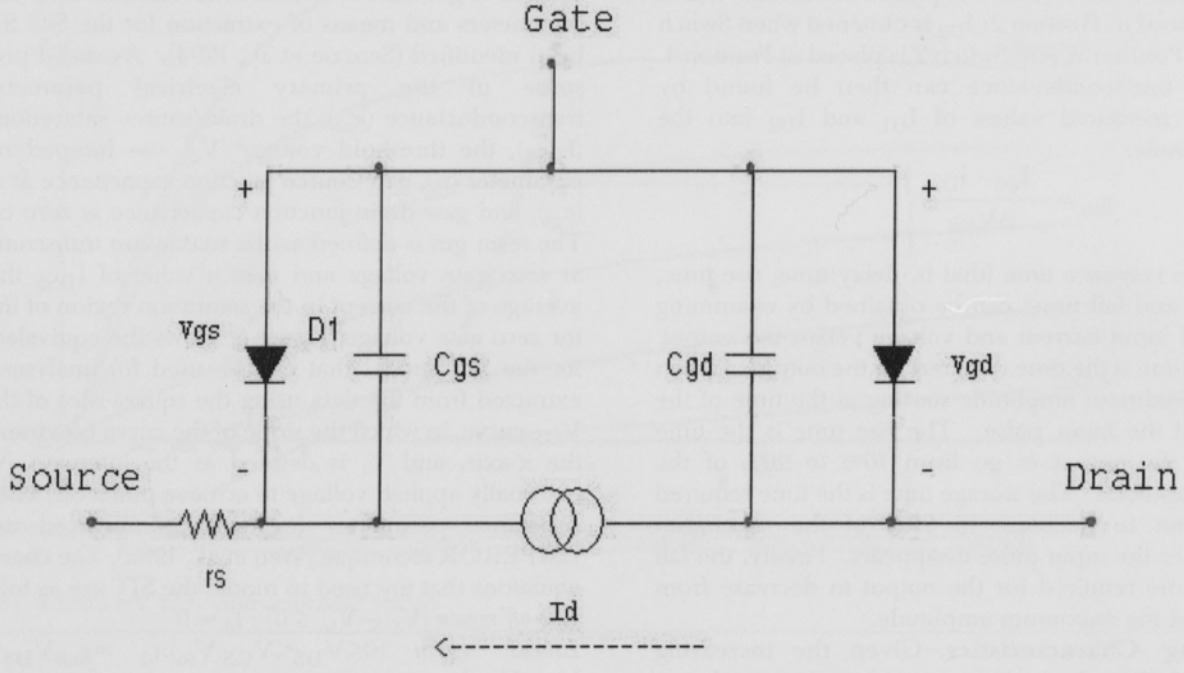

Fig. 8. Equivalent circuit for the SIT model.

where ζ is the pinch-off parameter that has been introduced in the model, for modeling the the SIT pinch-off effect. The transconductance of the SITs varies at the active and the saturation regions. These parameters and their extraction aid in making a robust model that can be used extensively in simulators. Temperature dependent modeling is also needed, since the SITs operate at high temperatures (theoretically up to 600°C). Repeated testing of the SITs at room temperature has already been performed at the MSCAD Laboratory. High-temperature study will be carried out at the HiDEC facility. The models will then be validated with actual device measurements with the SITs provided by the UA collaborators.

Conclusions

Currently, the SiC research that is being performed by the UA is increasingly demonstrating the versatility of these wide band gap devices. Before SiC SITs can be commercially launched, issues such as modeling and device physics need to be demonstrated. The characterization study currently under investigation has shown the excellent power density handling capabilities of these devices. The model of the SIT under development will be a very useful tool for power electronic circuit designers.

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