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Journal of the Arkansas Academy of Science

Volume 57 Article 23

2003

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Speer, Kevin M.; McNutt, Ty R.; Lostetter, Alexander B.; Mantooth, H. Alan; and Olejniczak, Kraig J. (2003) "Novel High Frequency Silicon Carbide Static Induction Transistor-Based Test-Bed for the Acquisition of SiC Power Device Reverse Recovery Characteristics," *Journal of the Arkansas Academy of Science*: Vol. 57 , Article 23.
Available at: http://scholarworks.uark.edu/jaas/vol57/iss1/23

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A Novel High Frequency Silicon Carbide Static Induction Transistor-Based Test-Bed for the Acquisition of SiC Power Device Reverse Recovery Characteristics

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Abstract

A test system is presented that utilizes a high-frequency Silicon Carbide (SiC) Static Induction Transistor (SIT) in place of the traditional MOSFET to test reverse recovery characteristics for the new class of SiC power diodes. An easily implementable drive circuit is presented that can drive the high-frequency SIT. The SiC SIT is also compared to a commonly used Si MOSFET in the test circuit application.

Introduction

In this paper, a high-speed reverse recovery test system is developed that offers ease of implementation and well-characterized components and parasitic phenomena. The system is specifically designed for the characterization of high-speed SiC power diodes; this characterization is done by emulating a wide range of application conditions by independently controlling the applied diode voltage, forward diode current, di_D/dt, and dv_D/dt at turn-off. By emulating such a wide range of application conditions, the system is very useful in characterizing the power diode's forward and reverse recovery phenomena, thus providing a controlled environment of known parameters for conducting parameter extraction for compact model development. The system further demonstrates its value by providing a means of model validation, the final step in model development (McNutt et al., 2002).

SiC PiN diodes have demonstrated reverse recovery times of 6 ns (McNutt et al., 2001; Hefner et al., 2001), and the SiC Schottky and Merged Pin Schottky (MPS) rectifiers have demonstrated even faster switching times than PiN rectifiers due to the unipolar nature of their operation range (Hefner et al., 2000). Due to the advantageous electrical properties of SiC, SiC diodes are orders of magnitude faster than application-comparable Si diodes; thus, a new test circuit was developed that can stress the SiC diodes (McNutt et al., 2002). As such, the SIT is a noteworthy candidate for the semiconductor switch in the high-speed reverse recovery test circuit shown in Fig. 1. The SIT has a lower parasitic capacitance and a faster switching speed than the conventionally-utilized power MOSFET. The primary reason for using a SIT is the aforementioned increase in switching speed; however, another amenity is the SIT's superior voltage blocking capability that legitimizes its use in high power applications, making it an ideal switch for the acquisition of reverse recovery characteristics of SiC diodes.

Methods

Circuit Description.--Figure 1 illustrates the developed test-bed circuit for the acquisition of SiC power diode reverse recovery characteristics. It is important to note that the circuit is very well characterized, meaning that the electrical values of all circuit components and parasitic elements within the circuit are precisely known after independent measurements. The circuit of Fig. 1 would normally use a power MOSFET as the control switch, but the importance of the work described here is in the replacement of the control switch with a high frequency SiC transistor; in previous work (McNutt et al., 2001; Hefner et al., 2001; Hefner et al., 2000), a 6LF6 vacuum tube was

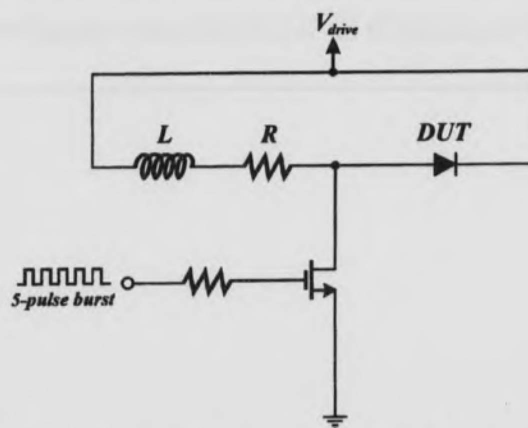

Fig. 1. Circuit diagram for the high-speed diode reverse recovery test system.

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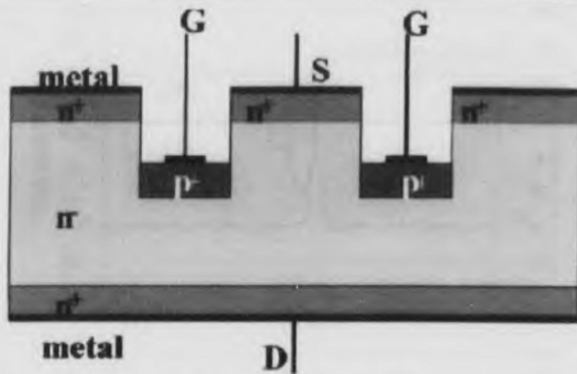

Fig. 2. Cross-section of a V-channel SIT.

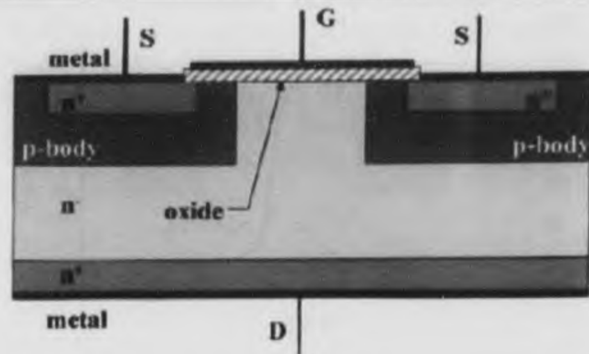

Fig. 3. Cross-section of a VDMOSFET.

substituted for the MOSFET switch to achieve low parasitic capacitance at the Device Under Test (DUT) anode as well as an extremely fast switching speed.

The implementation of such a vacuum tube control switch requires extensive knowledge of the design of the tube screen negative drive circuit, as well as requiring that the circuit be implemented between $-V_{drive}$ and 0 V. On the other hand, the three-terminal SIT only requires a function generator capable of providing a –10 V to 0 V gate-drive pulse with a variable rise/fall time.

The switch control signal used in the test-bed is a low-duty cycle, five-pulse burst, triggered by a 10 Hz pulse, thus enabling the use of the SIT for tests normally outside of its range of power operation. The five-pulse burst also reduces both DUT and switch self-heating, yielding characterization of device phenomena at the intended temperature; still further, the burst eliminates the need for power supplies that provide a large value of output current, as the output filter capacitance used to minimize the ac ripple can store a sufficient amount of charge to output adequate levels of current.

The test-bed itself allows for the performance of reverse recovery tests for various values of forward diode current, V_{drive}, di_D/dt, and dv_D/dt, where the value of forward diode current is controlled by the input pulse width to the gate drive circuit; di_D/dt is controlled by varying the value of the gate resistor; and dv_D/dt is controlled by placing various capacitors across the DUT. By independently controlling these parameters, the test circuit enables testing of the new SiC technology for the full range of application conditions: Varying the value of V_{drive} emulates the application conditions for circuits with different DC buss voltages; varying the value of di_D/dt emulates the application conditions of different speed anti-parallel switching devices; varying the value of dv_D/dt emulates the application conditions of using anti-parallel switching devices of different output capacitances; and for model parameter extraction purposes, varying the value of the forward diode current at turn-off aids in the determination of the portion of diode current that is due to emitter recombination and the portion that contributes to charge storage. In addition, variation of dv_D/dt aids in the determination of the portion of the diode recovery due to charge storage and the portion due to device capacitance.

Static Induction Transistor versus MOSFET.--A cross section of the 4H-SiC V-channel SIT used in this work is illustrated in Fig. 2. In this work, the SIT is operated in its unipolar region of operation (i.e., the gate p-n junctions do not become forward biased). The gate voltage controls the current flow through the means of depletion regions that extend from the gate junctions into the n-type channel, extending deeper as the magnitude of the negative gate-to-source voltage increases. When the depletion regions from both sides of the channel intersect, the device current is cutoff, at which point $V_{GS} = V_P$, the pinch-off voltage. The SIT is a normally ON device that is switched between –10 V and 0 V. Due to the device construction, it is commonly used in low voltage, high frequency applications, where parasitic device capacitances inhibit the turn-on/turn-off times of inferior switching devices. By keeping the duty cycle low in this application, the SIT is able to operate at these higher frequencies, thus providing the needed stress in testing the SiC diodes.

A typical VDMOSFET structure is shown in Fig. 3. High parasitic capacitances can be credited for severely limiting power MOSFETs' operation to frequencies well below those of the SITs: First, a capacitance can be seen in Figure 4 that results from overlapping areas of the gate and the source. Denoted C_{gs}, the capacitance is directly proportional to the gate-source overlap area, and thus is assumed to be constant. Secondly, and more influential to switching performance, the Miller capacitance between the gate and drain, C_{gd}, determines the gate and drain currents and the drain-to-source and gate-to-source voltages (Budihardjo et al., 1997). Lastly, the parasitic capacitance between the drain and source, C_{ds}, which is a combination of the gate oxide capacitance and the depletion layer capacitance beneath the gate, has negligible effect on

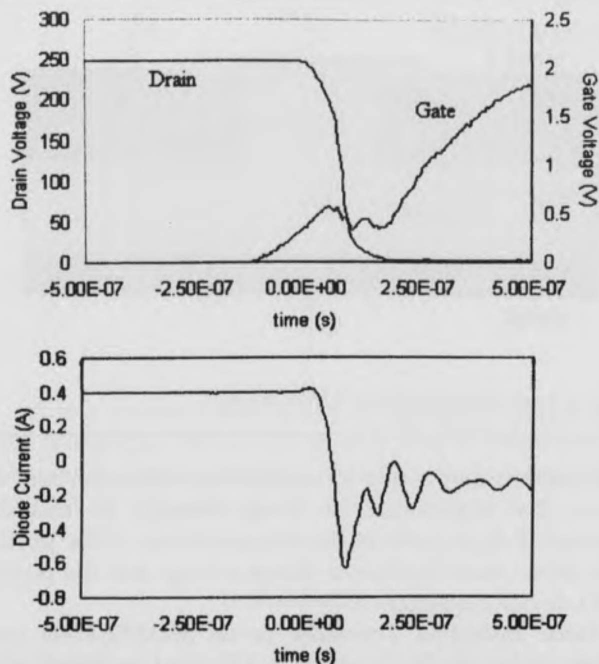

Fig. 4. Diode reverse recovery test with t_{rise}=400ns utilizing IF PG40 Si MOSFET.

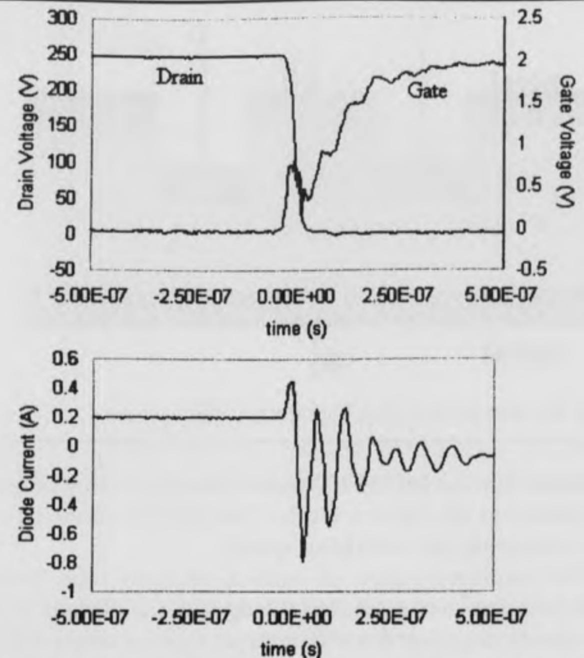

Fig. 5. Diode reverse recovery test utilizing IRF PG40 Si MOSFET with t_{rise}=5ns, demonstrating limits of MOSFET in high-speed test circuit.

switching characteristics (Mohan et al., 1995); in any event, the end result is that the combination of the larger parasitic capacitances of the MOSFET structure limits the device's switching time and thus makes the SIT the switching device of choice for high frequency applications.

SIT Test Circuit Results.--In Figs. 4, 5, and 6, an initial forward current is established in the diode before the diode is switched off by applying a constant negative di/dt with the control switch. The switch current increases linearly until the voltage reaches the voltage supply value, V_{drive}. Figure 4 and 5 illustrate the results of using a typical IRF820 Si MOSFET (International Rectifier, HEXFET Power MOSFET, Datasheet #PD-9.324O) in the test circuit of Fig. 1, and Fig. 6 shows the results of using the SiC SIT.

As functions of time, Figs. 4 and 5 show the MOSFET gate and drain/DUT voltages, directly below which are the corresponding DUT currents at turn-off. The rise time used for Fig. 4 is t_{rise} = 400 ns, and the rise time represented in Fig. 5 is t_{rise} = 5 ns. It can be seen that as the rise time of the control signal is decreased (i.e., the gate pulse is faster to reach its final value), the di/dt of the DUT at turn-off increases. For the case of the Si MOSFET, decreasing the rise time (or synonymously, increasing the di/dt of the DUT) is restricted by the parasitic capacitances of the MOSFET structure. The current waveform in Fig. 5 is a clear demonstration of this; reducing the rise time to t_{rise} = 5 ns forces large oscillations in the current waveform due to the parasitic capacitance of the MOSFET structure. Also evident from these waveforms at the MOSFET turn-on is the three-stage rise of the gate voltage.

For the case of the SiC SIT, Fig. 6 shows the results when t_{rise} = 5 ns. The capability to increase the di/dt of the DUT at DUT turn-off is improved by the reduction in parasitic capacitance of the SIT structure. The reader should note that the gate voltage waveform of Fig. 6 is a single-phase rise that reaches the maximum gate voltage value very quickly after the drain voltage decreases to its minimum value. This boldly demonstrates that the gate voltage can increase to its maximum value much faster than in the case of the MOSFET due to the severe reduction of the Miller capacitance offered by the SIT structure.

Conclusions

It is shown that a SiC SIT is capable of much faster switching speeds than the traditional power MOSFET when used in the diode characterization test-bed. Due to the device structure, the SIT provides less parasitic capacitance and, ultimately, the capability to switch at much higher frequencies, while retaining the capability to adequately stress the diode under test. In addition, the SIT offers convenience, since it boasts an easy to implement control system that does not require elaborate circuit design when compared to a vacuum tube.

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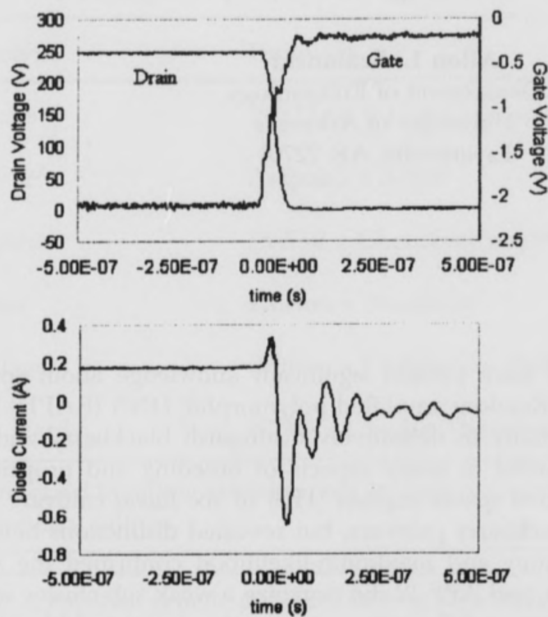

Fig. 6. High-speed diode reverse recovery test with t_{rise}=5ns utilizing SiC SIT.

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